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DATABOOK

2002 Edition

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National Semiconductor

Introduction

National continues its leadership in both Analog and Interface with innovations in performance, packaging, and integration. We are pleased to bring you highlights of all our Analog and Interface products in this databook.

Since the late 1960s, when our first operational amplifiers and regulators were developed, National has been a leading manufacturer of analog integrated circuits. Interface products, beginning with line drivers and receivers, were added in 1973. From the first monolithic regulator, the LM100, to the new chip-scale-packaged product families, many of these products have been 'firsts' in performance and function.

The 2002 Analog/Interface Databook contains abbreviated datasheets for thousands of Analog and Interface products. Providing an overview of product capabilities and applications, these short datasheets are the first few pages extracted from the complete document. Selection guides give additional assistance in selecting the products needed to meet the system requirements.

A CD-ROM accompanies this databook, containing the full datasheet for each product. In addition, the CD-ROM includes application notes, information on Military-Aerospace products, and complete mechanical specifications for packages.

Information on all National products, including those released since this publication, can be found on the National web site at www.national.com.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by National Semiconductor Corporation. The data sheet is printed for reference information only.

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Section 1
Amplifiers - Low-Power, General Purpose and Buffers

Section 1 Contents

National Semiconductor

Low Power/General Purpose Operational Amplifiers

TABLE 1. SINGLE LOW POWER OPERATIONAL AMPLIFIERS

Specifications at T_A = 25°C @ V_S = +5V. * Typical Output Swing with R_L = 2kΩ. ** Typical Output Swing with V_S = +2.7V

Part Number	Supply Current	Input Offset Voltage	Input Bias Current	Common Mode Voltage Range	Output Swing (V)	Gain Bandwidth	Supply Voltage		Packages (Note 1)	Operating Temp Ranges (Note 2)
	I_S (μA) Typ	V_{OS} (mV) Max	Ib (fA) Typ	CMVR (V) Typ	Typ with R_L = 100kΩ unless otherwise Specified	GBW (MHz) Typ	Min (V)	Max (V)		
LPV321	9	7	1.5nA	−0.2 to 4.2	0.09 to 4.997	0.152	2.7	5	M7, M5	I
LM4250	10 (adj)	6	30nA	0.9 to 4.1	0.9 to 4.1	0.2	2	36	M08, N08, H08	C, M
LMC6041	14	6	2	−0.4 to 3.1	0.004 to 4.987	0.075	5	15	M08, N08	I
LMC6041A	14	3	2	−0.4 to 3.1	0.004 to 4.987	0.075	5	15	M08, N08	I
LMC6061	20	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15	M08, N08	I
LMC6061A	20	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15	M08, N08	I, M
LMC7111A	25	3	100	−0.3 to 5.25	0.01 to 4.99	0.05	2.5	11	M5, N08	I
LMC7111B	25	7	100	−0.3 to 5.25	0.01 to 4.99	0.05	2.5	11	M5, N08	I
LPC661	55	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M08	I
LMV321	130	7	15nA	−0.2 to 4.2	0.065 to 4.9	1	2.7	5	M7, M5	I
LMV921	160	6	12nA	−0.3 to 5.35	0.035 to 4.965*	1	1.5	5	M7, M5	I
LM611	210	3	10nA	0 to 3.2	0.8 to 3.6	0.8	4	36	J08, M14	CIM
LM10	300	4	40nA	−0.3 to 4.9	0.015 to 4.9	0.05	1.2	40	M08, N08, H08	I, M
LMV821	300	3.5	40nA	−0.2 to 4.2	0.55 to 4.9	5	2.7	5	M7, M5	I
LMC6001A	450	0.35	25	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	N08	I
LMC6001B	450	1	100	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	N08	I
LMC6001C	450	1	1000	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	N08	I
LMC6081	450	0.8	10	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	M08, N08	I
LMC6081A	450	0.35	10	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	M08, N08	I, M
LMC7101A	500	3	1000	−0.3 to 5.3	0.10 to 4.90*	1.1	2.7	15	M5	I
LMC7101B	500	7	1000	−0.3 to 5.3	0.10 to 4.90*	1.1	2.7	15	M5	I
LM7301	600	6	90nA	−0.1 to 5.1	0.14 to 4.87*	4	1.8	32	M5, M08	I
LMV751	600	1	1500	−0.2 to 3.6	0.086 to 4.89	5	2.7	5	M5	I
LMC8101	700	5	1000	−0.2 to 5.2	0.02 to 4.97	1	2.7	10	BP08, MM08	I
LMC2001	750	0.04	3pA	0 to 4	0.03 to 4.97	6	4.5	5.5	M08, M5	I,C
LM8261	970	5	1.18μA	−0.3 to 5.3	0.07 to 4.87	24	2.5	30	M5	I
LMV721	1030	3	260nA	−0.3 to 4.1	0.046 to 4.962*	10	2.2	5	M7, M5	I
LMV710	1.17 mA	3	4pA	-0.3 to 5.3	0.01 to 4.98	5	2.7	5.5	M5	I
LMV711	1.17 mA	3	4pA	-0.3 to 5.3	0.01 to 4.98	5	2.7	5.5	M6	I

TABLE 2. DUAL LOW POWER OPERATIONAL AMPLIFIERS

Specifications at T_A = 25˚C @ V_S = +5V. * Typical Output Swing with R_L = 2kΩ. ** Typical Output Swing with V_S = +2.7V.

Part Number	Supply Current I_S (µA) Typ	Input Offset Voltage V_{OS} (mV) Max	Input Bias Current Ib (fA) Typ	Common Mode Voltage Range CMVR (V) Typ	Output Swing (V) Typ with R_L = 100kΩ unless otherwise Specified	Gain Bandwidth GBW (MHz) Typ	Supply Voltage		Packages (Note 1)	Operating Temp Ranges (Note 2)
							Min (V)	Max (V)		
LMC6442	2	7	5	−0.4 to 4.1	0.02 to 4.99	0.01	1.5	15	M14, MM14, N14	I
LMC6442A	2	3	5	−0.4 to 4.1	0.02 to 4.99	0.01	1.5	15	M08, N08, MM08, WG10, J08	I, M
LPV358	14	10	2nA	−0.2 to 4.2	0.09 to 4.997	0.152	2.7	5	MM08, M08	I
LMC6042	20	6	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15	M08, N08	I
LMC6042A	20	3	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15	M08, N08	I
LMC6062	32	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15	M08, N08	I
LMC6062A	32	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15	M08, N08, J08	I, M
LMC6462A	40	0.5	150	−0.2 to 5.3	0.005 to 4.995	0.05	3	15	M08, N08	I, M
LMC6462B	40	3	150	−0.2 to 5.3	0.005 to 4.995	0.05	3	15	M08, N08	I
LMC6572A	76	3.3	20	−0.2 to 1.9	0.005 to 2.695**	0.22	2.7	11	M08, N08	I
LMC6572B	76	3.7	20	−0.2 to 1.9	0.005 to 2.695**	0.22	2.7	11	M08, N08, MM08	I
LMC6022	86	9	40	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M08	I
LPC662	86	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M08	I
LPC662A	86	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M08	I, M
LMV358	210	7	15nA	−0.2 to 4.2	0.065 to 4.9	1	2.7	5	MM08, M08	I
LM613	224	5	25nA	0.8 to 3.5	0.8 to 3.5	0.8	4	36	M16	I
LMV922	400	8	12nA	−0.2 to 5.2	0.035 to 4.965	1	1.5	5	M08, MM08	I
LMV822	500	3.5	40nA	−0.2 to 4.2	0.55 to 4.9	5	2.7	5	MM08, M08	I
LM6132A	720	2	110nA	−0.25 to 5.25	0.007 to 4.992	10	2.7	24	M08, N08,	I
LM6132B	720	6	110nA	−0.25 to 5.25	0.007 to 4.992	10	2.7	24	M08, N08,	I
LMC662	750	6	2	−0.4 to 3.1	0.1 to 4.87	2	5	15	M08, N08	I
LMC662A	750	3	2	−0.4 to 3.1	0.10 to 4.87*	1.4	5	15	M08, N08	I
LMC6032	750	9	40	−0.4 to 3.1	0.10 to 4.87*	1.4	5	15	M08, N08	I
LMC6035	800	5	20	−0.5 to 4.5	0.08 to 4.9*	1.4	2	15	M08, MM08, BP08	I
LMC6082	900	0.8	10	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	M08, N08	I
LMC6082A	900	0.35	10	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	M08, N08	I
LM392	1000	5	50nA	0 to 3.5	0 to 3.5	1	3	32	M08, N08	C
LMC6482	1000	3	20	−0.3 to 5.3	0.10 to 4.9*	1.3	3	15	M08, N08, MM08	I
LMC6482A	1000	0.75	20	−0.3 to 5.3	0.10 to 4.9*	1.3	3	15	M08, N08, MM08, J08	I, M
LMC6492A	1000	3	150	−0.3 to 5.3	0.10 to 4.9*	1.5	5	15	M08, N08	E
LMC6492B	1000	6	150	−0.3 to 5.3	0.10 to 4.9*	1.5	5	15	M08, N08	E
LM6142A	1300	1	180nA	−0.25 to 5.25	0.005 to 4.995	17	1.8	24	M08, N08, J08	I, M
LM6142B	1300	2.5	180nA	−0.25 to 5.25	0.005 to 4.995	17	1.8	24	M08, N08	I
LMV722	1830	3.5	260nA	−0.3 to 4.1	0.046 to 4.962*	10	2.2	5	MM08, M08	I
LM6152A	2800	2	500nA	−0.25 to 5.25	0.006 to 4.992	75	2.7	24	M08, N08	I
LM6152B	2800	5	500nA	−0.25 to 5.25	0.006 to 4.992	75	2.7	24	M08, N08	I

TABLE 3. QUAD LOW POWER OPERATIONAL AMPLIFIERS

Specifications at T_A = 25°C @ V_S = +5V. * Typical Output Swing with R_L = 2kΩ. ** Typical Output Swing with V_S = +2.7V

Part Number	Supply Current	Input Offset Voltage	Input Bias Current	Common Mode Voltage Range	Output Swing (V)	Gain Bandwidth	Supply Voltage		Packages (Note 1)	Operating Temp Ranges (Note 2)
	I_S (μA) Typ	V_{OS} (mV) Max	Ib (fA) Typ	CMVR (V) Typ	Typ with R_L = 100kΩ unless otherwise Specified	GBW (MHz) Typ	Min (V)	Max (V)		
LPV324	28	10	2nA	−0.2 to 4.2	0.09 to 4.997	0.152	2.7	5	MT14, M14	I
LMC6044	40	6	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15	M14, N14	I
LMC6044A	40	3	2	−0.4 to 3.1	0.004 to 4.987	0.1	5	15	M14, N14	I
LMC6064	64	0.8	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15	M14, N14	I
LMC6064A	64	0.35	10	−0.4 to 3.1	0.005 to 4.995	0.1	5	15	M14, N14, J14	I, M
LMC6464A	80	0.5	150	−0.2 to 5.3	0.005 to 4.995	0.05	3	15	M14, N14, J14, WG14	I, M
LMC6464B	80	3	150	−0.2 to 5.3	0.005 to 4.995	0.05	3	15	M14, N14	I
LP324	85	4	10nA	−0.1 to 4.9	0.7 to 3.6	0.1	3	32	MT14, M14	I
LP2902	85	10	2nA	−0.1 to 4.9	0.7 to 3.6	0.1	3	32	MT14, M14	E
LMC6024	160	9	40	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M14, N14	I
LMC6574A	160	3	20	−0.2 to 1.9	0.005 to 2.695*	0.22	2.7	11	M14, N14	I
LMC6574B	160	7	20	−0.2 to 1.9	0.005 to 2.695*	0.22	2.7	11	M14, N14	I
LPC660	160	6	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M14	I
LPC660A	160	3	2	−0.4 to 3.1	0.004 to 4.987	0.35	5	15	M14	I
LMV324	410	7	15nA	−0.2 to 4.2	0.065 to 4.9	1	2.7	5	MT14, M14	I
LMV924	750	8	12nA	−0.2 to 5.2	0.03 to 4.97	1	1.8	5	M14, MT14	I
LMV824	1000	3.5	40nA	−0.2 to 4.2	0.055 to 4.9	5.6	2.7	5	MT14, M14	I
LMC6036	1300	5	20	−0.5 to 4.5	0.08 to 4.9*	1.4	2	15	M14	I
LM6134A	1440	2	110nA	−0.25 to 5.25	0.005 to 4.995	10	2.7	24	M14, N14	I
LM6134B	1440	6	110nA	−0.25 to 5.25	0.005 to 4.995	10	2.7	24	M14, N14	I
LMC660A	1500	3	2	−0.4 to 3.1	0.10 to 4.87*	1.4	5	15	M14, N14	I
LMC660C	1500	6	2	−0.4 to 3.1	0.10 to 4.87*	1.4	5	15	M14, N14	I
LMC6034	1500	9	40	−0.4 to 3.1	0.10 to 4.87*	1.4	5	15	M14	I
LMC6084	1800	0.8	10	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	M14, N14	I
LMC6084A	1800	0.35	10	−0.4 to 3.1	0.10 to 4.87*	1.3	5	15	M14, N14	I
LMC6484	2000	3	20	−0.3 to 5.3	0.10 to 4.9*	1.3	3	15	M14, N14	I, M
LMC6484A	2000	0.75	20	−0.3 to 5.3	0.10 to 4.9*	1.3	3	15	M14, N14, J14, WG14	I, M
LMC6494A	2000	3	150	−0.3 to 5.3	0.10 to 4.9*	1.5	2.5	15	M14, N14	E
LMC6494B	2000	6	150	−0.3 to 5.3	0.10 to 4.9*	1.5	2.5	15	M14, N14	E
LM6144A	2600	1	180nA	−0.25 to 5.25	0.005 to 4.995	17	1.8	24	M14, N14	I
LM6144B	2600	2.5	180nA	−0.25 to 5.25	0.005 to 4.995	17	1.8	24	M14, N14	I
LM6154B	5600	5	500nA	−0.25 to 5.25	0.005 to 4.995	75	2.7	24	M14, N14	I

TABLE 4. SPECIAL FUNCTION OPERATIONAL AMPLIFIERS

Specifications at T_A = 25°C @ V_S = +5V.

Part Number	V_{OS} (mV) Max	I_B (nA) Max	GBW (MHz) Typ	Slew Rate (V/µs) Typ	Supply Current (mA) Max	Supply Voltage		Packages (Note 2)	Operating Temp Ranges (Note 2)	Special Note
						Min (V)	Max (V)			
LM12	15	150	0.7	0.7	9	15	80	K	C	80W Operational Amplifier
LM359		15µA	30	30	60	5	22	M14, N14	C	Dual high speed programmable 'Norton' amplifier
LM392	5	250	1	1	2	4	36	M14, N14	C	Low power op amp with voltage comparator
LM611	5	35	0.8	0.7	0.35	4	36	M14, J14	I, C, M	Single amplifier with adjustable voltage reference from 1.2V to 6.3V
LM613	5	35	0.8	0.7	1	4	36	N16, J16	I, M	Dual comparator and dual amplifiers with adjustable voltage reference from 1.2V to 6.3V
LMV711	3	4pA	5	5	1.7	2.7	5	M6	I	R-R I/O Op Amp with High Output Current Drive and Shutdown
LMV8101	5	1	1	1	1	2.7	10	BP08, MM08	I	R-R I/O Op Amp in µSMD with Selectable Shutdown Polarity
LM614	5	35	0.8	0.7	1	4	36	M16	C	Quad Operational Amplifier with Adjustable Reference
LM675	10	2µA	5.5	5.5	8	12	60	T	C	3 Amp Power Op Amp
CLC5509			33		11	8	11	M08	I	0.58nV/Hz Preamp Plus Buffer
LM194/394	0.1, 0.2		200					K06, N08	I, M	Supermatch Transistor Pair
LMV101			1.6	1	0.25	2.7	5	M5, M7	C	LMV321 Type/w Built-In Feedback R's, Fixed Gain of −1
LMV102			1.8	1	0.25	2.7	5	M5, M7	C	LMV321 Type/w Built-In Feedback R's, Fixed Gain of −2
LMV105			0.8	1	0.25	2.7	5	M5, M7	C	LMV321 Type/w Built-In Feedback R's, Fixed Gain of −5
LMV110			0.2	1	0.25	2.7	5	M5, M7	C	LMV321 Type/w Built-In Feedback R's, Fixed Gain of −10
LMV111			1	1	0.25	2.7	5	M5, M7	C	LMV321 Type/w Built-In $V_S/2$ Divider R's on Non-Inverting Input

TABLE 5. SINGLE GENERAL PURPOSE OPERATIONAL AMPLIFIERS

Specifications at $T_A = 25^{\circ}C$.

Part Number	GBW (MHz) Typ	V_{OS} (mV) Max	I_B (nA) Max	Slew Rate (V/μs) Typ	Supply Current (mA) Max	Supply Voltage		Packages (Note 1)	Operating Temp Ranges (Note 1)
						Min (V)	Max (V)		
LM725	0.5	1	100	0.3	4.5	6	44	H08	M
LM725A	0.5	0.5	80	0.3	4.5	6	44	H08	M
LM725C	0.5	2.5	125	0.3	4.8	6	44	H08, N08	C
LM101A/201A	1	2	75	10	3	10	44	H08, J08, J14, W10	M, I
LM301A	1	7.5	250	10	3	10	36	H08, N08	C
LM709	1	5	500	0.25	5.5	10	36	H08	M
LM709A	1	2	200	0.25	3.6	10	36	H08	M
LM709C	1	7.5	1500	0.25	6.6	10	36	H08	C
LM748	1	5	500	1	2.8	10	40	H08	M
LM741	1.5	5	500	0.5	2.8	6	44	H08, J08, W10	M
LM741A	1.5	3	80	0.7	2.8	6	44	H08	M
LM741C	1.5	6	500	0.5	2.8	6	36	H08, N08	C
LF155	2.5	5	0.1	5	4	10	44	H08	M, I
LF155A	2.5	2.5	0.05	5	4	10	44	H08	M
LF156	5	5	0.1	12	7	10	44	H08	M, I
LF156A	5	2	0.05	12	7	10	44	H08	M
LM118/218	15	4	250	70	8	10	40	H08, J08, W10, J14	M, I
LM318	15	10	750	70	10	10	40	H08, M08, N08	C
LF157	20	5	0.1	50	7	10	44	H08	M, I
LF157A	20	2	0.05	50	7	10	44	H08	M

TABLE 6. DUAL GENERAL PURPOSE OPERATIONAL AMPLIFIERS

Specifications at T_A = 25°C.

Part Number	GBW (MHz) Typ	V_{OS} (mV) Max	I_B (nA) Max	Slew Rate (V/µs) Typ	Supply Current (mA) Max	Supply Voltage		Packages (Note 1)	Operating Temp Ranges (Note 2)
						Min (V)	Max (V)		
LF442	1	5	0.1	1	0.5	10	36	H08, N08, J08	C, M
LF442A	1	1	0.05	1	0.4	10	44	H08, N08	C, M
LM158/258	1	5	150	0.5	2	3	32	H08, J08	M, I
LM158A	1	2	50	0.5	2	3	32	H08, J08	M
LM358	1	7	250	0.5	2	3	32	H08, M08, N08	C
LM358A	1	3	100	0.5	2	3	32	M08, N08	C
LM1458	1	6	500	1	5.6	10	36	H08, M08, N08	C
LM1558	1	5	500	1	5	10	44	H08, J08	M
LM2904	1	7	250	0.5	2	3	26	M08, N08	I
LM747	1.5	5	500	0.5	5	10	44	H10, J14	M
LF353	4	10	0.2	13	6.5	10	36	N08, M08	C
LF412	4	3	0.2	15	6.5	10	36	H08, N08, J08	C, M
LF412A	4	1	0.2	15	5.6	10	36	N08	C, M
TL082	4	15	0.4	13	5.6	10	36	M08, N08	C
LM833	15	5	1000	7	8	10	32	MM08, M08, N08	C
LM6218A	17	1	350	140	7	10	42	J08, N08, E20	M, I
LM6218	17	3	500	140	7	10	42	N08, WM14	I
LM6118	17	1	350	75	7	10	42	J08	M

TABLE 7. QUAD GENERAL PURPOSE OPERATIONAL AMPLIFIERS

Specifications at T_A = 25˚C.

Part Number	GBW (MHz) Typ	V_{OS} (mV) Max	I_B (nA) Max	Slew Rate (V/µs) Typ	Supply Current (mA) Max	Supply Voltage		Packages (Note 1)	Operating Temp Ranges (Note 2)
						Min (V)	Max (V)		
LF444	1	10	0.1	1	1	10	36	M08, N08, D14	C, M
LF444A	1	5	0.05	1	0.8	10	44	N14	C
LM124/224	1	5	150	0.5	3	3	32	J14, W14	I
LM124A	1	2	50	0.5	3	3	32	J14, W14, E20	M
LM148	1	5	100	0.5	3.6	10	44	J14, E20	M
LM224A	1	3	80	0.5	3	3	32	J14	I
LM324	1	7	250	0.5	3	3	32	M14, N14, J14	C
LM324A	1	3	100	0.5	3	3	32	M14, N14	C
LM348	1	6	200	0.5	4.5	10	36	M14, N14, J14	C
LM2902	1	7	250	0.5	3	3	26	M14, N14	I
LM146	1.2	5	100	0.4	2	3	44	J16	M
LM346	1.2	6	250	0.4	2.5	3	36	M16, N16	C
LF147	4	5	0.1	13	11	10	44	J14	M
LF347	4	10	0.2	13	11	10	36	M14, N14	C
LM149	4	5	100	2	3.6	10	44	J14	M
LM837	25	5	1000	10	15	10	32	M14, N14	C

Note 1: (Letter = Pkg. Type, Number = # of pins)

Code Letter	Package Type
BP	microSMD
E	LCC
H/G	Metal Can
J/D	Ceramic Dual-In-Line
K	Metal Can (TO-3)
M	SOIC
MF	TSSOP
MM	MSOP
M3	SOT23-3
M5	SOT23-5
M6	SOT23-6
N	Plastic Dual-In-Line (PDIP)
T	TO-220
V	PLCC
W	Flatpak
WG	Ceramic SOIC
Z	TO-92

Note 2: Temperature Ranges:

C =	Commercial (0°C to + 70°C)
E =	Extended (−40°C to + 125°C)
I =	Industrial (−40°C to + 85°C)
M =	Military (−55°C to +125°C)

National Semiconductor

Operational Amplifier Definition Of Terms

Gain Bandwidth (GWB): The open loop gain times the frequency at a specified frequency higher than the first pole.

Unity Gain Bandwidth: The frequency where the amplifier open loop gain equals to one. It equals GBW if single pole roll off exist.

Common-Mode Rejection Ratio (CMRR): The ratio of differential voltage amplification to common-mode voltage amplification. It is measured by determining the ratio of a change in input common-mode voltage to the resulting change in input offset voltage change.

$$CMRR(dB) = 20\log 10\ (\Delta V_{CM}/\Delta V_{OS})$$

Total Harmonic Distortion (THD): When a pure sinusoid given as $V_{in}\ (\omega) = V_p \sin(\omega t)$ is applied to the input of an operational amplifier, the output with harmonic distortion will be $V_{out}(\omega)a_1V_p\sin(\omega t)+a_2V_p\sin(\omega t)+...+a_nV_p\sin(n\omega t)$. THD is express as

$$THD(\%) = [(a_2^2 + a_3^2 + ... + a_n^2)^{1/2}/a_1] \times 100$$

Input Current (I_B or I_{in}): The average of the two input currents.

Input Common-Mode Voltage Range (V_{CM}): Typically the range of voltages on the input terminals for which the amplifier's performance is specified.

Input Impedance (Z_{in}): The ratio of input AC voltage to input AC current.

Common-Mode Input Resistance: The ratio of the common-mode input voltage change to the inverting or non-inverting input current change.

Differential Input Resistance: The ratio of the differential input voltage change to the input current change.

Input Offset Current (I_{OS}): The difference of the currents between the two input terminals.

Input Offset Voltage (V_{OS}): The DC error voltage which exists between the input terminals due to non-ideal balancing of the input stage to the output. It is multiplied by the closed loop gain.

Large-Signal Voltage Gain (A_V): The ratio of the output voltage change to the change in input voltage. This parameter is usually specified at a large output voltage, less than maximum output Voltage, and typically under DC condition.

Output Impedance (Z_O): The apparent output impedance of an op amp, typically illustrated with an ideal op amp with zero output impedance in series with an output impedance, Zout, measured under AC condition.

Output Resistance: The apparent output resistance of an op amp, typically illustrated with an ideal op amp with zero output resistance in series with an output resistor, Rout, measured under DC condition.

Output Voltage Swing (V_O): The maximum peak-to-peak output voltage swing under specified load and supply voltages.

Offset Voltage Temperature Coefficient (TCV_{OS}): The average rate of change in offset voltage for the junction temperature variation over a specified temperature range.

Power Supply Rejection Ratio (PSRR): The ratio of the change in input offset voltage to the change in power supply voltages producing it.

$$PSRR(dB) = 20\log 10\ (\Delta V_{OS}/\Delta V_S)$$

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band, which is expressed as the ±percentage of the total voltage change.

Slew Rate (SR): The rate that an amplifier output changes from one voltage level to another when a step or square wave input is applied. Typically it is the average rate measured from 10% to 90% of the total output voltage change.

Supply Current (I_S): The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions. Usually small signal is less than 100mV.

Input Voltage Noise (e_n): The equivalent voltage noise applied in series with the input of the noiseless amplifier.

Input Current Noise (i_n): The equivalent current noise applied in parallel with the input of the noiseless amplifier.

Phase Margin (Φm): The open-loop phase shift between the output and the inverting input at the unity frequency.

Gain Margin (C_m): Open loop gain at the frequency where the phase between inverting input and output crosses zero.

Rise Time (t_r): The time required for an output voltage step to change from 10% to 90% of its final value.

Short-Circuit Output Current: The maximum available current out of the output of an op amp.

Open loop Gain: The ratio of the voltage change at the output to the voltage change at the input, usually under AC condition.

Note: All parameters are under specific conditions.

National Semiconductor

LF147/LF347
Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

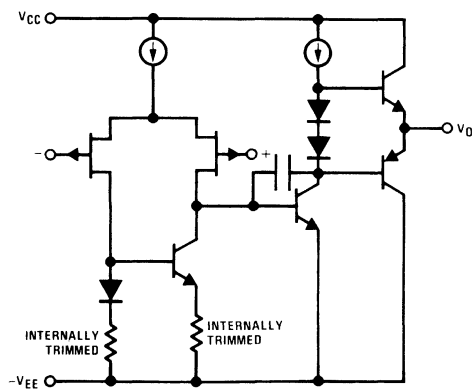
The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 5 mV max
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 7.2 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

Simplified Schematic

¼ Quad



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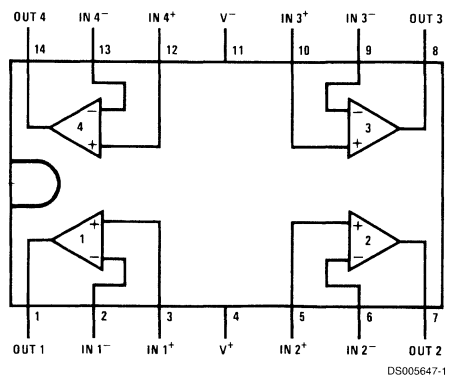
Connection Diagram

Dual-In-Line Package



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Note 1: LF147 available as per JM38510/11906.

Top View
Order Number LF147J, LF147J-SMD, LF347M, LF347BN, LF347N, LF147J/883, or JL147 BCA (Note 1)
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF147	LF347B/LF347
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 3)	±19V	±15V
Output Short Circuit Duration (Note 4)	Continuous	Continuous
Power Dissipation (Notes 5, 11)	900 mW	1000 mW
T_j max	150°C	150°C
θ_{jA}		
Ceramic DIP (J) Package		70°C/W
Plastic DIP (N) Package		75°C/W
Surface Mount Narrow (M)		100°C/W
Surface Mount Wide (WM)		85°C/W
Operating Temperature Range	(Note 6)	(Note 6)
Storage Temperature Range	$-65°C \le T_A \le 150°C$	
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)		260°C
Small Outline Package		
Vapor Phase (60 seconds)		215°C
Infrared (15 seconds)		220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 12) 900V

DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C		1	5		3	5		5	10	mV
		Over Temperature			8			7			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10			10			10		μV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 7, 8)		25	100		25	100		25	100	pA
		Over Temperature			25			4			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 7, 8)		50	200		50	200		50	200	pA
		Over Temperature			50			8			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	100		50	100		25	100		V/mV
		V_O=±10V, R_L=2 kΩ										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		±11	+15		±11	+15		V
	Range			−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤10 kΩ	80	100		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)	80	100		80	100		70	100		dB
I_S	Supply Current			7.2	11		7.2	11		7.2	11	mA

AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF147			LF347B			LF347			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz (Input Referred)		−120			−120			−120		dB
SR	Slew Rate	V_S=±15V, T_A=25°C	8	13		8	13		8	13		V/μs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	2.2	4		2.2	4		2.2	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1000 Hz		20			20			20		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz–20 kHz		<0.02			<0.02			<0.02		%

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 5: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 6: The LF147 is available in the military temperature range −55°C≤T_A≤125°C, while the LF347B and the LF347 are available in the commercial temperature range 0°C≤T_A≤70°C. Junction temperature can rise to T_j max = 150°C.

Note 7: Unless otherwise specified the specifications apply over the full temperature range and for V_S=±20V for the LF147 and for V_S=±15V for the LF347B/LF347. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Note 8: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from V_S = ± 5V to ±15V for the LF347 and LF347B and from V_S = ±20V to ±5V for the LF147.

Note 10: Refer to RETS147X for LF147D and LF147J military specifications.

Note 11: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 12: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LF155/LF156/LF256/LF257/LF355/LF356/LF357 JFET Input Operational Amplifiers

General Description

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

Features

Advantages

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

Applications

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

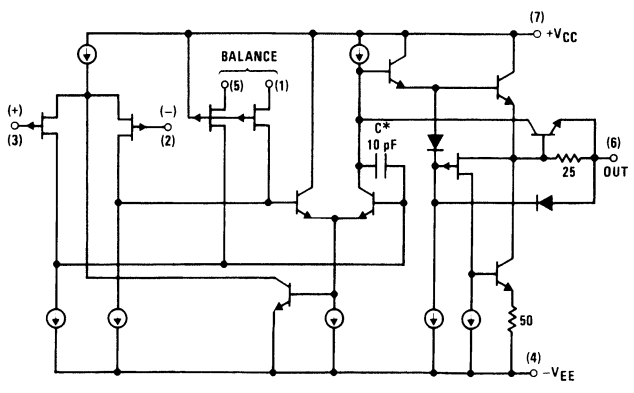
Common Features

- Low input bias current: 30pA
- Low Input Offset Current: 3pA
- High input impedance: $10^{12}\Omega$
- Low input noise current: $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio: 100 dB
- Large dc voltage gain: 106 dB

Uncommon Features

	LF155/ LF355	LF156/ LF256/ LF356	LF257/ LF357 (A_V=5)	Units
■ Extremely fast settling time to 0.01%	4	1.5	1.5	μs
■ Fast slew rate	5	12	50	V/μs
■ Wide gain bandwidth	2.5	5	20	MHz
■ Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

Simplified Schematic



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*3pF in LF357 series.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

	LF155/6	LF256/7/LF356B	LF355/6/7
Supply Voltage	±22V	±22V	±18V
Differential Input Voltage	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous
T_{JMAX}			
H-Package	150°C	115°C	115°C
N-Package		100°C	100°C
M-Package		100°C	100°C
Power Dissipation at T_A = 25°C (Notes 1, 8)			
H-Package (Still Air)	560 mW	400 mW	400 mW
H-Package (400 LF/Min Air Flow)	1200 mW	1000 mW	1000 mW
N-Package		670 mW	670 mW
M-Package		380 mW	380 mW
Thermal Resistance (Typical) θ_{JA}			
H-Package (Still Air)	160°C/W	160°C/W	160°C/W
H-Package (400 LF/Min Air Flow)	65°C/W	65°C/W	65°C/W
N-Package		130°C/W	130°C/W
M-Package		195°C/W	195°C/W
(Typical) θ_{JC}			
H-Package	23°C/W	23°C/W	23°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Soldering Information (Lead Temp.)			
Metal Can Package			
Soldering (10 sec.)	300°C	300°C	300°C
Dual-In-Line Package			
Soldering (10 sec.)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 sec.)		215°C	215°C
Infrared (15 sec.)		220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD tolerance			
(100 pF discharged through 1.5kΩ)	1000V	1000V	1000V

DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=50Ω, T_A=25°C		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=50Ω		5			5			5		μV/°C
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	R_S=50Ω, (Note 4)		0.5			0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	T_J=25°C, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_J \leq T_{HIGH}$			20			1			2	nA

DC Electrical Characteristics (Continued)

(Note 3)

Symbol	Parameter	Conditions	LF155/6			LF256/7 LF356B			LF355/6/7			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_B	Input Bias Current	T_J=25°C, (Notes 3, 5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	T_J=25°C		10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	50	200		50	200		25	200		V/mV
		V_O=±10V, R_L=2k										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k	±12	±13		±12	±13		±12	±13		V
		V_S=±15V, R_L=2k	±10	±12		±10	±12		±10	±12		V
V_{CM}	Input Common-Mode Voltage Range	V_S=±15V	±11	+15.1 −12		±11	±15.1 −12		+10	+15.1 −12		V V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = ±15V$

Parameter	LF155		LF355		LF156/256/257/356B		LF356		LF357		Units
	Typ	Max	Typ	Max	Typ	Max	Typ	Max	Typ	Max	
Supply Current	2	4	2	4	5	7	5	10	5	10	mA

AC Electrical Characteristics

$T_A = T_J = 25°C$, $V_S = ±15V$

Symbol	Parameter	Conditions	LF155/355	LF156/256/ 356B	LF156/256/356/ LF356B	LF257/357	Units
			Typ	Min	Typ	Typ	
SR	Slew Rate	LF155/6: A_V=1,	5	7.5	12		V/μs
		LF357: A_V=5				50	V/μs
GBW	Gain Bandwidth Product		2.5		5	20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5	1.5	μs
e_n	Equivalent Input Noise Voltage	R_S=100Ω					
		f=100 Hz	25		15	15	$nV/\sqrt{Hz}$
		f=1000 Hz	20		12	12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f=100 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
		f=1000 Hz	0.01		0.01	0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3	3	pF

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D=(T_{JMAX}-T_A)/\theta_{JA}$ or the 25°C P_{dMAX}, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

Notes for Electrical Characteristics (Continued)

	LF155/156	LF256/257	LF356B	LF355/6/7
Supply Voltage, V_S	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \le \pm 20V$	$\pm 15V \le V_S \pm 20V$	$V_S = \pm 15V$
T_A	$-55^\circ C \le T_A \le +125^\circ C$	$-25^\circ C \le T_A \le +85^\circ C$	$0^\circ C \le T_A \le +70^\circ C$	$0^\circ C \le T_A \le +70^\circ C$
T_{HIGH}	$+125^\circ C$	$+85^\circ C$	$+70^\circ C$	$+70^\circ C$

and V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta_{JA}$ Pd where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Note 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF357, $A_V = -5$, the feedback resistor from output to input is 2kΩ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

National Semiconductor

LF353
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

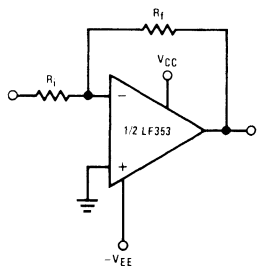
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 10 mV
- Low input bias current: 50pA
- Low input noise voltage: 25 nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 3.6 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion : ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

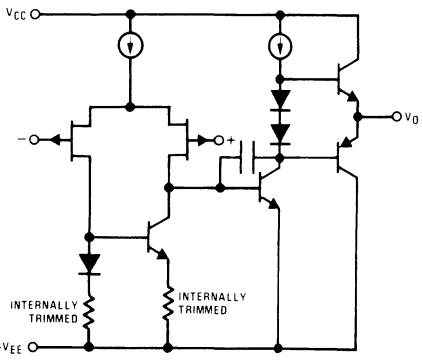
Typical Connection



DS005649-14

Simplified Schematic

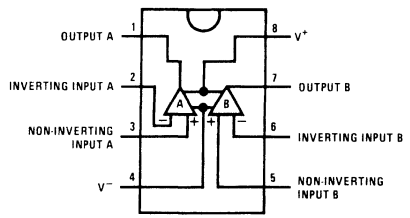
1/2 Dual



DS005649-16

Connection Diagram

Dual-In-Line Package



DS005649-17

Top View
Order Number LF353M, LF353MX or LF353N
See NS Package Number M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
T_j(MAX)	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 8)	1700V
θ_{JA} M Package	TBD

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

DC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10kΩ, T_A=25°C		5	10	mV
		Over Temperature			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j=25°C, (Notes 5, 6)		25	100	pA
		T_j≤70°C			4	nA
I_B	Input Bias Current	T_j=25°C, (Notes 5, 6)		50	200	pA
		T_j≤70°C			8	nA
R_{IN}	Input Resistance	T_j=25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, T_A=25°C	25	100		V/mV
		V_O=±10V, R_L=2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage	V_S=±15V	±11	+15		V
	Range			−12		V
CMRR	Common-Mode Rejection Ratio	R_S≤ 10kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	6.5	mA

AC Electrical Characteristics

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz–20 kHz		−120		dB
		(Input Referred)				
SR	Slew Rate	V_S=±15V, T_A=25°C	8.0	13		V/µs
GBW	Gain Bandwidth Product	V_S=±15V, T_A=25°C	2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω,		16		nV/$\sqrt{Hz}$
		f=1000 Hz				
i_n	Equivalent Input Noise Current	T_j=25°C, f=1000 Hz		0.01		pA/$\sqrt{Hz}$

AC Electrical Characteristics (Continued)

(Note 5)

Symbol	Parameter	Conditions	LF353			Units
			Min	Typ	Max	
THD	Total Harmonic Distortion	A_V=+10, RL=10k, V_O=20Vp-p, BW=20 Hz-20 kHz		<0.02		%

Note 2: For operating at elevated temperatures, the device must be derated based on a thermal resistance of 115˚C/W typ junction to ambient for the N package, and 158˚C/W typ junction to ambient for the H package.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for V_S=±15V and 0˚C≤T_A≤+70˚C. V_{OS}, $I_B$and I_{OS} are measured at V_{CM}=0.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LF411
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

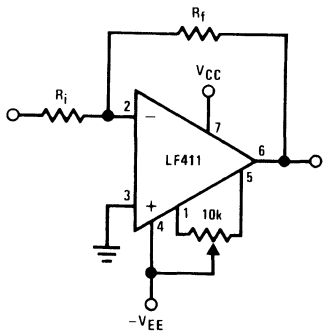
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

■ Internally trimmed offset voltage:	0.5 mV(max)
■ Input offset voltage drift:	10 μV/°C(max)
■ Low input bias current:	50 pA
■ Low input noise current:	0.01 pA/√Hz
■ Wide gain bandwidth:	3 MHz(min)
■ High slew rate:	10V/μs(min)
■ Low supply current:	1.8 mA
■ High input impedance:	$10^{12}\Omega$
■ Low total harmonic distortion:	≤0.02%
■ Low 1/f noise corner:	50 Hz
■ Fast settling time to 0.01%:	2 μs

Typical Connection



DS005655-1

Ordering Information

LF411XYZ

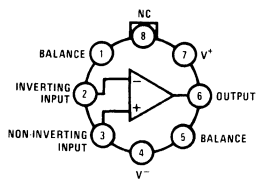
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package

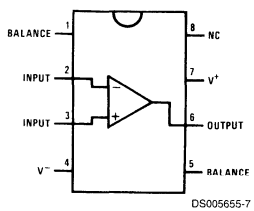


DS005655-5

Note: Pin 4 connected to case.

Top View
Order Number LF411ACH
or LF411MH/883 (Note 11)
See NS Package Number H08A

Dual-In-Line Package



DS005655-7

Top View
Order Number LF411ACN, LF411CN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF411A	LF411
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 2)	±19V	±15V
Output Short Circuit Duration	Continuous	Continuous

	H Package	N Package
Power Dissipation (Notes 3, 10)	670 mW	670 mW
$T_j$max	150°C	115°C
θ_jA	162°C/W (Still Air) 65°C/W (400 LF/min Air Flow)	120°C/W
θ_jC	20°C/W	
Operating Temp. Range	(Note 4)	(Note 4)
Storage Temp. Range	−65°C≤T_A≤150°C	−65°C≤T_A≤150°C
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance	Rating to be determined.	

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF411A			LF411			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ (Note 6)			7	10		7	20 (Note 6)	µV/°C
I_{OS}	Input Offset Current	V_S=±15V (Notes 5, 7)	T_j=25°C		25	100		25	100	pA
			T_j=70°C			2			2	nA
			T_j=125°C			25			25	nA
I_B	Input Bias Current	V_S=±15V (Notes 5, 7)	T_j=25°C		50	200		50	200	pA
			T_j=70°C			4			4	nA
			T_j=125°C			50			50	nA
R_{IN}	Input Resistance	T_j=25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 8)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

AC Electrical Characteristic (Note 5)

Symbol	Parameter	Conditions	LF411A			LF411			Units
			Min	Typ	Max	Min	Typ	Max	
SR	Slew Rate	V_S=±15V, T_A=25°C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1 kHz		25			25		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A=25°C, f=1 kHz		0.01			0.01		pA/$\sqrt{Hz}$
THD	Total Harmonic Distortion	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz–20 kHz		<0.02			<0.02		%

AC Electrical Characteristic (Note 5) (Continued)

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_jA.

Note 4: These devices are available in both the commercial temperature range $0^\circ C \leq T_A \leq 70^\circ C$ and the military temperature range $-55^\circ C \leq T_A \leq 125^\circ C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF411A and for $V_S = \pm 15V$ for the LF411. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

Note 9: RETS 411X for LF411MH and LF411MJ military specifications.

Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

National Semiconductor

LF412
Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

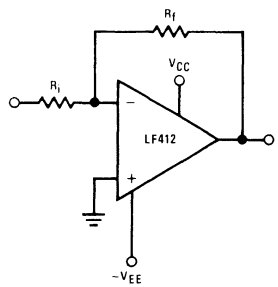
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage: 1 mV (max)
- Input offset voltage drift: 10 μV/°C (max)
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/$\sqrt{\text{Hz}}$
- Wide gain bandwidth: 3 MHz (min)
- High slew rate: 10V/μs (min)
- Low supply current: 1.8 mA/Amplifier
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

Typical Connection



DS005656-41

Ordering Information

LF412XYZ

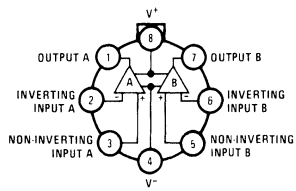
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



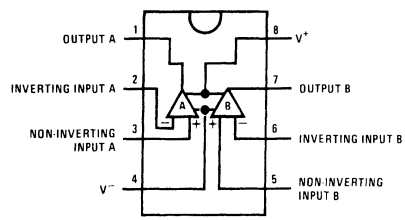
Note. Pin 4 connected to case.

TOP VIEW

DS005656-42

Order Number LF412MH, LF412CH or LF412MH/883 (Note 1)
See NS Package Number H08A

Dual-In-Line Package



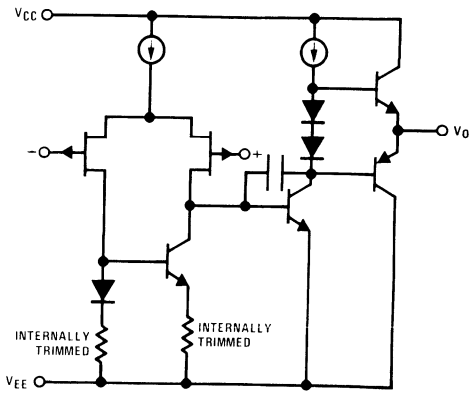
TOP VIEW

DS005656-44

Order Number LF412ACN, LF412CN or LF412MJ/883 (Note 1)
See NS Package Number J08A or N08E

Simplified Schematic

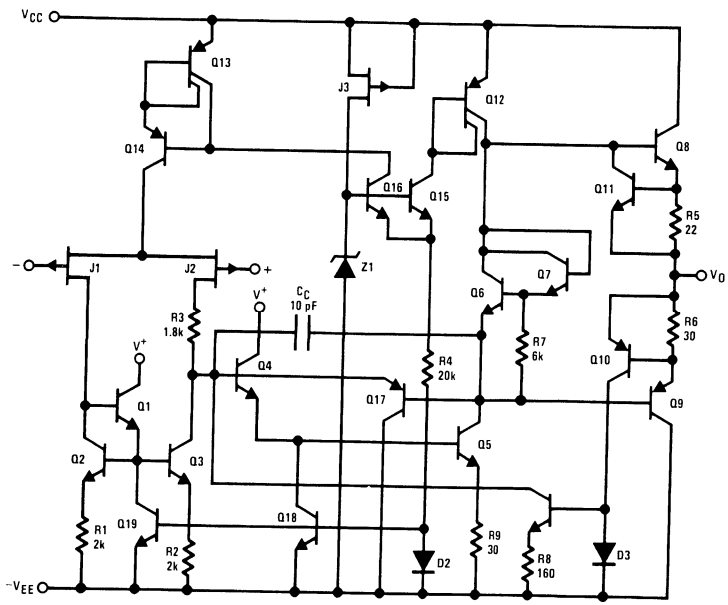
1/2 Dual



DS005656-43

Note 1: Available per JM38510/11905

Detailed Schematic



DS005656-32

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 11)

	LF412A	LF412
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input voltage Range (Note 3)	±19V	±15V
Output Short Circuit Duration (Note 4)	Continuous	Continuous

	H Package	N Package
Power Dissipation (Note 12)	(Note 5)	670 mW

	H Package	N Package
T_j max	150°C	115°C
θ_{jA} (Typical)	152°C/W	115°C/W
Operating Temp. Range	(Note 6)	(Note 6)
Storage Temp. Range	−65°C≤T_A≤150°C	−65°C≤T_A≤150°C
Lead Temp. (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance (Note 13)	1700V	1700V

DC Electrical Characteristics

(Note 7)

Symbol	Parameter	Conditions		LF412A			LF412			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C			0.5	1.0		1.0	3.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ (Note 8)			7	10		7	20	µV/°C
I_{OS}	Input Offset Current	V_S=±15V (Notes 7, 9)	T_j=25°C		25	100		25	100	pA
			T_j=70°C			2			2	nA
			T_j=125°C			25			25	nA
I_B	Input Bias Current	V_S=±15V (Notes 7, 9)	T_j=25°C		50	200		50	200	pA
			T_j=70°C			4			4	nA
			T_j=125°C			50			50	nA
R_{IN}	Input Resistance	T_j=25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 10)		80	100		70	100		dB
I_S	Supply Current	V_O = 0V, R_L = ∞			3.6	5.6		3.6	6.5	mA

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

AC Electrical Characteristics

(Note 7)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A=25°C, f=1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	V_S=±15V, T_A=25°C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	3	4		2.7	4		MHz

AC Electrical Characteristics (Continued)

(Note 7)

Symbol	Parameter	Conditions	LF412A			LF412			Units
			Min	Typ	Max	Min	Typ	Max	
THD	Total Harmonic Dist	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz-20 kHz		≤0.02			≤0.02		%
e_n	Equivalent Input Noise Voltage	T_A=25˚C, R_S=100Ω, f=1 kHz		25			25		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A=25˚C, f=1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: Any of the amplifier outputs can be shorted to ground indefintely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 5: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 6: These devices are available in both the commercial temperature range 0˚C≤T_A≤70˚C and the military temperature range −55˚C≤T_A≤125˚C. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature T_j max.

Note 7: Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF412A and for V_S=±15V for the LF412. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.

Note 8: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

Note 9: The input bias currents are junction leakage currents which approximately double for every 10˚C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_j=T_A+θ_{jA} P_D where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 10: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Note 11: Refer to RETS412X for LF412MH and LF412MJ military specifications.

Note 12: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 13: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LF442
Dual Low Power JFET Input Operational Amplifier

General Description

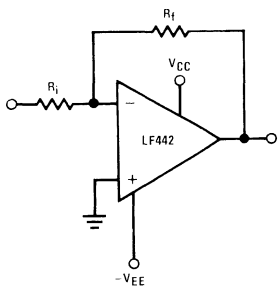
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

- 1/10 supply current of a LM1458: 400 μA (max)
- Low input bias current: 50 pA (max)
- Low input offset voltage: 1 mV (max)
- Low input offset voltage drift: 10 μV/°C (max)
- High gain bandwidth: 1 MHz
- High slew rate: 1 V/μs
- Low noise voltage for low power: 35 nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- High input impedance: $10^{12}\Omega$
- High gain $V_O = \pm 10V$, R_L = 10k: 50k (min)

Typical Connection



DS009155-1

Ordering Information

LF442XYZ

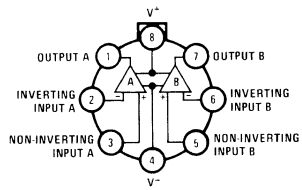
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package

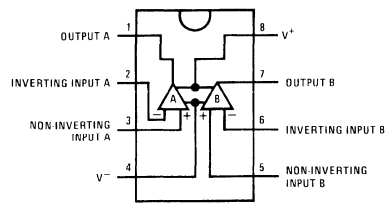


DS009155-2

Pin 4 connected to case

Top View
Order Number LF442AMH or LF442MH/883
See NS Package Number H08A

Dual-In-Line Package



DS009155-4

Top View
Order Number LF442ACN or LF442CN
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF442A	LF442
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 2)	±19V	±15V
Output Short Circuit Duration (Note 3)	Continuous	Continuous

	H Package	N Package
T_j max	150°C	115°C

	H Package	N Package
θ_{JA} (Typical) (Note 4)	65°C/W	114°C/W
θ_{JA} (Typical) (Note 5)	165°C/W	152°C/W
θ_{JC} (Typical)	21°C/W	
Operating Temperature Range	(Note 5)	(Note 5)
Storage Temperature Range	−65°C≤T_A≤150°C	−65°C≤T_A≤150°C
Lead Temperature (Soldering, 10 sec.)	260°C	260°C
ESD Tolerance	Rating to be determined	

DC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions		LF442A			LF442			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C			0.5	1.0		1.0	5.0	mV
		Over Temperature							7.5	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ			7	10		7		μV/°C
I_{OS}	Input Offset Current	V_S = ±15V (Notes 7, 8)	T_j = 25°C		5	25		5	50	pA
			T_j = 70°C			1.5			1.5	nA
			T_j = 125°C			10				nA
I_B	Input Bias Current	V_S = ±15V (Notes 7, 8)	T_j = 25°C		10	50		10	100	pA
			T_j = 70°C			3			3	nA
			T_j = 125°C			20				nA
R_{IN}	Input Resistance	T_j = 25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, V_O = ±10V, R_L = 10 kΩ, T_A = 25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18 −17		±11	+14 −12		V V
CMRR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 9)		80	100		70	90		dB
I_S	Supply Current				300	400		400	500	μA

AC Electrical Characteristics (Note 7)

Symbol	Parameter	Conditions	LF442A			LF442			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1 Hz-20 kHz (Input Referred)		−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	0.8	1		0.6	1		V/μs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C	0.8	1		0.6	1		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1 kHz		35			35		$nV/\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A = 25°C, f = 1 kHz		0.01			0.01		$pA/\sqrt{Hz}$

AC Electrical Characteristics (Note 7) (Continued)

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 4: The value given is in 400 linear feet/min air flow.

Note 5: The value given is in static air.

Note 6: These devices are available in both the commercial temperature range $0^{\circ}C \leq T_A \leq 70^{\circ}C$ and the military temperature range $-55^{\circ}C \leq T_A \leq 125^{\circ}C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 7: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF442A and for $V_S = \pm 15V$ for the LF442. V_{OS}, I_B, and I_{OS} are measured at $V_{CM} = 0$.

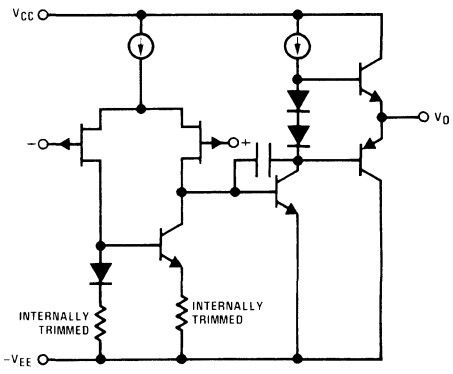
Note 8: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 9: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF442 and ±20V to ±5V for the LF442A.

Note 10: Refer to RETS442X for LF442MH military specifications.

Simplified Schematic

1/2 Dual



DS009155-3

National Semiconductor

LF444
Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 kΩ load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

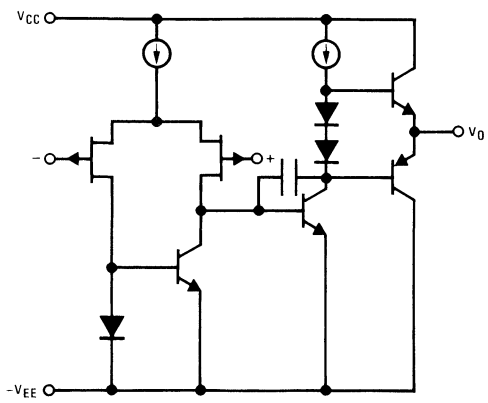
The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Features

- ¼ supply current of a LM148: 200 µA/Amplifier (max)
- Low input bias current: 50 pA (max)
- High gain bandwidth: 1 MHz
- High slew rate: 1 V/µs
- Low noise voltage for low power 35 nV/$\sqrt{Hz}$
- Low input noise current 0.01 pA/$\sqrt{Hz}$
- High input impedance: $10^{12}\Omega$
- High gain: 50k (min)

Simplified Schematic

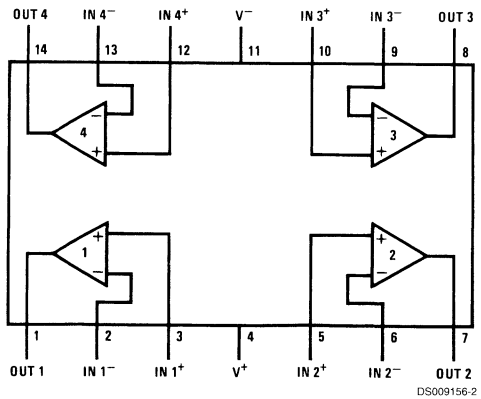
1/4 Quad



DS009156-1

Connection Diagram

Dual-In-Line Package



DS009156-2

Top View
Order Number LF444CM, LF444CMX, LF444ACN, LF 444CN or LF444MD/883
See NS Package Number D14E, M14A or N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range
"M" for military, "C" for commercial

Z indicates package type "D", "M" or "N"

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LF444A	LF444
Supply Voltage	±22V	±18V
Differential Input Voltage	±38V	±30V
Input Voltage Range (Note 1)	±19V	±15V
Output Short Circuit Duration (Note 2)	Continuous	Continuous

	D Package	N, M Packages
Power Dissipation (Notes 3, 9)	900 mW	670 mW
T_j max	150°C	115°C
θ_{jA} (Typical)	100°C/W	85°C/W

	LF444A/LF444
Operating Temperature Range	(Note 4)
Storage Temperature Range	$-65°C \le T_A \le 150°C$
ESD Tolerance (Note 10)	Rating to be determined
Soldering Information	
Dual-In-Line Packages	
(Soldering, 10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions		LF444A			LF444			Units
				Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10k, T_A = 25°C			2	5		3	10	mV
		0°C ≤ T_A ≤ +70°C				6.5			12	mV
		−55°C ≤ T_A ≤ +125°C				8				mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ			10			10		µV/°C
I_{OS}	Input Offset Current	V_S = ±15V (Notes 5, 6)	T_j = 25°C		5	25		5	50	pA
			T_j = 70°C			1.5			1.5	nA
			T_j = 125°C			10				nA
I_B	Input Bias Current	V_S = ±15V (Notes 5, 6)	T_j = 25°C		10	50		10	100	pA
			T_j = 70°C			3			3	nA
			T_j = 125°C			20				nA
R_{IN}	Input Resistance	T_j = 25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, V_O = ±10V		50	100		25	100		V/mV
		R_L = 10 kΩ, T_A = 25°C								
		Over Temperature		25			15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range			±16	+18		±11	+14		V
					−17			−12		V
CMRR	Common-Mode Rejection Ratio	R_S ≤ 10 kΩ		80	100		70	95		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)		80	100		70	90		dB
I_S	Supply Current				0.6	0.8		0.6	1.0	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	LF444A			LF444			Units
			Min	Typ	Max	Min	Typ	Max	
	Amplifier-to-Amplifier Coupling			−120			−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C		1			1		V/μs
GBW	Gain-Bandwidth Product	V_S = ±15V, T_A = 25°C		1			1		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1 kHz		35			35		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	T_A = 25°C, f = 1 kHz		0.01			0.01		pA/$\sqrt{Hz}$

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{jA}.

Note 4: The LF444A is available in both the commercial temperature range 0°C ≤ T_A ≤ 70°C and the military temperature range −55°C ≤ T_A ≤ 125°C. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for V_S = ±20V for the LF444A and for V_S = ±15V for the LF444. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA}P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from ±15V to ±5V for the LF444 and from ±20V to ±5V for the LF444A.

Note 8: Refer to RETS444X for LF444MD military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 10: Human body model, 1.5 kΩ in series with 100 pF.

Note 11: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

National Semiconductor

LM10
Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270μA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV.

The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

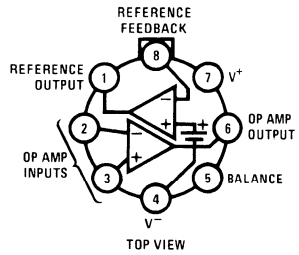
This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Features

- input offset voltage: 2.0 mV (max)
- input offset current: 0.7 nA (max)
- input bias current: 20 nA (max)
- reference regulation: 0.1% (max)
- offset voltage drift: 2μV/°C
- reference drift: 0.002%/°C

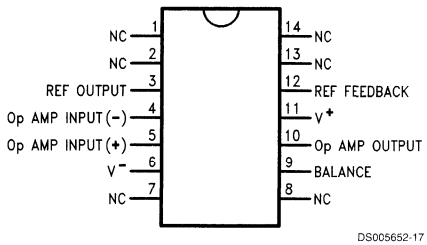
Connection and Functional Diagrams

Metal Can Package (H)



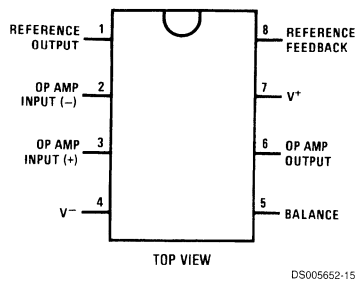
Order Number LM10BH, LM10CH, LM10CLH or LM10H/883 available per SMA# 5962-8760401
See NS Package Number H08A

Small Outline Package (WM)

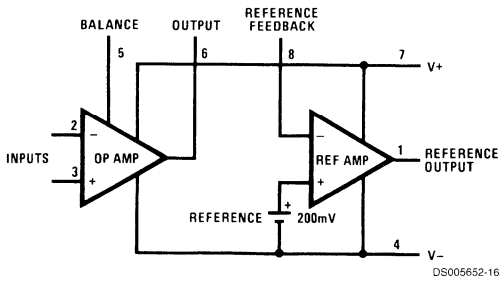


Order Number LM10CWM or LM10CWMX
See NS Package Number M14B

Dual-In-Line Package (N)



Order Number LM10CN or LM10CLN
See NS Package Number N08E



Absolute Maximum Ratings (Notes 1, 8)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM10/LM10B/ LM10C	LM10BL/ LM10CL
Total Supply Voltage	45V	7V
Differential Input Voltage (Note 2)	±40V	±7V
Power Dissipation (Note 3)	internally limited	
Output Short-circuit Duration (Note 4)	continuous	
Storage-Temp. Range	−55°C to +150°C	
Lead Temp. (Soldering, 10 seconds)		
Metal Can	300°C	
Lead Temp. (Soldering, 10 seconds) DIP	260°C	
Vapor Phase (60 seconds)	215°C	
Infrared (15 seconds)	220°C	

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

Maximum Junction Temperature

LM10	150°C
LM10B	100°C
LM10C	85°C

Operating Ratings

Package Thermal Resistance

θ_{JA}	
H Package	150°C/W
N Package	87°C/W
WM Package	90°C/W
θ_{JC}	
H Package	45°C/W

Electrical Characteristics

T_J=25°C, $T_{MIN} \le T_J \le T_{MAX}$ **(Boldface type refers to limits over temperature range)** (Note 5)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current			0.25	0.7		0.4	2.0	nA
(Note 6)				**1.5**			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage gain	V_S=±20V, I_{OUT}=0	120	400		80	400		V/mV
	V_{OUT}=±19.95V	**80**			**50**			V/mV
	V_S=±20V, V_{OUT}=±19.4V	50	130		25	130		V/mV
	I_{OUT}=±20 mA **(±15 mA)**	**20**			**15**			V/mV
	V_S=±0.6V **(0.65V)**, I_{OUT}=±2 mA	1.5	3.0		1.0	3.0		V/mV
	V_{OUT}=±0.4V **(±0.3V)**, V_{CM}=−0.4V	**0.5**			**0.75**			V/mV
Shunt gain (Note 7)	1.2V **(1.3V)** ≤V_{OUT}≤40V,	14	33		10	33		V/mV
	R_L=1.1 kΩ							
	0.1 mA≤I_{OUT}≤5 mA	**6**			**6**			V/mV
	1.5V≤V^+≤40V, R_L=250Ω	8	25		6	25		V/mV
	0.1 mA≤I_{OUT}≤20 mA	**4**			**4**			V/mV
Common-mode rejection	−20V≤V_{CM}≤19.15V **(19V)**	93	102		90	102		dB
	V_S=±20V	**87**			**87**			dB
Supply-voltage rejection	−0.2V≥V^-≥−39V	90	96		87	96		dB
	V^+=1.0V **(1.1V)**	**84**			**84**			dB
	1.0V **(1.1V)** ≤V^+≤39.8V	96	106		93	106		dB
	V^-=−0.2V	**90**			**90**			dB
Offset voltage drift			2.0			5.0		µV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift	T_C<100°C		60			90		pA/°C
Line regulation	1.2V **(1.3V)** ≤V_S≤40V		0.001	0.003		0.001	0.008	%/V
	0≤I_{REF}≤1.0 mA, V_{REF}=200 mV			**0.006**			**0.01**	%/V

Electrical Characteristics (Continued)

T_J=25°C, $T_{MIN} \le T_J \le T_{MAX}$ **(Boldface type refers to limits over temperature range)** (Note 5)

Parameter	Conditions	LM10/LM10B			LM10C			Units
		Min	Typ	Max	Min	Typ	Max	
Load regulation	$0 \le I_{REF} \le 1.0$ mA		0.01	0.1		0.01	0.15	%
	$V^+ - V_{REF} \ge 1.0V$ **(1.1V)**			**0.15**			**0.2**	%
Amplifier gain	$0.2V \le V_{REF} \le 35V$	50	75		25	70		V/mV
		23			**15**			V/mV
Feedback sense voltage		195	200	205	190	200	210	mV
		194		**206**	**189**		**211**	mV
Feedback current			20	50		22	75	nA
				65			**90**	nA
Reference drift			0.002			0.003		%/°C
Supply current			270	400		300	500	µA
				500			**570**	µA
Supply current change	1.2V **(1.3V)** $\le V_S \le 40V$		15	**75**		15	**75**	µA

Electrical Characteristics

T_J=25°C, $T_{MIN} \le T_J \le T_{MAX}$ **(Boldface type refers to limits over temperature range)** (Note 5)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage			0.3	2.0		0.5	4.0	mV
				3.0			**5.0**	mV
Input offset current (Note 6)			0.1	0.7		0.2	2.0	nA
				1.5			**3.0**	nA
Input bias current			10	20		12	30	nA
				30			**40**	nA
Input resistance		250	500		150	400		kΩ
		150			**115**			kΩ
Large signal voltage gain	$V_S = \pm 3.25V$, I_{OUT}=0	60	300		40	300		V/mV
	$V_{OUT} = \pm 3.2V$	**40**			**25**			V/mV
	$V_S = \pm 3.25V$, I_{OUT}=10 mA	10	25		5	25		V/mV
	$V_{OUT} = \pm 2.75$ V	**4**			**3**			V/mV
	$V_S = \pm 0.6V$ **(0.65V)**, $I_{OUT} = \pm 2$ mA	1.5	3.0		1.0	3.0		V/mV
	$V_{OUT} = \pm 0.4V$ **(±0.3V)**, $V_{CM} = -0.4V$	**0.5**			**0.75**			V/mV
Shunt gain (Note 7)	$1.5V \le V^+ \le 6.5V$, $R_L = 500\Omega$	8	30		6	30		V/mV
	$0.1\ mA \le I_{OUT} \le 10$ mA	**4**			**4**			V/mV
Common-mode rejection	$-3.25V \le V_{CM} \le 2.4V$ **(2.25V)**	89	102		80	102		dB
	$V_S = \pm 3.25V$	**83**			**74**			dB
Supply-voltage rejection	$-0.2V \ge V^- \ge -5.4V$	86	96		80	96		dB
	V^+=1.0V **(1.2V)**	**80**			**74**			dB
	1.0V **(1.1V)** $\le V^+ \le 6.3V$	94	106		80	106		dB
	V^-=0.2V	**88**			**74**			dB
Offset voltage drift			2.0			5.0		µV/°C
Offset current drift			2.0			5.0		pA/°C
Bias current drift			60			90		pA/°C
Line regulation	1.2V **(1.3V)** $\le V_S \le 6.5V$		0.001	0.01		0.001	0.02	%/V
	$0 \le I_{REF} \le 0.5$ mA, V_{REF}=200 mV			**0.02**			**0.03**	%/V
Load regulation	$0 \le I_{REF} \le 0.5$ mA		0.01	0.1		0.01	0.15	%
	$V^+ - V_{REF} \ge 1.0V$ **(1.1V)**			**0.15**			**0.2**	%

Electrical Characteristics (Continued)

T_J=25°C, $T_{MIN} \leq T_J \leq T_{MAX}$ **(Boldface type refers to limits over temperature range)** (Note 5)

Parameter	Conditions	LM10BL			LM10CL			Units
		Min	Typ	Max	Min	Typ	Max	
Amplifier gain	$0.2V \leq V_{REF} \leq 5.5V$	30	70		20	70		V/mV
		20			**15**			V/mV
Feedback sense voltage		195	200	205	190	200	210	mV
		194		**206**	**189**		**211**	mV
Feedback current			20	50		22	75	nA
				65			**90**	nA
Reference drift			0.002			0.003		%/°C
Supply current			260	400		280	500	µA
				500			**570**	µA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The Input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{IN} < V^-$.

Note 3: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 4: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Note 5: These specifications apply for $V^- \leq V_{CM} \leq V^+ - 0.85V$ **(1.0V),** 1.2V **(1.3V)** $< V_S \leq V_{MAX}$, V_{REF}=0.2V and $0 \leq I_{REF} \leq 1.0$ mA, unless otherwise specified: V_{MAX}=40V for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation;** this is −55°C to 125°C for the LM10, −25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \cong 20$ ms), die heating ($\tau_2 \cong 0.2$s) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 6: For T_J>90°C, I_{OS} may exceed 1.5 nA for $V_{CM}=V^-$. With T_J=125°C and $V^- \leq V_{CM} \leq V^- + 0.1V$, $I_{OS} \leq 5$ nA.

Note 7: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Note 8: Refer to RETS10X for LM10H military specifications.

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^-, on the reference feedback terminal while operating in regulation.

Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

National Semiconductor

LM13700
Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers. The output buffers of the LM13700 differ from those of the LM13600 in that their input bias currents (and hence their output DC levels) are independent of I_{ABC}. This may result in performance superior to that of the LM13600 in audio applications.

Features

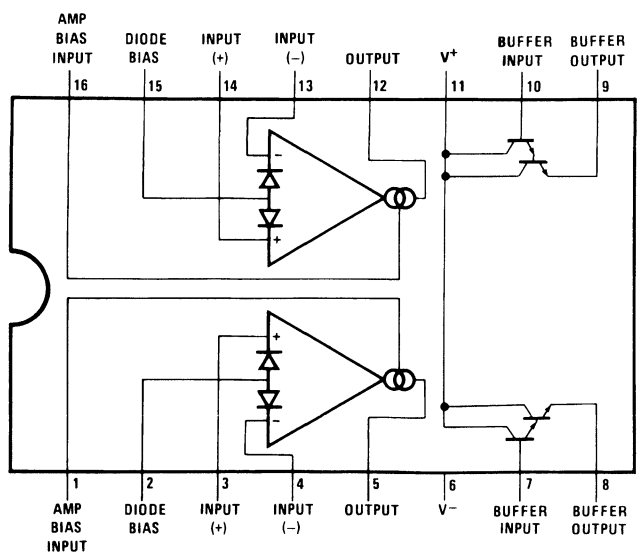
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal-to-noise ratio

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample-and-hold circuits

Connection Diagram

Dual-In-Line and Small Outline Packages



Top View
Order Number LM13700M, LM13700MX or LM13700N
See NS Package Number M16A or N16A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (Note 2)
LM13700 — 36 V_{DC} or ±18V
Power Dissipation (Note 3) T_A = 25°C
LM13700N — 570 mW
Differential Input Voltage — ±5V
Diode Bias Current (I_D) — 2 mA
Amplifier Bias Current (I_{ABC}) — 2 mA
Output Short Circuit Duration — Continuous
Buffer Output Current (Note 4) — 20 mA

Operating Temperature Range
LM13700N — 0°C to +70°C
DC Input Voltage — $+V_S$ to $-V_S$
Storage Temperature Range — −65°C to +150°C
Soldering Information
Dual-In-Line Package
Soldering (10 sec.) — 260°C
Small Outline Package
Vapor Phase (60 sec.) — 215°C
Infrared (15 sec.) — 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 5)

Parameter	Conditions	LM13700			Units
		Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4	mV
	Over Specified Temperature Range				
	I_{ABC} = 5 µA		0.3	4	
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 µA		0.5	5	mV
Input Offset Change	5 µA ≤ I_{ABC} ≤ 500 µA		0.1	3	mV
Input Offset Current			0.1	0.6	µA
Input Bias Current	Over Specified Temperature Range		0.4	5	µA
			1	8	
Forward		6700	9600	13000	µmho
Transconductance (g_m)	Over Specified Temperature Range	5400			
g_m Tracking			0.3		dB
Peak Output Current	R_L = 0, I_{ABC} = 5 µA		5		µA
	R_L = 0, I_{ABC} = 500 µA	350	500	650	
	R_L = 0, Over Specified Temp Range	300			
Peak Output Voltage					
Positive	R_L = ∞, 5 µA ≤ I_{ABC} ≤ 500 µA	+12	+14.2		V
Negative	R_L = ∞, 5 µA ≤ I_{ABC} ≤ 500 µA	−12	−14.4		V
Supply Current	I_{ABC} = 500 µA, Both Channels		2.6		mA
V_{OS} Sensitivity					
Positive	$\Delta V_{OS}/\Delta V^+$		20	150	µV/V
Negative	$\Delta V_{OS}/\Delta V^-$		20	150	µV/V
CMRR		80	110		dB
Common Mode Range		±12	±13.5		V
Crosstalk	Referred to Input (Note 6)		100		dB
	20 Hz < f < 20 kHz				
Differential Input Current	I_{ABC} = 0, Input = ±4V		0.02	100	nA
Leakage Current	I_{ABC} = 0 (Refer to Test Circuit)		0.2	100	nA
Input Resistance		10	26		kΩ
Open Loop Bandwidth			2		MHz
Slew Rate	Unity Gain Compensated		50		V/µs
Buffer Input Current	(Note 6)		0.5	2	µA
Peak Buffer Output Voltage	(Note 6)	10			V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For selections to a supply voltage above ±22V, contact factory.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at ambient temperatures above 25˚C, the device must be derated based on a 150˚C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90˚C/W; LM13700M, 110˚C/W.

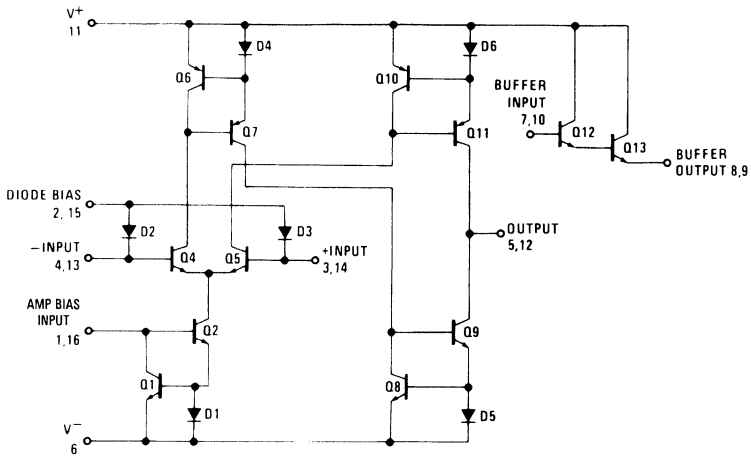
Note 4: Buffer output current should be limited so as to not exceed package dissipation.

Note 5: These specifications apply for V_S = ±15V, T_A = 25˚C, amplifier bias current (I_{ABC}) = 500 µA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 6: These specifications apply for V_S = ±15V, I_{ABC} = 500 µA, R_{OUT} = 5 kΩ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

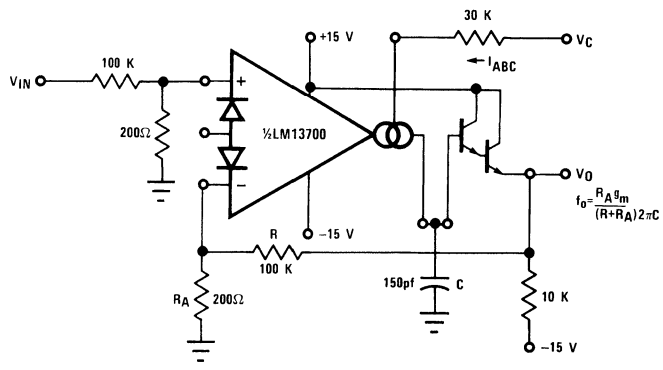
Schematic Diagram

One Operational Transconductance Amplifier



DS007981-1

Typical Application



DS007981-18

Voltage Controlled Low-Pass Filter

National Semiconductor

LM101A/LM201A/LM301A Operational Amplifiers

General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

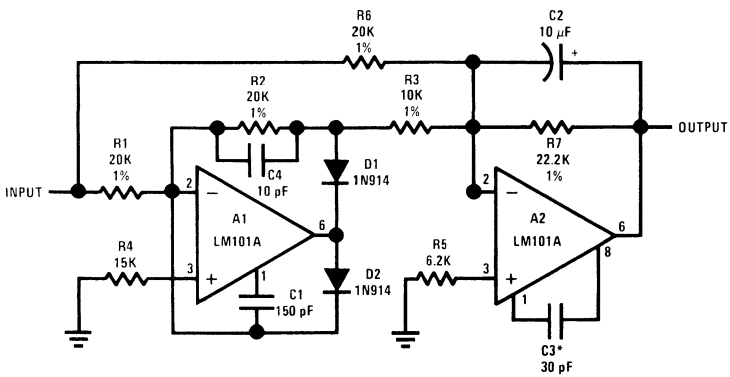
- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

The LM101A is guaranteed over a temperature range of −55°C to +125°C, the LM201A from −25°C to +85°C, and the LM301A from 0°C to +70°C.

Fast AC/DC Converter (Note 1)



Note 1: Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM101A/LM201A	LM301A
Supply Voltage	±22V	±18V
Differential Input Voltage	±30V	±30V
Input Voltage (Note 3)	±15V	±15V
Output Short Circuit Duration (Note 4)	Continuous	Continuous
Operating Ambient Temp. Range	−55°C to +125°C (LM101A) −25°C to +85°C (LM201A)	0°C to +70°C
T_J Max		
H-Package	150°C	100°C
N-Package	150°C	100°C
J-Package	150°C	100°C
Power Dissipation at T_A = 25°C		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	700 mW
N-Package	900 mW	500 mW
J-Package	1000 mW	650 mW
Thermal Resistance (Typical) θ_{jA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	67°C/W	67°C/W
N Package	135°C/W	135°C/W
J-Package	110°C/W	110°CmW
(Typical) θ_{jC}		
H-Package	25°C/W	25°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)		
Metal Can or Ceramic	300°C	300°C
Plastic	260°C	260°C
ESD Tolerance (Note 7)	2000V	2000V

Electrical Characteristics (Note 5)

$T_A = T_J$

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, $R_S \le 50\ k\Omega$			0.7	2.0		2.0	7.5	mV
Input Offset Current	T_A = 25°C			1.5	10		3.0	50	nA
Input Bias Current	T_A = 25°C			30	75		70	250	nA
Input Resistance	T_A = 25°C		1.5	4.0		0.5	2.0		MΩ
Supply Current	T_A = 25°C	V_S = ±20V		1.8	3.0				mA
		V_S = ±15V					1.8	3.0	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \ge 2\ k\Omega$		50	160		25	160		V/mV
Input Offset Voltage	$R_S \le 50\ k\Omega$				3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S \le 50\ k\Omega$			3.0	15		6.0	30	µV/°C
Input Offset Current					20			70	nA
Average Temperature Coefficient of Input Offset Current	25°C ≤ $T_A \le T_{MAX}$			0.01	0.1		0.01	0.3	nA/°C
	$T_{MIN} \le T_A \le$ 25°C			0.02	0.2		0.02	0.6	nA/°C
Input Bias Current					0.1			0.3	µA
Supply Current	$T_A = T_{MAX}$, V_S = ±20V			1.2	2.5				mA

Electrical Characteristics (Note 5) (Continued)

$T_A = T_J$

Parameter	Conditions		LM101A/LM201A			LM301A			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L \geq 2k$		25			15			V/mV
Output Voltage Swing	$V_S = \pm15V$	R_L = 10 kΩ	±12	±14		±12	±14		V
		R_L = 2 kΩ	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm20V$		±15						V
	$V_S = \pm15V$			+15, −13		±12	+15, −13		V
Common-Mode Rejection Ratio	$R_S \leq 50$ kΩ		80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50$ kΩ		80	96		70	96		dB

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.Operating ratings indicate for which the device is functional, but do no guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 75°C for LM101A/LM201A, and 70°C and 55°C respectively for LM301A.

Note 5: Unless otherwise specified, these specifications apply for C1 = 30 pF, $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq +125°C$ (LM101A), $\pm5V \leq V_S \leq \pm20V$ and $-25°C \leq T_A \leq +85°C$ (LM201A), $\pm5V \leq V_S \leq \pm15V$ and $0°C \leq T_A \leq +70°C$ (LM301A).

Note 6: Refer to RETS101AX for LM101A military specifications and RETS101X for LM101 military specifications.

Note 7: Human body model, 100 pF discharged through 1.5 kΩ.

National Semiconductor

LM118/LM218/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over 150V/μs and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under 1 μs.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active filters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

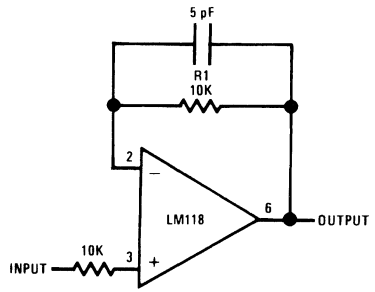
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a −25°C to +85°C temperature range. The LM318 is specified from 0°C to +70°C.

Features

- 15 MHz small signal bandwidth
- Guaranteed 50V/μs slew rate
- Maximum bias current of 250 nA
- Operates from supplies of ±5V to ±20V
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Fast Voltage Follower

(Note 1)



DS007766-13

Note 1: Do not hard-wire as voltage follower (R1 ≥ 5 kΩ)

Absolute Maximum Ratings (Note 7)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±20V
Power Dissipation (Note 2)	500 mW
Differential Input Current (Note 3)	±10 mA
Input Voltage (Note 4)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LM118	−55°C to +125°C
LM218	−25°C to +85°C
LM318	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	
Hermetic Package	300°C
Plastic Package	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.	
ESD Tolerance (Note 8)	2000V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM118/LM218			LM318			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C		2	4		4	10	mV
Input Offset Current	T_A = 25°C		6	50		30	200	nA
Input Bias Current	T_A = 25°C		120	250		150	500	nA
Input Resistance	T_A = 25°C	1	3		0.5	3		MΩ
Supply Current	T_A = 25°C		5	8		5	10	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \geq 2$ kΩ	50	200		25	200		V/mV
Slew Rate	T_A = 25°C, V_S = ±15V, A_V = 1 (Note 6)	50	70		50	70		V/μs
Small Signal Bandwidth	T_A = 25°C, V_S = ±15V		15			15		MHz
Input Offset Voltage				6			15	mV
Input Offset Current				100			300	nA
Input Bias Current				500			750	nA
Supply Current	T_A = 125°C		4.5	7				mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \geq 2$ kΩ	25			20			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 2 kΩ	±12	±13		±12	±13		V
Input Voltage Range	V_S = ±15V	±11.5			±11.5			V
Common-Mode Rejection Ratio		80	100		70	100		dB
Supply Voltage Rejection Ratio		70	80		65	80		dB

Note 2: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 5: These specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ +125°C (LM118), −25°C ≤ T_A ≤ +85°C (LM218), and 0°C ≤ T_A ≤ +70°C (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

Note 6: Slew rate is tested with V_S = ±15V. The LM118 is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/μs.

Note 7: Refer to RETS118X for LM118H and LM118J military specifications.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM12CL
80W Operational Amplifier

General Description

The LM12 is a power op amp capable of driving ±25V at ±10A while operating from ±30V supplies. The monolithic IC can deliver 80W of sine wave power into a 4Ω load with 0.01% distortion. Power bandwidth is 60 kHz. Further, a peak dissipation capability of 800W allows it to handle reactive loads such as transducers, actuators or small motors without derating. Important features include:

- input protection
- controlled turn on
- thermal limiting
- overvoltage shutdown
- output-current limiting
- dynamic safe-area protection

The IC delivers ±10A output current at any output voltage yet is completely protected against overloads, including shorts to the supplies. The dynamic safe-area protection is provided by instantaneous peak-temperature limiting within the power transistor array.

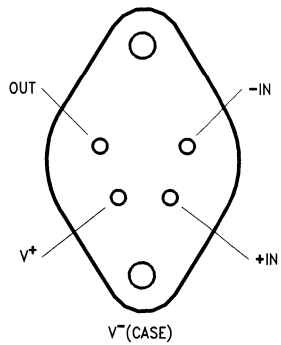
The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 14V. The output is also opened as the case temperature exceeds 150°C or as the supply voltage approaches the BV_{CEO} of the output transistors. The IC withstands overvoltages to 80V.

This monolithic op amp is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/µs, even as a follower. Distortion and capacitive-load stability rival that of the best designs using complementary output transistors. Further, the IC withstands large differential input voltages and is well behaved should the common-mode range be exceeded.

The LM12 establishes that monolithic ICs can deliver considerable output power without resorting to complex switching schemes. Devices can be paralleled or bridged for even greater output capability. Applications include operational power supplies, high-voltage regulators, high-quality audio amplifiers, tape-head positioners, x-y plotters or other servo-control systems.

The LM12 is supplied in a four-lead, TO-3 package with V– on the case. A gold-eutectic die-attach to a molybdenum interface is used to avoid thermal fatigue problems. The LM12 is specified for either military or commercial temperature range.

Connection Diagram

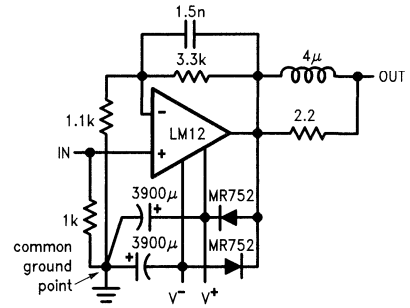


DS008704-1

4-pin glass epoxy TO-3 socket is available from AUGAT INC. Part number 8112-AG7

Bottom View
Order Number LM12CLK
See NS Package Number K04A

Typical Application*



DS008704-2

*Low distortion (0.01%) audio amplifier

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage (Note 1)	80V
Input Voltage	(Note 2)
Output Current	Internally Limited
Junction Temperature	(Note 3)
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Ratings

Total Supply Voltage	15V to 60V
Case Temperature (Note 4)	0°C to 70°C

Electrical Characteristics (Note 4)

Parameter	Conditions	Typ 25°C	LM12CL Limits	Units
Input Offset Voltage	$\pm 10V \le V_S \le \pm 0.5\ V_{MAX}$, $V_{CM} = 0$	2	15/**20**	mV (max)
Input Bias Current	$V- + 4V \le V_{CM} \le V+ -2V$	0.15	0.7/**1.0**	µA (max)
Input Offset Current	$V- +4V \le V_{CM} \le V+ -2V$	0.03	0.2/**0.3**	µA (max)
Common Mode Rejection	$V- +4V \le V_{CM} \le V+ -2V$	86	70/**65**	dB (min)
Power Supply Rejection	$V+ = 0.5\ V_{MAX}$, $-6V \ge V- \ge -0.5\ V_{MAX}$	90	70/**65**	dB (min)
	$V- = -0.5\ V_{MAX}$, $6V \le V+ \le 0.5\ V_{MAX}$	110	75/**70**	dB (min)
Output Saturation Threshold	t_{ON} = 1 ms, ΔV_{IN} = 5 (**10**) mV,			
	I_{OUT} = 1A	1.8	2.2/**2.5**	V (max)
	8A	4	5/**7**	V (max)
	10A	5		V (max)
Large Signal Voltage Gain	t_{ON} = 2 ms,			
	V_{SAT} = 2V, I_{OUT} = 0	100	30/**20**	V/mV (min)
	V_{SAT} = 8V, $R_L = 4\Omega$	50	15/**10**	V/mV (min)
Thermal Gradient Feedback	P_{DISS} = 50W, t_{ON} = 65 ms	30	100	µV/W (max)
Output-Current Limit	t_{ON} = 10 ms, V_{DISS} = 10V	13	16	A (max)
	t_{ON} = 100 ms, V_{DISS} = 58V	1.5	0.9/**0.6**	A (min)
		1.5	1.7	A (max)
Power Dissipation Rating	t_{ON} = 100 ms, V_{DISS} = 20V	100	80/**55**	W (min)
	V_{DISS} = 58V	80	52/**35**	W (min)
DC Thermal Resistance	(Note 5) V_{DISS} = 20V	2.3	2.9	°C/W (max)
	V_{DISS} = 58V	2.7	4.5	°C/W (max)
AC Thermal Resistance	(Note 5)	1.6	2.1	°C/W (max)
Supply Current	V_{OUT} = 0, I_{OUT} = 0	60	120/**140**	mA (max)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. The maximum voltage for which the LM12 is guaranteed to operate is given in the operating ratings and in Note 4. With inductive loads or output shorts, other restrictions described in applications section apply.

Note 2: Neither input should exceed the supply voltage by more than 50 volts nor should the voltage between one input and any other terminal exceed 60 volts.

Note 3: Operating junction temperature is internally limited near 225°C within the power transistor and 160°C for the control circuitry.

Note 4: The supply voltage is ±30V (V_{MAX} = 60V), unless otherwise specified. The voltage across the conducting output transistor (supply to output) is V_{DISS} and internal power dissipation is P_{DISS}. Temperature range is $0°C \le T_C \le 70°C$ where T_C is the case temperature. Standard typeface indicates limits at 25°C **while boldface type refers to limits or special conditions over full temperature range.** With no heat sink, the package will heat at a rate of 35°C/sec per 100W of internal dissipation.

Note 5: This thermal resistance is based upon a peak temperature of 200°C in the center of the power transistor and a case temperature of 25°C measured at the center of the package bottom. The maximum junction temperature of the control circuitry can be estimated based upon a dc thermal resistance of 0.9°C/W or an ac thermal resistance of 0.6°C/W for any operating voltage.

Although the output and supply leads are resistant to electrostatic discharges from handling, the input leads are not. The part should be treated accordingly.

National Semiconductor

LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

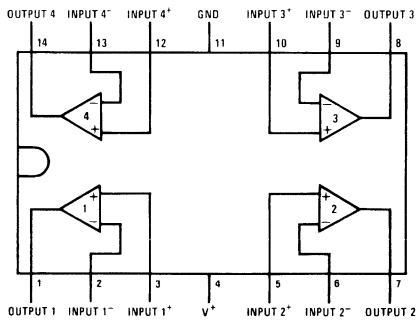
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3V to 32V
  or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 µA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ − 1.5V

Connection Diagram

Dual-In-Line Package



DS009299-1

Top View

Order Number LM124J, LM124AJ, LM124J/883 (Note 2), **LM124AJ/883** (Note 1), **LM224J, LM224AJ, LM324J, LM324M, LM324MX, LM324AM, LM324AMX, LM2902M, LM2902MX, LM324N, LM324AN, LM324MT, LM324MTX or LM2902N LM124AJRQML and LM124AJRQMLV**(Note 3)

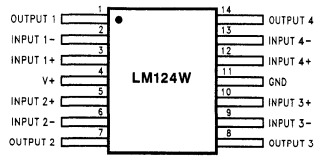
See NS Package Number J14A, M14A or N14A

Note 1: LM124A available per JM38510/11006

Note 2: LM124 available per JM38510/11005

Connection Diagram (Continued)

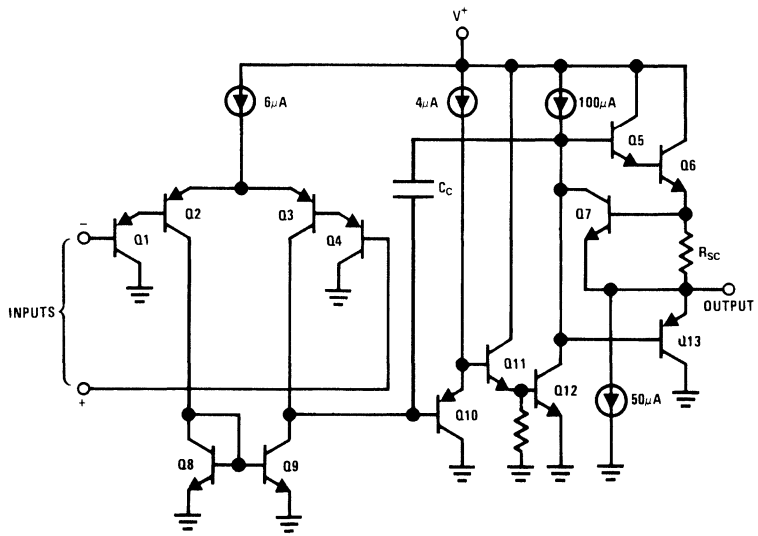
Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device



DS009299-33

Order Number LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
LM124AWRQML and LM124AWRQMLV(Note 3)
See NS Package Number W14B
LM124AWGRQML and LM124AWGRQMLV(Note 3)
See NS Package Number WG14A

Schematic Diagram (Each Amplifier)



DS009299-2

Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current		
(V_{IN} < −0.3V) (Note 6)	50 mA	50 mA
Power Dissipation (Note 4)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND		
(One Amplifier) (Note 5)		
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 13)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25^\circ C$		1	2		1	3		2	3	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		20	50		40	80		45	100	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25^\circ C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range										
	$R_L = \infty$ On All Op Amps										mA
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5	3		1.5	3		1.5	3	
	$V^+ = 5V$		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2k\Omega$, ($V_O = 1V$ to 11V), $T_A = 25^\circ C$	50	100		50	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25^\circ C$	70	85		70	85		65	85		dB

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter		Conditions		LM124A			LM224A			LM324A			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V), T_A = 25°C		65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 5) V^+ = 15V, T_A = 25°C			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				4			4			5	mV
V_{OS} Drift		R_S = 0Ω			7	20		7	20		7	30	µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				30			30			75	nA
I_{OS} Drift		R_S = 0Ω			10	200		10	200		10	300	pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	100		40	100		40	200	nA
Input Common-Mode Voltage Range (Note 10)		V^+ = +30V (LM2902, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			25			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V (LM2902, V^+ = 26V)	R_L = 2 kΩ	26			26			26			V
			R_L = 10 kΩ	27	28		27	28		27	28		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	10	15		5	8		5	8		

Electrical Characteristics

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter	Conditions	LM124/LM224			LM324			LM2902			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) T_A = 25°C		2	5		2	7		2	7	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		45	150		45	250		45	250	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		3	30		5	50		5	50	nA
Input Common-Mode Voltage Range (Note 10)	V^+ = 30V, (LM2902, V^+ = 26V), T_A = 25°C	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V
Supply Current	Over Full Temperature Range R_L = ∞ On All Op Amps										mA
	V^+ = 30V (LM2902 V^+ = 26V)		1.5	3		1.5	3		1.5	3	
	V^+ = 5V		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	V^+ = 15V, $R_L \geq$ 2kΩ, (V_O = 1V to 11V), T_A = 25°C	50	100		25	100		25	100		V/mV
Common-Mode Rejection Ratio	DC, V_{CM} = 0V to V^+ − 1.5V, T_A = 25°C	70	85		65	85		50	70		dB
Power Supply Rejection Ratio	V^+ = 5V to 30V (LM2902, V^+ = 5V to 26V),	65	100		65	100		50	100		dB

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 7), unless otherwise stated

Parameter		Conditions		LM124/LM224			LM324			LM2902			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		T_A = 25°C											
Amplifier-to-Amplifier Coupling (Note 11)		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred)			−120			−120			−120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C		10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 200 mV, T_A = 25°C		12	50		12	50		12	50		µA
Short Circuit to Ground		(Note 5) V^+ = 15V, T_A = 25°C			40	60		40	60		40	60	mA
Input Offset Voltage		(Note 8)				7			9			10	mV
V_{OS} Drift		R_S = 0Ω			7			7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V				100			150		45	200	nA
I_{OS} Drift		R_S = 0Ω			10			10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$			40	300		40	500		40	500	nA
Input Common-Mode Voltage Range (Note 10)		V^+ = +30V (LM2902, V^+ = 26V)		0		V^+−2	0		V^+−2	0		V^+−2	V
Large Signal Voltage Gain		V^+ = +15V (V_OSwing = 1V to 11V) $R_L \geq 2$ kΩ		25			15			15			V/mV
Output Voltage Swing	V_{OH}	V^+ = 30V (LM2902, V^+ = 26V)	R_L = 2 kΩ	26			26			22			V
			R_L = 10 kΩ	27	28		27	28		23	24		
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	100	mV
Output Current	Source	V_O = 2V	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V	10	20		10	20		10	20		mA
	Sink		V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V	5	8		5	8		5	8		

Note 4: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers — use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

Note 5: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 7: These specifications are limited to −55°C ≤ T_A ≤ +125°C for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 8: $V_O \cong$ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V) for LM2902, V^+ from 5V to 26V.

Note 9: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 10: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ − 1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902), independent of the magnitude of V^+.

Note 11: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 12: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

Note 13: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM1458/LM1558
Dual Operational Amplifier

General Description

The LM1458 and the LM1558 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

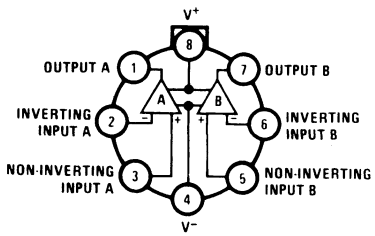
The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to +70°C instead of −55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead can and 8-lead mini DIP
- No latch up when input common mode range is exceeded

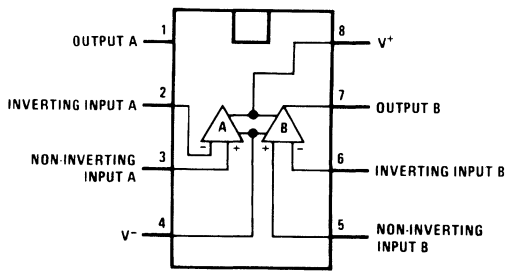
Connection Diagrams

Metal Can Package



Top View
Order Number LM1558H, LM1558H/883 or LM1458H
See NS Package Number H08C

Dual-In-Line Package



Top View
Order Number LM1558J/883, LM1458M, LM1458MX or LM1458N
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 5)

Supply Voltage	
LM1558	±22V
LM1458	±18V
Power Dissipation (Note 2)	
LM1558H/LM1458H	500 mW
LM1458N	400 mW
Differential Input Voltage	±30V
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	
LM1558	−55°C to +125°C
LM1458	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 6)	300V

Electrical Characteristics (Note 4)

Parameter	Conditions	LM1558			LM1458			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, $R_S \le 10$ kΩ		1.0	5.0		1.0	6.0	mV
Input Offset Current	T_A = 25°C		80	200		80	200	nA
Input Bias Current	T_A = 25°C		200	500		200	500	nA
Input Resistance	T_A = 25°C	0.3	1.0		0.3	1.0		MΩ
Supply Current Both Amplifiers	T_A = 25°C, V_S = ±15V		3.0	5.0		3.0	5.6	mA
Large Signal Voltage Gain	T_A = 25°C, V_S = ±15V V_{OUT} = ±10V, $R_L \ge 2$ kΩ	50	160		20	160		V/mV
Input Offset Voltage	$R_S \le 10$ kΩ			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V $R_L \ge$ kΩ	25			15			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±14		±12	±14		V
	R_L = 2 kΩ	±10	±13		±10	±13		V
Input Voltage Range	V_S = ±15V	±12			±12			V
Common Mode Rejection Ratio	$R_S \le 10$ kΩ	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \le 10$ kΩ	77	96		77	96		dB

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 20°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

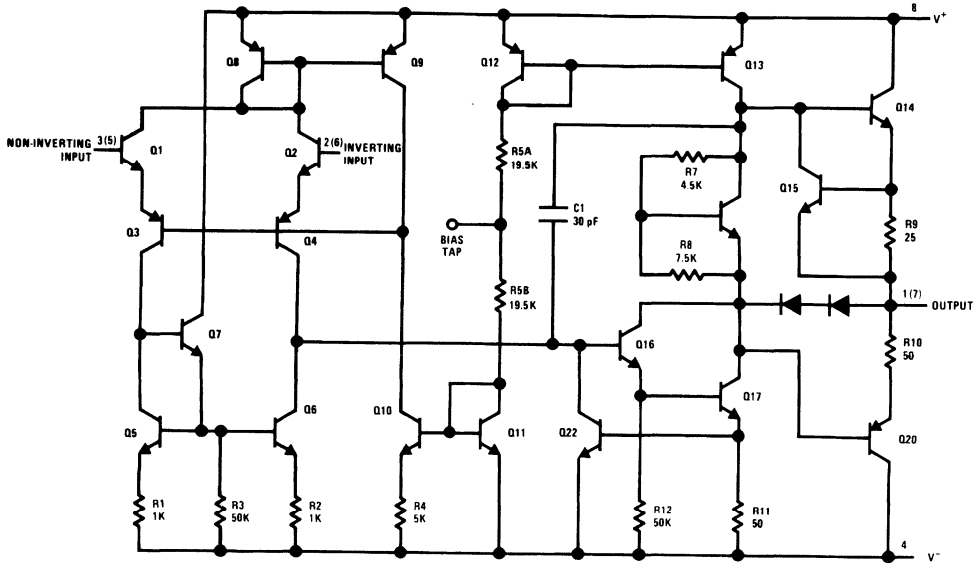
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for V_S = ±15V and −55°C ≤ T_A < 125°C, unless otherwise specified. With the LM1458, however, all specifications are limited to 0°C ≤ T_A ≤ 70°C and V_S = ±15V.

Note 5: Refer to RETS 1558V for LM1558J and LM1558H military specifications.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



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Numbers in parentheses are pin numbers for amplifier B.

National Semiconductor

LM146/LM346
Programmable Quad Operational Amplifiers

General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

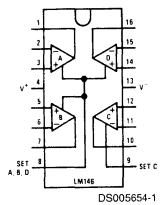
Features

(I_{SET}=10 µA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current: 350 µA/amplifier
- Guaranteed gain bandwidth product: 0.8 MHz min
- Large DC voltage gain: 120 dB
- Low noise voltage: 28 **nV/√Hz**
- Wide power supply range: ±1.5V to ±22V
- Class AB output stage–*no crossover distortion*
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagram

Dual-In-Line Package



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Top View
Order Number LM146J, LM146J/883, LM346M,LM346MX or LM346N
See NS Package Number J16A, M16A or N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 µA)

Gain Bandwidth Product = 1 MHz (I_{SET}/10 µA)

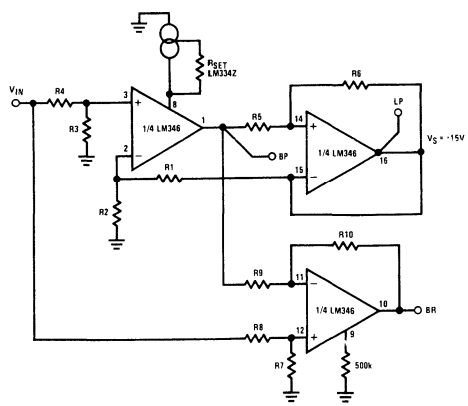
Slew Rate = 0.4V/µs (I_{SET}/10 µA)

Input Bias Current ≅ 50 nA (I_{SET}/10 µA)

I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Capacitorless Active Filters (Basic Circuit)



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Absolute Maximum Ratings (Notes 1, 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM146	LM346
Supply Voltage	±22V	±18V
Differential Input Voltage (Note 1)	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW
Output Short-Circuit Duration (Note 3)	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C
Maximum Junction Temperature	150°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Thermal Resistance (θ_{jA}), (Note 2)		
Cavity DIP (J) Pd	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W
Small Outline (M) θ_{jA}		115°C/W
Molded DIP (N) Pd		500 mW
θ_{jA}		90°C/W
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	+260°C	+260°C
Small Outline Package		
Vapor Phase (60 seconds)	+215°C	+215°C
Infrared (15 seconds)	+220°C	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

DC Electrical Characteristics

(V_S=±15V, I_{SET}=10 μA), (Note 4)

Parameter	Conditions	LM146			LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{CM}=0V, R_S≤50Ω, T_A=25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM}=0V, T_A=25°C		2	20		2	100	nA
Input Bias Current	V_{CM}=0V, T_A=25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A=25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L=10 kΩ, ΔV_{OUT}=±10V, T_A=25°C	100	1000		50	1000		V/mV
Input CM Range	T_A=25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	R_S≤10 kΩ, T_A=25°C	80	100		70	100		dB
Power Supply Rejection Ratio	R_S≤10 kΩ, T_A=25°C, V_S = ±5 to ±15V	80	100		74	100		dB
Output Voltage Swing	R_L≥10 kΩ, T_A=25°C	±12	±14		±12	±14		V
Short-Circuit	T_A=25°C	5	20	35	5	20	35	mA
Gain Bandwidth Product	T_A=25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A=25°C		60			60		Deg
Slew Rate	T_A=25°C		0.4			0.4		V/μs
Input Noise Voltage	f=1 kHz, T_A=25°C		28			28		$nV/\sqrt{Hz}$
Channel Separation	R_L=10 kΩ, ΔV_{OUT}=0V to ±12V, T_A=25°C		120			120		dB
Input Resistance	T_A=25°C		1.0			1.0		MΩ
Input Capacitance	T_A=25°C		2.0			2.0		pF

DC Electrical Characteristics (Continued)

(V_S=±15V, I_{SET}=10 µA), (Note 4)

Parameter	Conditions	LM146			LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{CM}=0V, R_S≤50Ω		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM}=0V		2	25		2	100	nA
Input Bias Current	V_{CM}=0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.7	2.2		1.7	2.5	mA
Large Signal Voltage Gain	R_L=10 kΩ, ΔV_{OUT}=±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	R_S≤50Ω	70	100		70	100		dB
Power Supply Rejection Ratio	R_S≤50Ω, V_S = ±5V to ±15V	76	100		74	100		dB
Output Voltage Swing	R_L≥10 kΩ	±12	±14		±12	±14		V

DC Electrical Characteristic

(V_S=±15V, I_{SET}=10 µA)

Parameter	Conditions	LM146			LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{CM}=0V, R_S≤50Ω, T_A=25°C		0.5	5		0.5	7	mV
Input Bias Current	V_{CM}=0V, T_A=25°C		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	T_A=25°C		140	250		140	300	µA
Gain Bandwidth Product	T_A=25°C	80	100		50	100		kHz

DC Electrical Characteristics

(V_S=±1.5V, I_{SET}=10 µA)

Parameter	Conditions	LM146			LM346			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	V_{CM}=0V, R_S≤50Ω, T_A=25°C		0.5	5		0.5	7	mV
Input CM Range	T_A=25°C	±0.7			±0.7			V
CM Rejection Ratio	R_S≤50Ω, T_A=25°C		80			80		dB
Output Voltage Swing	R_L≥10 kΩ, T_A=25°C	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d=(T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Note 5: Refer to RETS146X for LM146J military specifications.

National Semiconductor

LM148/LM248/LM348
Quad 741 Op Amps
LM149
Wide Band Decompensated ($A_{V\ (MIN)}$ = 5)

General Description

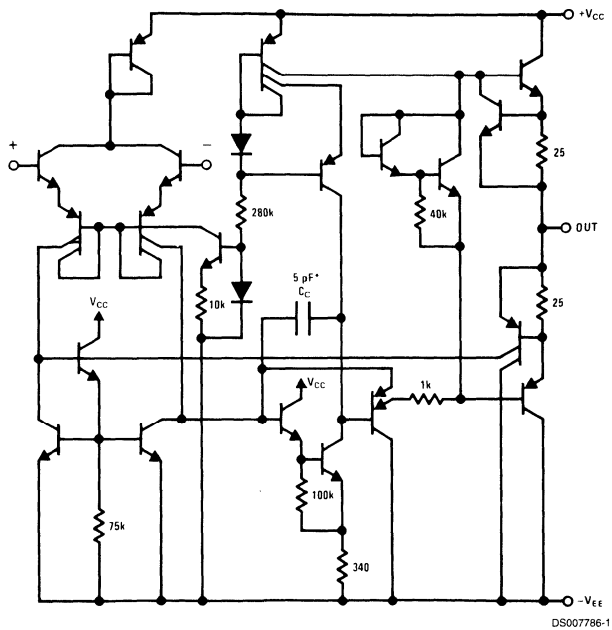
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required. For lower power refer to LF444.

Features

- 741 op amp operating characteristics
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Overload protection for inputs and outputs
- Low supply current drain: 0.6 mA/Amplifier
- Low input offset voltage: 1 mV
- Low input offset current: 4 nA
- Low input bias current 30 nA
- High degree of isolation between amplifiers: 120 dB
- Gain bandwidth product
- LM148 (unity gain): 1.0 MHz
- LM149 ($A_V \geq 5$): 4 MHz

Schematic Diagram



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* 1 pF in the LM149

Absolute Maximum Ratings (Note 4)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM148/LM149	LM248	LM348
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage	±44V	±36V	±36V
Output Short Circuit Duration (Note 1)	Continuous	Continuous	Continuous
Power Dissipation (P_d at 25°C) and Thermal Resistance (θ_{jA}), (Note 2)			
Molded DIP (N) P_d	—	—	750 mW
θ_{jA}	—	—	100°C/W
Cavity DIP (J) P_d	1100 mW	800 mW	700 mW
θ_{JA}	110°C/W	110°C/W	110°C/W
Maximum Junction Temperature (T_{jMAX})	150°C	110°C	100°C
Operating Temperature Range	$-55°C \le T_A \le +125°C$	$-25°C \le T_A \le +85°C$	$0°C \le T_A \le +70°C$
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.) Ceramic	300°C	300°C	300°C
Lead Temperature (Soldering, 10 sec.) Plastic			260°C
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)	260°C	260°C	260°C
Small Outline Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	220°C	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD tolerance (Note 5)	500V	500V	500V

Electrical Characteristics

(Note 3)

Parameter	Conditions	LM148/LM149			LM248			LM348			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, $R_S \le 10\ k\Omega$		1.0	5.0		1.0	6.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		4	25		4	50		4	50	nA
Input Bias Current	$T_A = 25°C$		30	100		30	200		30	200	nA
Input Resistance	$T_A = 25°C$	0.8	2.5		0.8	2.5		0.8	2.5		MΩ
Supply Current All Amplifiers	$T_A = 25°C$, $V_S = \pm15V$		2.4	3.6		2.4	4.5		2.4	4.5	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L \ge 2\ k\Omega$	50	160		25	160		25	160		V/mV
Amplifier to Amplifier Coupling	$T_A = 25°C$, f = 1 Hz to 20 kHz (Input Referred) See Crosstalk Test Circuit		−120			−120			−120		dB
Small Signal Bandwidth	LM148 Series $T_A = 25°C$		1.0			1.0			1.0		MHz
	LM149 Series		4.0			4.0			4.0		MHz
Phase Margin	LM148 Series ($A_V = 1$) $T_A = 25°C$		60			60			60		degrees
	LM149 Series ($A_V = 5$)		60			60			60		degrees
Slew Rate	LM148 Series ($A_V = 1$) $T_A = 25°C$		0.5			0.5			0.5		V/μs
	LM149 Series ($A_V = 5$)		2.0			2.0			2.0		V/μs
Output Short Circuit Current	$T_A = 25°C$		25			25			25		mA
Input Offset Voltage	$R_S \le 10\ k\Omega$			6.0			7.5			7.5	mV
Input Offset Current				75			125			100	nA

Electrical Characteristics (Continued)

(Note 3)

Parameter	Conditions	LM148/LM149			LM248			LM348			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Bias Current				325			500			400	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, R_L > 2 kΩ	25			15			15			V/mV
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13		±12	±13		±12	±13		V
	R_L = 2 kΩ	±10	±12		±10	±12		±10	±12		V
Input Voltage Range	V_S = ±15V	±12			±12			±12			V
Common-Mode Rejection Ratio	R_S ≤ 10 kΩ	70	90		70	90		70	90		dB
Supply Voltage Rejection	R_S ≤ 10 kΩ, ±5V ≤ V_S ≤ ±15V	77	96		77	96		77	96		dB

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

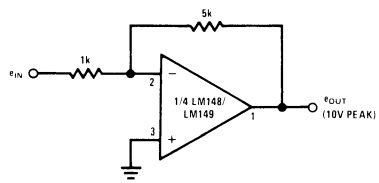
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dicated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25˚C P_{dMAX}, whichever is less.

Note 3: These specifications apply for V_S = ±15V and over the absolute maximum operating temperature range ($T_L \le T_A \le T_H$) unless otherwise noted.

Note 4: Refer to RETS 148X for LM148 military specifications and refer to RETS 149X for LM149 military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Cross Talk Test Circuit



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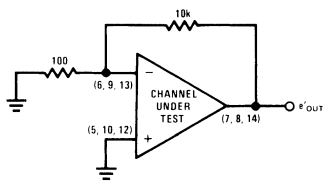

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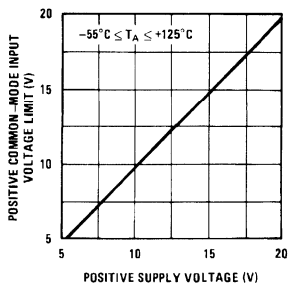

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V_S = ±15V

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

National Semiconductor

LM158/LM258/LM358/LM2904
Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

The LM358 is also available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

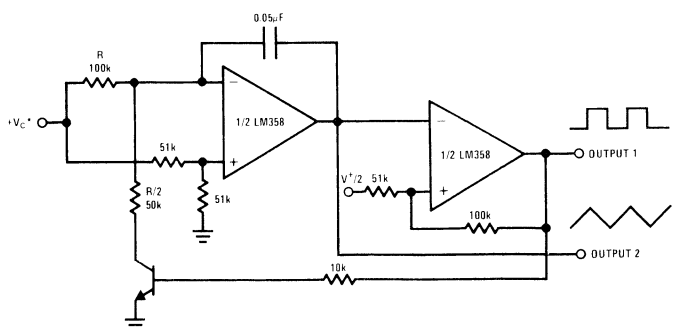
Advantages

- Two internally compensated op amps
- Eliminates need for dual supplies
- Allows direct sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual op amp

Features

- Available in 8-Bump micro SMD chip sized package, (See AN-1112)
- Internally frequency compensated for unity gain
- Large dc voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz (temperature compensated)
- Wide power supply range:
  — Single supply: 3V to 32V
  — or dual supplies: ±1.5V to ±16V
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage: 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing: 0V to V^+− 1.5V

Voltage Controlled Oscillator (VCO)



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Absolute Maximum Ratings (Note 9)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP	830 mW	830 mW
Metal Can	550 mW	
Small Outline Package (M)	530 mW	530 mW
micro SMD	435mW	
Output Short-Circuit to GND		
(One Amplifier) (Note 2)		
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3V$) (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature, DIP		
(Soldering, 10 seconds)	260°C	260°C
Lead Temperature, Metal Can		
(Soldering, 10 seconds)	300°C	300°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 10)	250V	250V

Electrical Characteristics

$V^+ = +5.0V$, unless otherwise stated

Parameter	Conditions	LM158A			LM358A			LM158/LM258			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5), $T_A = 25^\circ C$		1	2		2	3		2	5	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^\circ C$, $V_{CM} = 0V$, (Note 6)		20	50		45	100		45	150	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		2	10		5	30		3	30	nA
Input Common-Mode Voltage Range	$V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25^\circ C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps										
	$V^+ = 30V$ (LM2904 $V^+ = 26V$)		1	2		1	2		1	2	mA
	$V^+ = 5V$		0.5	1.2		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, unless otherwise stated

Parameter	Conditions	LM358			LM2904			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 5) , T_A = 25°C		2	7		2	7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C, V_{CM} = 0V, (Note 6)		45	250		45	250	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V, T_A = 25°C		5	50		5	50	nA
Input Common-Mode Voltage Range	V^+ = 30V, (Note 7) (LM2904, V^+ = 26V), T_A = 25°C	0		V^+–1.5	0		V^+–1.5	V
Supply Current	Over Full Temperature Range $R_L = \infty$ on All Op Amps							
	V^+ = 30V (LM2904 V^+ = 26V)		1	2		1	2	mA
	V^+ = 5V		0.5	1.2		0.5	1.2	mA

Electrical Characteristics

V^+ = +5.0V, (Note 4), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2\ k\Omega$, (For V_O = 1V to 11V)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to V^+–1.5V	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 8)		–120			–120			–120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V, V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V, T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 2), V^+ = 15V		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7	mV
Input Offset Voltage Drift		R_S = 0Ω		7	15		7	20		7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		R_S = 0Ω		10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 7) (LM2904, V^+ = 26V)	0		V^+–2	0		V^+–2	0		V^+–2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 4), unless otherwise stated

Parameter		Conditions		LM158A			LM358A			LM158/LM258			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		25			15			25			V/mV
Output Voltage Swing	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			26			26			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		27	28		27	28		V
	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	20		5	20	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		10	15		5	8		5	8		mA

Electrical Characteristics

V^+ = +5.0V, (Note 4), unless otherwise stated

Parameter		Conditions	LM358			LM2904			Units
			Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = 15V, T_A = 25°C, $R_L \geq 2\ k\Omega$, (For V_O = 1V to 11V)	25	100		25	100		V/mV
Common-Mode Rejection Ratio		T_A = 25°C, V_{CM} = 0V to V^+–1.5V	65	85		50	70		dB
Power Supply Rejection Ratio		V^+ = 5V to 30V (LM2904, V^+ = 5V to 26V), T_A = 25°C	65	100		50	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, T_A = 25°C (Input Referred), (Note 8)		–120			–120		dB
Output Current	Source	V_{IN}^+ = 1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V, T_A = 25°C	20	40		20	40		mA
	Sink	V_{IN}^- = 1V, V_{IN}^+ = 0V V^+ = 15V, T_A = 25°C, V_O = 2V	10	20		10	20		mA
		V_{IN}^- = 1V, V_{IN}^+ = 0V T_A = 25°C, V_O = 200 mV, V^+ = 15V	12	50		12	50		µA
Short Circuit to Ground		T_A = 25°C, (Note 2), V^+ = 15V		40	60		40	60	mA
Input Offset Voltage		(Note 5)			9			10	mV
Input Offset Voltage Drift		R_S = 0Ω		7			7		µV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			150		45	200	nA
Input Offset Current Drift		R_S = 0Ω		10			10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	500		40	500	nA
Input Common-Mode Voltage Range		V^+ = 30 V, (Note 7) (LM2904, V^+ = 26V)	0		V^+–2	0		V^+ –2	V

Electrical Characteristics (Continued)

V^+ = +5.0V, (Note 4), unless otherwise stated

Parameter		Conditions		LM358			LM2904			Units
				Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		V^+ = +15V (V_O = 1V to 11V) $R_L \geq 2\ k\Omega$		15			15			V/mV
Output Voltage	V_{OH}	V^+ = +30V	R_L = 2 kΩ	26			22			V
		(LM2904, V^+ = 26V)	R_L = 10 kΩ	27	28		23	24		V
Swing	V_{OL}	V^+ = 5V, R_L = 10 kΩ			5	20		5	100	mV
Output Current	Source	V_{IN}^+ = +1V, V_{IN}^- = 0V, V^+ = 15V, V_O = 2V		10	20		10	20		mA
	Sink	V_{IN}^- = +1V, V_{IN}^+ = 0V, V^+ = 15V, V_O = 2V		5	8		5	8		mA

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 120°C/W for MDIP, 182°C/W for Metal Can, 189°C/W for Small Outline package, and 230°C/W for micro SMD, which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM358/LM358A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2904 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4V$, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ −1.5V) at 25°C. For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2904), independent of the magnitude of V^+.

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

Note 10: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM321
Low Power Single Op Amp

General Description

The LM321 brings performance and economy to low power systems. With a high unity gain frequency and a guaranteed 0.4V/µs slew rate, the quiescent current is only 430µA/amplifier (5V). The input common mode range includes ground and therefore the device is able to operate in single supply applications as well as in dual supply applications. It is also capable of comfortably driving large capacitive loads.

The LM321 is available in the SOT23-5 package. Overall the LM321 is a low power, wide supply range performance op amp that can be designed into a wide range of applications at an economical price without sacrificing valuable board space.

Features

(V_{CC} = 5V, T_A = 25°C. Typical values unless specified).

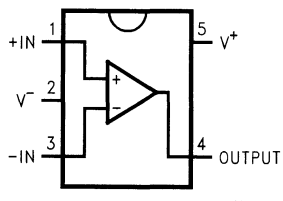
- Gain-Bandwidth product 1MHz
- Low supply current 430µA
- Low input bias current 45nA
- Wide supply voltage range +3V to +32V
- Stable with high capacitive loads
- Single version of LM324

Applications

- Chargers
- Power supplies
- Industrial: controls, instruments
- Desktops
- Communications infrastructure

Connection Diagram

SOT23-5



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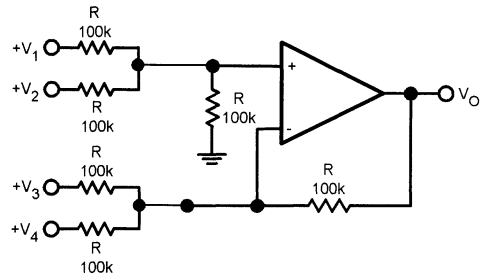
Top View

Application Circuit

DC Summing Amplifier
($V_{IN's} \geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)



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Where: $V_0 = V_1 + V_2 - V_3 - V_4$, $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LM321MF	A63A	1k Units Tape and Reel	MF05A
	LM321MFX		3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Input Current (V_{IN} < −0.3V) (Note 6)	50mA
Supply Voltage (V^+ - V^-)	32V
Input Voltage	−0.3V to +32V
Output Short Circuit to GND, $V^+ \leq 15V$ and $T_A = 25°C$ (Note 2)	Continuous
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 3)	150°C
Mounting Temperature	
Lead Temp (Soldering, 10 sec)	260°C
Infrared (10 sec)	215°C
Thermal Resistance to Ambient (θ_{JA})	265°C/W
ESD Tolerance (Note 10)	300V

Operating Ratings (Note 1)

Temperature Range	−40°C to 85°C
Supply Voltage	3V to 30V

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at $T_A = 25°C$; $V^+ = 5V$, $V^- = 0V$, $V_O = 1.4V$. **Boldface** limits apply at temperature extremes.

Symbol	Parameter		Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage		(Note 7)		2	7 **9**	mV
I_{OS}	Input Offset Current				5	50 **150**	nA
I_B	Input Bias Current (Note 8)				45	250 **500**	nA
V_{CM}	Input Common-Mode Voltage Range		$V^+ = 30V$ (Note 9) For CMRR > = 50dB	0		V^+ - 1.5 **V^+ -2**	V
A_V	Large Signal Voltage Gain		($V^+ = 15V$, $R_L = 2k\Omega$ $V_O = 1.4V$ to 11.4V)	25 **15**	100		V/mV
PSRR	Power Supply Rejection Ratio		$R_S \leq 10k\Omega$, $V^+ \leq 5V$ to 30V	65	100		dB
CMRR	Common Mode Rejection Ratio		$R_S \leq 10k\Omega$	65	85		dB
V_O	Output Swing	V_{OH}	$V^+ = 30V$, $R_L = 2k\Omega$	**26**			V
			$V^+ = 30V$, $R_L = 10k\Omega$	**27**	**28**		
		V_{OL}	$V^+ = 5V$, $R_L = 10k\Omega$		**5**	**20**	mV
I_S	Supply Current, No Load		$V^+ = 5V$		0.430 **0.7**	1.15 **1.2**	mA
			$V^+ = 30V$		0.660 **1.5**	2.85 **3**	
I_{SOURCE}	Output Current Sourcing		$V_{ID} = +1V$, $V^+ = 15V$, $V_O = 2V$	20 **10**	40 **20**		mA
I_{SINK}	Output Current Sinking		$V_{ID} = -1V$ $V^+ = 15V$, $V_O = 2V$	10 **5**	20 **8**		mA
			$V_{ID} = -1V$ $V^+ = 15V$, $V_O = 0.2V$	12	100		µA
I_O	Output Short Circuit to Ground (Note 2)		$V^+ = 15V$		40	85	mA
SR	Slew Rate		$V^+ = 15V$, $R_L = 2k\Omega$, $V_{IN} = 0.5$ to 3V $C_L = 100pF$, Unity Gain		0.4		V/µs
GBW	Gain Bandwidth Product		$V^+ = 30V$, f = 100kHz, $V_{IN} = 10mV$, $R_L = 2k\Omega$, $C_L = 100pF$		1		MHz
ϕm	Phase Margin				60		deg

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_A = 25°C; V^+ = 5V, V^- = 0V, V_O = 1.4V. **Boldface** limits apply at temperature extremes. (Continued)

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
THD	Total Harmonic Distortion	f = 1kHz, A_V = 20dB R_L = 2kΩ, V_O = $2V_{PP}$, C_L = 100pF, V^+ = 30V		0.015		%
e_n	Equivalent Input Noise Voltage	f = 1kHz, R_S = 100Ω V^+ = 30V		40		nV/$\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Short circuits from the output V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground the maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.36V (at 25°C).

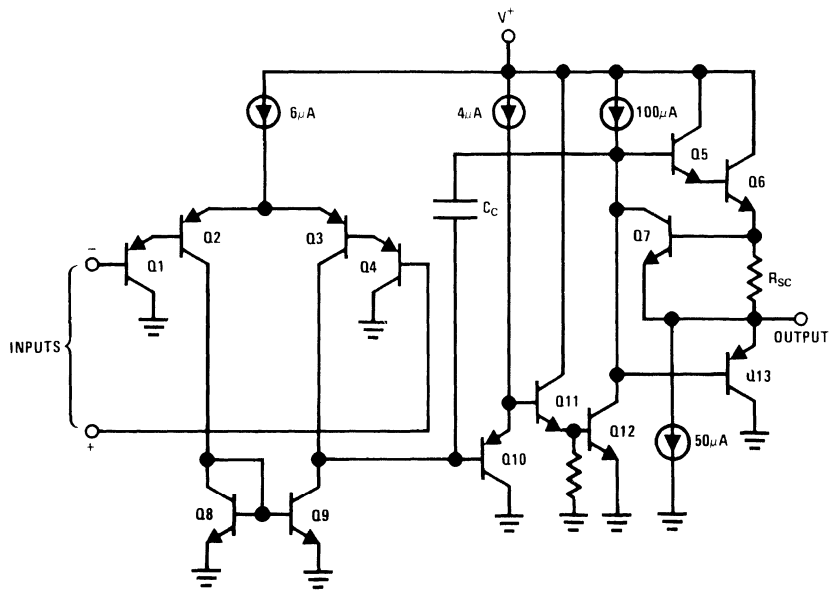
Note 7: V_O ≅ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ - 1.5V) at 25°C.

Note 8: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 9: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ - 1.5V at 25°C, but either or both inputs can go to +32V without damage, independent of the magnitude of V^+.

Note 10: Human Body Model, 1.5kΩ in series with 100pF.

Simplified Schematic



National Semiconductor

LM359
Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

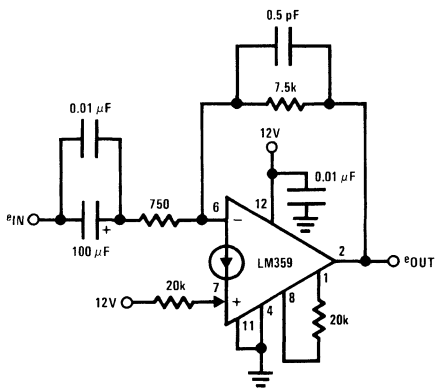
Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product (I_{SET} = 0.5 mA)
  400 MHz for A_V = 10 to 100
  30 MHz for A_V = 1
- High slew rate (I_{SET} = 0.5 mA)
  60 V/μs for A_V = 10 to 100
  30 V/μs for A_V = 1
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to V_{CC} − 2V
- Low spot noise, $6\ nV/\sqrt{Hz}$, for f > 1 kHz

Typical Application

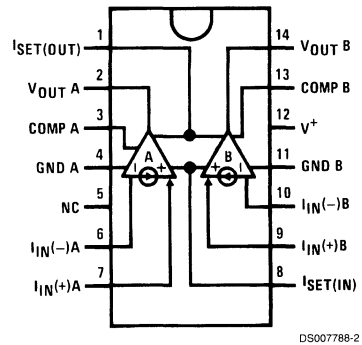


DS007788-1

- A_V = 20 dB
- −3 dB bandwidth = 2.5 Hz to 25 MHz
- Differential phase error < 1° at 3.58 MHz
- Differential gain error < 0.5% at 3.58 MHz

Connection Diagram

Dual-In-Line Package



DS007788-2

Top View
Order Number LM359M or LM359N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage 22 V_{DC}
or ±11 V_{DC}

Power Dissipation (Note 2)
- J Package 1W
- N Package 750 mW

Maximum T_J
- J Package +150°C
- N Package +125°C

Thermal Resistance

J Package

θ_{jA} 147°C/W still air
110°C/W with 400 linear feet/min air flow

N Package

θ_{jA} 100°C/W still air
75°C/W with 400 linear feet/min air flow

Input Currents, $I_{IN}(+)$ or $I_{IN}(-)$ 10 mA_{DC}

Set Currents, $I_{SET(IN)}$ or $I_{SET(OUT)}$ 2 mA_{DC}

Operating Temperature Range
- LM359 0°C to +70°C

Storage Temperature Range −65°C to +150°C

Lead Temperature
- (Soldering, 10 sec.) 260°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 sec.) 260°C
- Small Outline Package
  - Vapor Phase (60 sec.) 215°C
  - Infrared (15 sec.) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12$V, $T_A = 25$°C unless otherwise noted

Parameter	Conditions	LM359			Units
		Min	Typ	Max	
Open Loop Voltage	$V_{supply} = 12$V, $R_L = 1$k, f = 100 Hz	62	72		dB
Gain	$T_A = 125$°C		68		dB
Bandwidth	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF	15	30		MHz
Unity Gain					
Gain Bandwidth Product	$R_{IN} = 50\Omega$ to 200Ω	200	400		MHz
Gain of 10 to 100					
Slew Rate					
Unity Gain	$R_{IN} = 1$ kΩ, $C_{comp} = 10$ pF		30		V/μs
Gain of 10 to 100	$R_{IN} < 200\Omega$		60		V/μs
Amplifier to Amplifier Coupling	f = 100 Hz to 100 kHz, $R_L = 1$k		−80		dB
Mirror Gain	at 2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA, $T_A = 25$°C	0.9	1.0	1.1	μA/μA
(Note 3)	at 0.2 mA $I_{IN}(+)$, $I_{SET} = 5$ μA	0.9	1.0	1.1	μA/μA
	Over Temp.				
	at 20 μA $I_{IN}(+)$, $I_{SET} = 5$ μA	0.9	1.0	1.1	μA/μA
	Over Temp.				
ΔMirror Gain	at 20 μA to 0.2 mA $I_{IN}(+)$		3	5	%
(Note 3)	Over Temp, $I_{SET} = 5$ μA				
Input Bias Current	Inverting Input, $T_A = 25$°C		8	15	μA
	Over Temp.			30	μA
Input Resistance (βre)	Inverting Input		2.5		kΩ
Output Resistance	$I_{OUT} = 15$ mA rms, f = 1 MHz		3.5		Ω
Output Voltage Swing	$R_L = 600\Omega$				
V_{OUT} High	$I_{IN}(-)$ and $I_{IN}(+)$ Grounded	9.5	10.3		V
V_{OUT} Low	$I_{IN}(-) = 100$ μA, $I_{IN}(+) = 0$		2	50	mV

Electrical Characteristics (Continued)

$I_{SET(IN)} = I_{SET(OUT)} = 0.5$ mA, $V_{supply} = 12V$, $T_A = 25°C$ unless otherwise noted

Parameter	Conditions	LM359			Units
		Min	Typ	Max	
Output Currents					
Source	$I_{IN}(-)$ and $I_{IN}(+)$ Grounded, $R_L = 100\Omega$	16	40		mA
Sink (Linear Region)	$V_{comp}-0.5V = V_{OUT} = 1V$, $I_{IN}(+) = 0$		4.7		mA
Sink (Overdriven)	$I_{IN}(-) = 100\ \mu A$, $I_{IN}(+) = 0$, V_{OUT} Force = 1V	1.5	3		mA
Supply Current	Non-Inverting Input Grounded, $R_L = \infty$		18.5	22	mA
Power Supply Rejection (Note 4)	f = 120 Hz, $I_{IN}(+)$ Grounded	40	50		dB

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: See Maximum Power Dissipation graph.

Note 3: Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $\left(A_I = \frac{I_{IN}(-)}{I_{IN}(+)}\right)$

ΔMirror Gain is the % change in A_I for two different mirror currents at any given temperature.

Note 4: See Supply Rejection graphs.

National Semiconductor

LM392
Low Power Operational Amplifier/Voltage Comparator

General Description

The LM392 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM392 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM358 dual op amp and the LM393 dual comparator

Features

- Wide power supply voltage range
  Single supply: 3V to 32V
  Dual supply: ±1.5V to ±16V
- Low supply current drain — essentially independent of supply voltage: 600 µA
- Low input biasing current: 50 nA
- Low input offset voltage: 2 mV
- Low input offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

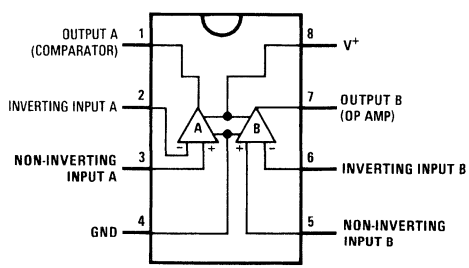
- Internally frequency compensated for unity gain
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz
- Large output voltage swing: 0V to V^+ – 1.5V

ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Connection Diagram

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)
Dual-In-Line Package



(Top View)
Order Number LM392M or LM392MX
See NS Package Number M08A
Order Number LM392N
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM392
Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (Note 2)	
Molded DIP (LM392N)	820 mW
Small Outline Package (LM392M)	530 mW
Output Short-Circuit to Ground (Note 3)	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 4)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD rating to be determined.	
Soldering Information	
Dual-in-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 5)

Parameter	Conditions	LM392			Units
		Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$, (Note 6)		±2	±5	mV
Input Bias Current	IN(+) or IN(−), $T_A = 25°C$, (Note 7) , V_{CM} = 0V		50	250	nA
Input Offset Current	IN(+) − IN(−), $T_A = 25°C$		±5	±50	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 8)	0		V^+−1.5	V
Supply Current	$R_L = \infty$, $V^+ = 30$ V		1	2	mA
Supply Current	$R_L = \infty$, $V^+ = 5$ V		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 9)		−100		dB
Input Offset Voltage	(Note 6)			±7	mV
Input Bias Current	IN(+) or IN(−)			400	nA
Input Offset Current	IN(+) − IN(−)			150	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 8)	0		V^+−2	V
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V^-, if used) (Note 10)			32	V

Electrical Characteristics (Continued)

(V^+ = 5 V_{DC}; specifications apply to both amplifiers unless otherwise stated) (Note 5)

Parameter	Conditions	LM392			Units
		Min	Typ	Max	
OP AMP ONLY					
Large Signal Voltage Gain	V^+ = 15 V_{DC}, V_o swing = 1 V_{DC} to 11 V_{DC}, R_L = 2 kΩ, T_A = 25°C	25	100		V/mV
Output Voltage Swing	R_L = 2 kΩ, T_A = 25°C	0		V^+–1.5	V
Common-Mode Rejection Ratio	DC, T_A = 25°C, V_{CM}= 0, V_{DC} to V^+–1.5 V_{DC}	65	70		dB
Power Supply Rejection Ratio	DC, T_A = 25°C	65	100		dB
Output Current Source	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(-)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o = 2 V_{DC}, T_A = 25°C	20	40		mA
Output Current Sink	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o =2V_{DC}, T_A = 25°C	10	20		mA
	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o =200 mV, T_A = 25°C	12	50		µA
Input Offset Voltage Drift	R_S = 0Ω		7		µV/°C
Input Offset Current Drift	R_S = 0Ω		10		pA_{DC}/°C
COMPARATOR ONLY					
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC}, T_A = 25°C	50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC} V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		1.3		µs
Output Sink Current	$V_{IN(-)}$ =1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V_O ≥1.5 V_{DC}, T_A = 25°C	6	16		mA
Saturation Voltage	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400	mV
	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA			700	mV
Output Leakage Current	$V_{IN(-)}$ = 0, $V_{IN(+)}$ ≥ 1 V_{DC}, V_o = 5 V_{DC}, T_A = 25°C		0.1		nA
	$V_{IN(-)}$ = 0, $V_{IN(+)}$ > 1 V_{DC}, V_o = 30 V_{DC}			1.0	µA

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For operating at temperatures above 25°C, the LM392 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 5: These specifications apply for V^+ = 5V, unless otherwise stated. For the LM392, temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 6: At output switch point, V_O ≅ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V).

Note 7: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 8: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to 32V without damage.

Note 9: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

Note 10: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 11: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

National Semiconductor

LM4250
Programmable Operational Amplifier

General Description

The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

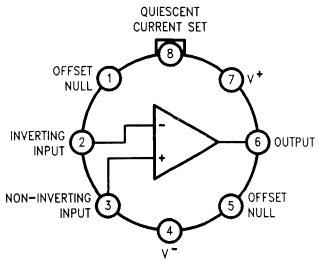
The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to +70°C temperature range instead of the −55°C to +125°C temperature range of the LM4250.

Features

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

Connection Diagrams

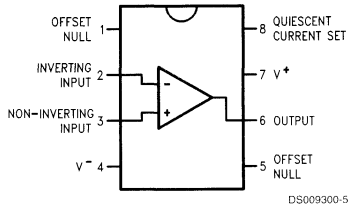
Metal Can Package



DS009300-2

Top View

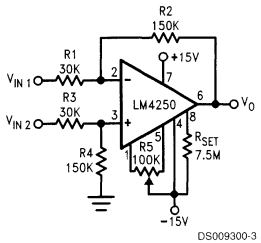
Dual-In-Line Package



DS009300-5

Top View

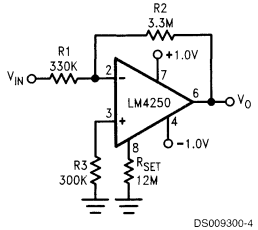
X5 Difference Amplifier



DS009300-3

Quiescent P_D = 0.6 mW

500 Nano-Watt X10 Amplifier



DS009300-4

Quiescent P_D = 500 nW

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 3)

	LM4250	LM4250C
Supply Voltage	±18V	±18V
Operating Temp. Range	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	$0^{\circ}C \leq T_A \leq +70^{\circ}C$
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
I_{SET} Current	150 nA	150 nA
Output Short Circuit Duration	Continuous	Continuous
T_{JMAX}		
H-Package	150°C	100°C
N-Package		100°C
J-Package	150°C	100°C
M-Package		100°C
Power Dissipation at $T_A = 25^{\circ}C$		
H-Package (Still Air)	500 mW	300 mW
(400 LF/Min Air Flow)	1200 mW	1200 mW
N-Package		500 mW
J-Package	1000 mW	600 mW
M-Package		350 mW
Thermal Resistance (Typical) θ_{JA}		
H-Package (Still Air)	165°C/W	165°C/W
(400 LF/Min Air Flow)	65°C/W	65°C/W
N-Package		130°C/W
J-Package	108°C/W	108°C/W
M-Package		190°C/W
(Typical) θ_{JC}		
H-Package	21°C/W	21°C/W
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C

Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.	
ESD tolerance (Note 4)	800V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Refer to RETS4250X for military specifications.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Resistor Biasing

Set Current Setting Resistor to V^-

	I_{SET}				
V_S	0.1 µA	0.5 µA	1.0 µA	5 µA	10 µA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

Electrical Characteristics

LM4250 ($-55^\circ C \le T_A \le +125^\circ C$ unless otherwise specified.) $T_A = T_J$

Parameter	Conditions	V_S = ±1.5V			
		I_{SET} = 1 µA		I_{SET} = 10 µA	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100$ kΩ, $T_A = 25^\circ C$		3 mV		5 mV
I_{OS}	$T_A = 25^\circ C$		3 nA		10 nA
I_{bias}	$T_A = 25^\circ C$		7.5 nA		50 nA
Large Signal Voltage Gain	R_L = 100 kΩ, $T_A = 25^\circ C$ V_O = ±0.6V, R_L = 10 kΩ	40k		 50k	
Supply Current	$T_A = 25^\circ C$		7.5 µA		80 µA
Power Consumption	$T_A = 25^\circ C$		23 µW		240 µW
V_{OS}	$R_S \le 100$ kΩ		4 mV		6 mV
I_{OS}	$T_A = +125^\circ C$ $T_A = -55^\circ C$		5 nA 3 nA		10 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	V_O = ±0.5V, R_L = 100 kΩ R_L = 10 kΩ	30k		 30k	
Output Voltage Swing	R_L = 100 kΩ R_L = 10 kΩ	±0.6V		 ±0.6V	
Common Mode Rejection Ratio	$R_S \le 10$ kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \le 10$ kΩ	76 dB		76 dB	
Supply Current			8 µA		90 µA

Parameter	Conditions	V_S = ±15V			
		I_{SET} = 1 µA		I_{SET} = 10 µA	
		Min	Max	Min	Max
V_{OS}	$R_S \le 100$ kΩ, $T_A = 25^\circ C$		3 mV		5 mV
I_{OS}	$T_A = 25^\circ C$		3 nA		10 nA
I_{bias}	$T_A = 25^\circ C$		7.5 nA		50 nA
Large Signal Voltage Gain	R_L = 100 kΩ, $T_A = 25^\circ C$ V_O = ±10V, R_L = 10 kΩ	100k		 100k	
Supply Current	$T_A = 25^\circ C$		10 µA		90 µA
Power Consumption	$T_A = 25^\circ C$		300 µW		2.7 mW
V_{OS}	$R_S \le 100$ kΩ		4 mV		6 mV
I_{OS}	$T_A = +125^\circ C$ $T_A = -55^\circ C$		25 nA 3 nA		25 nA 10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	

Electrical Characteristics (Continued)

Parameter	Conditions	V_S = ±15V			
		I_{SET} = 1 µA		I_{SET} = 10 µA	
		Min	Max	Min	Max
Large Signal Voltage Gain	V_O = ±10V, R_L = 100 kΩ R_L = 10 kΩ	50k		 50k	
Output Voltage Swing	R_L = 100 kΩ R_L = 10 kΩ	±12V		 ±12V	
Common Mode Rejection Ratio	R_S ≤ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	R_S ≤ 10 kΩ	76 dB		76 dB	
Supply Current			11 µA		100 µA
Power Consumption			330 µW		3 mW

Electrical Characteristics

LM4250C (0°C ≤ T_A ≤ +70°C unless otherwise specified.) T_A = T_J

Parameter	Conditions	V_S = ±1.5V			
		I_{SET} = 1 µA		I_{SET} = 10 µA	
		Min	Max	Min	Max
V_{OS}	R_S ≤ 100 kΩ, T_A = 25°C		5 mV		6 mV
I_{OS}	T_A = 25°C		6 nA		20 nA
I_{bias}	T_A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	R_L = 100 kΩ, T_A = 25°C V_O = ±0.6V, R_L = 10 kΩ	25k		 25k	
Supply Current	T_A = 25°C		8 µA		90 µA
Power Consumption	T_A = 25°C		24 µW		270 µW
V_{OS}	R_S ≤ 10 kΩ		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	V_O = ±0.5V, R_L = 100 kΩ R_L = 10 kΩ	25k		 25k	
Output Voltage Swing	R_L = 100 kΩ R_L = 10 kΩ	±0.6V		 ±0.6V	
Common Mode Rejection Ratio	R_S ≤ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	R_S ≤ 10 kΩ	74 dB		74 dB	
Supply Current			8 µA		90 µA
Power Consumption			24 µW		270 µW

Parameter	Conditions	V_S = ±15V			
		I_{SET} = 1 µA		I_{SET} = 10 µA	
		Min	Max	Min	Max
V_{OS}	R_S ≤ 100 kΩ, T_A = 25°C		5 mV		6 mV
I_{OS}	T_A = 25°C		6 nA		20 nA
I_{bias}	T_A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	R_L = 100 kΩ, T_A = 25°C V_O = ±10V, R_L = 10 kΩ	60k		 60k	
Supply Current	T_A = 25°C		11 µA		100 µA
Power Consumption	T_A = 25°C		330 µW		3 mW
V_{OS}	R_S ≤ 100 kΩ		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA

Electrical Characteristics (Continued)

Parameter	Conditions	V_S = ±15V			
		I_{SET} = 1 µA		I_{SET} = 10 µA	
		Min	Max	Min	Max
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	V_O = ±10V, R_L = 100 kΩ R_L = 10 kΩ	50k		 50k	
Output Voltage Swing	R_L = 100 kΩ R_L = 10 kΩ	±12V		 ±12V	
Common Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq$ 10 kΩ	74 dB		74 dB	
Supply Current			11 µA		100 µA
Power Consumption			330 µW		3 mW

National Semiconductor

LM611
Operational Amplifier and Adjustable Reference

General Description

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current: 300 µA (op amp)
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+–1.8V)
- Wide differential input voltage: ±36V
- Available in low cost 8-pin DIP
- Available in plastic package rated for Military Temperature Range Operation

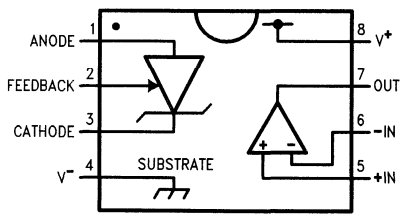
REFERENCE

- Adjustable output voltage: 1.2V to 6.3V
- Tight initial tolerance available: ±0.6%
- Wide operating current range: 17 µA to 20 mA
- Reference floats above ground
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and Mass Flow Control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



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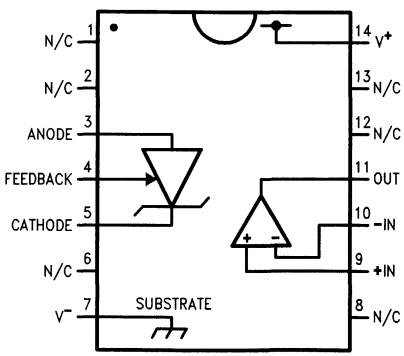

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pins Except V_R (referred to V^- pin) (Note 2)	36V (Max) −0.3V (Min)
Current through Any Input Pin and V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65^\circ C \le T_J \le +150^\circ C$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient (Note 3)	
N Package	100°C/W
M Package	150°C/W
Soldering Information Soldering (10 seconds)	
N Package	260°C
M Package	220°C
ESD Tolerance (Note 4)	±1 kV

Operating Temperature Range

LM611AI, LM611I, LM611BI	$-40^\circ C \le T_J \le +85^\circ C$
LM611AM, LM611M	$-55^\circ C \le T_J \le +125^\circ C$
LM611C	$0^\circ C \le T_J \le 70^\circ C$

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$,	210	300	350	µA max
		$4V \le V^+ \le 36V$ (32V for LM611C)	**221**	**320**	**370**	µA max
V_S	Supply Voltage Range		2.2	2.8	2.8	V min
			2.9	**3**	**3**	V min
			46	36	32	V max
			43	**36**	**32**	V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$	1.5	3.5	5.0	mV max
		($4V \le V^+ \le 32V$ for LM611C)	**2.0**	**6.0**	**7.0**	mV max
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} =	1.0	3.5	5.0	mV max
		($V^+ - 1.8V$), V^+ = 30V, V^- = 0V	**1.5**	**6.0**	**7.0**	mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 6)	**15**			µV/°C max
I_B	Input Bias Current		10	25	35	nA max
			11	**30**	**40**	nA max
I_{OS}	Input Offset Current		0.2	4	4	nA max
			0.3	**5**	**5**	nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1800			MΩ
		Common-Mode	3800			MΩ
C_{IN}	Input Capacitance	Common-Mode	5.7			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection-Ratio	V^+ = 30V, $0V \le V_{CM} \le (V^+ - 1.8V)$	95	80	75	dB min
		$CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	**90**	**75**	**70**	dB min

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
OPERATIONAL AMPLIFIER						
PSRR	Power Supply Rejection-Ratio	4V ≤ V^+ ≤ 30V, $V_{CM} = V^+/2$, PSRR = 20 log ($\Delta V^+/\Delta V_{OS}$)	110 **100**	80 **75**	75 **70**	dB min dB min
A_V	Open Loop Voltage Gain	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V	500 **50**	100 **40**	94 **40**	V/mV min
SR	Slew Rate	V^+ = 30V (Note 7)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/µs
GBW	Gain Bandwidth	C_L = 50 pF	0.80 **0.50**			MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V for LM611C)	$V^+ - 1.4$ **$V^+ - 1.6$**	$V^+ - 1.7$ **$V^+ - 1.9$**	$V^+ - 1.8$ **$V^+ - 1.9$**	V min V min
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V for LM611C)	$V^- + 0.8$ **$V^- + 0.9$**	$V^- + 0.9$ **$V^- + 1.0$**	$V^- + 0.95$ **$V^- + 1.0$**	V max V max
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V_{+IN} = 0V, V_{-IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source	30 **40**	50 **60**	50 **60**	mA max mA max
		V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink	30 **32**	60 **80**	70 **90**	mA max mA max
VOLTAGE REFERENCE						
V_R	Reference Voltage	(Note 8)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T_J}$	Average Temperature Drift	(Note 9)	**10**	**80**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	Hyst = (Vro' − Vro)/ΔT_J (Note 10)	**3.2**			µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 11)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 µA	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro\ =\ Vr)} - V_{R(Vro\ =\ 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 36V)}$ (V^+ = 32V for LM611C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV max mV max
		$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV max mV max

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range.**

Symbol	Parameter	Conditions	Typical (Note 5)	LM611AM LM611AI Limits (Note 6)	LM611M LM611BI LM611I LM611C Limits (Note 6)	Units
VOLTAGE REFERENCE						
$\frac{\Delta V_R}{\Delta V_{ANODE}}$	V_R Change with V_{ANODE} Change	$V^+ = V^+$ max, $\Delta V_R = V_R$				
		(@ $V_{ANODE} = V^- = GND) - V_R$	0.7	1.5	1.6	mV max
		(@ $V_{ANODE} = V^+ - 1.0V$)	**3.3**	**3.0**	**3.0**	mV max
I_{FB}	FEEDBACK Bias Current	I_{FB}; $V_{ANODE} \leq V_{FB} \leq 5.06V$	22	35	50	nA max
			29	**40**	**55**	nA max
e_n	V_R Noise	10 Hz to 10,000 Hz, $V_{RO} = V_R$	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is 90°C/W for the N package and 135°C/W for the M package.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values in standard typeface are for T_J = 25°C; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold face type)**.

Note 7: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Note 8: V_R is the cathode-feedback voltage, nominally 1.244V.

Note 9: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \bullet \Delta V_R / (V_{R[25°C]} \bullet \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 10: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

Note 11: Low contact resistance is required for accurate measurement.

Note 12: Military RETS 611AMX electrical test specification is available on request. The LM611AMJ/883 can also be procured as a Standard Military Drawing.

National Semiconductor

LM432
Dual Op Amp with On-Chip Fixed 2.5V Reference

General Description

The LM432 integrates two operational amplifiers and one 2.5V reference. The reference is based on the LMV431 adjustable shunt regulator with the output voltage adjusted to a fixed 2.5V. The Op Amps are similar to the LM358 with a common-mode input range that includes ground. Integrating the reference and Op Amps creates a solution for low cost charging applications.

Applications

- Low cost charging circuitry
- Power supplies and adapters

Features

Dual Op Amp Circuitry

(Typical for V_S= 5V)

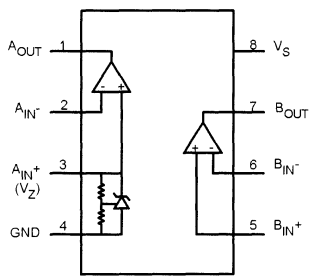
- Input offset voltage 0.6mV
- Input offset current 1nA
- Input bias current 3nA
- Common-mode input voltage range 0V to V_S−1V
- Power supply current 150µA

Reference Circuitry

- Reference voltage 2.5V
- Reference voltage deviation (−40˚C to 85˚C) 4mV
- Sink Current Capability 0.2mA to 10mA

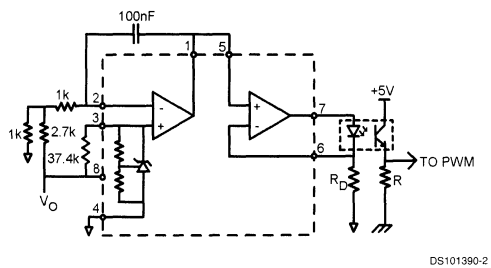
Connection Diagram

8-Pin SOIC



Top View

Application Circuit



Optocoupler Driver Circuit for Power Supply Isolation

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LM432MA	LM432MA	Rails	M08A
	LM432MAX	LM432MA	2.5k Unit Tape and Reel	

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Suppy Voltage (V_S)	20V
Storage Temperature	−65°C to 150°C
Junction Temperature (T_J)	150°C
ESD Human Body Model	2kV
Input Voltage Range	−0.3V to 20V

Operating Ratings (Notes 2, 3)

Temperature Range	−40°C to 85°C
Supply Voltage (Note 8)	2.5V to 16V
Thermal Resistance(θ_{JA})	162°C/W

Electrical Characteristics

The following specifications apply for both amplifiers at V_S = 5V, V_{CM} = 2.5V, V_O = 2.5V, R_L = ∞, and T_J = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
OP Amp Circuitry						
V_{OS}	Input Offset Voltage	Amplifier B only	−4	0.6	4	mV
I_{OS}	Input Offset Current	Amplifier B only		1	50	nA
I_B	Input Bias Current	Amplifier B only		3	150	nA
V_{CM}	Common-Mode Input Voltage Range	Amplifier B only, CMRR > 50dB	0		V_S-1	V
I_S	Power Supply Current	Total for both amplifiers		150	500	µA
A_V	Voltage Gain	V_S = 16V, 1V < V_O < 11V, R_L = 10kΩ connected to V_S/2	65	100		dB
V_{OL}	Output Voltage Low			2	50	mV
V_{OH}	Output Voltage High		V_S − 1.5	V_S − 1.3		V
I_{SOURCE}	Output Current Source		20	30		mA
I_{SINK}	Output Current Sink		5	11		mA
Reference Circuitry For Op Amp A The following specifications apply for I_Z = 200µA and T_J = 25°C, unless otherwise noted.						
V_Z	Reference Voltage at IN+ Terminal		2.450	2.5	2.550	V
V_{ZDEV}	Reference Voltage Deviation at IN+ Terminal Over Temperature (Note 6),(Note 9)	−40°C ≤ T_J ≤ 85°C		4	65	mV
$I_{Z\ (MIN)}$	Minimum Cathode Current for Regulation at IN+ (V_Z) Terminal			150	200	µA
r_z	Dynamic Output Impedance (Note 7)	200µA < I_Z < 1mA, Freq = 0Hz		0.2		Ω

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Rating indicate conditions for which the device is functional. These rating do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND = $0V_{DC}$, unless otherwise specified.

Note 4: Typicals represent the most likely parametic norm.

Note 5: Guaranteed to National's Average Outgoing Quality Level (AOQL).

Note 6: Reference voltage deviation, V_{ZDEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.

Note 7: The Dynamic Output Impendance, r_z, is defined as $r_z = \Delta V_Z/\Delta I_Z$.

Note 8: Minimum value of operating voltage is for Amplifier B only.

Note 9: Typical Temperature drift $\Delta V/\Delta T$ = 12.8ppm/°C

National Semiconductor

LM433
Dual Op Amp with On-Chip Fixed 2.5V Reference

General Description

The LM433 integrates two operational amplifiers and one 2.5V reference. The reference is based on the LMV431 adjustable shunt regulator with the output voltage adjusted to a fixed 2.5V. The Op Amps are similar to the LM358 with a common-mode input range that includes ground. Integrating the reference and Op Amps creates a solution for low cost charging applications.

Applications

- Low cost charging circuitry
- Power supplies and adapters

Features

Dual Op Amp Circuitry

(Typical for V_S = 5V)

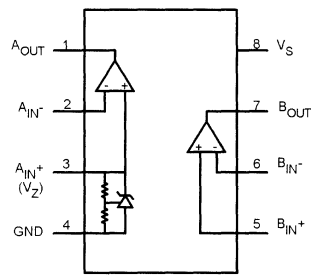
- Input offset voltage 0.6mV
- Input offset current 1nA
- Input bias current 3nA
- Common-mode input voltage range 0V to V_S–1V
- Power supply current 150µA

Reference Circuitry

- Reference voltage 2.5V
- Reference voltage deviation (−40˚C to 85˚C) 4mV
- Sink Current Capability 0.2mA to 10mA

Connection Diagram

8-Pin SOIC



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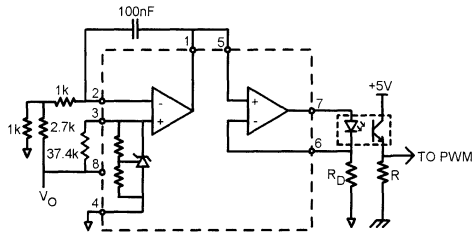
Top View

Application Circuit



DS200039-2

Optocoupler Driver Circuit for Power Supply Isolation

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LM433MA	LM433MA	Rails	M08A
	LM433MAX	LM433MA	2.5k Unit Tape and Reel	

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Suppy Voltage (V_S)	20V
Storage Temperature	−65°C to 150°C
Junction Temperature (T_J)	150°C
ESD Human Body Model	2kV
Input Voltage Range	−0.3V to 20V

Operating Ratings (Notes 2, 3)

Temperature Range	−40°C to 85°C
Supply Voltage (Note 8)	2.5V to 16V
Thermal Resistance(θ_{JA})	162°C/W

Electrical Characteristics

The following specifications apply for both amplifiers at V_S = 5V, V_{CM} = 2.5V, V_O = 2.5V, R_L = ∞, and T_J = 25°C, unless otherwise noted.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
OP Amp Circuitry						
V_{OS}	Input Offset Voltage	Amplifier B only	−7	2	7	mV
I_{OS}	Input Offset Current	Amplifier B only		1	50	nA
I_B	Input Bias Current	Amplifier B only		3	150	nA
V_{CM}	Common-Mode Input Voltage Range	Amplifier B only, CMRR > 50dB	0		V_S-1	V
I_S	Power Supply Current	Total for both amplifiers		150	500	µA
A_V	Voltage Gain	V_S = 16V, 1V < V_O < 11V, R_L = 10kΩ connected to V_S/2	65	100		dB
V_{OL}	Output Voltage Low			2	50	mV
V_{OH}	Output Voltage High		V_S − 1.5	V_S − 1.3		V
I_{SOURCE}	Output Current Source		20	30		mA
I_{SINK}	Output Current Sink		5	11		mA
Reference Circuitry For Op Amp A The following specifications apply for I_Z = 200µA and T_J = 25°C, unless otherwise noted.						
V_Z	Reference Voltage at IN^+ Terminal		2.425	2.5	2.575	V
V_{ZDEV}	Reference Voltage Deviation at IN^+ Terminal Over Temperature (Note 6),(Note 9)	−40°C ≤ T_J ≤ 85°C		4	65	mV
$I_{Z\ (MIN)}$	Minimum Cathode Current for Regulation at IN^+ (V_Z) Terminal			150	200	µA
r_z	Dynamic Output Impedance (Note 7)	200µA < I_Z < 1mA, Freq = 0Hz		0.2		Ω

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Note 2: Operating Rating indicate conditions for which the device is functional. These rating do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND = $0V_{DC}$, unless otherwise specified.

Note 4: Typicals represent the most likely parametic norm.

Note 5: Guaranteed to National's Average Outgoing Quality Level (AOQL).

Note 6: Reference voltage deviation, V_{ZDEV}, is defined as the maximum variation of the reference input voltage over the full temperature range.

Note 7: The Dynamic Output Impendance, r_z, is defined as $r_z = \Delta V_Z/\Delta I_Z$.

Note 8: Minimum value of operating voltage is for Amplifier B only.

Note 9: Typical Temperature drift $\Delta V/\Delta T$ = 12.8ppm/°C

National Semiconductor

LM613
Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

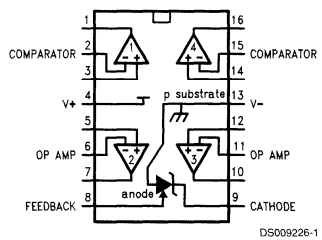
- Low operating current (Op Amp): 300 µA
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+ – 1.8V)
- Wide differential input voltage: ±36V
- Available in plastic package rated for Military Temp. Range Operation

REFERENCE

- Adjustable output voltage: 1.2V to 6.3V
- Tight initial tolerance available: ±0.6%
- Wide operating current range: 17 µA to 20 mA
- Tolerant of load capacitance

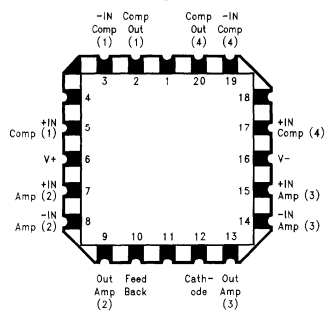
Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

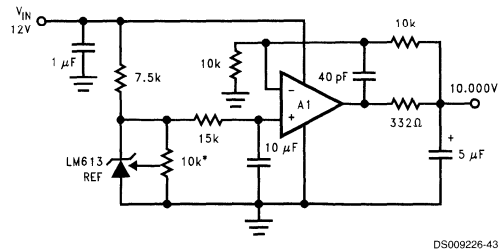


Top View

E Package Pinout



Ultra Low Noise, 10.00V Reference.
Total output noise is typically 14 μV_{RMS}.



*10k must be low t.c. trimpot

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin & V_H Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65^\circ C \le T_J \le +150^\circ C$
Maximum Junction Temp.(Note 4)	150°C
Thermal Resistance, Junction-to-Ambient (Note 5)	
N Package	100°C/W
WM Package	150°C/W
Soldering Information (10 Sec.)	
N Package	260°C
WM Package	220°C
ESD Tolerance (Note 6)	±1 kV

Operating Temperature Range

LM613AI, LM613BI:	$-40^\circ C$ to $+85^\circ C$
LM613AM, LM613M:	$-55^\circ C$ to $+125^\circ C$
LM613C:	$0^\circ C \le T_J \le +70^\circ C$

Electrical Characteristics

These specifications apply for $V^- = GND = 0V$, $V^+ = 5V$, $V_{CM} = V_{OUT} = 2.5V$, $I_R = 100\ \mu A$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ C$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$,	450	940	1000	µA (Max)
		$4V \le V^+ \le 36V$ (32V for LM613C)	**550**	**1000**	**1070**	µA (Max)
V_S	Supply Voltage Range		2.2	2.8	2.8	V (Min)
			2.9	**3**	**3**	V (Min)
			46	36	32	V (Max)
			43	**36**	**32**	V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$	1.5	3.5	5.0	mV (Max)
		$(4V \le V^+ \le 32V$ for LM613C)	**2.0**	**6.0**	**7.0**	mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} =	1.0	3.5	5.0	mV (Max)
		$(V^+ - 1.8V)$, $V^+ = 30V$, $V^- = 0V$	**1.5**	**6.0**	**7.0**	mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 8)	**15**			µV/°C (Max)
I_B	Input Bias Current		10	25	35	nA (Max)
			11	**30**	**40**	nA (Max)
I_{OS}	Input Offset Current		0.2	4	4	nA (Max)
			0.3	**5**	**5**	nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode	$V^+ = 30V$, $0V \le V_{CM} \le (V^+ - 1.8V)$	95	80	75	dB (Min)
	Rejection Ratio	$CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	**90**	**75**	**70**	dB (Min)

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
OPERATIONAL AMPLIFIERS						
PSRR	Power Supply Rejection Ratio	4V ≤ V^+ ≤ 30V, V_{CM} = V^+/2, PSRR = 20 log ($\Delta V^+/V_{OS}$)	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V	500 **50**	100 **40**	94 **40**	V/mV (Min)
SR	Slew Rate	V^+ = 30V (Note 9)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/µs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND, V^+ = 36V (32V for LM613C)	V^+ − 1.4 **V^+ − 1.6**	V^+ − 1.7 **V^+ − 1.9**	V^+ − 1.8 **V^+ − 1.9**	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+, V^+ = 36V (32V for LM613C)	V^- + 0.8 **V^- + 0.9**	V^- + 0.9 **V^- + 1.0**	V^- + 0.95 **V^- + 1.0**	V (Max) V (Max)
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V^+_{IN} = 0V, V^-_{IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V^+_{IN} = 0V, V^-_{IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V^+_{IN} = 3V, V^-_{IN} = 2V	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		V_{OUT} = 5V, V^+_{IN} = 2V, V^-_{IN} = 3V	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C), R_L = 15 kΩ	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	0V ≤ V_{CM} ≤ 36V, V^+ = 36V, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			µV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	R_L = 10 kΩ to 36V (32V for LM613C) 2V ≤ V_{OUT} ≤ 27V	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	V^+_{IN} = 1.4V, V^-_{IN} = TTL Swing, R_L = 5.1 kΩ	1.5 **2.0**			µs µs
I_{SINK}	Output Sink Current	V^+_{IN} = 0V, V^-_{IN} = 1V, V_{OUT} = 1.5V	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		V_{OUT} = 0.4V	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
COMPARATORS						
I_{LEAK}	Output Leakage Current	V^+_{IN} = 1V, V^-_{IN} = 0V, V_{OUT} = 36V (32V for LM613C)	0.1 **0.2**	10	10	µA (Max) µA (Max)
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 10)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(Note 11)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 12)	**3.2**			µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 13)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 µA	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro\ =\ Vr)} - V_{R(Vro\ =\ 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V^+}$	V_R Change with V_{ANODE} Change	$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 36V)}$ (V^+ = 32V for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz, V_{RO} = V_R	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for T_J = 25°C; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

Electrical Characteristics (Continued)

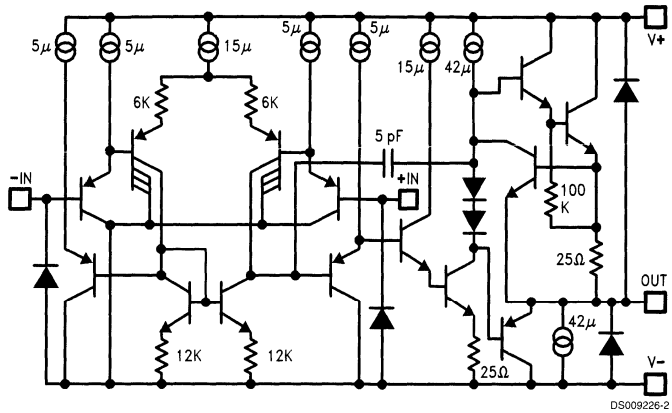
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25˚C and at the temperature extremes. The drift, in ppm/˚C, is $10^6 \cdot \Delta V_R / (V_{R[25^\circ C]} \cdot \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25^\circ C]}$ is the value at 25˚C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 12: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25˚C: 25˚C, 85˚C, −40˚C, 70˚C, 0˚C, 25˚C.

Note 13: Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Op Amp



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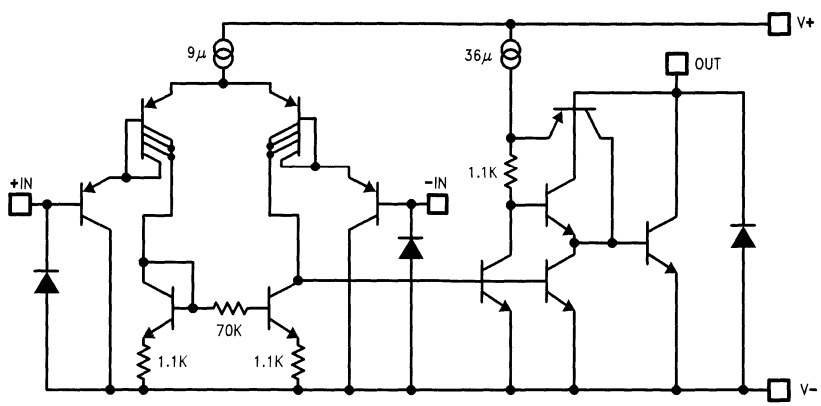
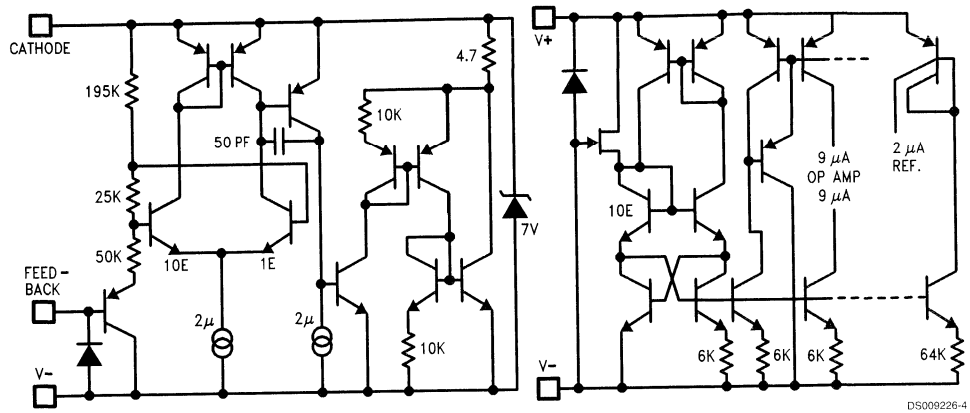
Comparator



DS009226-3

Simplified Schematic Diagrams (Continued)

Reference/Bias



DS009226-4

National Semiconductor

LM6132 /LM6134
Dual and Quad Low Power 10 MHz Rail-to-Rail I/O Operational Amplifiers

General Description

The LM6132/34 provides new levels of speed vs power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only 360 µA/amp supply current, the 10 MHz gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

The LM6132/34 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6132/34 can also drive large capacitive loads without oscillating.

Operating on supplies from 2.7V to over 24V, the LM6132/34 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Features

(For 5V Supply, Typ Unless Noted)

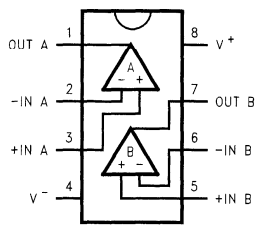
- Rail-to-Rail input CMVR −0.25V to 5.25V
- Rail-to-Rail output swing 0.01V to 4.99V
- High gain-bandwidth, 10 MHz at 20 kHz
- Slew rate 12 V/µs
- Low supply current 360 µA/Amp
- Wide supply range 2.7V to over 24V
- CMRR 100 dB
- Gain 100 dB with R_L = 10k
- PSRR 82 dB

Applications

- Battery operated instrumentation
- Instrumentation Amplifiers
- Portable scanners
- Wireless communications
- Flat panel display driver

Connection Diagrams

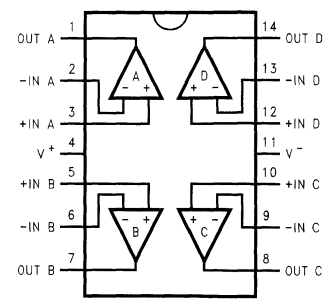
8-Pin DIP/SO



DS012349-1

Top View

14-Pin DIP/SO



DS012349-2

Top View

Ordering Information

Package	Temperature Range Industrial, −40°C to +85°C	NSC Drawing	Transport Media
8-Pin Molded DIP	LM6132AIN, LM6132BIN	N08E	Rails
8-Pin Small Outline	LM6132AIM, LM6132BIM	M08A	Rails
	LM6132AIMX, LM6132BIMX	M08A	Tape and Reel
14-Pin Molded DIP	LM6134AIN, LM6134BIN	N14A	Rails
14-Pin Small Outline	LM6134AIM, LM6134BIM	M14A	Rails
	LM6134AIMX, LM6134BIMX	M14A	Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	$(V^+)+0.3V$, $(V^-)-0.3V$
Supply Voltage (V^+-V^-)	35V
Current at Input Pin	±10 mA
Current at Output Pin (Note 3)	±25 mA
Current at Power Supply Pin	50 mA
Lead Temp. (soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \le V_S \le 24V$
Junction Temperature Range	
LM6132, LM6134	$-40°C \le T_J \le +85°C$
Thermal resistance (θ_{JA})	
N Package, 8-pin Molded DIP	115°C/W
M Package, 8-pin Surface Mount	193°C/W
N Package, 14-pin Molded DIP	81°C/W
M Package, 14-pin Surface Mount	126°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V_S/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6134AI LM6132AI Limit (Note 6)	LM6134BI LM6132BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.25	2 **4**	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**5**			µV/C
I_B	Input Bias Current	$0V \le V_{CM} \le 5V$	110	140 **300**	180 **350**	nA max
I_{OS}	Input Offset Current		3.4	30 **50**	30 **50**	nA max
R_{IN}	Input Resistance, CM		104			MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 4V$	100	75 **70**	75 **70**	dB min
		$0V \le V_{CM} \le 5V$	80	60 **55**	60 **55**	
PSRR	Power Supply Rejection Ratio	$\pm 2.5V \le V_S \le \pm 12V$	82	78 **75**	78 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range		−0.25	**0**	**0**	V
			5.25	**5.0**	**5.0**	
A_V	Large Signal Voltage Gain	R_L = 10k	100	25 **8**	15 **6**	V/mV min
V_O	Output Swing	100k Load	4.992	4.98 **4.93**	4.98 **4.93**	V min
			0.007	0.017 **0.019**	0.017 **0.019**	V max
		10k Load	4.952	4.94 **4.85**	4.94 **4.85**	V min
			0.032	0.07 **0.09**	0.07 **0.09**	V max
		5k Load	4.923	4.90 **4.85**	4.90 **4.85**	V min
			0.051	0.095 **0.12**	0.095 **0.12**	V max
I_{SC}	Output Short Circuit Current LM6132	Sourcing	4	2 **2**	2 **1**	mA min
		Sinking	3.5	1.8 **1.8**	1.8 **1**	mA min

5.0V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V_S/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6134AI LM6132AI Limit (Note 6)	LM6134BI LM6132BI Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current LM6134	Sourcing	3	2 **1.6**	2 **1**	mA min
		Sinking	3.5	1.8 **1.3**	1.8 **1**	mA min
I_S	Supply Current	Per Amplifier	360	400 **450**	400 **450**	µA max

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V_S/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM6134AI LM6132AI Limit (Note 6)	LM6134BI LM6132BI Limit (Note 6)	Units
SR	Slew Rate	±4V @ V_S = ±6V R_S < 1 kΩ	14	8 **7**	8 **7**	V/µs min
GBW	Gain-Bandwidth Product	f = 20 kHz	10	7.4 **7**	7.4 **7**	MHz min
θm	Phase Margin	R_L = 10k	33			deg
G_m	Gain Margin	R_L = 10k	10			dB
e_n	Input Referred Voltage Noise	f = 1 kHz	27			$\frac{nV}{\sqrt{Hz}}$
i_n	Input Referred Current Noise	f = 1 kHz	0.18			$\frac{pA}{\sqrt{Hz}}$

National Semiconductor

LM614
Quad Operational Amplifier and Adjustable Reference

General Description

The LM614 consists of four op-amps and a programmable voltage reference in a 16-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with four wide output swing op-amps makes the LM614 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), initial tolerance (2.0%), and the ability to be programmed from 1.2V to 5.0V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

Op Amp

- Low operating current: 450μA
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+– 1.8V)
- Wide differential input voltage: ±36V

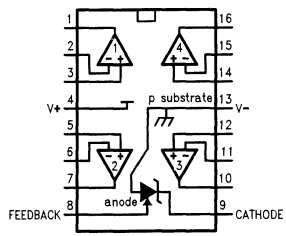
Reference

- Adjustable output voltage: 1.2V to 5.0V
- Initial tolerance: ±2.0%
- Wide operating current range: 17μA to 20mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver and signal processing
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagram



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Ordering Information

Package	Temperature Range	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin Wide Body SOIC	0°C to 70°C	LM614CWM	LM614CWM	Rails	M16B
		LM614CWMX	LM614CWM	1k Units Tape and Reel	
	−40°C to 85°C	LM614IWM	LM614IWM	Rails	
		LM614IWMX	LM614IWM	1k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pins except V_R (referred to V^- pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin & V_R Pin	±20 mA
Differential Input Voltage	
LM614I	±36V
LM614C	±32V
Storage Temperature Range	$-65^\circ C \le T_J \le +150^\circ C$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient (Note 4)	150°C
Soldering Information (Soldering, 10 sec.)	220°C
ESD Tolerance (Note 5)	±1kV

Operating Temperature Range

LM614I	$-40^\circ C \le T_J \le +85^\circ C$
LM614C	$0^\circ C \le T_J \le +70^\circ C$

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **Boldface type** apply over the **Operating Temperature Range** .

Symbol	Parameter	Conditions	Typ (Note 6)	LM614I LM614C Limits (Note 7)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$, $4V \le V^+ \le 36V$ (32V for LM614C)	450	1000	µA max
			550	**1070**	µA max
V_S	Supply Voltage Range		2.2	2.8	V min
			2.9	**3**	V min
			46	32	V max
			43	**32**	V max
OPERATIONAL AMPLIFIER					
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$	1.5	5.0	mV max
		$(4V \le V^+ \le 32V$ for LM614C)	**2.0**	**7.0**	mV max
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} =	1.0	5.0	mV max
		$(V^+ - 1.8V)$, V^+ = 30V	**1.5**	**7.0**	mV max
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 7)	**15**		µV/°C max
I_B	Input Bias Current		10	35	nA max
			11	**40**	nA max
I_{OS}	Input Offset Current		0.2	4	nA max
			0.3	**5**	nA max
$\frac{I_{OS1}}{\Delta T}$	Average Offset Drift Current		**4**		pA/°C
R_{IN}	Input Resistance	Differential	1800		MΩ
		Common-Mode	3800		MΩ
C_{IN}	Input Capacitance	Common-Mode Input	5.7		pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74		$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58		$fA/\sqrt{Hz}$
CMRR	Common-Mode Rejection Ratio	V^+ = 30V, $0V \le V_{CM} \le (V^+ - 1.8V)$, CMRR = 20 log $(\Delta V_{CM}/\Delta V_{OS})$	95	75	dB min
			90	**70**	dB min
PSRR	Power Supply Rejection Ratio	$4V \le V^+ \le 30V$, $V_{CM} = V^+/2$, PSRR = 20 log $(\Delta V^+/\Delta V_{OS})$	110	75	dB min
			100	**70**	dB min

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100μA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **Boldface type** apply over the **Operating Temperature Range** .

Symbol	Parameter	Conditions	Typ (Note 6)	LM614I LM614C Limits (Note 7)	Units
A_V	Open Loop Voltage Gain	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V	500 **50**	94 **40**	V/mV min
SR	Slew Rate	V^+ = 30V (Note 8)	±0.70 **±0.65**	±0.50 **±0.45**	V/μs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.52**		MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND V^+ = 36V (32V for LM614C)	V^+ − 1.4 **V^+ − 1.6**	V^+ − 1.8 **V^+ − 1.9**	V min V min
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+ V^+ = 36V (32V for LM614C)	V^- + 0.8 **V^- + 0.9**	V^- + 0.95 **V^- + 1.0**	V max V max
I_{OUT}	Output Source	V_{OUT} = 2.5V, V_{+IN} = 0V, V_{-IN} = −0.3V	25 **15**	16 **13**	mA min mA min
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V_{+IN} = 0V, V_{-IN} = 0.3V	17 **9**	13 **8**	mA min mA min
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V_{+IN} = 3V, V_{-IN} = 2V, Source	30 **40**	50 **60**	mA max mA max
		V_{OUT} = 5V, V_{+IN} = 2V, V_{-IN} = 3V, Sink	30 **32**	70 **90**	mA max mA max
VOLTAGE REFERENCE					
V_R	Voltage Reference	(Note 9)	1.244	1.2191 1.2689 (±2.0%)	V min V max
$\frac{\Delta V_R}{\Delta T}$	Average Temperature Drift	(Note 10)	**10**	**150**	PPM/°C max
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 11)	**3.2**		μV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	mV max mV max
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 12)	1.5 **2.0**	5 **5.5**	mV max mV max
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 μA	**0.2** **0.6**	**0.56** **13**	Ω max Ω max
$\frac{\Delta V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro\ =\ Vr)} - V_{R(Vro\ =\ 5.0V)}$ (3.76V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	mV max mV max
$\frac{\Delta V_R}{\Delta V^+}$	V_R Change with V^+ Change	$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 36V)}$ (V^+ = 32V for LM614C)	0.1 **0.1**	1.2 **1.3**	mV max mV max
		$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 3V)}$	0.01 **0.01**	1 **1.5**	mV max mV max
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	50 **55**	nA max nA max
e_n	Voltage Noise	BW = 10 Hz to 10 kHz,	30		μV_{RMS}

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25˚C; limits in **Boldface type** apply over the **Operating Temperature Range** .

Symbol	Parameter	Conditions	Typ (Note 6)	LM614I LM614C Limits (Note 7)	Units
		$V_{RO} = V_R$			

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Junction temperature may be calculated using $T_J = T_A + P_D\theta_{jA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{jA} is 90˚C/W for the WM package.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 6: Typical values in standard typeface are for T_J = 25˚C; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 7: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.

Note 8: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 9: V_R is the Cathode-feedback voltage, nominally 1.244V.

Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25˚C and at the temperature extremes. The drift, in ppm/˚C, is $10^6 \cdot \Delta V_R / (V_{R[25^\circ C]} \cdot \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25^\circ C]}$ is the value at 25˚C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 11: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, cycle its junction temperature in the following pattern, spiraling in toward 25˚C: 25˚C, 85˚C, −40˚C, 70˚C, 0˚C, 25˚C.

Note 12: Low contact resistance is required for accurate measurement.

National Semiconductor

LM6142 and LM6144
17 MHz Rail-to-Rail Input-Output Operational Amplifiers

General Description

Using patent pending new circuit topologies, the LM6142/44 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/44 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 µA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Features

At V_S = 5V. Typ unless noted.

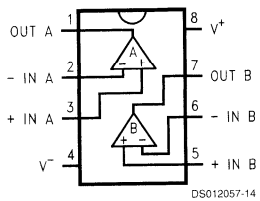
- Rail-to-rail input CMVR −0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17 MHz at 50 kHz (typ)
- Slew rate:
  - Small signal, 5V/µs
  - Large signal, 30V/µs
- Low supply current 650 µA/Amplifier
- Wide supply range 1.8V to 24V
- CMRR 107 dB
- Gain 108 dB with R_L = 10k
- PSRR 87 dB

Applications

- Battery operated instrumentation
- Depth sounders/fish finders
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

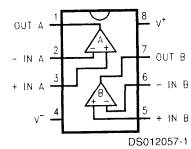
Connection Diagrams

8-Pin CDIP



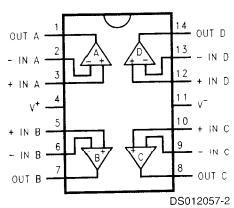
Top View

8-Pin DIP/SO



Top View

14-Pin DIP/SO



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	(V+) + 0.3V, (V−) − 0.3V
Supply Voltage (V+ − V−)	35V
Current at Input Pin	±10 mA
Current at Output Pin (Note 3)	±25 mA
Current at Power Supply Pin	50 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \le V+ \le 24V$
Junction Temperature Range	
LM6142, LM6144	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, V+ = 5.0V, V− = 0V, $V_{CM} = V_O = V+/2$ and $R_L > 1\ M\Omega$ to V+/2. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.3	1.0	2.5	mV
				2.2	**3.3**	max
TCV_{OS}	Input Offset Voltage Average Drift		**3**			µV/°C
I_B	Input Bias Current		170	250	300	nA
		$0V \le V_{CM} \le 5V$	180	280		max
				526	**526**	
I_{OS}	Input Offset Current		3	30	30	nA
				80	**80**	max
R_{IN}	Input Resistance, C_M		126			MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 4V$	107	84	84	
				78	**78**	
		$0V \le V_{CM} \le 5V$	82	66	66	dB
			79	**64**	**64**	min
PSRR	Power Supply Rejection Ratio	$5V \le V^+ \le 24V$	**87**	80	80	
				78	**78**	
V_{CM}	Input Common-Mode Voltage Range		−0.25	**0**	**0**	V
			5.25	**5.0**	**5.0**	
A_V	Large Signal Voltage Gain	R_L = 10k	270	100	80	V/mV
			70	**33**	**25**	min
V_O	Output Swing	R_L = 100k	0.005	0.01	0.01	V
				0.013	**0.013**	max
			4.995	4.98	4.98	V
				4.93	**4.93**	min
		R_L = 10k	0.02			V max
			4.97			V min
		R_L = 2k	0.06	0.1	0.1	V
				0.133	**0.133**	max
			4.90	4.86	4.86	V
				4.80	**4.80**	min

5.0V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V+ = 5.0V, V− = 0V, $V_{CM} = V_O$ = V+/2 and R_L > 1 MΩ to V+/2. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
I_{SC}	Output Short Circuit Current LM6142	Sourcing	13	10	8	mA
				4.9	**4**	min
				35	**35**	mA
						max
		Sinking	24	10	10	mA
				5.3	**5.3**	min
				35	**35**	mA
						max
I_{SC}	Output Short Circuit Current LM6144	Sourcing	8	6	6	mA
				3	**3**	min
				35	**35**	mA
						max
		Sinking	22	8	8	mA
				4	**4**	min
				35	**35**	mA
						max
I_S	Supply Current	Per Amplifier	650	800	800	µA
				880	**880**	max

5.0V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for T_J = 25°C, V+ = 5.0V, V− = 0V, $V_{CM} = V_O$ = V+/2 and R_L > 1 MΩ to $V_S/2$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6144AI LM6142AI Limit (Note 6)	LM6144BI LM6142BI Limit (Note 6)	Units
SR	Slew Rate	8 V_{p-p} @ V_{CC} 12V	25	15	13	V/µs
		R_S > 1 kΩ		**13**	**11**	min
GBW	Gain-Bandwidth Product	f = 50 kHz	17	10	10	MHz
				6	**6**	min
ϕ_m	Phase Margin		38			Deg
	Amp-to-Amp Isolation		130			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	16			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.22			$\frac{pA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	f = 10 kHz, R_L = 10 kΩ,	0.003			%

National Semiconductor

LM6152/LM6154
Dual and Quad 75 MHz GBW Rail-to-Rail I/O Operational Amplifiers

General Description

Using patented circuit topologies, the LM6152/54 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only 1.4 mA/amplifier supply current, the 75 MHz gain bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life. The slew rate of the devices increases with increasing input differential voltage, thus allowing the device to handle capacitive loads while maintaining large signal amplitude.

The LM6152/54 can be driven by voltages that exceed both power supply rails, thus eliminating concerns about exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Operating on supplies from 2.7V to over 24V, the LM6152/54 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Features

At V_S = 5V, Typ unless noted

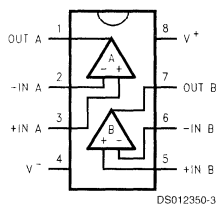
- Greater than Rail-to-Rail Input CMVR −0.25V to 5.25V
- Rail-to-Rail Output Swing 0.01V to 4.99V
- Wide Gain-Bandwidth: 75 MHz @ 100 kHz
- Slew Rate:
  - Small signal 5V/µs
  - Large signal 45V/µs
- Low supply current 1.4mA/amplifier
- Wide supply range 2.7V to 24V
- Fast settling time of 1.1µs for 2V step (to 0.01%)
- PSRR 91 dB
- CMRR 84 dB

Applications

- Portable high speed instrumentation
- Signal conditioning amplifier/ADC buffers
- Barcode scanners

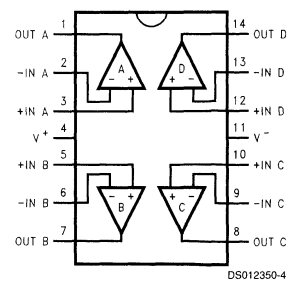
Connection Diagrams

8-Pin DIP/SO



Top View

14-Pin DIP/SO



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	35V
Current at Input Pin	±10mA
Current at Output Pin (Note 3)	±25mA
Current at Power Supply Pin	50mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7V \le V_S \le 24V$
Junction Temperature Range	
LM6152,LM6154	$0°C \le T_J \le +70°C$
Thermal Resistance (θ_{JA})	
N Pkg, 8-pin Molded Dip	115°C/W
M Pkg, 8-pin Surface Mount	193°C/W
N Pkg, 14-pin Molded Dip	81°C/W
M Pkg, 14-pin Surface Mount	126°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6154AC LM6152AC Limit (Note 6)	LM6154BC LM6152BC Limt (Note 6)	Units
V_{OS}	Input Offset Voltage		0.54	2 **4**	5 **7**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			µV/°C
I_B	Input Bias Current	$0V \le V_{CM} \le 5V$	500 **750**	980 **1500**	980 **1500**	nA max
I_{OS}	Input Offset Current		32 **40**	100 **160**	100 **160**	nA max
R_{IN}	Input Resistance, CM	$0V \le V_{CM} \le 4V$	30			MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 4V$	94	70	70	dB min
		$0V \le V_{CM} \le 5V$	84	60	60	
PSRR	Power Supply Rejection Ratio	$5V \le V^+ \le 24V$	91	80	80	dB min
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	5.25	**5.0**	**5.0**	V
A_V	Large Signal Voltage Gain	R_L = 10kΩ	214	50	50	V/mV min
V_O	Output Swing	R_L = 100kΩ	0.006	0.02 **0.03**	0.02 **0.03**	V max
			4.992	4.97 **4.96**	4.97 **4.96**	V min
		R_L = 2kΩ	0.04	0.10 **0.12**	0.10 **0.12**	V max
			4.89	4.80 **4.70**	4.80 **4.70**	V min
I_{SC}	Output Short Circuit Current	Sourcing	6.2	3 **2.5**	3 **2.5**	mA min
				27 **17**	27 **17**	mA max
		Sinking	16.9	7 **5**	7 **5**	mA min
				40	40	mA max

5.0V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6154AC LM6152AC Limit (Note 6)	LM6154BC LM6152BC Limt (Note 6)	Units
I_S	Supply Current	Per Amplifier	1.4	2 **2.25**	2 **2.25**	mA max

5.0V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6154AC LM6152AC Limit (Note 6)	LM6154BC LM6152BC Limt (Note 6)	Units
SR	Slew Rate	±4V Step @ V_S = ±6V, R_S < 1 kΩ	30	24 **15**	24 **15**	V/μs min
GBW	Gain-Bandwidth Product	f = 100 kHz	75			MHz
	Amp-to-Amp Isolation	R_L = 10kΩ	125			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	9			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.34			$pA/\sqrt{Hz}$
T.H.D	Total Harmonic Distortion	f = 10 kHz, R_L = 10kΩ	0.002			%
ts	Settling Time	2V Step to 0.01%	1.1			μs

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LM6154AC LM6152AC Limit (Note 6)	LM6154BC LM6152BC Limt (Note 6)	Units
V_{OS}	Input Offset Voltage		0.8	2 **5**	5 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**10**			μV/°C
I_B	Input Bias Current		500			nA
I_{OS}	Input Offset Current		50			nA
R_{IN}	Input Resistance, CM	0V ≤ V_{CM} ≤ 1.8V	30			MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.8V	88			dB
		0V ≤ V_{CM} ≤ 2.7V	78			
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 5V	69			dB
V_{CM}	Input Common-Mode Voltage Range	Low	−0.25	0	0	V
		High	2.95	2.7	2.7	V
A_V	Large Signal Voltage Gain	R_L = 10kΩ	5.5			V/mV
V_O	Output Swing	R_L = 10kΩ	0.032	0.07 **0.11**	0.07 **0.11**	V max
			2.68	2.64 **2.62**	2.64 **2.62**	V min
I_S	Supply Current	Per Amplifier	1.35			mA

National Semiconductor

LM6118/LM6218
Fast Settling Dual Operational Amplifiers

General Description

The LM6118/LM6218 are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ±20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ±5V to ±20V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIP™ (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

Features

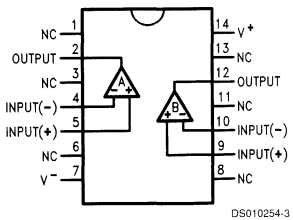
	Typical
■ Low offset voltage:	0.2 mV
■ 0.01% settling time:	400 ns
■ Slew rate A_v = −1:	140 V/µs
■ Slew rate A_v = +1:	75 V/µs
■ Gain bandwidth:	17 MHz
■ Total supply current:	5.5 mA
■ Output drives 50Ω load (±1V)	

Applications

- D/A converters
- Fast integrators
- Active filters

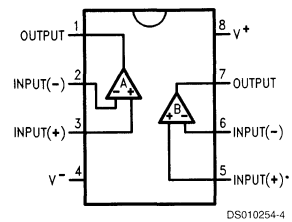
Connection Diagrams and Order Information

Small Outline Package (WM)



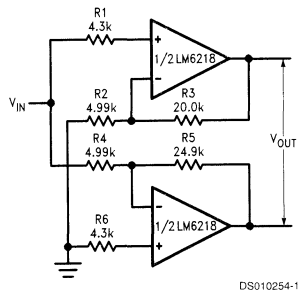
Top View
Order Number LM6218WM, LM6218WMX
See NS Package Number M14B

Dual-In-Line Package (J or N)



Top View
Order Number LM6118J/883 or LM6218N
See NS Package Number N08E, J08A

Typical Applications



Single ended input to differential output
A_V = 10, BW = 3.2 MHz
40 V_{PP} Response = 1.4 MHz
V_S = ±15V

Wide-Band, Fast-Settling
40 V_{PP} Amplifier

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage	42V
Input Voltage	(Note 2)
Differential Input Current (Note 3)	±10 mA
Output Current (Note 4)	Internally Limited
Power Dissipation (Note 5)	500 mW
ESD Tolerance	
(C = 100 pF, R = 1.5 kΩ)	±2 kV
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	300°C

Operating Temp. Range

LM6118	−55°C to +125°C
LM6218	−40°C to +85°C

Electrical Characteristics

$\pm 5V \le V_S \le \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for T_J = 25°C, and **Bold Face Type** are for **Temperature Extremes.**

Parameter	Conditions	Typ 25°C	LM6118 Limits (Note 6)	LM6218 Limits (Note 6)	Units
Input Offset Voltage	$V_S = \pm 15V$	0.2	1 **2**	3 **4**	mV (max)
Input Offset Voltage	$V- + 3V \le V_{CM} \le V+ - 3.5V$	0.3	1.5 **2.5**	3.5 **4.5**	mV (max)
Input Offset Current	$V- + 3V \le V_{CM} \le V+ - 3.5V$	20	50 **250**	100 **200**	nA (max)
Input Bias Current	$V- + 3V \le V_{CM} \le V+ - 3.5V$	200	350 **950**	500 **1250**	nA (max)
Input Common Mode Rejection Ratio	$V- + 3V \le V_{CM} \le V+ - 3.5V$ $V_S = \pm 20V$	100	90 **85**	80 **75**	dB (min)
Positive Power Supply Rejection Ratio	$V- = -15V$ $5V \le V+ \le 20V$	100	90 **85**	80 **75**	dB (min)
Negative Power Supply Rejection Ratio	$V+ = 15V$ $-20V \le V- \le -5V$	100	90 **85**	80 **75**	dB (min)
Large Signal Voltage Gain	$V_{out} = \pm 15V$ R_L = 10k $V_S = \pm 20V$	500	150 **100**	100 **70**	V/mV (min)
	$V_{out} = \pm 10V$ R_L = 500 $V_S = \pm 15V$ (±20 mA)	200	50 **30**	40 **25**	V/mV (min)
V_O Output Voltage Swing	Supply = ±20V R_L = 10k	17.3	±17	±17	V (min)
Total Supply Current	$V_S = \pm 15V$	5.5	7 **7.5**	7 **7.5**	mA (max)
Output Current Limit	$V_S = \pm 15V$, Pulsed	65	100	100	mA (max)
Slew Rate, Av = −1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f$ = 2k, C_f = 10 pF	140	100 **50**	100 **50**	V/µs (min)
Slew Rate, Av = +1	$V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f$ = 2k, C_f = 10 pF	75	50 **30**	50 **30**	V/µs (min)
Gain-Bandwidth Product	$V_S = \pm 15V$, f_o = 200 kHz	17	14	13	MHz (min)
0.01% Settling Time A_V = −1	ΔV_{out} = 10V, $V_S = \pm 15V$, $R_S = R_f$ = 2k, C_f = 10 pF	400			ns
Input Capacitance	Inverter	5			pF
	Follower	3			pF

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is $(V^+ - 1V)$ to (V^-).

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

Electrical Characteristics (Continued)

Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

Note 5: Devices must be derated using a thermal resistance of 90°C/W for the N and WM packages.

Note 6: Limits are guaranteed by testing or correlation.

National Semiconductor

LM675
Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

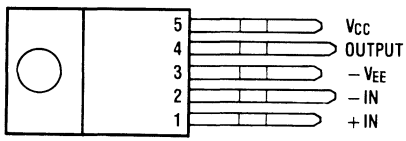
- 3A current capability
- A_{VO} typically 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/μs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)

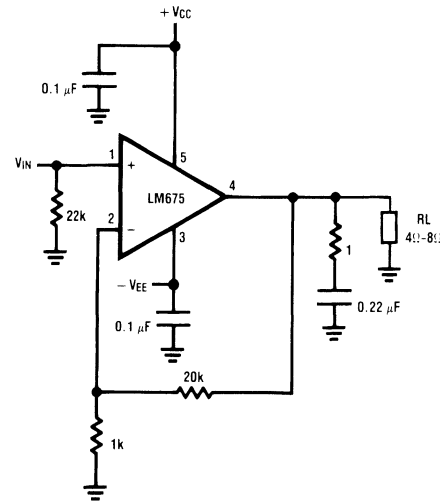


*The tab is internally connected to pin 3 ($-V_{EE}$)

Front View
Order Number LM675T
See NS Package T05D

Typical Applications

Non-Inverting Amplifier



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±30V
Input Voltage	$-V_{EE}$ to V_{CC}
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Power Dissipation (Note 2)	30W
Lead Temperature (Soldering, 10 seconds)	260°C

ESD rating to be determined.

Electrical Characteristics

V_S=±25V, T_A=25°C unless otherwise specified.

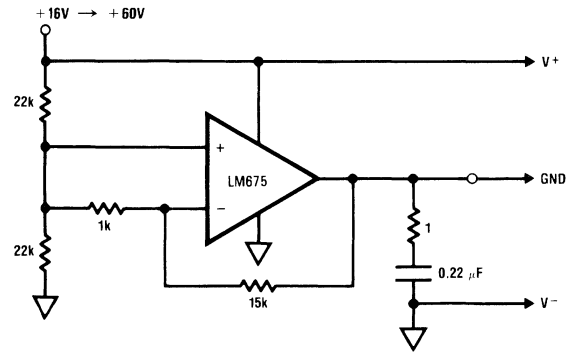
Parameter	Conditions	Typical	Tested Limit	Units
Supply Current	P_{OUT} = 0W	18	50 (max)	mA
Input Offset Voltage	V_{CM} = 0V	1	10 (max)	mV
Input Bias Current	V_{CM} = 0V	0.2	2 (max)	μA
Input Offset Current	V_{CM} = 0V	50	500 (max)	nA
Open Loop Gain	R_L = ∞Ω	90	70 (min)	dB
PSRR	ΔV_S = ±5V	90	70 (min)	dB
CMRR	V_{IN} = ±20V	90	70 (min)	dB
Output Voltage Swing	R_L = 8Ω	±21	±18 (min)	V
Offset Voltage Drift Versus Temperature	R_S < 100 kΩ	25		μV/°C
Offset Voltage Drift Versus Output Power		25		μV/W
Output Power	THD = 1%, f_O = 1 kHz, R_L = 8Ω	25	20	W
Gain Bandwidth Product	f_O = 20 kHz, A_{VCL} = 1000	5.5		MHz
Max Slew Rate		8		V/μs
Input Common Mode Range		±22	±20 (min)	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: Assumes T_A equal to 70°C. For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C.

Typical Applications

Generating a Split Supply From a Single Supply



DS006739-3

V_S = ±8V → ±30V

National Semiconductor

LM725
Operational Amplifier

General Description

The LM725/LM725A/LM725C are operational amplifiers featuring superior performance in applications where low noise, low drift, and accurate closed-loop gain are required. With high common mode rejection and offset null capability, it is especially suited for low level instrumentation applications over a wide supply voltage range.

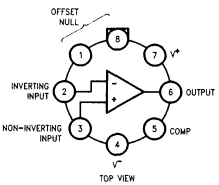
The LM725A has tightened electrical performance with higher input accuracy and like the LM725, is guaranteed over a −55˚C to +125˚C temperature range. The LM725C has slightly relaxed specifications and has its performance guaranteed over a 0˚C to 70˚C temperature range.

Features

- High open loop gain 3,000,000
- Low input voltage drift 0.6 µV/˚C
- High common mode rejection 120 dB
- Low input noise current 0.15 pA/$\sqrt{\text{Hz}}$
- Low input offset current 2 nA
- High input voltage range ±14V
- Wide power supply range ±3V to ±22V
- Offset null capability
- Output short circuit protection

Connection Diagram

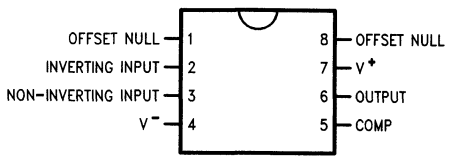
Metal Can Package



DS010474-1

Order Number LM725H/883, LM725CH or LM725AH/883
See NS Package Number H08C

Dual-In-Line Package

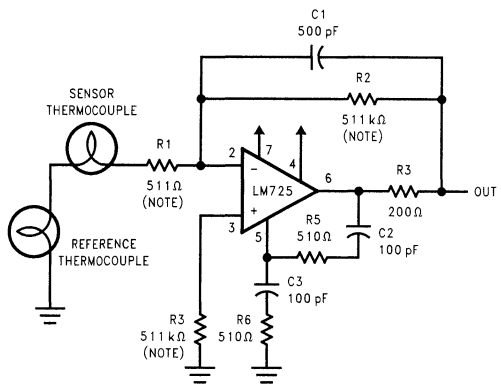


DS010474-2

Order Number LM725CN
See NS Package Number N08E

Typical Applications

Thermocouple Amplifier



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±22V
Internal Power Dissipation (Note 2)	500 mW
Differential Input Voltage	±5V
Input Voltage (Note 3)	±22V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	260°C
Maximum Junction Temperature	150°C

Operating Temperature Range	$T_{A(MIN)}$		$T_{A(MAX)}$
LM725	−55°C	to	+125°C
LM725A	−55°C	to	+125°C
LM725C	0°C	to	+70°C

Electrical Characteristics (Note 4)

Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Without External Trim)	T_A = 25°C, $R_S \le 10$ kΩ			0.5		0.5	1.0		0.5	2.5	mV
Input Offset Current	T_A = 25°C		2.0	5.0		2.0	20		2.0	35	nA
Input Bias Current	T_A = 25°C		42	80		42	100		42	125	nA
Input Noise Voltage	T_A = 25°C										
	f_o = 10 Hz		15			15			15		nV/√Hz
	f_o = 100 Hz		9.0			9.0			9.0		nV/√Hz
	f_o = 1 kHz		8.0			8.0			8.0		nV/√Hz
Input Noise Current	T_A = 25°C										
	f_o = 10 Hz		1.0			1.0			1.0		pA/√Hz
	f_o = 100 Hz		0.3			0.3			0.3		pA/√Hz
	f_o = 1 kHz		0.15			0.15			0.15		pA/√Hz
Input Resistance	T_A = 25°C		1.5			1.5			1.5		MΩ
Input Voltage Range	T_A = 25°C	±13.5	±14		±13.5	±14		±13.5	±14		V
Large Signal Voltage Gain	T_A = 25°C, $R_L \ge 2$ kΩ, V_{OUT} = ±10V	1000	3000		1000	3000		250	3000		V/mV
Common-Mode Rejection Ratio	T_A = 25°C, $R_S \le 10$ kΩ	120			110	120		94	120		dB
Power Supply Rejection Ratio	T_A = 25°C, $R_S \le 10$ kΩ		2.0	5.0		2.0	10		2.0	35	μV/V
Output Voltage Swing	T_A = 25°C,										
	$R_L \ge 10$ kΩ	±12.5	±13.5		±12	±13.5		±12	±13.5		V
	$R_L \ge 2$ kΩ	±12.0	±13.5		±10	±13.5		±10	±13.5		V
Power Consumption	T_A = 25°C		80	105		80	105		80	150	mW
Input Offset Voltage (Without External Trim)	$R_S \le 10$ kΩ			0.7			1.5			3.5	mV
Average Input Offset Voltage Drift (Without External Trim)	R_S = 50Ω			2.0		2.0	5.0		2.0		μV/°C
Average Input Offset Voltage Drift (With External Trim)	R_S = 50Ω		0.6	1.0		0.6			0.6		μV/°C
Input Offset Current	$T_A = T_{MAX}$		1.2	4.0		1.2	20		1.2	35	nA
	$T_A = T_{MIN}$		7.5	18.0		7.5	40		4.0	50	nA
Average Input Offset Current Drift			35	90		35	150		10		pA/°C
Input Bias Current	$T_A = T_{MAX}$		20	70		20	100			125	nA
	$T_A = T_{MIN}$		80	180		80	200			250	nA

Electrical Characteristics (Note 4) (Continued)

Parameter	Conditions	LM725A			LM725			LM725C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$ $T_A = T_{MAX}$	1,000,000			1,000,000			125,000			V/V
	$R_L \geq 2\ k\Omega$ $T_A = T_{MIN}$	500,000			250,000			125,000			V/V
Common-Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110			100				115		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$			8.0			20		20		μV/V
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±12			±10			±10			V

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

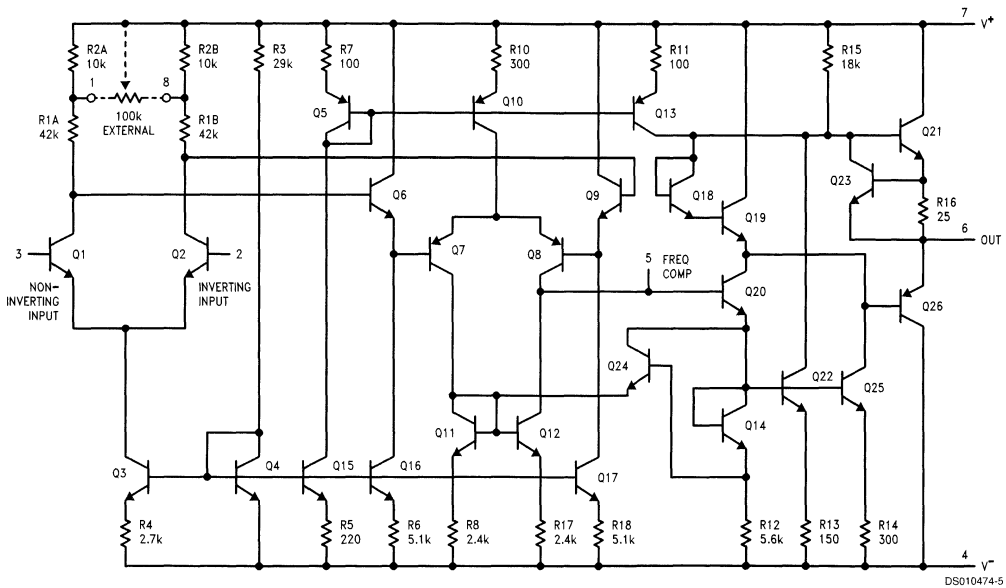
Note 2: Derate at 150°C/W for operation at ambient temperatures above 75°C.

Note 3: For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for V_S = ±15V unless otherwise specified.

Note 5: For Military electrical specifications RETS725AX are available for LM725AH and RETS725X are available for LM725H.

Schematic Diagram



National Semiconductor

LM7301
Low Power, 4 MHz GBW, Rail-to-Rail Input-Output Operational Amplifier in TinyPak™ Package

General Description

The LM7301 provides high performance in a wide range of applications. The LM7301 offers greater than rail-to-rail input range, full rail-to-rail output swing, large capacitive load driving ability and low distortion.

With only 0.6 mA supply current, the 4 MHz gain-bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

The LM7301 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

Operating on supplies of 1.8V–32V, the LM7301 is excellent for a very wide range of applications in low power systems.

Placing the amplifier right at the signal source reduces board size and simplifies signal routing. The LM7301 fits easily on low profile PCMCIA cards.

Features

at V_S = 5V (Typ unless otherwise noted)

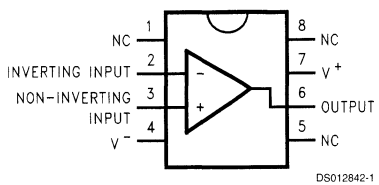
- Tiny SOT23-5 package saves space
- Greater than Rail-to-Rail Input CMVR −0.25V to 5.25V
- Rail-to-Rail Output Swing 0.07V to 4.93V
- Wide Gain-Bandwidth 4 MHz
- Low Supply Current 0.60 mA
- Wide Supply Range 1.8V to 32V
- High PSRR 104 dB
- High CMRR 93 dB
- Excellent Gain 97 dB

Applications

- Portable instrumentation
- Signal conditioning amplifiers/ADC buffers
- Active filters
- Modems
- PCMCIA cards

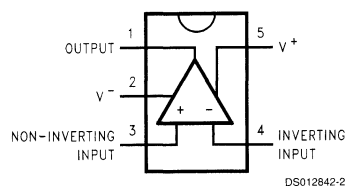
Connection Diagrams

8-Pin SO-8



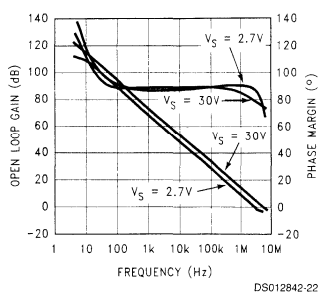
Top View

5-Pin SOT23

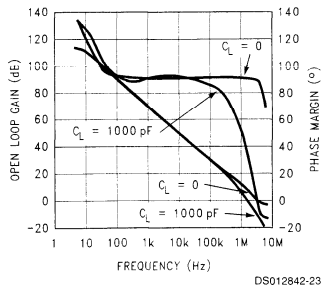


Top View

Gain and Phase



Gain and Phase, 2.7V Supply



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2500V
Differential Input Voltage	15V
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	35V
Current at Input Pin	±10 mA
Current at Output Pin (Note 3)	±20 mA
Current at Power Supply Pin	25 mA
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \le V_S \le 32V$
Junction Temperature Range	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
M5 Package, 5-Pin SOT23	325°C/W
M Package, 8-Pin Surface Mount	165°C/W

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7301 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.03	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**2**		µV/°C
I_B	Input Bias Current	V_{CM} = 0V	90	200 **250**	nA max
		V_{CM} = 5V	−40	−75 **−85**	nA min
I_{OS}	Input Offset Current	V_{CM} = 0V	0.7	70 **80**	nA max
		V_{CM} = 5V	0.7	55 **65**	
R_{IN}	Input Resistance, CM	$0V \le V_{CM} \le 5V$	39		MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 5V$	88	70 **67**	dB min
		$0V \le V_{CM} \le 3.5V$	93		
PSRR	Power Supply Rejection Ratio	$2.2V \le V^+ \le 30V$	104	87 **84**	
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 65 dB	5.1		V
			−0.1		V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ $V_O = 4.0V_{PP}$	71	14 **10**	V/mV min
V_O	Output Swing	R_L = 10 kΩ	0.07	0.12 **0.15**	V max
			4.93	4.88 **4.85**	V min
		R_L = 2 kΩ	0.14	0.20 **0.22**	V max
			4.87	4.80 **4.78**	V min
I_{SC}	Output Short Circuit Current	Sourcing	11.0	8.0 **5.5**	mA min
		Sinking	9.5	6.0 **5.0**	mA min

5.0V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7301 Limit (Note 6)	Units
I_S	Supply Current		0.60	1.10 **1.24**	mA max

AC Electrical Characteristics

T_J = 25°C, V^+ = 2.2V to 30V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	±4V Step @ V_S ±6V	1.25	V/μs
GBW	Gain-Bandwidth Product	f = 100 kHz, R_L = 10 kΩ	4	MHz
e_n	Input-Referred Voltage Noise	f = 1 kHz	36	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.24	$\frac{pA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	f = 10 kHz	0.006	%

2.2V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.2V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7301 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.04	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**2**		μV/°C
I_B	Input Bias Current	V_{CM} = 0V	89	200 **250**	nA max
		V_{CM} = 2.2V	−35	−75 **−85**	nA min
I_{OS}	Input Offset Current	V_{CM} = 0V	0.8	70 **80**	nA max
		V_{CM} = 2.2V	0.4	55 **65**	
R_{IN}	Input Resistance	0V ≤ V_{CM} ≤ 2.2V	18		MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 2.2V	82	60 **56**	dB min
PSRR	Power Supply Rejection Ratio	2.2V ≤ V^+ ≤ 30V	104	87 **84**	
V_{CM}	Input Common-Mode Voltage Range	CMRR > 60 dB	2.3		V
			−0.1		V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ V_O = $1.6V_{PP}$	46	6.5 **5.4**	V/mV min

2.2V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.2V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7301 Limit (Note 6)	Units
V_O	Output Swing	R_L = 10 kΩ	0.05	0.08 **0.10**	V max
			2.15	2.10 **2.00**	V min
		R_L = 2 kΩ	0.09	0.13 **0.14**	V max
			2.10	2.07 **2.00**	V min
I_{SC}	Output Short Circuit Current	Sourcing	10.9	8.0 **5.5**	mA min
		Sinking	7.7	6.0 **5.0**	mA min
I_S	Supply Current		0.57	0.97 **1.24**	mA max

30V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 30V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7301 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.04	6 **8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**2**		µV/°C
I_B	Input Bias Current	V_{CM} = 0V	103	300 **500**	nA max
		V_{CM} = 30V	−50	−100 **−200**	nA min
I_{OS}	Input Offset Current	V_{CM} = 0V	1.2	90 **190**	nA max
		V_{CM} = 30V	0.5	65 **135**	nA max
R_{IN}	Input Resistance	0V ≤ V_{CM} ≤ 30V	200		MΩ
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 30V	104	80 **78**	dB min
		0V ≤ V_{CM} ≤ 27V	115	90 **88**	
PSRR	Power Supply Rejection Ratio	2.2V ≤ V^+ ≤ 30V	104	87 **84**	
V_{CM}	Input Common-Mode Voltage Range	CMRR > 80 dB	30.1		V
			−0.1		V
A_V	Large Signal Voltage Gain	R_L = 10 kΩ V_O = $28V_{PP}$	105	30 **20**	V/mV min

30V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V^+ = 30V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LM7301 Limit (Note 6)	Units
V_O	Output Swing	R_L = 10 kΩ	0.16	0.275 **0.375**	V max
			29.8	29.75 **28.65**	V min
I_{SC}	Output Short Circuit Current	Sourcing (Note 4)	11.7	8.8 **6.5**	mA min
		Sinking (Note 4)	11.5	8.2 **6.0**	mA min
I_S	Supply Current		0.72	1.30 **1.35**	mA max

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

National Semiconductor

LM741
Operational Amplifier

General Description

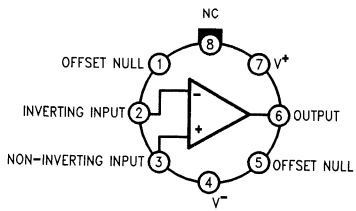
The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C is identical to the LM741/LM741A except that the LM741C has their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Connection Diagrams

Metal Can Package

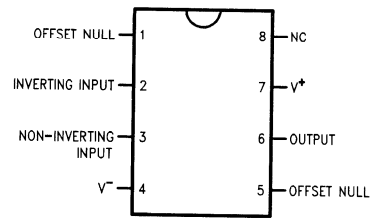


DS009341-2

Note 1: LM741H is available per JM38510/10101

Order Number LM741H, LM741H/883 (Note 1), **LM741AH/883 or LM741CH**
See NS Package Number H08C

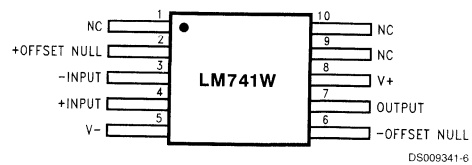
Dual-In-Line or S.O. Package



DS009341-3

Order Number LM741J, LM741J/883, LM741CN
See NS Package Number J08A, M08A or N08E

Ceramic Flatpak

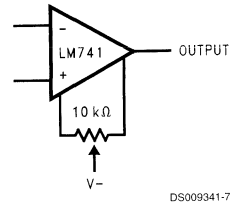


DS009341-6

Order Number LM741W/883
See NS Package Number W10A

Typical Application

Offset Nulling Circuit



DS009341-7

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

(Note 7)

	LM741A	LM741	LM741C
Supply Voltage	±22V	±22V	±18V
Power Dissipation (Note 3)	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V
Input Voltage (Note 4)	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	150°C	100°C
Soldering Information			
N-Package (10 seconds)	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C
M-Package			
Vapor Phase (60 seconds)	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.			
ESD Tolerance (Note 8)	400V	400V	400V

Electrical Characteristics (Note 5)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	$T_A = 25°C$										
	$R_S \leq 10\ k\Omega$					1.0	5.0		2.0	6.0	mV
	$R_S \leq 50\Omega$		0.8	3.0							mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 50\Omega$			4.0							mV
	$R_S \leq 10\ k\Omega$						6.0			7.5	mV
Average Input Offset Voltage Drift				15							µV/°C
Input Offset Voltage Adjustment Range	$T_A = 25°C$, $V_S = \pm 20V$	±10				±15			±15		mV
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			70		85	500			300	nA
Average Input Offset Current Drift				0.5							nA/°C
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500	nA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$			0.210			1.5			0.8	µA
Input Resistance	$T_A = 25°C$, $V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0		MΩ
	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$	0.5									MΩ
Input Voltage Range	$T_A = 25°C$							±12	±13		V
	$T_{AMIN} \leq T_A \leq T_{AMAX}$				±12	±13					V

Electrical Characteristics (Note 5) (Continued)

Parameter	Conditions	LM741A			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain	$T_A = 25°C$, $R_L \geq 2\ k\Omega$										
	$V_S = \pm 20V$, $V_O = \pm 15V$	50									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				50	200		20	200		V/mV
	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$R_L \geq 2\ k\Omega$,										
	$V_S = \pm 20V$, $V_O = \pm 15V$	32									V/mV
	$V_S = \pm 15V$, $V_O = \pm 10V$				25			15			V/mV
	$V_S = \pm 5V$, $V_O = \pm 2V$	10									V/mV
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	±16									V
	$R_L \geq 2\ k\Omega$	±15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$				±10	±13		±10	±13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$,										
	$V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		µs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 6)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/µs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 2: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Electrical Characteristics (Note 5) (Continued)

Note 3: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 4: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

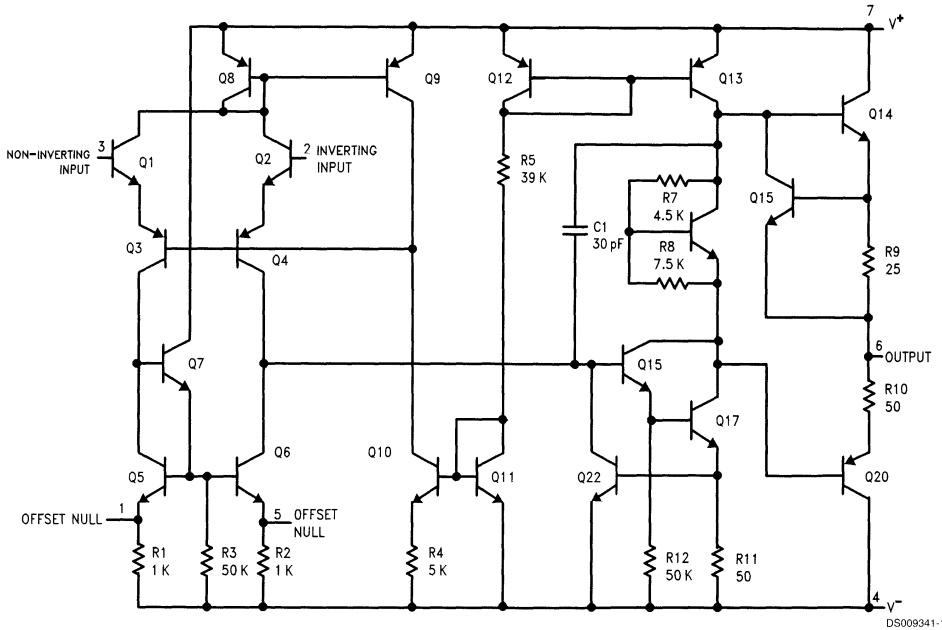
Note 5: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 6: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 7: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Schematic Diagram



National Semiconductor

LM8261 Single RRIO, High Output Current & Unlimited Cap Load Op Amp in SOT23-5

General Description

The LM8261 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and guaranteed high speed and slew rate while requiring only 0.97mA supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.5V to 30V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage. The output stage has low distortion (0.05% THD+N) and can supply a respectable amount of current (15mA) with minimal headroom from either rail (300mV).

The LM8261 is offered in the space saving SOT23-5 package.

Features

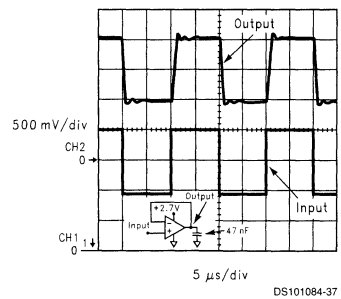
(V_S = 5V, T_A = 25°C, Typical values unless specified).

- GBWP 21MHz
- Wide supply voltage range 2.5V to 30V
- Slew rate 12V/µs
- Supply current 0.97 mA
- Cap load limit Unlimited
- Output short circuit current +53mA/−75mA
- +/−5% Settling time 400ns (500pF, 100mV_{PP} step)
- Input common mode voltage 0.3V beyond rails
- Input voltage noise 15nV/$\sqrt{Hz}$
- Input current noise 1pA/$\sqrt{Hz}$
- THD+N < 0.05%

Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

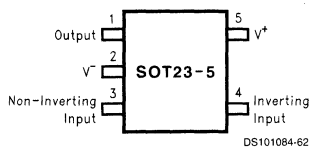
Output Response with Heavy Capacitive Load



DS101084-37

Connection Diagram

SOT23-5



DS101084-62

Top View

Ordering Information

Package	Ordering Info	Pkg Marking	Supplied As	NSC Drawing
5-Pin SOT-23	LM8261M5	A45A	1K Units Tape and Reel	MA05B
	LM8261M5X		3K Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2) 200V(Note 9)
V_{IN} Differential	+/−10V
Output Short Circuit Duration	(Notes 3, 11)
Supply Voltage (V^+ - V^-)	32V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C
Soldering Information:	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings

Supply Voltage (V^+ - V^-)	2.5V to 30V
Junction Temperature Range(Note 4)	−40°C to +85°C
Package Thermal Resistance, θ_{JA},(Note 4)	
SOT23-5	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 2.2V	+/−0.7	+/−5 **+/−7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 2.2V (Note 12)	+/−2	–	µV/C
I_B	Input Bias Current	V_{CM} = 0.5V (Note 7)	−1.20	−2.00 **−2.70**	µA max
		V_{CM} = 2.2V (Note 7)	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V & V_{CM} = 2.2V	20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 1.0V	100	76 **60**	dB min
		V_{CM} stepped from 1.7V to 2.7V	100		
		V_{CM} stepped from 0V to 2.7V	70	58 **50**	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V	104	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0.0**	V max
			3.0	2.8 **2.7**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 2.2V, R_L = 10K to V^-	78	70 **67**	dB min
		V_O = 0.5 to 2.2V, R_L = 2K to V^-	73	67 **63**	dB min
V_O	Output Swing High	R_L = 10K to V^-	2.59	2.49 **2.46**	V min
		R_L = 2K to V^-	2.53	2.45 **2.41**	
	Output Swing Low	R_L = 10K to V^-	90	100 **120**	mV max
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	48	30 **20**	mA min
		Sinking to V^+ V_{ID} = −200mV (Note 10)	65	50 **30**	mA min
I_S	Supply Current	No load, V_{CM} = 0.5V	0.95	1.20 **1.50**	mA max
SR	Slew Rate (Note 8)	A_V = +1,V_I = $2V_{PP}$	9	–	V/µs

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
f_u	Unity Gain-Frequency	V_I = 10mV, R_L = 2KΩ to V^+/2	10	–	MHz
GBWP	Gain Bandwidth Product	f = 50KHz	21	15.5 **14**	MHz min
Phi_m	Phase Margin	V_I = 10mV	50	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1		$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ll 10KΩ) to V^+/2	1	–	MHz

5V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 1V & V_{CM} = 4.5V	+/–0.7	+/–5 **+/– 7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 1V & V_{CM} = 4.5V (Note 12)	+/–2	–	µV/°C
I_B	Input Bias Current	V_{CM} = 1V (Note 7)	–1.18	–2.00 **–2.70**	µA max
		V_{CM} = 4.5V (Note 7)	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 1V & V_{CM} = 4.5V	20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 3.3V	110	84 **72**	dB min
		V_{CM} stepped from 4V to 5V	100	–	
		V_{CM} stepped from 0V to 5V	80	64 **61**	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V, V_{CM} = 0.5V	104	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–0.3	–0.1 **0.0**	V max
			5.3	5.1 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10K to V^-	84	74 **70**	dB min
		V_O = 0.5 to 4.5V, R_L = 2K to V^-	80	70 **66**	
V_O	Output Swing High	R_L = 10K to V^-	4.87	4.75 **4.72**	V min
		R_L = 2K to V^-	4.81	4.70 **4.66**	
	Output Swing Low	R_L = 10K to V^-	86	125 **135**	mV max
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	53	35 **20**	mA min
		Sinking to V^+ V_{ID} = –200mV (Note 10)	75	60 **50**	

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = $V^+/2$, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
I_S	Supply Current	No load, V_{CM} = 1V	0.97	1.25 **1.75**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $5V_{PP}$	12	10 **7**	V/µs min
f_u	Unity Gain Frequency	V_I = 10mV, R_L = 2KΩ to $V^+/2$	10.5	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	21	16 **15**	MHz min
Phi_m	Phase Margin	V_I = 10mV	53	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1	–	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ll 10kΩ) to $V^+/2$	900	–	KHz
t_S	Settling Time (+/–5%)	$100mV_{PP}$ Step, 500pF load	400	–	ns
THD+N	Total Harmonic Distortion + Noise	R_L = 1KΩ to $V^+/2$ f = 10KHz to A_V= +2, $4V_{PP}$ swing	0.05	–	%

+/–15V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 15V, V^- = –15V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = –14.5V & V_{CM} = 14.5V	+/–0.7	+/–7 **+/– 9**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = –14.5V & V_{CM} = 14.5V (Note 12)	+/–2	–	µV/°C
I_B	Input Bias Current	V_{CM} = –14.5V (Note 7)	–1.05	–2.00 **–2.80**	µA max
		V_{CM} = 14.5V (Note 7)	+0.49	+1.00 **+1.50**	
I_{OS}	Input Offset Current	V_{CM} = –14.5V & V_{CM} = 14.5V	30	275 **550**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from –15V to 13V	100	84 **80**	dB min
		V_{CM} stepped from 14V to 15V	100	–	
		V_{CM} stepped from –15V to 15V	88	74 **72**	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 12V to 15V	100	70 **66**	dB min
–PSRR	Negative Power Supply Rejection Ratio	V^- = –12V to –15V	100	70 **66**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–15.3	–15.1 **–15.0**	V max
			15.3	15.1 **15.0**	V min

+/−15V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 15V, V^- = −15V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
A_{VOL}	Large Signal Voltage Gain	V_O = 0V to +/−13V, R_L = 10KΩ	85	78 **74**	dB min
		V_O = 0V to +/−13V, R_L = 2KΩ	79	72 **66**	
V_O	Output Swing High	R_L = 10KΩ	14.83	14.65 **14.61**	V min
		R_L = 2KΩ	14.73	14.60 **14.55**	
	Output Swing Low	R_L = 10KΩ	−14.91	−14.75 **−14.65**	V max
		R_L = 2KΩ	−14.83	−14.65 **−14.60**	
I_{SC}	Output Short Circuit Current	Sourcing to ground V_{ID} = 200mV (Note 10)	60	40 **25**	mA min
		Sinking to ground V_{ID} = 200mV (Note 10)	100	70 **60**	
I_S	Supply Current	No load, V_{CM} = 0V	1.30	1.50 **1.90**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = 24V_{PP}	15	10 **8**	V/µs min
f_u	Unity Gain Frequency	V_I = 10mV, R_L = 2KΩ	14	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	24	18 **16**	MHz min
Phi_m	Phase Margin	V_I = 10mV	58	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1	–	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = 20pF ll 10KΩ	160	–	KHz
t_S	Settling Time (+/−1%, A_V = +1)	Positive Step, 5V_{PP}	320	–	ns
		Negative Step, 5V_{PP}	600	–	
THD+N	Total Harmonic Distortion +Noise	R_L = 1KΩ, f = 10KHz, A_V = +2, 28V_{PP} swing	0.01	–	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Note 9: Machine Model, 0Ω is series with 200pF.

Note 10: Short circuit test is a momentary test. See Note 11.

Note 11: Output short circuit duration is infinite for $V_S \leq$ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

Note 12: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

National Semiconductor

LM8262 Dual
RRIO, High Output Current & Unlimited Cap Load Op Amp in MSOP

General Description

The LM8262 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability, and provides tested and guaranteed high speed and slew rate. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage. The output stage has low distortion (0.05% THD+N) and can supply a respectable amount of current (15mA) with minimal headroom from either rail (300mV).

The LM8262 is offered in the space saving MSOP package.

Features

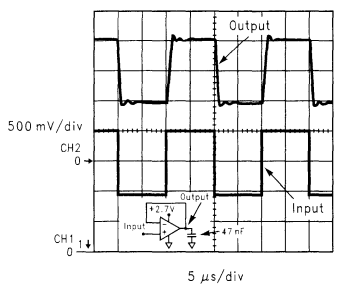
(V_S = 5V, T_A = 25°C, Typical values unless specified).

- GBWP 21MHz
- Wide supply voltage range 2.5V to 22V
- Slew rate 12V/µs
- Supply current/channel 1.15 mA
- Cap load limit Unlimited
- Output short circuit current +53mA/−75mA
- +/−5% Settling time 400ns (500pF, 100mV$_{PP}$ step)
- Input common mode voltage 0.3V beyond rails
- Input voltage noise 15nV/$\sqrt{Hz}$
- Input current noise 1pA/$\sqrt{Hz}$
- THD+N < 0.05%

Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

Output Response with Heavy Capacitive Load



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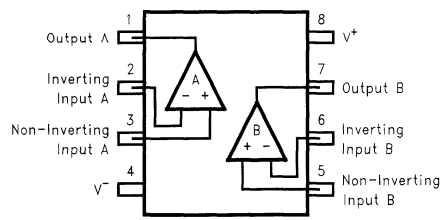
Connection Diagram

8-Pin MSOP



20021001

Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin MSOP	LM8262MM	A46	1k Units Tape and Reel	MUA08A
	LM8262MMX		3.5k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2) 200V(Note 9)
V_{IN} Differential	+/−10V
Output Short Circuit Duration	(Notes 3, 11)
Supply Voltage (V^+ - V^-)	24V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C
Soldering Information:	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings

Supply Voltage (V^+ - V^-)	2.5V to 22V
Junction Temperature Range(Note 4)	−40°C to +85°C
Package Thermal Resistance, θ_{JA},(Note 4)	
8-Pin MSOP	235°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 2.2V	–	+/−0.7	+/−5 **+/−7**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 2.2V (Note 12)	–	+/−2	–	µV/C
I_B	Input Bias Current	V_{CM} = 0.5V (Note 7)	–	−1.20	−2.00 **−2.70**	µA
		V_{CM} = 2.2V (Note 7)	–	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 0.5V & V_{CM} = 2.2V	–	20	250 **400**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 1.0V	76 **60**	100	–	dB
		V_{CM} stepped from 1.7V to 2.7V	–	100	–	
		V_{CM} stepped from 0V to 2.7V	58 **50**	70	–	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V	78 **74**	104	–	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–	−0.3	−0.1 **0.0**	V
			2.8 **2.7**	3.0	–	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 2.2V, R_L = 10K to V^-	70 **67**	78	–	dB
		V_O = 0.5 to 2.2V, R_L = 2K to V^-	67 **63**	73	–	dB
V_O	Output Swing High	R_L = 10K to V^-	2.49 **2.46**	2.59	–	V
		R_L = 2K to V^-	2.45 **2.41**	2.53	–	
	Output Swing Low	R_L = 10K to V^-	–	90	100 **120**	mV
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	30 **20**	48	–	mA
		Sinking to V^+ V_{ID} = −200mV (Note 10)	50 **30**	65	–	

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_S	Supply Current (both amps)	No load, V_{CM} = 0.5V	–	2.0	2.5 **3.0**	mA
SR	Slew Rate (Note 8)	A_V = +1, V_I = $2V_{PP}$	–	9	–	V/μs
f_u	Unity Gain-Frequency	V_I = 10mV, R_L = 2KΩ to V^+/2	–	10	–	MHz
GBWP	Gain Bandwidth Product	f = 50KHz	15.5 **14**	21	–	MHz
Phi_m	Phase Margin	V_I = 10mV	–	50	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	–	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	–	1	–	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ll 10KΩ) to V^+/2	–	1	–	MHz

5V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 1V & V_{CM} = 4.5V	–	+/–0.7	+/–5 **+/– 7**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = 1V & V_{CM} = 4.5V (Note 12)	–	+/–2	–	μV/°C
I_B	Input Bias Current	V_{CM} = 1V (Note 7)	–	–1.18	–2.00 **–2.70**	μA
		V_{CM} = 4.5V (Note 7)	–	+0.49	+1.00 **+1.60**	
I_{OS}	Input Offset Current	V_{CM} = 1V & V_{CM} = 4.5V	–	20	250 **400**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 3.3V	84 **72**	110	–	dB
		V_{CM} stepped from 4V to 5V	–	100	–	
		V_{CM} stepped from 0V to 5V	64 **61**	80	–	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 2.7V to 5V, V_{CM} = 0.5V	78 **74**	104	–	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–	–0.3	–0.1 **0.0**	V
			5.1 **5.0**	5.3	–	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10K to V^-	74 **70**	84	–	dB
		V_O = 0.5 to 4.5V, R_L = 2K to V^-	70 **66**	80	–	
V_O	Output Swing High	R_L = 10K to V^-	4.75 **4.72**	4.87	–	V
		R_L = 2K to V^-	4.70 **4.66**	4.81	–	
	Output Swing Low	R_L = 10K to V^-	–	86	125 **135**	mV

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	35 **20**	53	–	mA
		Sinking to V^+ V_{ID} = −200mV (Note 10)	60 **50**	75	–	
I_S	Supply Current (both amps)	No load, V_{CM} = 1V	–	2.3	2.8 **3.5**	mA
SR	Slew Rate (Note 8)	A_V = +1, V_I = $5V_{PP}$	10 **7**	12	–	V/µs
f_u	Unity Gain Frequency	V_I = 10mV, R_L = 2KΩ to V^+/2	–	10.5	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	16 **15**	21	–	MHz
Phi_m	Phase Margin	V_I = 10mV	–	53	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	–	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	–	1	–	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ‖ 10kΩ) to V^+/2	–	900	–	KHz
t_S	Settling Time (+/−5%)	$100mV_{PP}$ Step, 500pF load	–	400	–	ns
THD+N	Total Harmonic Distortion + Noise	R_L = 1KΩ to V^+/2 f = 10KHz to A_V= +2, $4V_{PP}$ swing	–	0.05	–	%

+/−11V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 11V, V^- = −11V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = −10.5V & V_{CM} = 10.5V	–	+/−0.7	+/−7 **+/− 9**	mV
TC V_{OS}	Input Offset Average Drift	V_{CM} = −10.5V & V_{CM} = 10.5V (Note 12)	–	+/−2	–	µV/°C
I_B	Input Bias Current	V_{CM} = −10.5V (Note 7)	–	−1.05	−2.00 **−2.80**	µA
		V_{CM} = 10.5V (Note 7)	–	+0.49	+1.00 **+1.50**	
I_{OS}	Input Offset Current	V_{CM} = −10.5V & V_{CM} = 10.5V	–	30	275 **550**	nA
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from −11V to 9V	84 **80**	100	–	dB
		V_{CM} stepped from 10V to 11V	–	100	–	
		V_{CM} stepped from −11V to 11V	74 **72**	88	–	
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 9V to 11V	70 **66**	100	–	dB
−PSRR	Negative Power Supply Rejection Ratio	V^- = −9V to −11V	70 **66**	100	–	dB

+/−11V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 11V, V^- = −11V, V_{CM} = 0V, V_O = 0V, and R_L > 1MΩ to 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	–	−11.3	−11.1 **−11.0**	V
			11.1 **11.0**	11.3	–	V
A_{VOL}	Large Signal Voltage Gain	V_O = 0V to +/−9V, R_L = 10kΩ	78 **74**	85	–	dB
		V_O = 0V to +/−9V, R_L = 2kΩ	72 **66**	79	–	
V_O	Output Swing High	R_L = 10kΩ	10.65 **10.61**	14.83	–	V
		R_L = 2kΩ	10.6 **10.55**	14.73	–	
	Output Swing Low	R_L = 10kΩ	–	−14.91	−10.75 **−10.65**	V
		R_L = 2kΩ	–	−14.83	−10.65 **−10.6**	
I_{SC}	Output Short Circuit Current	Sourcing to ground V_{ID} = 200mV (Note 10)	40 **25**	60	–	mA
		Sinking to ground V_{ID} = 200mV (Note 10)	65 **55**	100	–	
I_S	Supply Current	No load, V_{CM} = 0V	–	2.5	4 **5**	mA
SR	Slew Rate (Note 8)	A_V = +1, V_I = 16V_{PP}	10 **8**	15	–	V/µs
f_U	Unity Gain Frequency	V_I = 10mV, R_L = 2kΩ	–	13	–	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	18 **16**	24	–	MHz
Phi_m	Phase Margin	V_I = 10mV	–	58	–	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	–	15	–	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	–	1	–	$pA/\sqrt{Hz}$
t_S	Settling Time (+/−1%, A_V = +1)	Positive Step, 5V_{PP}	–	320	–	ns
		Negative Step, 5V_{PP}	–	600	–	
THD+N	Total Harmonic Distortion +Noise	R_L = 1kΩ, f = 10KHz, A_V = +2, 15V_{PP} swing	–	0.01	–	%
CT_{REJ}	Cross-Talk Rejection	f = 5MHz, Driver R_L = 10kΩ	–	68	–	dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Note 9: Machine Model, 0Ω is series with 200pF.

Note 10: Short circuit test is a momentary test. See Note 11.

Note 11: Output short circuit duration is infinite for $V_S \leq 6V$ at room temperature and below. For $V_S > 6V$, allowable short circuit duration is 1.5ms.

Note 12: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

National Semiconductor

LM8272 Dual
RRIO, High Output Current & Unlimited Cap Load Op Amp in Miniature Package

General Description

The LM8272 is a Rail-to-Rail input and output Op Amp which can operate with a wide supply voltage range. This device has high output current drive, greater than Rail-to-Rail input common mode voltage range, unlimited capacitive load drive capability while requiring only 0.95mA/channel supply current. It is specifically designed to handle the requirements of flat panel TFT panel V_{COM} driver applications as well as being suitable for other low power, and medium speed applications which require ease of use and enhanced performance over existing devices.

Greater than Rail-to-Rail input common mode voltage range with 50dB of Common Mode Rejection, allows high side and low side sensing, among many applications, without having any concerns over exceeding the range and no compromise in accuracy. Exceptionally wide operating supply voltage range of 2.5V to 24V alleviates any concerns over functionality under extreme conditions and offers flexibility of use in multitude of applications. In addition, most device parameters are insensitive to power supply variations; this design enhancement is yet another step in simplifying its usage.

The LM8272 is offered in the 8-pin MSOP package.

Features

(V_S = 12V, T_A = 25°C, Typical values unless specified).

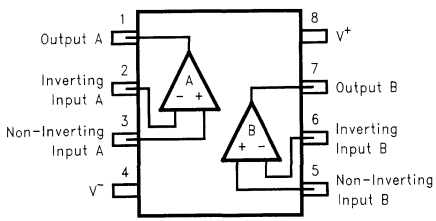
- GBWP 15MHz
- Wide supply voltage range 2.5V to 24V
- Slew rate 15V/µs
- Supply current/channel 0.95mA
- Cap load tolerance Unlimited
- Output short circuit current ±130mA
- Output current (1V from rails) ±65mA
- Input common mode voltage 0.3V beyond rails
- Input voltage noise $15nV/\sqrt{Hz}$
- Input current noise $1.4pA/\sqrt{Hz}$

Applications

- TFT-LCD flat panel V_{COM} driver
- A/D converter buffer
- High side/low side sensing
- Headphone amplifier

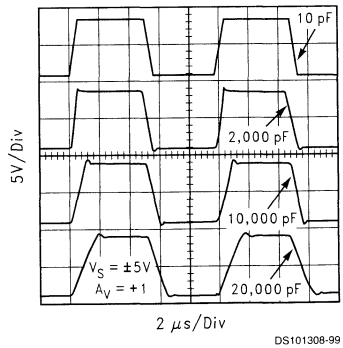
Connection Diagram

8-Pin MSOP



Top View

Large Signal Step Response for Various Cap. Load



Ordering Information

Package	Ordering Info	Pkg Marking	Supplied AS	NSC Drawing
8-Pin MSOP	LM8272MM	LM8272	1K Unit Tape and Reel	MUA08A
	LM8272MMX		3.5K Unit Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2) 200V(Note 9)
V_{IN} Differential	+/−10V
Output Short Circuit Duration	(Notes 3, 11)
Supply Voltage (V^+ - V^-)	27V
Voltage at Input/Output pins	V^+ +0.3V, V^- −0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C
Soldering Information:	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings

Supply Voltage (V^+ - V^-)	2.5V to 24V
Junction Temperature Range(Note 4)	−40°C to +85°C
Package Thermal Resistance, θ_{JA},(Note 4)	
8-Pin MSOP	235C/W

5V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 4.5V	+/−0.7	+/−5 **+/− 7**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 4.5V (Note 12)	+/−2	—	µV/°C
I_B	Input Bias Current	(Note 7)	—	±2.00 **±2.70**	µA max
I_{OS}	Input Offset Current		20	250 **400**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 5V	80	64 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V	100	78 **74**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0.0**	V max
			5.3	5.1 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 0.5 to 4.5V, R_L = 10kΩ to V^+/2	80	64 **60**	dB min
V_O	Output Swing High	R_L = 10kΩ to V^-	4.93	4.85	V min
		I_{SOURCE} = 5mA	4.85	4.70	
	Output Swing Low	R_L = 10kΩ to V^+	215	250	mV max
		I_{SINK} = 5mA	300	350	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	100	—	mA
		Sinking to V^+ V_{ID} = −200mV (Note 10)	100	—	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±55	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.8	2.3 **2.8**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $5V_{PP}$	12	—	V/µs
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2KΩ to V^+/2	7.5	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	13	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	55	—	Deg
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	$pA/\sqrt{Hz}$

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
f_{max}	Full Power Bandwidth	Z_L = (20pF ll 10kΩ) to V^+/2	700	—	KHz

12V Electrical Characteristics

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V & V_{CM} = 11.5V	+/−0.7	+/−7 **+/− 9**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.5V & V_{CM} = 11.5V (Note 12)	+/−2	—	µV/°C
I_B	Input Bias Current	(Note 7)	—	±2.00 **±2.80**	µA max
I_{OS}	Input Offset Current		30	275 **550**	nA max
CMRR	Common Mode Rejection Ratio	V_{CM} stepped from 0V to 12V	88	74 **72**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ from 4.5V to 13V, V_{CM} = 0.5V	100	78 **74**	dB min
−PSRR	Negative Power Supply Rejection Ratio		85	—	dB
CMVR	Input Common-Mode Voltage Range	CMRR > 50dB	−0.3	−0.1 **0**	V max
			12.3	12.1 **12.0**	V min
A_{VOL}	Large Signal Voltage Gain	V_O = 1V to 11V R_L = 10kΩ to V^+/2	83	74 **70**	dB min
V_O	Output Swing High	R_L 10kΩ to V^+/2	11.8	11.7	V min
		I_{SOURCE} = 5mA	11.6	11.5	
	Output Swing Low	R_L = 10kΩ to V^+/2	0.25	0.3	V max
		I_{SINK} = 5mA	.40	.45	
I_{SC}	Output Short Circuit Current	Sourcing to V^- V_{ID} = 200mV (Note 10)	130	110	mA min
		Sinking to V^+ V_{ID} = 200mV (Note 10)	130	110	
I_{OUT}	Output Current	V_{ID} = ±200mV, V_O = 1V from rails	±65	—	mA
I_S	Supply Current (Both Channel)	No load, V_{CM} = 0.5V	1.9	2.4 **2.9**	mA max
SR	Slew Rate (Note 8)	A_V = +1, V_I = $10V_{PP}$, C_L = 10pF	15	—	V/µs
		A_V = +1, V_I = $10V_{PP}$, C_L = 0.1µF	1	—	
R_{OUT}	Close Loop Output Resistance	A_V = +1, f = 100KHz	3	—	Ω
f_u	Unity Gain Frequency	V_I = 10mVp, R_L = 2kΩ to V^+/2	8	—	MHz
GBWP	Gain-Bandwidth Product	f = 50KHz	15	—	MHz
Phi_m	Phase Margin	V_I = 10mVp, R_L = 2KΩ to V^+/2	57	—	Deg
GM	Gain Margin	V_I = 10mVp, R_L = 2kΩ to V^+/2	20	—	dB
−3dB BW	Small Signal -3db Bandwidth	A_V = +1, R_L = 2kΩ to V^+/2	12.5	—	MHz
		A_V = +1, R_L = 600Ω to V^+/2	10.5	—	
		A_V = +10, R_L = 600Ω to V^+/2	1.0	—	

12V Electrical Characteristics (Continued)

Unless otherwise specified, all limited guaranteed for T_J = 25°C, V^+ = 12V, V^- = 0V, V_{CM} = 6V, V_O = 6V, and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
e_n	Input-Referred Voltage Noise	f = 2KHz, R_S = 50Ω	15	—	$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 2KHz	1.4	—	$pA/\sqrt{Hz}$
f_{max}	Full Power Bandwidth	Z_L = (20pF ll 10kΩ) to $V^+/2$	300	—	KHz
THD+N	Total Harmonic Distortion +Noise	A_V = +2, R_L = 2kΩ to $V^+/2$ V_O = $8V_{PP}$, V_S = ±5V	0.02	—	%
CT Rej.	Cross-Talk Rejection	f = 5MHz, Driver R_L = 10kΩ to $V^+/2$	68	—	dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Rating indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the slower of the rising and falling slew rates. Connected as a Voltage Follower.

Note 9: Machine Model, 0Ω is series with 200pF.

Note 10: Short circuit test is a momentary test. See Note 11.

Note 11: Output short circuit duration is infinite for $V_S \leq$ 6V at room temperature and below. For V_S > 6V, allowable short circuit duration is 1.5ms.

Note 12: Offset voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

National Semiconductor

LM833
Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

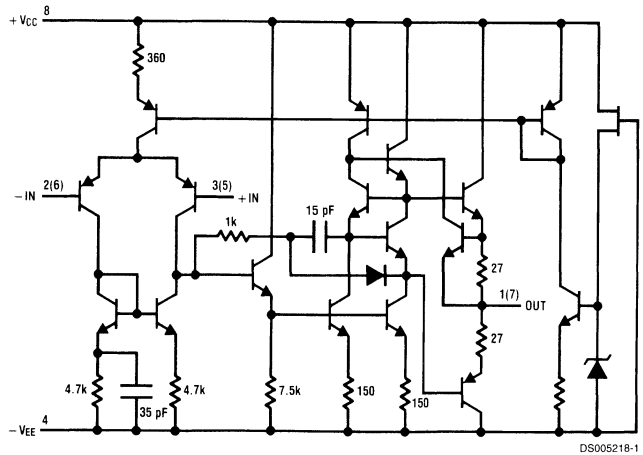
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

Features

- Wide dynamic range: >140dB
- Low input noise voltage: 4.5nV/√Hz
- High slew rate: 7 V/μs (typ); 5V/μs (min)
- High gain bandwidth: 15MHz (typ); 10MHz (min)
- Wide power bandwidth: 120KHz
- Low distortion: 0.002%
- Low offset voltage: 0.3mV
- Large phase margin: 60°
- Available in 8 pin MSOP package

Schematic Diagram (1/2 LM833)



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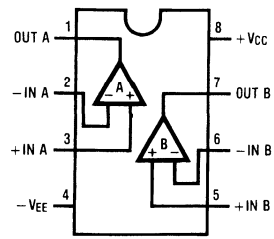
Connection Diagram



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Order Number LM833M, LM833MX, LM833N, LM833MM or LM833MMX
See NS Package Number
M08A, N08E or MUA08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage $V_{CC}-V_{EE}$	36V
Differential Input Voltage (Note 3) V_I	±30V
Input Voltage Range (Note 3) V_{IC}	±15V
Power Dissipation (Note 4) P_D	500 mW
Operating Temperature Range T_{OPR}	−40 ~ 85°C
Storage Temperature Range T_{STG}	−60 ~ 150°C

Soldering Information

Dual-In-Line Package Soldering (10 seconds)	260°C
Small Outline Package (SOIC and MSOP)	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 5) 1600V

DC Electrical Characteristics (Notes 1, 2)

(T_A = 25°C, V_S = ±15V)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 10Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Voltage Gain	R_L = 2 kΩ, V_O = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 10 kΩ	±12	±13.5		V
		R_L = 2 kΩ	±10	±13.4		V
V_{CM}	Input Common-Mode Range		±12	±14.0		V
CMRR	Common-Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15~5V, −15~−5V	80	100		dB
I_Q	Supply Current	V_O = 0V, Both Amps		5	8	mA

AC Electrical Characteristics

(T_A = 25°C, V_S = ±15V, R_L = 2 kΩ)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR	Slew Rate	R_L = 2 kΩ	5	7		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz	10	15		MHz

Design Electrical Characteristics

(T_A = 25°C, V_S = ±15V)

The following parameters are not tested or guaranteed.

Symbol	Parameter	Conditions	Typ	Units
$\Delta V_{OS}/\Delta T$	Average Temperature Coefficient of Input Offset Voltage		2	μV/°C
THD	Distortion	R_L = 2 kΩ, f = 20~20 kHz V_{OUT} = 3 Vrms, A_V = 1	0.002	%
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1 kHz	4.5	nV/$\sqrt{Hz}$
i_n	Input Referred Noise Current	f = 1 kHz	0.7	pA/$\sqrt{Hz}$
PBW	Power Bandwidth	V_O = 27 V_{pp}, R_L = 2 kΩ, THD ≤ 1%	120	kHz
f_U	Unity Gain Frequency	Open Loop	9	MHz
ϕ_M	Phase Margin	Open Loop	60	deg
	Input Referred Cross Talk	f = 20~20 kHz	−120	dB

Design Electrical Characteristics (Continued)

Note 1: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 3: If supply voltage is less than ±15V, it is equal to supply voltage.

Note 4: This is the permissible value at $T_A \leq 85^{\circ}C$.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM837
Low Noise Quad Operational Amplifier

General Description

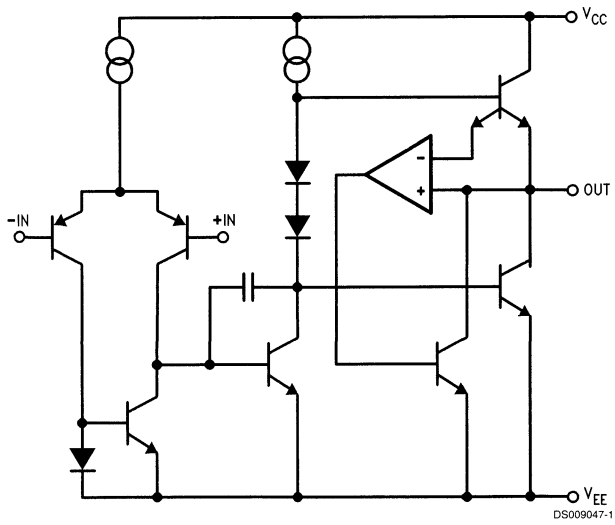
The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and can therefore be used to upgrade existing systems with little or no change.

Features

- High slew rate — 10 V/μs (typ); 8 V/μs (min)
- Wide gain bandwidth product (min) — 25 MHz (typ); 15 MHz
- Power bandwidth — 200 kHz (typ)
- High output current — ±40 mA
- Excellent output drive performance — >600Ω
- Low input noise voltage — 4.5 nV/√Hz
- Low total harmonic distortion — 0.0015%
- Low offset voltage — 0.3 mV

Schematic and Connection Diagrams



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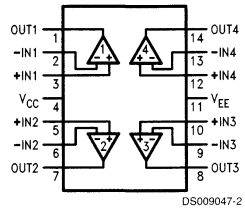
Dual-In-Line Package



DS009047-2

Top View
Order Number LM837M, LM837MX or LM837N
See NS Package Number M14A or N14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}/V_{EE} ±18V

Differential Input Voltage, V_{ID} (Note 2) ±30V

Common Mode Input Voltage, V_{IC} (Note 2) ±15V

Power Dissipation, P_D (Note 3) 1.2W (N) 830 mW (M)

Operating Temperature Range, T_{OPR} −40°C to +85°C

Storage Temperature Range, T_{STG} −60°C to +150°C

Soldering Information

Dual-In-Line Package
Soldering (10 seconds) 260°C

Small Outline Package
Vapor Phase (60 seconds) 215°C
Infrared (15 seconds) 220°C

ESD rating to be determined.

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics

T_A = 25°C, V_S = ±15V

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OS}	Input Offset Voltage	R_S = 50Ω		0.3	5	mV
I_{OS}	Input Offset Current			10	200	nA
I_B	Input Bias Current			500	1000	nA
A_V	Large Signal Voltage Gain	R_L = 2 kΩ, V_{OUT} = ±10V	90	110		dB
V_{OM}	Output Voltage Swing	R_L = 2 kΩ	±12	±13.5		V
		R_L = 600Ω	±10	±12.5		V
V_{CM}	Common Mode Input Voltage		±12	±14.0		V
CMRR	Common Mode Rejection Ratio	V_{IN} = ±12V	80	100		dB
PSRR	Power Supply Rejection Ratio	V_S = 15 ~ 5, −15 ~ −5	80	100		dB
I_S	Power Supply Current	R_L = ∞, Four Amps		10	15	mA

AC Electrical Characteristics

T_A = 25°C, V_S = ±15V

Symbol	Parameter	Condition	Min	Typ	Max	Units
SR	Slew Rate	R_L = 600Ω	8	10		V/μs
GBW	Gain Bandwidth Product	f = 100 kHz, R_L = 600Ω	15	25		MHz

Design Electrical Characteristics

T_A= 25°C, V_S=±15V (Note 4)

Symbol	Parameter	Condition	Min	Typ	Max	Units
PBW	Power Bandwidth	V_O = 25 V_{P-P}, R_L = 600Ω, THD < 1%		200		kHz
e_{n1}	Equivalent Input Noise Voltage	JIS A, R_S = 100Ω		0.5		μV
e_{n2}	Equivalent Input Noise Voltage	f = 1 kHz		4.5		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 1 kHz		0.7		pA/$\sqrt{Hz}$
THD	Total Harmonic Distortion	A_V = 1, V_{OUT} = 3 Vrms, f = 20 ~ 20 kHz, R_L = 600Ω		0.0015		%
f_U	Zero Cross Frequency	Open Loop		12		MHz
ϕ_m	Phase Margin	Open Loop		45		deg
	Input-Referred Crosstalk	f = 20 ~ 20 kHz		−120		dB
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage			2		μV/°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

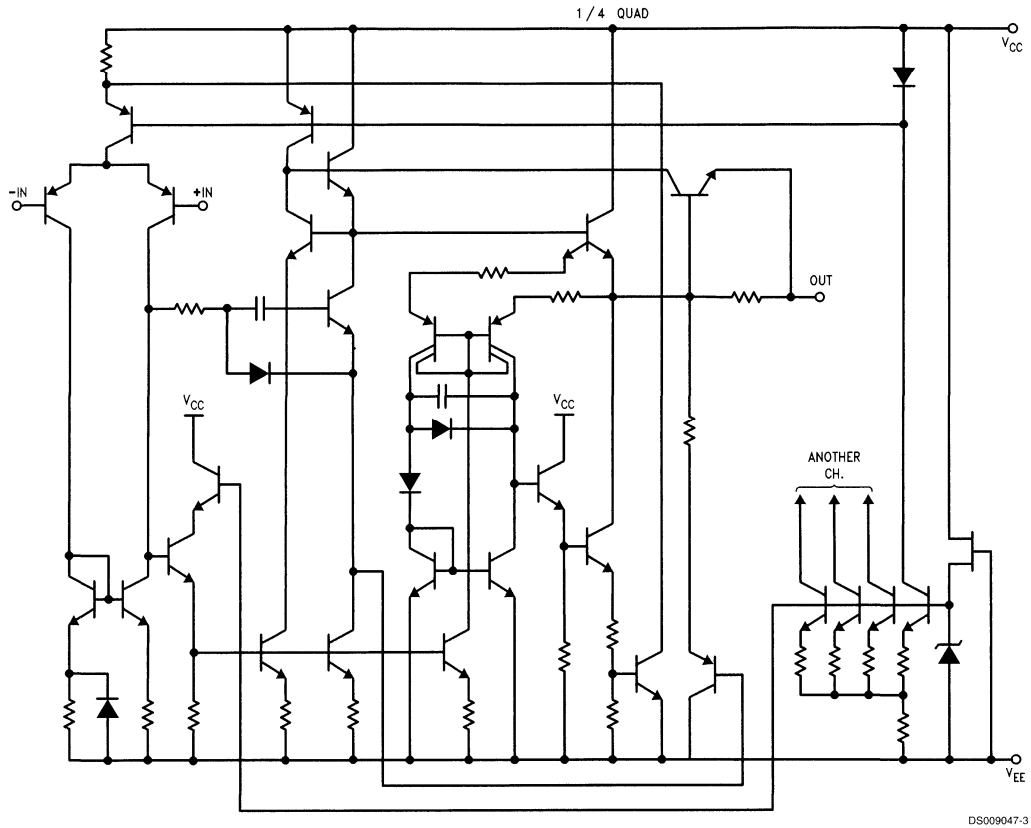
Note 2: Unless otherwise specified the absolute maximum input voltage is equal to the power supply voltage.

Design Electrical Characteristics (Continued)

Note 3: For operation at ambient temperatures above 25˚C, the device must be derated based on a 150˚C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM837N, 90˚C/W; LM837M, 150˚C/W.

Note 4: The following parameters are not tested or guaranteed.

Detailed Schematic



National Semiconductor

LMC2001
High Precision, 6MHz Rail-To-Rail Output Operational Amplifier

General Description

The LMC2001 is a new precision amplifier that offers unprecedented accuracy and stability at an affordable price and is offered in miniature (SOT23-5) package. This device utilizes patented techniques to measure and continually correct the input offset error voltage. The result is an amplifier which is ultra stable over time, and temperature. It has excellent CMRR and PSRR ratings, and does not exhibit the familiar 1/f voltage and current noise increase that plagues traditional amplifiers. The combination of the LMC2001 characteristics makes it a good choice for transducer amplifiers, high gain configurations, ADC buffer amplifiers, DAC I-V conversion, and any other 5V application requiring precision and/or stability.

Other useful benefits of the LMC2001 are rail-to-rail output, low supply current of 750µA, and wide gain-bandwidth product of 6MHz. The LMC2001 comes in 5 pin SOT23 and 8 pin SOIC. These extremely versatile features found in the LMC2001 provide high performance and ease of use.

Features

(Vs = 5V, R_L = 10K to V^+ /2, Typ. Unless Noted)

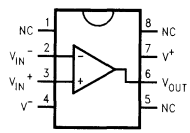
- Low Guaranteed V_{os} 40µV
- e_n With No 1/f 85nV/$\sqrt{Hz}$
- High CMRR 120dB
- High PSRR 120dB
- High A_{VOL} 137dB
- Wide Gain-Bandwidth Product 6MHz
- High Slew Rate 5V/µs
- Low Supply Current 750µA
- Rail-To-Rail Output 30mV from either rail
- No External Capacitors Required

Applications

- Precision Instrumentation Amplifiers
- Thermocouple Amplifiers
- Strain Gauge Bridge Amplifier

Connection Diagrams

8-Pin SO



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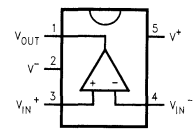
Top View

5-Pin SOT23



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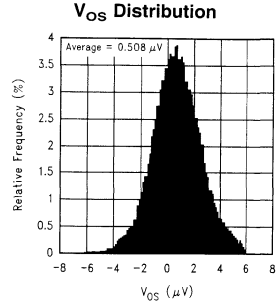
Top View

V_{OS} Distribution



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	100V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+ - V^-)	5.6V
Current At Input Pin	30mA
Current At Output Pin	30mA
Current At Power Supply Pin (Note 3)	50mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	-65°C to 150°C
Junction Temperature (T_J) (Note 4)	150°C

Operating Ratings (Note 1)

Supply voltage	4.75V to 5.25V
Temperature Range	
LMC2001AI	$-40°C \le T_J \le 85°C$
LMC2001AC	$0°C \le T_J \le 70°C$
Thermal resistance (θ_{JA})	
M Package, 8-pin Surface Mount	180°C /W
M5 Package, SOT23-5	274°C /W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	(Note 11)	0.5	40 **60**	µV max
	Offset Calibration Time		5	30	ms
TCV_{OS}	Input Offset Voltage	(Note 12)	0.015		µV/°C
	Long-Term Offset Drift	(Note 8)	0.006		µV/month
	Lifetime V_{OS} drift	(Note 8)	2.5	5	µV Max
I_{IN}	Input Current	(Note 9)	-3		pA
I_{OS}	Input Offset Current		6		pA
R_{IND}	Input Differential Resistance		9		MΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3.5V$	120	100	dB min
		$0.1V \le V_{CM} \le 3.5V$	**110**	**90**	dB min
PSRR	Power Supply Rejection Ratio	$4.75V \le V^+ \le 5.25V$	120	95 **90**	dB min
A_{VOL}	Large Signal Voltage Gain (Note 7)	R_L = 10kΩ	137	105 **100**	dB min
		R_L = 2kΩ	128	95 **90**	
V_O	Output Swing	R_L = 10kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.975	4.955 **4.955**	V min
			0.030	0.060 **0.060**	V max
		R_L = 2kΩ to 2.5V V_{IN}(diff) = ±0.5V	4.936		V
			0.075		V
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	5.9	4.1 **1.5**	mA min
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	14.5	4.5 **1.5**	mA min
I_S	Supply Current		0.75	1.0 **1.2**	mA max

AC Electrical Characteristics

T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, V_O = 2.5V, and R_L > 1MΩ.

Symbol	Parameter	Conditions		Typ (Note 5)	Units
SR	Slew Rate	A_V = +1, V_{IN} = 3.5Vpp		5	V/μs
GBW	Gain-Bandwidth Product			6	MHz
θ_m	Phase Margin			75	Deg
G_m	Gain Margin			12	dB
e_n	Input-Referred Voltage Noise	f = 0.1Hz		85	$nV/\sqrt{Hz}$
e_np-p	Input-Referred Voltage Noise	R_S = 100Ω, DC to 10Hz		1.6	μVpp
i_n	Input-Referred Current Noise	f = 0.1Hz		180	$fA/\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 1kHz, Av = -2 R_L = 10kΩ,V_O = 4.5Vpp		0.02	%
trec	Input Overload Recovery Time			50	ms
T_S	Output Settling time	(Note 10) A_V = +1, 1V step	1%	250	ns
			0.1%	400	
			0.01%	3200	
		(Note 10)A_V = −1, 1V step	1%	80	
			0.1%	860	
			0.01%	1400	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Note 3: Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis, unless otherwise noted.

Note 7: V^+ = 5V, V_{CM} = 2.5V, and R_L connected to 2.5V. For Sourcing tests, 2.5V ≤ V_O ≤ 4.8V. For Sinking tests, 0.2V ≤ V_O ≤ 2.5V.

Note 8: Guaranteed Vos Drift is based on 280 devices operated for 1000 hrs at 150°C (equivalent to 30 years @ 55°C).

Note 9: Guaranteed by design only.

Note 10: Settling times shown correspond to the worse case (positive or negative step) and does not include slew time. See the Application Note section for test schematic.

Note 11: The limits are set by the accuracy of high speed automatic test equipment. For the typical V_{OS} distribution, see the curve on page 4.

Note 12: Precision bench measurement of more than 300 units. More than 65% of units had less than 15nV /°C V_{OS} drift.

National Semiconductor

LMC6001
Ultra Ultra-Low Input Current Amplifier

General Description

Featuring 100% tested input currents of 25 fA max., low operating power, and ESD protection of 2000V, the LMC6001 achieves a new industry benchmark for low input current operational amplifiers. By tightly controlling the molding compound, National is able to offer this ultra-low input current in a lower cost molded package.

To avoid long turn-on settling times common in other low input current opamps, the LMC6001A is tested 3 times in the first minute of operation. Even units that meet the 25 fA limit are rejected if they drift.

Because of the ultra-low input current noise of 0.13 fA/$\sqrt{\text{Hz}}$, the LMC6001 can provide almost noiseless amplification of high resistance signal sources. Adding only 1 dB at 100 kΩ, 0.1 dB at 1 MΩ and 0.01 dB or less from 10 MΩ to 2,000 MΩ, the LMC6001 is an almost noiseless amplifier.

The LMC6001 is ideally suited for electrometer applications requiring ultra-low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. Since input referred noise is only 22 nV/$\sqrt{\text{Hz}}$, the LMC6001 can achieve higher signal to noise ratio than JFET input type electrometer amplifiers. Other applications of the LMC6001 include long interval integrators, ultra-high input impedance instrumentation amplifiers, and sensitive electrical-field measurement circuits.

Features

(Max limit, 25°C unless otherwise noted)

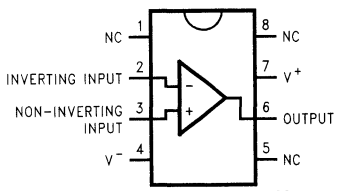
- Input current (100% tested): 25 fA
- Input current over temp.: 2 pA
- Low power: 750 µA
- Low V_{OS}: 350 µV
- Low noise: 22 nV/$\sqrt{\text{Hz}}$ @1 kHz Typ.

Applications

- Electrometer amplifier
- Photodiode preamplifier
- Ion detector
- A.T.E. leakage testing

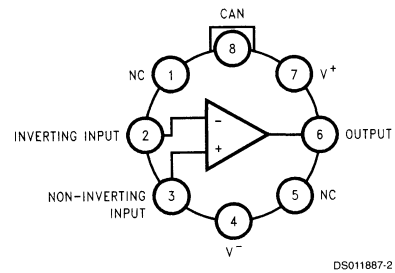
Connection Diagrams

8-Pin DIP



Top View

8-Pin Metal Can



Top View

Ordering Information

Package	Industrial Temperature Range −40°C to +85°C	NSC Package Drawing
8-Pin Molded DIP	LMC6001AIN, LMC6001BIN, LMC6001CIN	N08E
8-Pin Metal Can	LMC6001AIH, LMC6001BIH	H08C

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V, (V^-) - 0.3V$
Supply Voltage $(V^+ - V^-)$	−0.3V to +16V
Output Short Circuit to V^+	(Notes 2, 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temperature	−65°C to +150°C
Junction Temperature	150°C
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 9)
ESD Tolerance (Note 9)	2 kV

Operating Ratings (Note 1)

Temperature Range	
LMC6001AI, LMC6001BI, LMC6001CI	
$-40°C \le T_J \le +85°C$	
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (Note 11)	
θ_{JA}, N Package	100°C/W
θ_{JA}, H Package	145°C/W
θ_{JC}, H Package	45°C/W
Power Dissipation	(Note 8)

DC Electrical Characteristics

Limits in standard typeface are guaranteed for $T_J = 25°C$ and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, and $R_L > 1M$.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5) LMC6001AI	Limits (Note 5) LMC6001BI	Limits (Note 5) LMC6001CI	Units
I_B	Input Current	Either Input, $V_{CM} = 0V$, $V_S = \pm5V$	10	25 **2000**	100 **4000**	1000 **4000**	fA
I_{OS}	Input Offset Current		5	**1000**	**2000**	**2000**	
V_{OS}	Input Offset Voltage			0.35 **1.0**	1.0 **1.7**	1.0 **2.0**	mV
		$V_S = \pm5V$, $V_{CM} = 0V$		0.7 **1.35**	1.35 **2.0**	1.35	
TCV_{OS}	Input Offset Voltage Drift		2.5	10	10		µV/°C
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 7.5V$, $V^+ = 10V$	83	75 **72**	72 **68**	66 **63**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	73 **70**	66 **63**	66 **63**	
−PSRR	Negative Power Supply Rejection Ratio	$0V \ge V^- \ge -10V$	94	80 **77**	74 **71**	74 **71**	
A_V	Large Signal Voltage Gain	Sourcing, $R_L = 2 k\Omega$ (Note 6)	1400	400 **300**	300 **200**	300 **200**	V/mV min
		Sinking, $R_L = 2 k\Omega$ (Note 6)	350	180 **100**	90 **60**	90 **60**	
V_{CM}	Input Common-Mode Voltage	$V^+ = 5V$ and 15V For CMRR ≥ 60 dB	−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V min
V_O	Output Swing	$V^+ = 5V$, $R_L = 2 k\Omega$ to 2.5V	4.87	4.80 **4.73**	4.75 **4.67**	4.75 **4.67**	V min
			0.10	0.14 **0.17**	0.20 **0.24**	0.20 **0.24**	V max
		$V^+ = 15V$, $R_L = 2 k\Omega$ to 7.5V	14.63	14.50 **14.34**	14.37 **14.25**	14.37 **14.25**	V min
			0.26	0.35 **0.45**	0.44 **0.56**	0.44 **0.56**	V max

DC Electrical Characteristics (Continued)

Limits in standard typeface guaranteed for T_J = 25°C and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, and R_L > 1M.

Symbol	Parameter	Conditions	Typical (Note 4)	Limits (Note 5)			Units
				LMC6001AI	LMC6001BI	LMC6001CI	
I_O	Output Current	Sourcing, V^+ = 5V, V_O = 0V	22	16 **10**	13 **8**	13 **8**	mA min
		Sinking, V^+ = 5V, V_O = 5V	21	16 **13**	13 **10**	13 **10**	
		Sourcing, V^+ = 15V, V_O = 0V	30	28 **22**	23 **18**	23 **18**	
		Sinking, V^+ = 15V, V_O = 13V (Note 10)	34	28 **22**	23 **18**	23 **18**	
I_S	Supply Current	V^+ = 5V, V_O = 1.5V	450	750 **900**	750 **900**	750 **900**	µA max
		V^+ = 15V, V_O = 7.5V	550	850 **950**	850 **950**	850 **950**	

AC Electrical Characteristics

Limits in standard typeface guaranteed for T_J = 25°C and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V and R_L > 1M.

Symbol	Parameter	Conditions	Typical	Limits (Note 5)			Units
			(Note 4)	LM6001AI	LM6001BI	LM6001CI	
SR	Slew Rate	(Note 7)	1.5	0.8	0.8	0.8	V/µs
				0.6	**0.6**	**0.6**	min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕf_m	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/$\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.13				fA/$\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10, R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 7: V^+ = 15V. Connected as Voltage Follower with 10V step input. Limit specified is the lower of the positive and negative slew rates.

Note 8: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 9: Human body model, 1.5 kΩ in series with 100 pF.

Note 10: Do not connect the output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 11: All numbers apply for packages soldered directly into a printed circuit board.

National Semiconductor

LMC6022
Low Power CMOS Dual Operational Amplifier

General Description

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^-, low input bias current, and voltage gain (into 100k and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Features

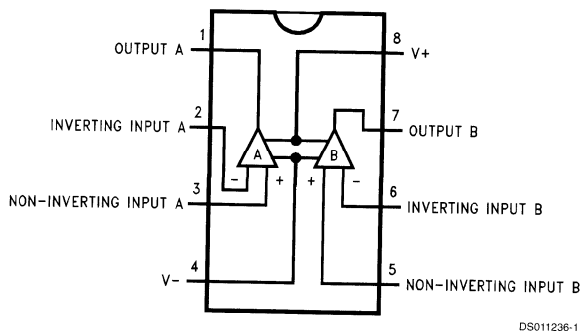
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain: 120 dB
- Low offset voltage drift: 2.5 μV/°C
- Ultra low input bias current: 40 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- Low distortion: 0.01% at 1 kHz
- Slew rate: 0.11 V/μs
- Micropower operation: 0.5 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

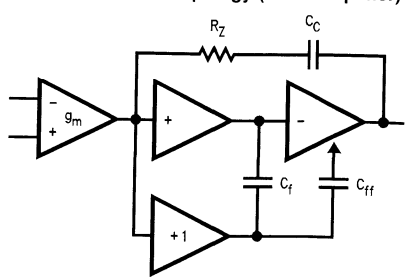
Connection Diagram

8-Pin DIP/SO



Top View

LMC6022 Circuit Topology (Each Amplifier)



Absolute Maximum Ratings (Note 1)

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Current at Input Pin	±5 mA
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 12)

Operating Ratings

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		µV/°C
I_B	Input Bias Current		0.04	 **200**	pA max
I_{OS}	Input Offset Current		0.01	 **100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **61**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	63 **61**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **73**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	V min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7) Sourcing	1000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 5 k\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.40 **4.43**	V min
			0.004	0.06 **0.09**	V max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.20 **4.00**	V min
			0.040	0.25 **0.35**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.00 **13.90**	V min
			0.007	0.06 **0.09**	V max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	13.70 **13.50**	V min
			0.110	0.32 **0.40**	V max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA min
		Sinking, $V_O = 5V$ (Note 2)	21	13 **9**	mA min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA min
		Sinking, $V_O = 13V$ (Note 12)	39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	86	140 **165**	μA max

AC Electrical Characteristics

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless other otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6022I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		0.35		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		nV/$\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{\text{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC6024
Low Power CMOS Quad Operational Amplifier

General Description

The LMC6024 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^-, low input bias current and voltage gain (into 100 kΩ and 5 kΩ loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6022 datasheet for a CMOS dual operational amplifier with these same features.

Features

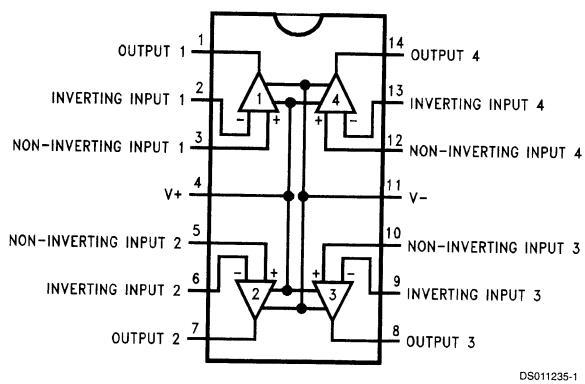
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low offset voltage drift 2.5 μV/°C
- Ultra low input bias current 40 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Micropower operation 1 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram

14-Pin DIP/SO



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Voltage at Output/Input Pin	(V^+) + 0.3V, (V^-) − 0.3V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV Max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.5		µV/°C
I_B	Input Bias Current		0.04	 **200**	pA Max
I_{OS}	Input Offset Current		0.01	 **100**	pA Max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **61**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	63 **61**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **73**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 DB	−0.4	−0.1 **0**	V Max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7) Sourcing	1000	200 **100**	V/mV Min
		Sinking	500	90 **40**	V/mV Min
		$R_L = 5 k\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV Min
		Sinking	250	50 **20**	V/mV Min

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
V_O	Output Voltage Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.40 **4.43**	V Min
			0.004	0.06 **0.09**	V Max
		$V^+ = 5V$ $R_L = 5\ k\Omega$ to 2.5V	4.940	4.20 **4.00**	V Min
			0.040	0.25 **0.35**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to 7.5V	14.970	14.00 **13.90**	V Min
			0.007	0.06 **0.09**	V Max
		$V^+ = 15V$ $R_L = 5\ k\Omega$ to 7.5V	14.840	13.70 **13.50**	V Min
			0.110	0.32 **0.40**	V Max
I_O	Output Current	$V^+ = 5V$ Sourcing, $V_O = 0V$	22	13 **9**	mA Min
		Sinking $V_O = 5V$ (Note 2)	21	13 **9**	mA Min
		$V^+ = 15V$ Sourcing, $V_O = 0V$	40	23 **15**	mA Min
		Sinking, $V_O = 13V$ (Note 12)	39	23 **15**	mA Min
I_S	Supply Current	All Four Amplifiers $V_O = 1.5V$	160	240 **280**	μA Max

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6024I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.11	0.05 **0.03**	V/μs Min
GBW	Gain-Bandwidth Product		0.35		MHz
θ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	42		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversly affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharge through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC6032
CMOS Dual Operational Amplifier

General Description

The LMC6032 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600Ω.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6034 datasheet for a CMOS quad operational amplifier with these same features. For higher performance characteristics refer to the LMC662.

Features

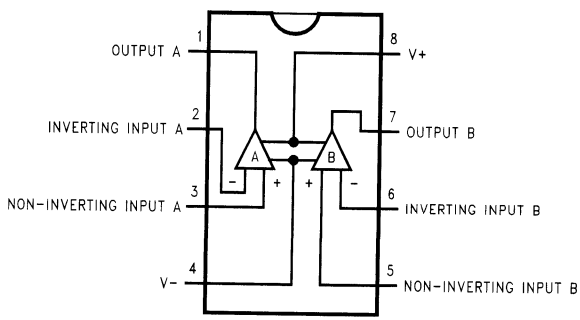
- Specified for 2 kΩ and 600Ω loads
- High voltage gain: 126 dB
- Low offset voltage drift: 2.3 μV/°C
- Ultra low input bias current: 40 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V^+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/μs
- Improved performance over TLC272

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

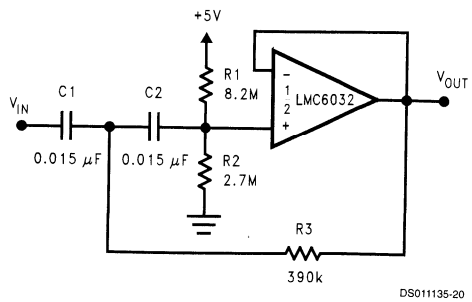
Connection Diagram

8-Pin DIP/SO



Top View

10 Hz High-Pass Filter



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	1000V
Power Dissipation	(Note 3)
Voltage at Output/Input Pin	(V^+) + 0.3V, (V^-) − 0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 11)
Thermal Resistance (θ_{JA}), (Note 12)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9	mV
				11	max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.3		µV/°C
I_B	Input Bias Current		0.04		pA
				200	max
I_{OS}	Input Offset Current		0.01		pA
				100	max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$, $V^+ = 15V$	83	63	dB
				60	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	83	63	dB
				60	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V, For CMRR ≥ 50 dB	−0.4	−0.1	V
				0	max
			$V^+ - 1.9$	$V^+ - 2.3$	V
				$V^+ - 2.6$	min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Note 7) Sourcing	2000	200	V/mV
				100	min
		Sinking	500	90	V/mV
				40	min
		R_L = 600Ω (Note 7) Sourcing	1000	100	V/mV
				75	min
		Sinking	250	50	V/mV
				20	min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
V_O	Output Voltage Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.20 **4.00**	V min
			0.10	0.25 **0.35**	V max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.00 **3.80**	V min
			0.30	0.63 **0.75**	V max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	13.50 **13.00**	V min
			0.26	0.45 **0.55**	V max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	12.50 **12.00**	V min
			0.79	1.45 **1.75**	V max
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V	22	13 **9**	mA min
		Sinking, V_O = 5V	21	13 **9**	mA min
		V^+ = 15V Sourcing, V_O = 0V	40	23 **15**	mA min
		Sinking, V_O = 13V (Note 10)	39	23 **15**	mA min
I_S	Supply Current	Both Amplifiers V_O = 1.5V	0.75	1.6 **1.9**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6032I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.1	0.8 **0.4**	V/μs min
GBW	Gain-Bandwidth Product		1.4		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		$pA/\sqrt{Hz}$
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold type face).

Note 7: V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 12: All numbers apply for packages soldered directly into a PC board.

National Semiconductor

LMC6034
CMOS Quad Operational Amplifier

General Description

The LMC6034 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 kΩ and 600Ω.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6032 datasheet for a CMOS dual operational amplifier with these same features. For higher performance characteristics refer to the LMC660.

Features

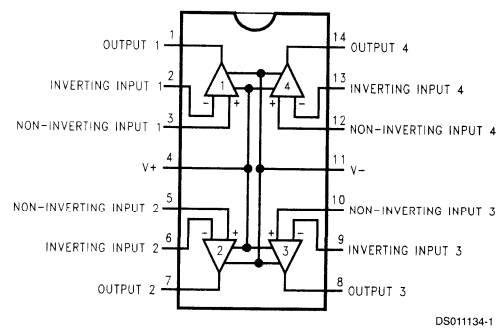
- Specified for 2 kΩ and 600Ω loads
- High voltage gain: 126 dB
- Low offset voltage drift: 2.3 μV/°C
- Ultra low input bias current: 40 fA
- Input common-mode range includes V^-
- Operating Range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V^+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/μs
- Improved performance over TLC274

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

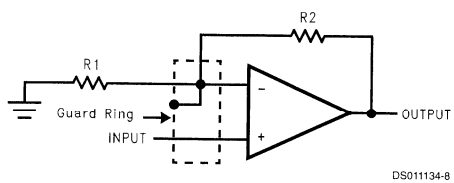
Connection Diagram

14-Pin DIP/SO



Top View

Guard Ring Connections
Non-Inverting Amplifier



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Power Dissipation	(Note 3)
Voltage at Output/Input Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Junction Temperature (Note 3)	150°C
ESD Tolerance (Note 4)	1000V

Operating Ratings (Note 1)

Temperature Range	$-40°C \le T_J \le +85°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 11)
Thermal Resistance (θ_{JA}), (Note 12)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = 1.5V$, $V_{OUT} = 2.5V$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	9 **11**	mV max
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Average Drift		2.3		µV/°C
I_B	Input Bias Current		0.04	 **200**	pA max
I_{OS}	Input Offset Current		0.01	 **100**	pA max
R_{IN}	Input Resistance		>1		TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12V$ $V^+ = 15V$	83	63 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	63 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	74 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	V max
			$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	V min
A_V	Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 7) Sourcing	2000	200 **100**	V/mV min
		Sinking	500	90 **40**	V/mV min
		$R_L = 600\Omega$ (Note 7) Sourcing	1000	100 **75**	V/mV min
		Sinking	250	50 **20**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V, and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
V_O	Output Voltage Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.20 **4.00**	V min
			0.10	0.25 **0.35**	V max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.00 **3.80**	V min
			0.30	0.63 **0.75**	V max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	13.50 **13.00**	V min
			0.26	0.45 **0.55**	V max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	12.50 **12.00**	V min
			0.79	1.45 **1.75**	V max
I_O	Output Current	V^+ = 5V Sourcing, V_O = 0V	22	13 **9**	mA min
		Sinking, V_O = 5V	21	13 **9**	mA min
		V^+ = 15V Sourcing, V_O = 0V	40	23 **15**	mA min
		Sinking, V_O = 13V (Note 10)	39	23 **15**	mA min
I_S	Supply Current	All Four Amplifiers V_O = 1.5V	1.5	2.7 **3.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = GND = 0V, V_{CM} = 1.5V, V_{OUT} = 2.5V, and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6034I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.1	0.8 **0.4**	V/μs min
GBW	Gain-Bandwidth Product		1.4		MHz
ϕ_M	Phase Margin		50		Deg
G_M	Gain Margin		17		dB
	Amp-to-Amp Isolation	(Note 9)	130		dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22		nV/$\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002		pA/$\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: V^+ = 15V, V_{CM} = 7.5V, and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 12: All numbers apply for packages soldered directly into a PC board.

National Semiconductor

LMC6035/LMC6036
Low Power 2.7V Single Supply CMOS Operational Amplifiers

General Description

The LMC6035/6 is an economical, low voltage op amp capable of rail-to-rail output swing into loads of 600Ω. LMC6035 is available in a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. Both allow for single supply operation and are guaranteed for 2.7V, 3V, 5V and 15V supply voltage. The 2.7 supply voltage corresponds to the End-of-Life voltage (0.9V/cell) for three NiCd or NiMH batteries in series, making the LMC6035/6 well suited for portable and rechargeable systems. It also features a well behaved decrease in its specifications at supply voltages below its guaranteed 2.7V operation. This provides a "comfort zone" for adequate operation at voltages significantly below 2.7V. Its ultra low input currents (I_{IN}) makes it well suited for low power active filter application, because it allows the use of higher resistor values and lower capacitor values. In addition, the drive capability of the LMC6035/6 gives these op amps a broad range of applications for low voltage systems.

Features

(Typical Unless Otherwise Noted)

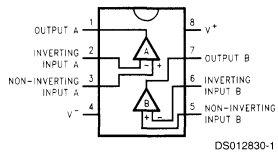
- LMC6035 in micro SMD Package
- Guaranteed 2.7V, 3V, 5V and 15V Performance
- Specified for 2 kΩ and 600Ω Loads
- Wide Operating Range: 2.0V to 15.5V
- Ultra Low Input Current: 20 fA
- Rail-to-Rail Output Swing
  @ 600Ω: 200 mV from either rail at 2.7V
  @ 100 kΩ: 5 mV from either rail at 2.7V
- High Voltage Gain: 126dB
- Wide Input Common-Mode Voltage Range
  -0.1V to 2.3V at Vs = 2.7V
- Low Distortion: 0.01% at 10 kHz
- LMC6035 Dual LMC6036 Quad

Applications

- Filters
- High Impedance Buffer or Preamplifier
- Battery Powered Electronics
- Medical Instrumentation

Connection Diagrams

8-Pin SO/MSOP



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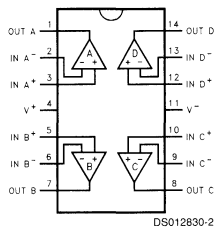
Top View

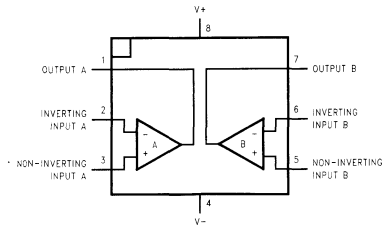
14-Pin SO/TSSOP



DS012830-2

Top View

8-Bump micro SMD



DS012830-65

Top View
(Bump Side Down)

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	3000V
Machine Model	300V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 8)
Output Short Circuit to V^-	(Note 3)
Lead Temperature (soldering, 10 sec.)	260°C
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	2.0V to 15.5V
Temperature Range	
LMC6035I and LMC6036I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
MSOP, 8-pin Mini Surface Mount	230°C/W
M Package, 8-pin Surface Mount	175°C/W
M Package, 14-pin Surface Mount	127°C/W
MTC Package, 14-pin TSSOP	137°C/W
BP, 8-Bump micro SMD Package	220°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.0V$, $V_O = 1.35V$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6035I LMC6036I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.5	5	mV
				6	max
TCV_{OS}	Input Offset Voltage Average Drift		2.3		µV/°C
I_{IN}	Input Current	(Note 11)	0.02		pA
				90	max
I_{OS}	Input Offset Current	(Note 11)	0.01		pA
				45	max
R_{IN}	Input Resistance		> 10		Tera Ω
CMRR	Common Mode Rejection Ratio	$0.7V \le V_{CM} \le 12.7V$, $V^+ = 15V$	96	63	dB
				60	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	93	63	dB
				60	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$, $V^+ = 5V$	97	74	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$, For CMRR ≥ 40 dB	−0.1	0.3	V
				0.5	max
			2.3	2.0	V
				1.7	min
		$V^+ = 3V$, For CMRR ≥ 40 dB	−0.3	0.1	V
				0.3	max
			2.6	2.3	V
				2.0	min
		$V^+ = 5V$, For CMRR ≥ 50 dB	−0.5	−0.2	V
				0.0	max
			4.5	4.2	V
				3.9	min
		$V^+ = 15V$, For CMRR ≥ 50 dB	−0.5	−0.2	V
				0.0	max
			14.4	14.0	V
				13.7	min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6035I LMC6036I Limit (Note 6)	Units
A_V	Large Signal Voltage Gain (Note 7)	R_L = 600Ω	Sourcing	1000	100	V/mV
					75	min
			Sinking	250	25	V/mV
					20	min
		R_L =2 kΩ	Sourcing	2000		V/mV
			Sinking	500		V/mV
V_O	Output Swing	V^+ = 2.7V R_L = 600Ω to 1.35V		2.5	2.0	V
					1.8	min
				0.2	0.5	V
					0.7	max
		V^+ = 2.7V R_L = 2 kΩ to 1.35V		2.62	2.4	V
					2.2	min
				0.07	0.2	V
					0.4	max
		V^+ = 15V R_L = 600Ω to 7.5V		14.5	13.5	V
					13.0	min
				0.36	1.25	V
					1.50	max
		V^+ = 15V R_L = 2 kΩ to 7.5V		14.8	14.2	V
					13.5	min
				0.12	0.4	V
					0.5	max
I_O	Output Current	V_O = 0V	Sourcing	8	4	mA
					3	min
		V_O = 2.7V	Sinking	5	3	mA
					2	min
I_S	Supply Current	LMC6035 for Both Amplifiers V_O = 1.35V		0.65	1.6	mA
					1.9	max
		LMC6036 for All Four Amplifiers V_O = 1.35V		1.3	2.7	mA
					3.0	max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 9)	1.5	V/μs
GBW	Gain Bandwidth Product	V^+ = 15V	1.4	MHz
θ_m	Phase Margin		48	°
G_m	Gain Margin		17	dB
	Amp-to-Amp Isolation	(Note 10)	130	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	27	nV/$\sqrt{\text{Hz}}$
i_n	Input Referred Current Noise	f = 1 kHz	0.2	fA/$\sqrt{\text{Hz}}$
THD	Total Harmonic Distortion	f = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 10V	0.01	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board with no air flow.

Note 5: Typical Values represent the most likely parametric norm or one sigma value.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+ when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: V^+ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Guaranteed by design.

National Semiconductor

LMC6041
CMOS Single Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

Features

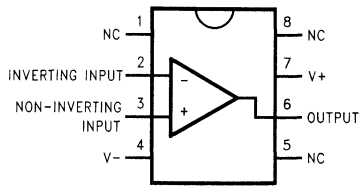
- Low supply current: 14 μA (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current: 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

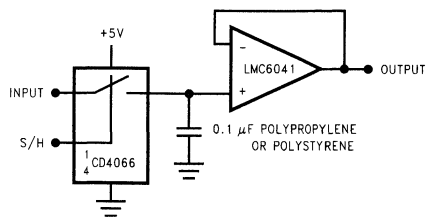
- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



Low-Leakage Sample and Hold



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^-	(Note 2)
Output Short Circuit to V^+	(Note 11)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	110°C
ESD Tolerance (Note 4)	500V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Power Dissipation	(Note 3)

Operating Ratings

Temperature Range	
LMC6041AI, LMC6041I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			µV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA max
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V max
				$V^+ - 1.9V$	$V^+ - 2.3V$ **$V^+ - 2.5V$**	$V^+ - 2.3V$ **$V^+ - 2.4V$**	V min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV min
			Sinking	500	180 **120**	90 **70**	V/mV min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV min
			Sinking	250	100 **60**	50 **40**	V/mV min

Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to $V^+/2$	4.980	4.920 **4.870**	4.870 **4.820**	V min
			0.010	0.080 **0.130**	0.130 **0.180**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V min
			0.022	0.100 **0.150**	0.150 **0.200**	V max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA min
		Sinking, $V_O = 13V$ (Note 11)	39	24 **8**	21 **8**	mA min
I_S	Supply Current	$V_O = 1.5V$	14	20 **24**	26 **30**	µA max
		$V^+ = 15V$	18	26 **31**	34 **39**	µA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/µs min
GBW	Gain-Bandwidth Product		75			kHz
ϕ_m	Phase Margin		60			Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{pp}$	0.01			%

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6041AI Limit (Note 6)	LMC6041I Limit (Note 6)	Units (Limit)
		±5V Supply				

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold face type).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC6042
CMOS Dual Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6042. Providing input currents of only 2 fA typical, the LMC6042 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6042 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6042 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6044 for a quad amplifier with these features.

Features

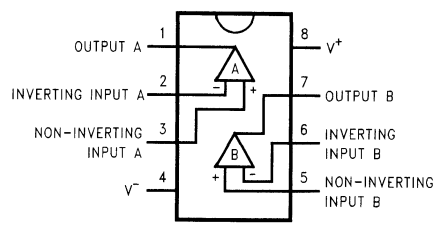
- Low supply current: 10 µA/Amp (typ)
- Operates from 4.5V to 15V single supply
- Ultra low input current: 2 fA (typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

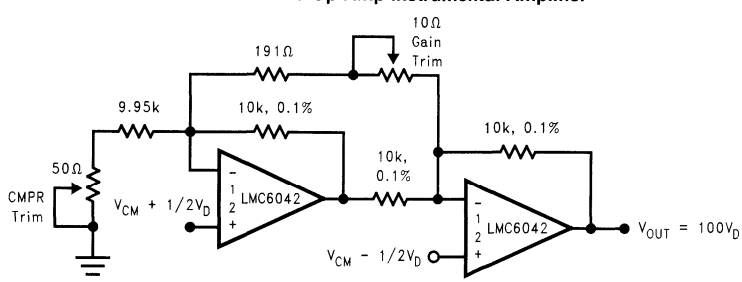
Connection Diagram

8-Pin DIP/SO



DS011137-1

Low-Power Two-Op-Amp Instrumental Amplifier



DS011137-13

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature	
(Soldering, 10 seconds)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$

Operating Ratings

Temperature Range	
LMC6042AI, LMC6042I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

Electrical Characteristics

Unless otherwise spec ified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			µV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA (Max)
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA (Max)
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB Min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9V$	$V^+ - 2.3V$ **$V^+ - 2.5V$**	$V^+ - 2.3V$ **$V^+ - 2.4V$**	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV Min
			Sinking	500	180 **120**	90 **70**	V/mV Min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV Min
			Sinking	250	100 **60**	50 **40**	V/mV Min

Electrical Characteristics (Continued)

Unless otherwise spec ified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to $V^+/2$	4.987	4.970 **4.950**	4.940 **4.910**	V Min
			0.004	0.030 **0.050**	0.060 **0.090**	V Max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to $V^+/2$	4.980	4.920 **4.870**	4.870 **4.820**	V Min
			0.010	0.080 **0.130**	0.130 **0.180**	V Max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V Min
			0.007	0.030 **0.050**	0.060 **0.090**	V Max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V Min
			0.022	0.100 **0.150**	0.150 **0.200**	V Max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA Min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA Min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA Min
		Sinking, $V_O = 13V$ (Note 12)	39	24 **8**	21 **8**	mA Min
I_S	Supply Current	Both Amplifiers $V_O = 1.5V$	20	34 **39**	45 **50**	μA Max
		Both Amplifiers $V^+ = 15V$	26	44 **51**	56 **65**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs Min
GBW	Gain-Bandwidth Product		100			kHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	83			$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.0002			$pA/\sqrt{Hz}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6042AI Limit (Note 6)	LMC6042I Limit (Note 6)	Units (Limit)
T.H.D.	Total Harmonic Distortion	f = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{PP}$ ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold face type).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to $V^+$when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC6044
CMOS Quad Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6044. Providing input currents of only 2 fA typical, the LMC6044 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6044 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6044 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6042 for a dual amplifier with these features.

Features

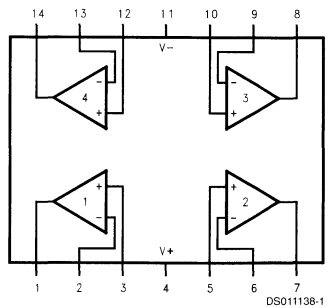
- Low supply current: 10 µA/Amp (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current: 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram

14-Pin DIP/SO



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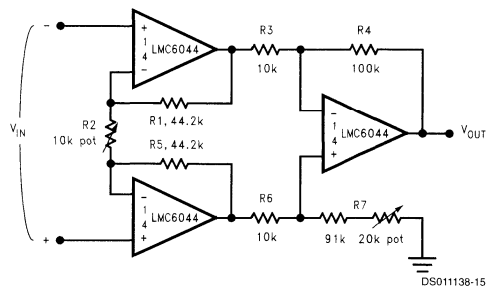
Instrumentation Amplifier



DS011138-15

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 2)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 3)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 3)	110°C
ESD Tolerance (Note 4)	500V
Voltage at I/O Pin (V^+)	+0.3V, (V^-) −0.3V

Operating Ratings

Temperature Range	
LMC6044AI, LMC6044I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V+ \le 15.5V$
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}), (Note 11)	
14-Pin DIP	85°C/W
14-Pin SO	115°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
V_{OS}	Input Offset Voltage			1	3 **3.3**	6 **6.3**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.3			µV/°C
I_B	Input Bias Current			0.002	**4**	**4**	pA max
I_{OS}	Input Offset Current			0.001	**2**	**2**	pA max
R_{IN}	Input Resistance			>10			TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		75	68 **66**	62 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		75	68 **66**	62 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$ $V_O = 2.5V$		94	84 **83**	74 **73**	dB min
CMR	Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB		−0.4	−0.1 **0**	−0.1 **0**	V max
				$V^+ - 1.9V$	$V^+ - 2.3V$ **$V^+ - 2.5V$**	$V^+ - 2.3V$ **$V^+ - 2.4V$**	V min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000	400 **300**	300 **200**	V/mV min
			Sinking	500	180 **120**	90 **70**	V/mV min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	1000	200 **160**	100 **80**	V/mV min
			Sinking	250	100 **60**	50 **40**	V/mV min

Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
V_O	Output Swing	$V^+ = 5V$ $R_L = 100\ k\Omega$ to 2.5V	4.987	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 5V$ $R_L = 25\ k\Omega$ to 2.5V	4.980	4.920 **4.870**	4.870 **4.820**	V min
			0.010	0.080 **0.130**	0.130 **0.180**	V max
		$V^+ = 15V$ $R_L = 100\ k\Omega$ to $V^+/2$	14.970	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.060 **0.090**	V max
		$V^+ = 15V$ $R_L = 25\ k\Omega$ to $V^+/2$	14.950	14.900 **14.850**	14.850 **14.800**	V min
			0.022	0.100 **0.150**	0.150 **0.200**	V max
I_{SC}	Output Current $V^+ = 5V$	Sourcing, $V_O = 0V$	22	16 **10**	13 **8**	mA min
		Sinking, $V_O = 5V$	21	16 **8**	13 **8**	mA min
I_{SC}	Output Current $V^+ = 15V$	Sourcing, $V_O = 0V$	40	15 **10**	15 **10**	mA min
		Sinking, $V_O = 13V$ (Note 12)	39	24 **8**	21 **8**	mA min
I_S	Supply Current	Four Amplifiers $V_O = 1.5V$	40	65 **72**	75 **82**	μA max
		Four Amplifiers $V^+ = 15V$	52	85 **94**	98 **107**	μA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
SR	Slew Rate	(Note 8)	0.02	0.015 **0.010**	0.010 **0.007**	V/μs min
GBW	Gain-Bandwidth Product		0.10			MHz
ϕ_m	Phase Margin		60			Deg
	Amp-to-Amp Isolation	(Note 9)	115			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83			nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002			pA/√Hz

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = V^+/2$, and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions	Typical (Note 5)	LMC6044AI Limit (Note 6)	LMC6044I Limit (Note 6)	Units (Limit)
T.H.D.	Total Harmonic Distortion	F = 1 kHz, $A_V = -5$ $R_L = 100\ k\Omega$, $V_O = 2\ V_{PP}$ ±5V Supply	0.01			%

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (bold face type).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\ V_{PP}$.

Note 10: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC poard.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC6061
Precision CMOS Single Micropower Operational Amplifier

General Description

The LMC6061 is a precision single low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6061 ideally suited for battery powered applications.

Other applications using the LMC6061 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6081 precision single operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6062 or LMC6064 respectively.

PATENT PENDING

Features

(Typical Unless Otherwise Noted)

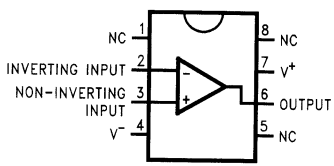
- Low offset voltage: 100 µV
- Ultra low supply current: 20 µA
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain: 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

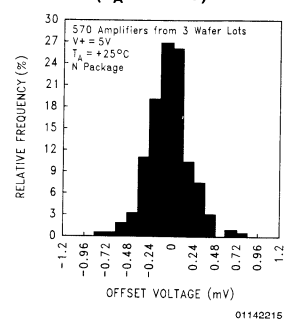
Connection Diagram

8-Pin DIP/SO



Top View

Distribution of LMC6061 Input Offset Voltage (T_A = +25°C)



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6061AM	$-55°C \le T_J \le +125°C$
LMC6061AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
Power Dissipation	(Note 9)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 9)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350	350	800	µV
					1200	**900**	**1300**	Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Bias Current			0.010				pA
					100	**4**	**4**	Max
I_{OS}	Input Offset Current			0.005				pA
					100	**2**	**2**	Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75	75	66	dB
					70	**72**	**63**	Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75	75	66	dB
					70	**72**	**63**	Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84	84	74	dB
					70	**81**	**71**	Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V for CMRR ≥ 60 dB		−0.4	−0.1	−0.1	−0.1	V
					0	**0**	**0**	Max
				$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
					$\mathbf{V^+ - 2.6}$	$\mathbf{V^+ - 2.5}$	$\mathbf{V^+ - 2.5}$	Min
A_V	Large Signal Voltage Gain	R_L = 100 kΩ (Note 7)	Sourcing	4000	400	400	300	V/mV
					200	**300**	**200**	Min
			Sinking	3000	180	180	90	V/mV
					70	**100**	**60**	Min
		R_L = 25 kΩ (Note 7)	Sourcing	3000	400	400	200	V/mV
					150	**150**	**80**	Min
			Sinking	2000	100	100	70	V/mV
					35	**50**	**35**	Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 9)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_l = 100 kΩ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		V^+ = 5V R_L = 25 kΩ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		V^+ = 15V R_L = 25 kΩ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, V_O = 13V (Note 10)	26	20 **7**	20 **8**	20 **8**	mA Min
I_S	Supply Current	V^+ = +5V, V_O = 1.5V	20	24 **35**	24 **32**	32 **40**	μA Max
		V^+ = +15V, V_O = 7.5V	24	30 **40**	30 **38**	40 **48**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6061AM Limit (Note 6)	LMC6061AI Limit (Note 6)	LMC6061I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5 R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: For guaranteed Military Temperature Range parameters see RETSMC6061X.

National Semiconductor

LMC6062
Precision CMOS Dual Micropower Operational Amplifier

General Description

The LMC6062 is a precision dual low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6062 ideally suited for battery powered applications.

Other applications using the LMC6062 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6082 precision dual operational amplifier.

PATENT PENDING

Features

(Typical Unless Otherwise Noted)

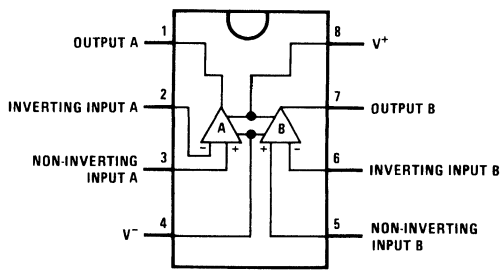
- Low offset voltage 100μV
- Ultra low supply current 16μA/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10fA
- Output swing within 10mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 140dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



Top View

Ordering Information

Package	Temperature Range		NSC Drawing	Transport Media
	Military −55°C to +125°C	Industrial −40°C to +85°C		
8-Pin Molded DIP	LMC6062AMN	LMC6062AIN LMC6062IN	N08E	Rail
8-Pin Small Outline		LMC6062AIM LMC6062IM	M08A	Rail
8-Pin Ceramic DIP	LMC6062AMJ/883		J08A	Rail

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6062AM	$-55°C \le T_J \le +125°C$
LMC6062AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
8-Pin Molded DIP	115°C/W
8-Pin SO	193°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350 **1200**	350 **900**	800 **1300**	µV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 25 k\Omega$ (Note 7)	Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V	4.995	4.990	4.990	4.950	V
		R_L = 100 kΩ to 2.5V		**4.970**	**4.980**	**4.925**	Min
			0.005	0.010	0.010	0.050	V
				0.030	**0.020**	**0.075**	Max
		V^+ = 5V	4.990	4.975	4.975	4.950	V
		R_L = 25 kΩ to 2.5V		**4.955**	**4.965**	**4.850**	Min
			0.010	0.020	0.020	0.050	V
				0.045	**0.035**	**0.150**	Max
		V^+ = 15V	14.990	14.975	14.975	14.950	V
		R_L = 100 kΩ to 7.5V		**14.955**	**14.965**	**14.925**	Min
			0.010	0.025	0.025	0.050	V
				0.050	**0.035**	**0.075**	Max
		V^+ = 15V	14.965	14.900	14.900	14.850	V
		R_L = 25 kΩ to 7.5V		**14.800**	**14.850**	**14.800**	Min
			0.025	0.050	0.050	0.100	V
				0.200	**0.150**	**0.200**	Max
I_O	Output Current	Sourcing, V_O = 0V	22	16	16	13	mA
	V^+ = 5V			**8**	**10**	**8**	Min
		Sinking, V_O = 5V	21	16	16	16	mA
				7	**8**	**8**	Min
I_O	Output Current	Sourcing, V_O = 0V	25	15	15	15	mA
	V^+ = 15V			**9**	**10**	**10**	Min
		Sinking, V_O = 13V	35	20	20	20	mA
		(Note 11)		**7**	**8**	**8**	Min
I_S	Supply Current	Both Amplifiers	32	38	38	46	µA
		V^+ = +5V, V_O = 1.5V		**60**	**46**	**56**	Max
		Both Amplifiers	40	47	47	57	µA
		V^+ = +15V, V_O = 7.5V		**70**	**55**	**66**	Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6062AM Limit (Note 6)	LMC6062AI Limit (Note 6)	LMC6062I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	155				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				nV/$\sqrt{\text{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{\text{Hz}}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5 R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 100 Hz to produce V_O = 12 V_{PP}.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

Note 13: For guaranteed Military Temperature Range parameters, see RETSMC6062X.

National Semiconductor

LMC6064
Precision CMOS Quad Micropower Operational Amplifier

General Description

The LMC6064 is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064 ideally suited for battery powered applications.

Other applications using the LMC6064 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

PATENT PENDING

Features

(Typical Unless Otherwise Noted)

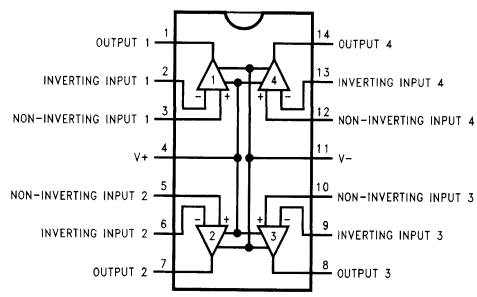
- Low offset voltage: 100 µV
- Ultra low supply current: 16 µA/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain: 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

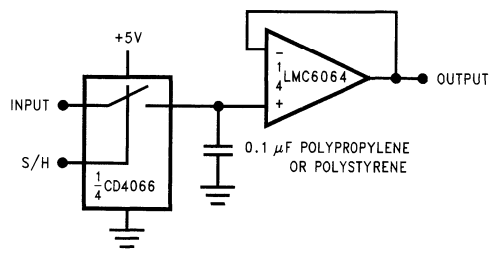
Connection Diagram

14-Pin DIP/SO



Top View

Low-Leakage Sample and Hold



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6064AM	$-55°C \le T_J \le +125°C$
LMC6064AI, LMC6064I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
14-Pin Molded DIP	81°C/W
14-Pin SO	126°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6064AM Limit (Note 6)	LMC6064AI Limit (Note 6)	LMC6064I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			100	350 **1200**	350 **900**	800 **1300**	µV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ V^+ = 15V		85	75 **70**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ V_O = 2.5V		85	75 **70**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		100	84 **70**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	R_L = 100 kΩ (Note 7)	Sourcing	4000	400 **200**	400 **300**	300 **200**	V/mV Min
			Sinking	3000	180 **70**	180 **100**	90 **60**	V/mV Min
		R_L = 25 kΩ (Note 7)	Sourcing	3000	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	2000	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6064AM Limit (Note 6)	LMC6064AI Limit (Note 6)	LMC6064I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.995	4.990 **4.970**	4.990 **4.980**	4.950 **4.925**	V Min
			0.005	0.010 **0.030**	0.010 **0.020**	0.050 **0.075**	V Max
		V^+ = 5V R_L = 25 kΩ to 2.5V	4.990	4.975 **4.955**	4.975 **4.965**	4.950 **4.850**	V Min
			0.010	0.020 **0.045**	0.020 **0.035**	0.050 **0.150**	V Max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.990	14.975 **14.955**	14.975 **14.965**	14.950 **14.925**	V Min
			0.010	0.025 **0.050**	0.025 **0.035**	0.050 **0.075**	V Max
		V^+ = 15V R_L = 25 kΩ to 7.5V	14.965	14.900 **14.800**	14.900 **14.850**	14.850 **14.800**	V Min
			0.025	0.050 **0.200**	0.050 **0.150**	0.100 **0.200**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **7**	16 **8**	16 **8**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	25	15 **9**	15 **10**	15 **10**	mA Min
		Sinking, V_O = 13V (Note 11)	26	20 **7**	20 **8**	20 **8**	mA Min
I_S	Supply Current	All Four Amplifiers V^+ = +5V, V_O = 1.5V	64	76 **120**	76 **92**	92 **112**	μA Max
		All Four Amplifiers V^+ = +15V, V_O = 7.5V	80	94 **140**	94 **110**	114 **132**	μA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6064AM Limit (Note 6)	LMC6064AI Limit (Note 6)	LMC6064I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	35	20 **8**	20 **10**	15 **7**	V/ms Min
GBW	Gain-Bandwidth Product		100				kHz
θ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	155				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	83				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −5 R_L = 100 kΩ, V_O = 2 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 100 Hz to produce V_O = 12 V_{PP}.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability witll be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

Note 13: For guaranteed Military Temperature Range parameters see RETSMC6064X.

National Semiconductor

LMC6081
Precision CMOS Single Operational Amplifier

General Description

The LMC6081 is a precision low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6081 ideally suited for precision circuit applications.

Other applications using the LMC6081 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6061 precision micropower operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6082 or LMC6084 respectively.

PATENT PENDING

Features

(Typical unless otherwise stated)

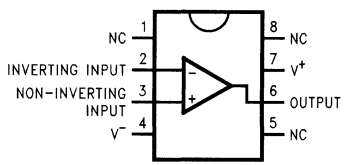
- Low offset voltage: 150 µV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain: 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Connection Diagram

8-Pin DIP/SO



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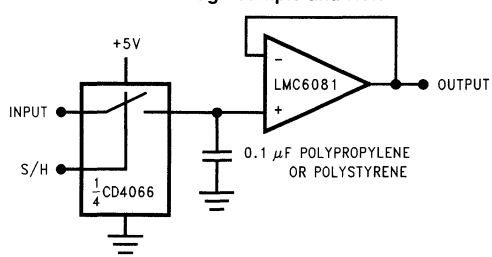
Top View

Low-Leakage Sample and Hold



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 10)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6081AM	$-55°C \le T_J \le +125°C$
LMC6081AI, LMC6081I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}), (Note 11)	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
Power Dissipation (Note 9)	

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.6}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	V Min
A_V	Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		$R_L = 600\Omega$ (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, V_O = 13V (Note 10)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	V^+ = +5V, V_O = 1.5V	450	750 **900**	750 **900**	750 **900**	µA Max
		V^+ = +15V, V_O = 7.5V	550	850 **950**	850 **950**	850 **950**	µA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6081AM Limit (Note 6)	LMC6081AI Limit (Note 6)	LMC6081 Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 11: All numbers apply for packages soldered directly into a PC board.

National Semiconductor

LMC6082
Precision CMOS Dual Operational Amplifier

General Description

The LMC6082 is a precision dual low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6082 ideally suited for precision circuit applications.

Other applications using the LMC6082 inciude precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6062 precision dual micropower operational amplifier.

PATENT PENDING

Features

(Typical unless otherwise stated)

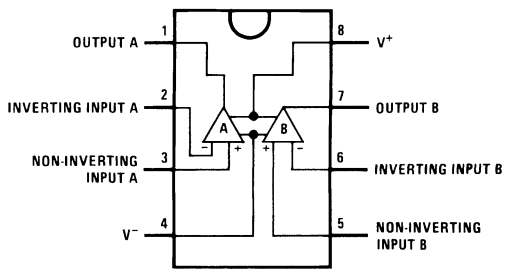
- Low offset voltage: 150 µV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain: 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

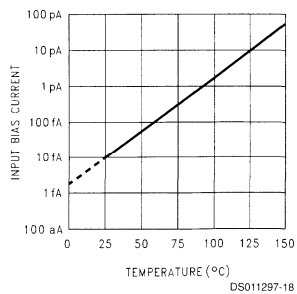
Connection Diagram

8-Pin DIP/SO



Top View

Input Bias Current vs Temperature



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6082AM	$-55°C \le T_J \le +125°C$
LMC6082AI, LMC6082I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
8-Pin Molded DIP	115°C/W
8-Pin SO	193°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	µV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V V_O = 2.5V		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		R_L = 600Ω (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, V_O = 13V (Note 11)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	Both Amplifiers V^+ = +5V, V_O = 1.5V	0.9	1.5 **1.8**	1.5 **1.8**	1.5 **1.8**	mA Max
		Both Amplifiers V^+ = +15V, V_O = 7.5V	1.1	1.7 **2**	1.7 **2**	1.7 **2**	mA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6082AM Limit (Note 6)	LMC6082AI Limit (Note 6)	LMC6082I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	140				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/√Hz
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

National Semiconductor

LMC6084
Precision CMOS Quad Operational Amplifier

General Description

The LMC6084 is a precision quad low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6084 ideally suited for precision circuit applications.

Other applications using the LMC6084 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6064 precision quad micropower operational amplifier.

For a single or dual operational amplifier with similar features, see the LMC6081 or LMC6082 respectively.

PATENT PENDING

Features

(Typical unless otherwise stated)

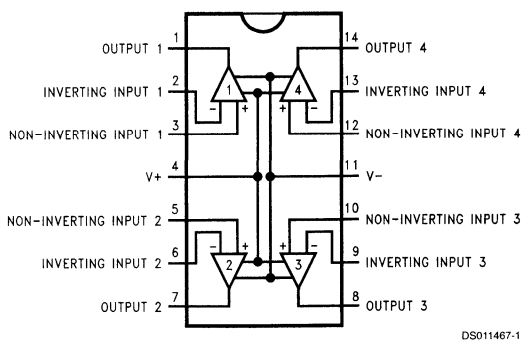
- Low offset voltage: 150 µV
- Operates from 4.5V to 15V single supply
- Ultra low input bias current: 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain: 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

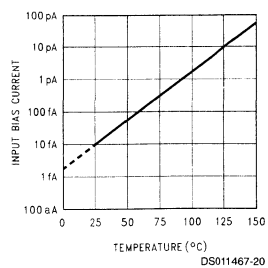
Connection Diagram

14-Pin DIP/SO



Top View

Input Bias Current vs Temperature



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 2)
Lead Temperature (Soldering, 10 Sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Tolerance (Note 4)	2 kV
Current at Input Pin	±10 mA
Current at Output Pin	±30 mA
Current at Power Supply Pin	40 mA
Power Dissipation	(Note 3)

Operating Ratings (Note 1)

Temperature Range	
LMC6084AM	$-55°C \le T_J \le +125°C$
LMC6084AI, LMC6084I	$-40°C \le T_J \le +85°C$
Supply Voltage	$4.5V \le V^+ \le 15.5V$
Thermal Resistance (θ_{JA}) (Note 12)	
14-Pin Molded DIP	81°C/W
14-Pin SO	126°C/W
Power Dissipation	(Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6084AM Limit (Note 6)	LMC6084AI Limit (Note 6)	LMC6084I Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			150	350 **1000**	350 **800**	800 **1300**	μV Max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				μV/°C
I_B	Input Bias Current			0.010	 **100**	 **4**	 **4**	pA Max
I_{OS}	Input Offset Current			0.005	 **100**	 **2**	 **2**	pA Max
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V		85	75 **72**	75 **72**	66 **63**	dB Min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V V_O = 2.5V		85	75 **72**	75 **72**	66 **63**	dB Min
−PSRR	Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V		94	84 **81**	84 **81**	74 **71**	dB Min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V and 15V for CMRR ≥ 60 dB		−0.4	−0.1 **0**	−0.1 **0**	−0.1 **0**	V Max
				$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.6$**	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.5$**	V Min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Note 7)	Sourcing	1400	400 **300**	400 **300**	300 **200**	V/mV Min
			Sinking	350	180 **70**	180 **100**	90 **60**	V/mV Min
		R_L = 600Ω (Note 7)	Sourcing	1200	400 **150**	400 **150**	200 **80**	V/mV Min
			Sinking	150	100 **35**	100 **50**	70 **35**	V/mV Min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6084AM Limit (Note 6)	LMC6084AI Limit (Note 6)	LMC6084I Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to 2.5V	4.87	4.80 **4.70**	4.80 **4.73**	4.75 **4.67**	V Min
			0.10	0.13 **0.19**	0.13 **0.17**	0.20 **0.24**	V Max
		V^+ = 5V R_L = 600Ω to 2.5V	4.61	4.50 **4.24**	4.50 **4.31**	4.40 **4.21**	V Min
			0.30	0.40 **0.63**	0.40 **0.50**	0.50 **0.63**	V Max
		V^+ = 15V R_L = 2 kΩ to 7.5V	14.63	14.50 **14.30**	14.50 **14.34**	14.37 **14.25**	V Min
			0.26	0.35 **0.48**	0.35 **0.45**	0.44 **0.56**	V Max
		V^+ = 15V R_L = 600Ω to 7.5V	13.90	13.35 **12.80**	13.35 **12.86**	12.92 **12.44**	V Min
			0.79	1.16 **1.42**	1.16 **1.32**	1.33 **1.58**	V Max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **8**	16 **10**	13 **8**	mA Min
		Sinking, V_O = 5V	21	16 **11**	16 **13**	13 **10**	mA Min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **18**	28 **22**	23 **18**	mA Min
		Sinking, V_O = 13V (Note 11)	34	28 **19**	28 **22**	23 **18**	mA Min
I_S	Supply Current	All Four Amplifiers V^+ = +5V, V_O = 1.5V	1.8	3.0 **3.6**	3.0 **3.6**	3.0 **3.6**	mA Max
		All Four Amplifiers V^+ = +15V, V_O = 7.5V	2.2	3.4 **4.0**	3.4 **4.0**	3.4 **4.0**	mA Max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6084AM Limit (Note 6)	LMC6084AI Limit (Note 6)	LMC6084I Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	1.5	0.8 **0.5**	0.8 **0.6**	0.8 **0.6**	V/μs Min
GBW	Gain-Bandwidth Product		1.3				MHz
ϕ_m	Phase Margin		50				Deg
	Amp-to-Amp Isolation	(Note 9)	140				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz	22				nV/$\sqrt{Hz}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} ±5V Supply	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

Note 4: Human body model, 1.5 kΩ in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

National Semiconductor

LMC6442
Dual Micropower Rail-to-Rail Output Single Supply Operational Amplifier

General Description

The LMC6442 is ideal for battery powered systems, where very low supply current (less than one microamp per amplifier) and Rail-to-Rail output swing is required. It is characterized for 2.2V to 10V operation, and at 2.2V supply, the LMC6442 is ideal for single (Li-Ion) or two cell (NiCad or alkaline) battery systems.

The LMC6442 is designed for battery powered systems that require long service life through low supply current, such as smoke and gas detectors, and pager or personal communications systems.

Operation from single supply is enhanced by the wide common mode input voltage range which includes the ground (or negative supply) for ground sensing applications. Very low (5fA, typical) input bias current and near constant supply current over supply voltage enhance the LMC6442's performance near the end-of-life battery voltage.

Designed for closed loop gains of greater than plus two (or minus one), the amplifier has typically 9.5 KHz GBWP (Gain Bandwidth Product). Unity gain can be used with a simple compensation circuit, which also allows capacitive loads of up to 300 pF to be driven, as described in the Application Notes section.

For compact assembly the LMC6442 is available in the MSOP 8 pin package, about one half the size required by the SOIC 8 pin package. 8 pin DIP and 8 pin SOIC are also available.

Features

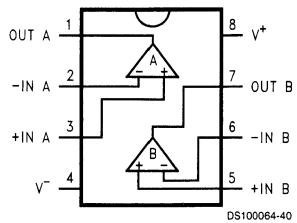
(Typical, V_S = 2.2V)

- Output Swing to within 30 mV of supply rail
- High voltage gain 103 dB
- Gain Bandwidth Product 9.5 KHz
- Guaranteed for: 2.2V, 5V, 10V
- Low Supply Current 0.95 µA/Amplifier
- Input Voltage Range −0.3V to V^+ -0.9V
- 2.1 µW/Amplifier Power consumption
- Stable for $A_V \geq +2$ or $A_V \leq -1$

Applications

- Portable instruments
- Smoke/gas/CO/fire detectors
- Pagers/cell phones
- Instrumentation
- Thermostats
- Occupancy sensors
- Cameras
- Active badges

Connection Diagram



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	±Supply Voltages
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Supply Voltage $(V^+ - V^-)$:	16V
Current at Input Pin (Note 10)	±5 mA
Current at Output Pin(Notes 3, 7)	±30 mA
Lead Temp. (soldering 10 sec)	260°C
Storage Temp. Range:	−65°C to +150°C
Junction Temp. (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$1.8V \le V_S \le 11V$
Junction Temperature	$-40°C < T_J < +85°C$
Range: LMC6442AI, LMC6442I	
Thermal Resistance (θ_{JA})	
M Package, 8-pin Surface Mount	193°C/W
MSOP Package	235°C/W
N Package, 8-pin Molded DIP	115°C/W

2.2V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.2V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6442AI Limit (Note 6)	LMC6442I Limit (Note 6)	Units
DC Electrical Characteristics						
V_{OS}	Input Offset Voltage		−0.75	±3 **±4**	±7 **±8**	mV max
TCV_{OS}	Temp. coefficient of input offset voltage		0.4			µV/°C
I_B	Input Bias Current	(Note 14)	0.005	**4**	**4**	pA max
I_{OS}	Input Offset Current	(Note 14)	0.0025	**2**	**2**	pA max
CMRR	Common Mode Rejection Ratio	$-0.1V \le V_{CM} \le 0.5V$	92	67 **67**	67 **67**	dB min
C_{IN}	Common Mode Input Capacitance		4.7			pF
PSRR	Power Supply Rejection Ratio	V_S = 2.5 V to 10V	95	75 **75**	75 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	1.3	1.05 **0.95**	1.05 **0.95**	V min
			−0.3	−0.2 **0**	−0.2 **0**	V max
A_V	Large Signal Voltage Gain	Sourcing (Note 11)	100			dB min
		Sinking(Note 11)	94			
		V_O = 0.22V to 2V	103	80	80	
V_O	Output Swing	V_{ID} = 100 mV (Note 13)	2.18	2.15 **2.15**	2.15 **2.15**	V min
		V_{ID} = −100 mV (Note 13)	22	60 **60**	60 **60**	mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100 mV (Notes 12, 13)	50	18 **17**	18 **17**	µA min
		Sinking, V_{ID} = −100 mV (Notes 12, 13)	50	20 **19**	20 **19**	
I_S	Supply Current (2 amplifiers)	R_L = open	1.90	2.4 **3.0**	2.6 **3.2**	µA max
		V^+ = 1.8V, R_L = open	2.10			
AC Electrical Characteristics						
SR	Slew Rate (Note 8)		2.2			V/ms

2.2V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.2V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6442AI Limit (Note 6)	LMC6442I Limit (Note 6)	Units
AC Electrical Characteristics						
GBWP	Gain-Bandwidth Product		9.5			KHz
ϕ_m	Phase Margin	(Note 15)	63			Degree

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$, and R_L = 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6442AI Limit (Note 6)	LMC6442I Limit (Note 6)	Units
DC Electrical Characteristics						
V_{OS}	Input Offset Voltage		−0.75	±3 **±4**	±7 **±8**	mV max
TCV_{OS}	Temp. coefficient of input offset voltage		0.4			µV/°C
I_B	Input Bias Current	(Note 14)	0.005	**4**	**4**	pA max
I_{OS}	Input Offset Current	(Note 14)	0.0025	**2**	**2**	pA max
CMRR	Common Mode Rejection Ratio	$-0.1V \le V_{CM} \le 3.5V$	102	70 **70**	70 **70**	dB min
C_{IN}	Common Mode Input Capacitance		4.1			pF
PSRR	Power Supply Rejection Ratio	V_S = 2.5 V to 10V	95	75 **75**	75 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	4.1	3.85 **3.75**	3.85 **3.75**	V min
			−0.4	−0.2 **0**	−0.2 **0**	V max
A_V	Large Signal Voltage Gain	Sourcing (Note 11)	100			dB min
		Sinking (Note 11)	94			
		V_O = 0.5V to 4.5V	103	80	80	
V_O	Output Swing	V_{ID} = 100 mV (Note 13)	4.99	4.95 **4.95**	4.95 **4.95**	V min
		V_{ID} = −100 mV (Note 13)	20	50 **50**	50 **50**	mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100 mV (Notes 12, 13)	500	300 **200**	300 **200**	µA min
		Sinking, V_{ID} = −100 mV (Notes 12, 13)	350	200 **150**	200 **150**	
I_S	Supply Current (2 amplifiers)	R_L = open	1.90	2.4 **3.0**	2.6 **3.2**	µA max
AC Electrical Characteristics						
SR	Slew Rate (Note 8)		4.1	2.5	2.5	V/ms
GBWP	Gain-Bandwidth Product		10			KHz
ϕ_m	Phase Margin	(Note 15)	64			Degree
THD	Total Harmonic Distortion	A_V = +2, f = 100 Hz, R_L = 10MΩ, V_{OUT} = 1 Vpp	0.08			%

10V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_O = V^+/2, and R_L = 1 MΩ to V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6442AI Limit (Note 6)	LMC6442I Limit (Note 6)	Units
DC Electrical Characteristics						
V_{OS}	Input Offset Voltage		−1.5	±3 **±4**	±7 **±8**	mV max
TCV_{OS}	Temp. coefficient of input offset voltage		0.4			µV/°C
I_B	Input Bias Current	(Note 14)	0.005	**4**	**4**	pA max
I_{OS}	Input Offset Current	(Note 14)	0.0025	**2**	**2**	pA max
CMRR	Common Mode Rejection Ratio	−0.1V ≤ V_{CM} ≤8.5V	105	70 **70**	70 **70**	dB min
C_{IN}	Common Mode Input Capacitance		3.5			pF
PSRR	Power Supply Rejection Ratio	V_S = 2.5 V to 10V	95	75 **75**	75 **75**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	9.1	8.85 **8.75**	8.85 **8.75**	V min
			−0.4	−0.2 **0**	−0.2 **0**	V max
A_V	Large Signal Voltage Gain	Sourcing (Note 11)	120			dB min
		Sinking (Note 11)	100			
		V_O = 0.5V to 9.5V	104	80	80	
V_O	Output Swing	V_{ID} = 100 mV (Note 13)	9.99	9.97 **9.97**	9.97 **9.97**	V min
		V_{ID} = −100 mV(Note 13)	22	50 **50**	50 **50**	mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100 mV (Notes 12, 13)	2100	1200 **1000**	1200 **1000**	µA min
		Sinking, V_{ID} = −100 mV (Notes 12, 13)	900	600 **500**	600 **500**	
I_S	Supply Current (2 amplifiers)	R_L = open	1.90	2.4 **3.0**	2.6 **3.2**	µA max
AC Electrical Characteristics						
SR	Slew Rate(Note 8)		4.1	2.5	2.5	V/ms
GBWP	Gain-Bandwidth Product		10.5			KHz
ϕ_m	Phase Margin	(Note 15)	68			Degree
e_n	Input-Referred Voltage Noise	R_L = open f = 10 Hz	170			nV/√Hz
i_n	Input-Referred Current Noise	R_L = open f = 10 Hz	0.0002			pA/√Hz
	Crosstalk Rejection	(Note 9)	85			dB

Electrical Characteristics (continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis unless otherwise specified.

Note 7: Do not short circuit output to V^+,when V^+ is greater than 13V or reliability will be adversely affected.

Note 8: Slew rate is the slower of the rising and falling slew rates.

Note 9: Input referred, V^+ = 10V and R_L = 10 MΩ connected to 5V. Each amp excited in turn with 1 KHz to produce about 10 Vpp output.

Note 10: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 11: R_L connected to $V^+/2$. For Sourcing Test, $V_O > V^+/2$. For Sinking tests, $V_O < V^+/2$.

Note 12: Output shorted to ground for sourcing, and shorted to V+ for sinking short circuit current test.

Note 13: V_{ID} is differential input voltage referenced to inverting input.

Note 14: Limits guaranteed by design.

Note 15: See the Typical Performance Characteristics and Application Notes sections for more details.

National Semiconductor

LMC6462 Dual/LMC6464 Quad Micropower, Rail-to-Rail Input and Output CMOS Operational Amplifier

General Description

The LMC6462/4 is a micropower version of the popular LMC6482/4, combining Rail-to-Rail Input and Output Range with very low power consumption.

The LMC6462/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier, guaranteed for loads down to 25 kΩ, assures maximum dynamic sigal range. This rail-to-rail performance of the amplifier, combined with its high voltage gain makes it unique among rail-to-rail amplifiers. The LMC6462/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6462/4, with guaranteed specifications at 3V and 5V, is especially well-suited for low voltage applications. A quiescent power consumption of 60 µW per amplifier (at V_S = 3V) can extend the useful life of battery operated systems. The amplifier's 150 fA input current, low offset voltage of 0.25 mV, and 85 dB CMRR maintain accuracy in battery-powered systems.

Features

(Typical unless otherwise noted)

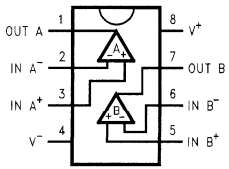
- Ultra Low Supply Current 20 µA/Amplifier
- Guaranteed Characteristics at 3V and 5V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing (within 10 mV of rail, V_S = 5V and R_L = 25 kΩ)
- Low Input Current 150 fA
- Low Input Offset Voltage 0.25 mV

Applications

- Battery Operated Circuits
- Transducer Interface Circuits
- Portable Communication Devices
- Medical Applications
- Battery Monitoring

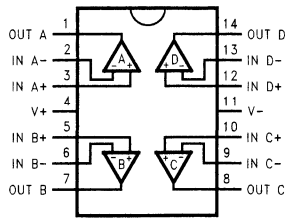
Connection Diagrams

8-Pin DIP/SO



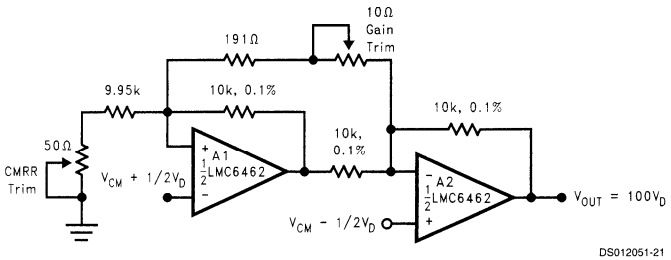
Top View

14-Pin DIP/SO



Top View

Low-Power Two-Op-Amp Instrumentation Amplifier



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.0 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6462AM, LMC6464AM	$-55°C \le T_J \le +125°C$
LMC6462AI, LMC6464AI	$-40°C \le T_J \le +85°C$
LMC6462BI, LMC6464BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.25	0.5 **1.2**	3.0 **3.7**	0.5 **1.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.5				µV/°C
I_B	Input Current	(Note 13)	0.15	**10**	**10**	**200**	pA max
I_{OS}	Input Offset Current	(Note 13)	0.075	**5**	**5**	**100**	pA max
C_{IN}	Common-Mode Input Capacitance		3				pF
R_{IN}	Input Resistance		>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$, $V^+ = 15V$	85	70 **67**	65 **62**	70 **65**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$	85	70 **67**	65 **62**	70 **65**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V^- = 0V$, $V_O = 2.5V$	85	70 **67**	65 **62**	70 **65**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V$, $V^+ = 0V$, $V_O = -2.5V$	85	70 **67**	65 **62**	70 **65**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ For CMRR ≥ 50 dB	−0.2	−0.10 **0.00**	−0.10 **0.00**	−0.10 **0.00**	V max
			5.30	5.25 **5.00**	5.25 **5.00**	5.25 **5.00**	V min
		$V^+ = 15V$ For CMRR ≥ 50 dB	−0.2	−0.15 **0.00**	−0.15 **0.00**	−0.15 **0.00**	V max
			15.30	15.25 **15.00**	15.25 **15.00**	15.25 **15.00**	V min

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
A_V	Large Signal Voltage Gain	R_L = 100 kΩ (Note 7)	Sourcing	3000				V/mV min
			Sinking	400				V/mV min
		R_L = 25 kΩ (Note 7)	Sourcing	2500				V/mV min
			Sinking	200				V/mV min
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to $V^+/2$		4.995	4.990 **4.980**	4.950 **4.925**	4.990 **4.970**	V min
				0.005	0.010 **0.020**	0.050 **0.075**	0.010 **0.030**	V max
		V^+ = 5V R_L = 25 kΩ to $V^+/2$		4.990	4.975 **4.965**	4.950 **4.850**	4.975 **4.955**	V min
				0.010	0.020 **0.035**	0.050 **0.150**	0.020 **0.045**	V max
		V^+ = 15V R_L = 100 kΩ to $V^+/2$		14.990	14.975 **14.965**	14.950 **14.925**	14.975 **14.955**	V min
				0.010	0.025 **0.035**	0.050 **0.075**	0.025 **0.050**	V max
		V^+ = 15V R_L = 25 kΩ to $V^+/2$		14.965	14.900 **14.850**	14.850 **14.800**	14.900 **14.800**	V min
				0.025	0.050 **0.150**	0.100 **0.200**	0.050 **0.200**	V max
I_{SC}	Output Short Circuit Current V+ = 5V	Sourcing, V_O = 0V		27	19 **15**	19 **15**	19 **15**	mA min
		Sinking, V_O = 5V		27	22 **17**	22 **17**	22 **17**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V		38	24 **17**	24 **17**	24 **17**	mA min
		Sinking, V_O = 12V (Note 8)		75	55 **45**	55 **45**	55 **45**	mA min
I_S	Supply Current	Dual, LMC6462 V^+ = +5V, $V_O = V^+/2$		40	55 **70**	55 **70**	55 **75**	µA max
		Quad, LMC6464 V^+ = +5V, $V_O = V^+/2$		80	110 **140**	110 **140**	110 **150**	µA max
		Dual, LMC6462 V^+ = +15V, $V_O = V^+/2$		50	60 **70**	60 **70**	60 **75**	µA max
		Quad, LMC6464 V^+ = +15V, $V_O = V^+/2$		90	120 **140**	120 **140**	120 **150**	µA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	28	15 **8**	15 **8**	15 **8**	V/ms min
GBW	Gain-Bandwidth Product	V^+ = 15V	50				kHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	130				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	80				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.03				$pA/\sqrt{Hz}$

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	2.0 **3.0**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/°C
I_B	Input Current	(Note 13)	0.15	**10**	**10**	**200**	pA
I_{OS}	Input Offset Current	(Note 13)	0.075	**5**	**5**	**100**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	60	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	60	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	−0.10	0.0	0.0	0.0	V max
			3.0	3.0	3.0	3.0	V min
V_O	Output Swing	R_L = 25 kΩ to $V^+/2$	2.95	2.9	2.9	2.9	V min
			0.15	0.1	0.1	0.1	V max
I_S	Supply Current	Dual, LMC6462 V_O = $V^+/2$	40	55 **70**	55 **70**	55 **70**	µA
		Quad, LMC6464 V_O = $V^+/2$	80	110 **140**	110 **140**	110 **140**	µA max

3V AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface limits** apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6462AI LMC6464AI Limit (Note 6)	LMC6462BI LMC6464BI Limit (Note 6)	LMC6462AM LMC6464AM Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	23				V/ms
GBW	Gain-Bandwidth Product		50				kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6462/4X.

National Semiconductor

LMC6482
CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

General Description

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

LMC6482 is also available in MSOP package which is almost half the size of a SO-8 device.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

Features

(Typical unless otherwise noted)

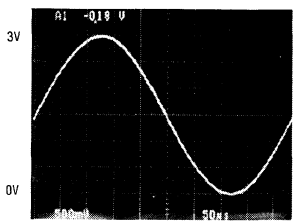
- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR: 82 dB
- Ultra Low Input Current: 20 fA
- High Voltage Gain (R_L = 500 kΩ): 130 dB
- Specified for 2 kΩ and 600Ω loads
- Available in MSOP Package

Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

3V Single Supply Buffer Circuit

Rail-To-Rail Input



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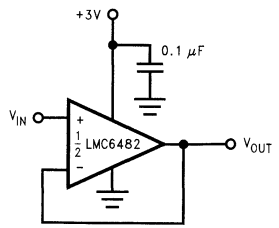
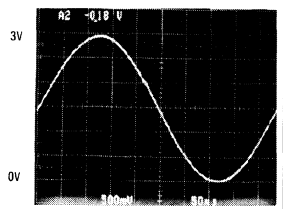


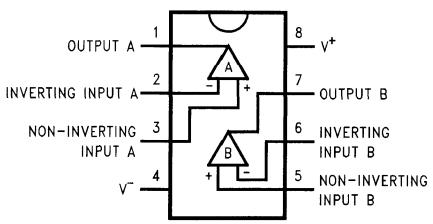
DS011713-2

Rail-To-Rail Output



DS011713-3

Connection Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	1.5 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V+ \le 15.5V$
Junction Temperature Range	
LMC6482AM	$-55°C \le T_J \le +125°C$
LMC6482AI, LMC6482I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	90°C/W
M Package, 8-Pin Surface Mount	155°C/W
MSOP package, 8-Pin Mini SO	194°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.11	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**10.0**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**5.0**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				TeraΩ
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$ $V^+ = 15V$		82	70 **67**	65 **62**	65 **60**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V^- = 0V$ $V_O = 2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V$, $V^+ = 0V$ $V_O = -2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		V^- − 0.3	− 0.25 **0**	− 0.25 **0**	− 0.25 **0**	V max
				V^+ + 0.3V	V^+ + 0.25 **V^+**	V^+ + 0.25 **V^+**	V^+ + 0.25 **V^+**	V min
A_V	Large Signal Voltage Gain	R_L = 2 kΩ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		R_L = 600Ω (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	20	16 **12**	16 **12**	16 **10**	mA min
		Sinking, V_O = 5V	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **22**	28 **22**	28 **20**	mA min
		Sinking, V_O = 12V (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	Both Amplifiers V^+ = +5V, $V_O = V^+/2$	1.0	1.4 **1.8**	1.4 **1.8**	1.4 **1.9**	mA max
		Both Amplifiers V^+ = 15V, $V_O = V^+/2$	1.3	1.6 **1.9**	1.6 **1.9**	1.6 **2.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/μs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{cm} = 1V	37				nV/√Hz

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
i_n	Input-Referred Current Noise	F = 1 kHz	0.03				pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01				%
		F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/°C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	V^- −0.25	0	0	0	V max
			V^+ + 0.25	V^+	V^+	V^+	V min
V_O	Output Swing	R_L = 2 kΩ to $V^+/2$	2.8				V
			0.2				V
		R_L = 600Ω to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	Both Amplifiers	0.825	1.2 **1.5**	1.2 **1.5**	1.2 **1.6**	mA max

AC Electrical Characteristics

Unless otherwise specified, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$, and R_L > 1M.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6482AI Limit (Note 6)	LMC6482I Limit (Note 6)	LMC6482M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/µs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 2 V_{PP}	0.01				%

AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limts beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature parameters see RETS6482X.

National Semiconductor

LMC6484
CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

Features

(Typical unless otherwise noted)

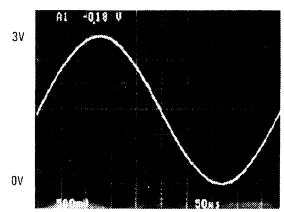
- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR: 82 dB
- Ultra Low Input Current: 20 fA
- High Voltage Gain (R_L = 500 kΩ): 130 dB
- Specified for 2 kΩ and 600Ω loads

Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

3V Single Supply Buffer Circuit

Rail-to-Rail Input



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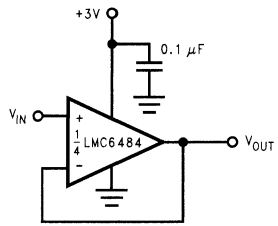

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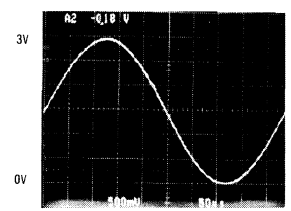
Rail-to-Rail Output



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2.0 kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin (Note 12)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$3.0V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6484AM	$-55°C \le T_J \le +125°C$
LMC6484AI, LMC6484I	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 14-Pin Molded DIP	70°C/W
M Package, 14-Pin Surface Mount	110°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage			0.110	0.750 **1.35**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift			1.0				µV/°C
I_B	Input Current	(Note 13)		0.02	**4.0**	**4.0**	**100**	pA max
I_{OS}	Input Offset Current	(Note 13)		0.01	**2.0**	**2.0**	**50**	pA max
C_{IN}	Common-Mode Input Capacitance			3				pF
R_{IN}	Input Resistance			>10				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 15.0V$, $V^+ = 15V$		82	70 **67**	65 **62**	65 **60**	dB min
		$0V \le V_{CM} \le 5.0V$ $V^+ = 5V$		82	70 **67**	65 **62**	65 **60**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V^- = 0V$, $V_O = 2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$-5V \le V^- \le -15V$, $V^+ = 0V$, $V_O = -2.5V$		82	70 **67**	65 **62**	65 **60**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB		$V^- - 0.3$	−0.25 **0**	−0.25 **0**	−0.25 **0**	V max
				$V^+ + 0.3$	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	V min
A_V	Large Signal Voltage Gain	$R_L = 2k\Omega$ (Notes 7, 13)	Sourcing	666	140 **84**	120 **72**	120 **60**	V/mV min
			Sinking	75	35 **20**	35 **20**	35 **18**	V/mV min
		$R_L = 600\Omega$ (Notes 7, 13)	Sourcing	300	80 **48**	50 **30**	50 **25**	V/mV min
			Sinking	35	20 **13**	15 **10**	15 **8**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.2**	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current V+ = 5V	Sourcing, V_O = 0V	20	16 **12**	16 **12**	16 **10**	mA min
		Sinking, V_O = 5V	15	11 **9.5**	11 **9.5**	11 **8.0**	mA min
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **22**	28 **22**	28 **20**	mA min
		Sinking, V_O = 12V (Note 8)	30	30 **24**	30 **24**	30 **22**	mA min
I_S	Supply Current	All Four Amplifiers V^+ = +5V, $V_O = V^+/2$	2.0	2.8 **3.6**	2.8 **3.6**	2.8 **3.8**	mA max
		All Four Amplifiers V^+ = +15V, $V_O = V^+/2$	2.6	3.0 **3.8**	3.0 **3.8**	3.0 **4.0**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484A Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	1.0 **0.7**	0.9 **0.63**	0.9 **0.54**	V/μs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5				MHz
ϕ_m	Phase Margin		50				Deg
G_m	Gain Margin		15				dB
	Amp-to-Amp Isolation	(Note 10)	150				dB
e_n	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	37				$nV/\sqrt{Hz}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.03				$pA/\sqrt{Hz}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484A Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	f = 1 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01				%
		f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01				%

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.9	2.0 **2.7**	3.0 **3.7**	3.0 **3.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0				µV/°C
I_B	Input Bias Current		0.02				pA
I_{OS}	Input Offset Current		0.01				pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V	74	64	60	60	dB min
PSRR	Power Supply Rejection Ratio	3V ≤ V^+ ≤ 15V, V^- = 0V	80	68	60	60	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	V^- − 0.25	0	0	0	V max
			V^+ + 0.25	V^+	V^+	V^+	V min
V_O	Output Swing	R_L = 2 kΩ to $V^+/2$	2.8				V
			0.2				V
		R_L = 600Ω to $V^+/2$	2.7	2.5	2.5	2.5	V min
			0.37	0.6	0.6	0.6	V max
I_S	Supply Current	All Four Amplifiers	1.65	2.5 **3.0**	2.5 **3.0**	2.5 **3.2**	mA max

AC Electrical Characteristics

Unless otherwise specified, V^+ = 3V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1M

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6484AI Limit (Note 6)	LMC6484I Limit (Note 6)	LMC6484M Limit (Note 6)	Units
SR	Slew Rate	(Note 11)	0.9				V/µs
GBW	Gain-Bandwidth Product		1.0				MHz
T.H.D.	Total Harmonic Distortion	f = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 2 V_{PP}	0.01				%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

AC Electrical Characteristics (Continued)

Note 2: Human body model, 1.5 kΩ in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $3.5V \le V_O \le 7.5V$.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15V$ and $R_L = 100\ k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12\ V_{PP}$.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6484X.

National Semiconductor

LMC6492 Dual/LMC6494 Quad CMOS Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6492/LMC6494 amplifiers were specifically developed for single supply applications that operate from −40°C to +125°C. This feature is well-suited for automotive systems because of the wide temperature range. A unique design topology enables the LMC6492/LMC6494 common-mode voltage range to accommodate input signals beyond the rails. This eliminates non-linear output errors due to input signals exceeding a traditionally limited common-mode voltage range. The LMC6492/LMC6494 signal range has a high CMRR of 82 dB for excellent accuracy in non-inverting circuit configurations.

The LMC6492/LMC6494 rail-to-rail input is complemented by rail-to-rail output swing. This assures maximum dynamic signal range which is particularly important in 5V systems.

Ultra-low input current of 150 fA and 120 dB open loop gain provide high accuracy and direct interfacing with high impedance sources.

Features

(Typical unless otherwise noted)

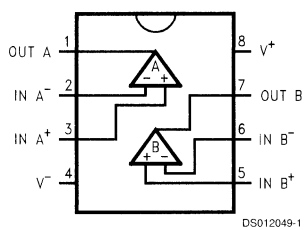
- Rail-to-Rail input common-mode voltage range, guaranteed over temperature
- Rail-to-Rail output swing within 20 mV of supply rail, 100 kΩ load
- Operates from 5V to 15V supply
- Excellent CMRR and PSRR 82 dB
- Ultra low input current 150 fA
- High voltage gain (R_L = 100 kΩ) 120 dB
- Low supply current (@ V_S = 5V) 500 µA/Amplifier
- Low offset voltage drift 1.0 µV/°C

Applications

- Automotive transducer amplifier
- Pressure sensor
- Oxygen sensor
- Temperature sensor
- Speed sensor

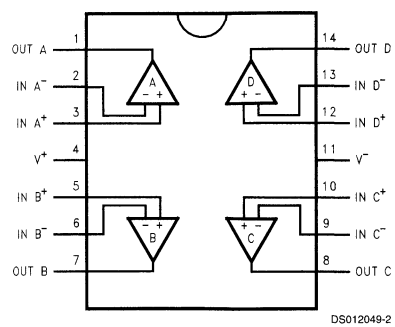
Connection Diagrams

8-Pin DIP/SO



Top View

14-Pin DIP/SO



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Conditions (Note 1)

Supply Voltage	$2.5V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC6492AE, LMC6492BE	$-40°C \le T_J \le +125°C$
LMC6494AE, LMC6494BE	$-40°C \le T_J \le +125°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	108°C/W
M Package, 8-Pin Surface Mount	171°C/W
N Package, 14-Pin Molded DIP	78°C/W
M Package, 14-Pin Surface Mount	118°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6492AE LMC6494AE Limit (Note 6)	LMC6492BE LMC6494BE Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11	3.0 **3.8**	6.0 **6.8**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			µV/°C
I_B	Input Bias Current	(Note 11)	0.15	**200**	**200**	pA max
I_{OS}	Input Offset Current	(Note 11)	0.075	**100**	**100**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
C_{IN}	Common-Mode Input Capacitance		3			pF
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 15V$ $V^+ = 15V$	82	65 **60**	63 **58**	dB min
		$0V \le V_{CM} \le 5V$	82	65 **60**	63 **58**	
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$, $V_O = 2.5V$	82	65 **60**	63 **58**	dB min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$, $V_O = 2.5V$	82	65 **60**	63 **58**	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 5V$ and 15V For CMRR ≥ 50 dB	V^- −0.3	−0.25 **0**	−0.25 **0**	V max
			$V^+ + 0.3$	$V^+ + 0.25$ **V^+**	$V^+ + 0.25$ **V^+**	V min
A_V	Large Signal Voltage Gain	$R_L = 2\ k\Omega$: Sourcing (Note 7) Sinking	300 40			V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6492AE LMC6494AE Limit (Note 6)	LMC6492BE LMC6494BE Limit (Note 6)	Units
V_O	Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.9	4.8 **4.7**	4.8 **4.7**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	V max
		V^+ = 5V R_L = 600Ω to $V^+/2$	4.7	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	V max
		V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.7	14.4 **14.0**	14.4 **14.0**	V min
			0.16	0.35 **0.5**	0.35 **0.5**	V max
		V^+ = 15V R_L = 600Ω to $V^+/2$	14.1	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.5**	1.0 **1.5**	V max
I_{SC}	Output Short Circuit Current V^+ = 5V	Sourcing, V_O = 0V	25	16 **10**	16 **10**	mA min
		Sinking, V_O = 5V	22	11 **8**	11 **8**	
I_{SC}	Output Short Circuit Current V^+ = 15V	Sourcing, V_O = 0V	30	28 **20**	28 **20**	
		Sinking, V_O = 5V (Note 8)	30	30 **22**	30 **22**	
I_S	Supply Current	LMC6492 V^+ = +5V, $V_O = V^+/2$	1.0	1.75 **2.1**	1.75 **2.1**	mA max
		LMC6492 V^+ = +15V, $V_O = V^+/2$	1.3	1.95 **2.3**	1.95 **2.3**	mA max
		LMC6494 V^+ = +5V, $V_O = V^+/2$	2.0	3.5 **4.2**	3.5 **4.2**	mA max
		LMC6494 V^+ = +15V, $V_O = V^+/2$	2.6	3.9 **4.6**	3.9 **4.6**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6492AE LMC6494AE Limit (Note 6)	LMC6492BE LMC6494BE Limit (Note 6)	Units
SR	Slew Rate	(Note 9)	1.3	0.7 **0.5**	0.7 **0.5**	Vμs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.5			MHz
ϕ_m	Phase Margin		50			Deg
G_m	Gain Margin		15			dB
	Amp-to-Amp Isolation	(Note 10)	150			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{CM} = 1V	37			$\frac{nV}{\sqrt{HZ}}$
i_n	Input-Referred Current Noise	F = 1 kHz	0.06			$\frac{pA}{\sqrt{HZ}}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −2 R_L = 10 kΩ, V_O = −4.1 V_{PP}	0.01			%
		F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP} V^+ = 10V	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 3.5V ≤ V_O ≤ 7.5V.

Note 8: Do not short circuit output to V^+, when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: V^+ = 15V. Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 10: Input referred, V^+ = 15V and R_L = 100 kΩ connected to 7.5V. Each amp excited in turn with 1 kHz to produce V_O = 12 V_{PP}.

Note 11: Guaranteed limits are dictated by tester limits and not device performance. Actual performance is reflected in the typical value.

National Semiconductor

LMC6572/LMC6574 Dual and Quad Low Voltage (2.7V and 3V) Operational Amplifier

General Description

Low voltage operation and low power dissipation make the LMC6574/2 ideal for battery-powered systems.

3V amplifier performance is backed by 2.7V guarantees to ensure operation throughout battery lifetime. These guarantees also enable analog circuits to operate from the same 3.3V supply used for digital logic.

Battery life is maximized because each amplifier dissipates only micro-watts of power.

The LMC6574/2 does not sacrifice functionality for low voltage operation. The LMC6574/2 generates 120 dB of open-loop gain just like a conventional amplifier, but the LMC6574/2 can do this from a 2.7V supply.

These amplifiers are designed with features that optimize low voltage operation. The output voltage swings rail-to-rail to maximize signal-to-noise ratio and dynamic signal range. The common-mode input voltage range extends from 800 mV below the positive supply to 100 mV below ground.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

LMC6572 is also available in MSOP package which is almost half the size of a SO-8 device.

Features

(Typical unless otherwise noted)

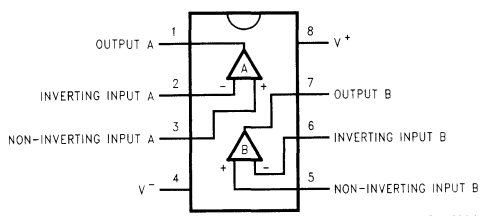
- Guaranteed 2.7V and 3V Performance
- Rail-to-Rail Output Swing (within 5 mV of supply rail, 100 kΩ load)
- Ultra-Low Supply Current: 40 μA/Amplifier
- Low Cost
- Ultra-Low Input Current: 20 fA
- High Voltage Gain @ V_S=2.7V, R_L=100 kΩ: 120 dB
- Specified for 100 kΩ and 5 kΩ loads
- Available in MSOP Package

Applications

- Transducer Amplifier
- Portable or Remote Equipment
- Battery-Operated Instruments
- Data Acquisition Systems
- Medical Instrumentation
- Improved Replacement for TLV2322 and TLV2324

Connection Diagrams

8-Pin DIP/SO/MSOP



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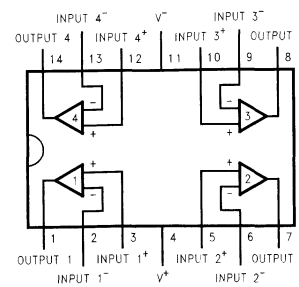
Order Number LMC6572AIN, LMC6572BIN, LMC6572AIM, LMC6572AIMX, LMC6572BIM, LMC6572BIMX, LMC6572BIMM or LMC6572BIMMX
See NS Package Number N08E, M08A or MUA08A

14-Pin DIP/SO



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Order Number LMC6574AIN, LMC6574BIN, LMC6574AIM, LMC6574AIMX, LMC6574BIM or LMC6574BIMX
See NS Package Number N14A or M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Supply Voltage $(V^+ - V^-)$	12V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±10 mA
Current at Power Supply Pin	35 mA
Lead Temperature (Soldering, 10 Seconds)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7V \le V^+ \le 11V$
Junction Temperature Range	
LMC6572AI, LMC6572BI	$-40°C \le T_J \le +85°C$
LMC6574AI, LMC6574BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M Package, 8-Pin Surface Mount	193°C/W
MSOP Package, 8-Pin Mini SO	217°C/W
N Package, 14-Pin Molded DIP	81°C/W
M Package, 14-Pin Surface Mount	126°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$ and 3V		0.5	3	7	mV
					3.5	**7.5**	Max
TCV_{OS}	Input Offset Voltage Average Drift			1.5			µV/°C
I_B	Input Current			0.02			pA
					10	**10**	Max
I_{OS}	Input Offset Current			0.01			pA
					6	**6**	Max
R_{IN}	Input Resistance			>1			Tera Ω
C_{IN}	Common-Mode Input Capacitance			3			pF
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 3.5V$ $V^+ = 5V$		75	63	60	dB
					60	**57**	Min
+PSRR	Positive Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$, $V^- = 0V$		75	67	60	dB
					65	**58**	Min
−PSRR	Negative Power Supply Rejection Ratio	$-2.7V \le V^- \le -5V$, $V^+ = 0V$		83	75	67	dB
					73	**65**	Min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$ and 3V for CMRR ≥ 50 dB		−0.1	−0.05	−0.05	V
					0	**0**	Max
				$V^+ - 0.8$	$V^+ - 1.0$	$V^+ - 1.0$	V
					$V^+ - 1.3$	**$V^+ - 1.3$**	Min
A_V	Large Signal Voltage Gain	$R_L = 100 k\Omega$ (Note 7)	Sourcing	1000			V/mV
			Sinking	500			V/mV

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
V_O	Output Swing	V^+ = 2.7V	2.695	2.68	2.65	V
		R_L = 100 kΩ to $V^+/2$		**2.66**	**2.62**	Min
			0.005	0.03	0.06	V
				0.05	**0.09**	Max
		V^+ = 2.7V	2.66	2.55	2.45	V
		R_L = 5 kΩ to $V^+/2$		**2.45**	**2.35**	Min
			0.04	0.15	0.25	V
				0.25	**0.35**	Max
		V^+ = 3V	2.995	2.98	2.95	V
		R_L = 100 kΩ to $V^+/2$		**2.96**	**2.93**	Min
			0.005	0.03	0.06	V
				0.05	**0.09**	Max
		V^+ = 3V	2.96	2.85	2.75	V
		R_L = 5 kΩ to $V^+/2$		**2.75**	**2.65**	Min
			0.04	0.15	0.25	V
				0.25	**0.35**	Max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	6.0	4.0	3.0	mA
				3.0	**2.0**	Min
		Sinking, V_O = 2.7V	4.0	3.0	2.5	mA
				2.0	**1.5**	Min
I_S	Supply Current	Quad Package	160	240	240	µA
		V^+ = +2.7V, V_O = $V^+/2$		**280**	**280**	Max
		Quad Package	160	240	240	µA
		V^+ = +3V, V_O = $V^+/2$		**280**	**280**	Max
		Dual Package	80	120	120	µA
		V^+ = +2.7V, V_O = $V^+/2$		**140**	**140**	Max
		Dual Package	80	120	120	µA
		V^+ = +3V, V_O = $V^+/2$		**140**	**140**	Max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
SR	Slew Rate	V^+ = 2.7V and 3V	90	30	30	V/ms
		(Note 8)		**10**	**10**	Min
GBW	Gain-Bandwidth Product	V^+ = 3V	0.22			MHz
ϕ_m	Phase Margin		60			Deg
G_m	Gain Margin		12			dB
	Amp-to-Amp Isolation	(Note 9)	120			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{CM} = 1V	45			$nV/\sqrt{Hz}$

2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6574AI LMC6572AI Limit (Note 6)	LMC6574BI LMC6572BI Limit (Note 6)	Units
i_n	Input-Referred Current Noise	F = 1 kHz	0.002			pA/√Hz
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 1.0 V_{PP}	0.05			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 3V, V_{CM} = 1.5V and R_L connected to 1.5V. For Sourcing tests, 1.5V ≤ V_O ≤ 2.5V. For Sinking tests, 0.5V ≤ V_O ≤ 1.5V.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred, V^+ = 3V and R_L = 100 kΩ connected to 1.5V. Each amp excited in turn with 1 KHz to produce V_O = 2 V_{PP}.

National Semiconductor

LMC660
CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Features

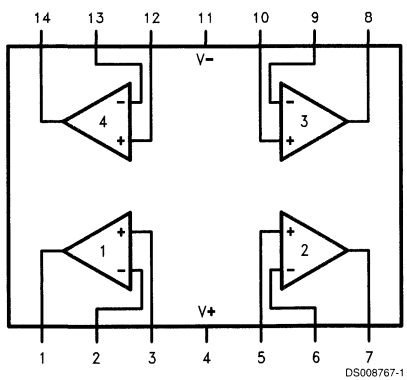
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain: 126 dB
- Low input offset voltage: 3 mV
- Low offset voltage drift: 1.3 μV/°C
- Ultra low input bias current: 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 375 μA/amplifier; independent of V^+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/μs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-Hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

14-Pin DIP/SO



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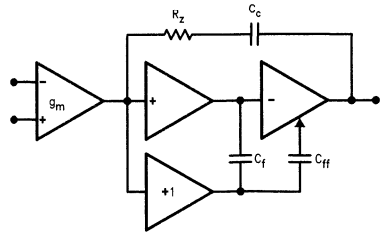
LMC660 Circuit Topology (Each Amplifier)



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Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 1)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD tolerance (Note 8)	1000V

Operating Ratings

Temperature Range	
LMC660AI	$-40°C \le T_J \le +85°C$
LMC660C	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}) (Note 11)	
14-Pin Molded DIP	85°C/W
14-Pin SO	115°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3 **3.3**	6 **6.3**	mV max
Input Offset Voltage Average Drift		1.3			µV/°C
Input Bias Current		0.002	 **4**	 **2**	pA max
Input Offset Current		0.001	 **2**	 **1**	pA max
Input Resistance		>1			TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	63 **62**	dB min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70 **68**	63 **62**	dB min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **83**	74 **73**	dB min
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.4$**	V min
Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 5) Sourcing	2000	440 **400**	300 **200**	V/mV min
	Sinking	500	180 **120**	90 **80**	V/mV min
	$R_L = 600\Omega$ (Note 5) Sourcing	1000	220 **200**	150 **100**	V/mV min
	Sinking	250	100 **60**	50 **40**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.87	4.82 **4.79**	4.78 **4.76**	V min
		0.10	0.15 **0.17**	0.19 **0.21**	V max
	V^+ = 5V R_L = 600Ω to $V^+/2$	4.61	4.41 **4.31**	4.27 **4.21**	V min
		0.30	0.50 **0.56**	0.63 **0.69**	V max
	V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.63	14.50 **14.44**	14.37 **14.32**	V min
		0.26	0.35 **0.40**	0.44 **0.48**	V max
	V^+ = 15V R_L = 600Ω to $V^+/2$	13.90	13.35 **13.15**	12.92 **12.76**	V min
		0.79	1.16 **1.32**	1.45 **1.58**	V max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **14**	13 **11**	mA min
	Sinking, V_O = 5V	21	16 **14**	13 **11**	mA min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	28 **25**	23 **21**	mA min
	Sinking, V_O = 13V (Note 12)	39	28 **24**	23 **20**	mA min
Supply Current	All Four Amplifiers V_O = 1.5V	1.5	2.2 **2.6**	2.7 **2.9**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	1.1	0.8 **0.6**	0.8 **0.7**	V/μs min
Gain-Bandwidth Product		1.4			MHz
Phase Margin		50			Deg
Gain Margin		17			dB
Amp-to-Amp Isolation	(Note 7)	130			dB
Input Referred Voltage Noise	F = 1 kHz	22			$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002			$pA/\sqrt{Hz}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01			%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC660AMJ/883 RETS spec complied fully with the **boldface** limits in this column. The LMC660AMJ/883 may also be procured to a Standard Military Drawing specification.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC662
CMOS Dual Operational Amplifier

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Features

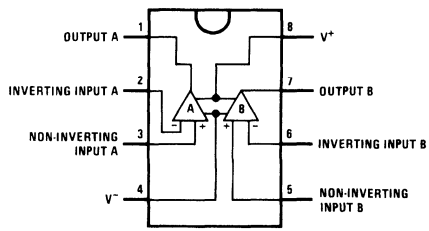
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain: 126 dB
- Low input offset voltage: 3 mV
- Low offset voltage drift: 1.3 μV/°C
- Ultra low input bias current: 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- I_{SS} = 400 μA/amplifier; independent of V+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/μs
- Available in extended temperature range (−40°C to +125°C); ideal for automotive applications
- Available to a Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

8-Pin DIP/SO



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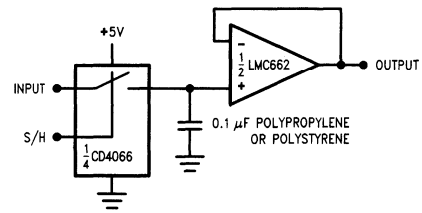
Typical Application

Low-Leakage Sample-and-Hold



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Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 12)
Output Short Circuit to V^-	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Voltage at Input/Output Pins	(V^+) +0.3V, (V^-) −0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD Tolerance (Note 8)	1000V

Operating Ratings (Note 3)

Temperature Range	
LMC662AI	$-40°C \le T_J \le +85°C$
LMC662C	$0°C \le T_J \le +70°C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 10)
Thermal Resistance (θ_{JA}) (Note 11)	
8-Pin Ceramic DIP	100°C/W
8-Pin Molded DIP	101°C/W
8-Pin SO	165°C/W
8-Pin Side Brazed Ceramic DIP	100°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AI Limit (Note 4)	LMC662C Limit (Note 4)	Units
Input Offset Voltage		1	3 **3.3**	6 **6.3**	mV max
Input Offset Voltage Average Drift		1.3			µV/°C
Input Bias Current		0.002	 **4**	 **2**	pA max
Input Offset Current		0.001	 **2**	 **1**	pA max
Input Resistance		>1			TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	63 **62**	dB min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70 **68**	63 **62**	dB min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **83**	74 **73**	dB min
Input Common-Mode Voltage Range	$V^+ = 5V$ & 15V For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ **$V^+ - 2.5$**	$V^+ - 2.3$ **$V^+ - 2.4$**	V min
Large Signal Voltage Gain	$R_L = 2 k\Omega$ (Note 5) Sourcing	2000	440 **400**	300 **200**	V/mV min
	Sinking	500	180 **120**	90 **80**	V/mV min
	$R_L = 600\Omega$ (Note 5) Sourcing	1000	220 **200**	150 **100**	V/mV min
	Sinking	250	100 **60**	50 **40**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AI	LMC662C	Units
			Limit (Note 4)	Limit (Note 4)	
Output Swing	V^+ = 5V	4.87	4.82	4.78	V
	R_L = 2 kΩ to $V^+/2$		**4.79**	**4.76**	min
		0.10	0.15	0.19	V
			0.17	**0.21**	max
	V^+ = 5V	4.61	4.41	4.27	V
	R_L = 600Ω to $V^+/2$		**4.31**	**4.21**	min
		0.30	0.50	0.63	V
			0.56	**0.69**	max
	V^+ = 15V	14.63	14.50	14.37	V
	R_L = 2 kΩ to $V^+/2$		**14.44**	**14.32**	min
		0.26	0.35	0.44	V
			0.40	**0.48**	max
	V^+ = 15V	13.90	13.35	12.92	V
	R_L = 600Ω to $V^+/2$		**13.15**	**12.76**	min
		0.79	1.16	1.45	V
			1.32	**1.58**	max
Output Current	Sourcing, V_O = 0V	22	16	13	mA
V^+ = 5V			**14**	**11**	min
	Sinking, V_O = 5V	21	16	13	mA
			14	**11**	min
Output Current	Sourcing, V_O = 0V	40	28	23	mA
V^+ = 15V			**25**	**21**	min
	Sinking, V_O = 13V	39	28	23	mA
	(Note 12)		**24**	**20**	min
Supply Current	Both Amplifiers	0.75	1.3	1.6	mA
	V_O = 1.5V		**1.5**	**1.8**	max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC662AI	LMC662C	Units
			Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	1.1	0.8	0.8	V/μs
			0.6	**0.7**	min
Gain-Bandwidth Product		1.4			MHz
Phase Margin		50			Deg
Gain Margin		17			dB
Amp-to-Amp Isolation	(Note 7)	130			dB
Input-Referred Voltage Noise	F = 1 kHz	22			$nV/\sqrt{Hz}$
Input-Referred Current Noise	F = 1 kHz	0.0002			$pA/\sqrt{Hz}$
Total Harmonic Distortion	F = 10 kHz, A_V = −10 R_L = 2 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01			%

AC Electrical Characteristics (Continued)

Note 1: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 10 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: Human body model, 1.5 kΩ in series with 100 pF.

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC662AMJ/883 RETS spec complied fully with the **boldface** limits in this column. The LMC662AMJ/883 may also be procured to a Standard Military Drawing specification.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J-T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LMC7101
Tiny Low Power Operational Amplifier with Rail-To-Rail Input and Output

General Description

The LMC7101 is a high performance CMOS operational amplifier available in the space saving SOT 23-5 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/4 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

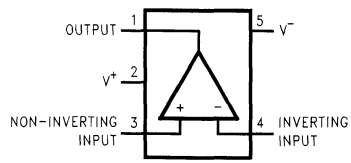
- Tiny SOT23-5 package saves space—typical circuit layouts take half the space of SO-8 designs
- Guaranteed specs at 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5 mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1.0 MHz gain-bandwidth
- Similar to popular LMC6482/4
- Input common-mode range includes V^- and V^+
- Tiny package outside dimensions—120 x 118 x 56 mils, 3.05 x 3.00 x 1.43 mm

Applications

- Mobile communications
- Notebooks and PDAs
- Battery powered products
- Sensor interface

Connection Diagram

5-Pin SOT23-5



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Top View

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied As
5-Pin SOT 23-5	LMC7101AIM5	MA05A	A00A	1k Units on Tape and Reel
	LMC7101AIM5X	MA05A	A00A	3k Units Tape and Reel
	LMC7101BIM5	MA05A	A00B	1k Units on Tape and Reel
	LMC7101BIM5X	MA05A	A00B	3k Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2000V
Difference Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	16V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±35 mA
Current at Power Supply Pin	35 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Recommended Operating Conditions (Note 1)

Supply Voltage	$2.7V \le V^+ \le 15.5V$
Junction Temperature Range	
LMC7101AI, LMC7101BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
M05A Package, 5-Pin Surface Mt.	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.11	6	9	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			µV/°C
I_B	Input Bias Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$ $V^+ = 2.7V$	70	55	50	dB min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = V$ For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.0	2.7	2.7	V max
PSRR	Power Supply Rejection Ratio	$V^+ = 1.35V$ to $1.65V$ $V^- = -1.35V$ to $-1.65V$ $V_{CM} = 0$	60	50	45	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$R_L = 2\ k\Omega$	2.45	2.15	2.15	V min
			0.25	0.5	0.5	V max
		$R_L = 10\ k\Omega$	2.68	2.64	2.64	V min
			0.025	0.06	0.06	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	mA max
SR	Slew Rate	(Note 8)	0.7			V/µs
GBW	Gain-Bandwidth Product		0.6			MHz

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11	4 **6**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1			µV/°C
I_B	Input Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3V V^+ = 3V	74	64	60	db min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	0.0	0.0	0.0	V min
			3.3	3.0	3.0	V max
PSRR	Power Supply Rejection Ratio	V^+ = 1.5V to 7.5V V^- = −1.5V to −7.5V V_O = V_{CM} = 0	80	68	60	dB min
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	R_L = 2 kΩ	2.8	2.6	2.6	V min
			0.2	0.4	0.4	V max
		R_L = 600Ω	2.7	2.5	2.5	V min
			0.37	0.6	0.6	V max
I_S	Supply Current		0.5	0.81 **0.95**	0.81 **0.95**	mA max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 5V	0.11	3 **5**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			µV/°C
I_B	Input Current		1	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	82	65 **60**	60 **55**	db min
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V to 15V V^- = 0V, V_O = 1.5V	82	70 **65**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V^- = −5V to −15V V^+ = 0V, V_O = −1.5V	82	70 **65**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			5.3	5.20 **5.00**	5.20 **5.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	R_L = 2 kΩ	4.9	4.7 **4.6**	4.7 **4.6**	V min
			0.1	0.18 **0.24**	0.18 **0.24**	V max
		R_L = 600Ω	4.7	4.5 **4.24**	4.5 **4.24**	V min
			0.3	0.5 **0.65**	0.5 **0.65**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	24	16 **11**	16 **11**	mA min
		Sinking, V_O = 5V	19	11 **7.5**	11 **7.5**	mA min
I_S	Supply Current		0.5	0.85 **1.0**	0.85 **1.0**	mA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 4.0 V_{PP}	0.01			%
SR	Slew Rate		1.0			V/µs
GBW	Gain_Bandwidth Product		1.0			MHz

15V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 15V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.11			mV max
TCV_{OS}	Input Offset Voltage Average Drift		1.0			μV/°C
I_B	Input Current		1.0	**64**	**64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	**32**	pA max
R_{IN}	Input Resistance		>1			Tera Ω
CMRR	Common-Mode Rejection Ratio	0V ≤ V_{CM} ≤ 15V	82	70 **65**	65 **60**	dB min
+PSRR	Positive Power Supply Rejection Ratio	V^+ = 5V to 15V V^- = 0V, V_O = 1.5V	82	70 **65**	65 **62**	dB min
−PSRR	Negative Power Supply Rejection Ratio	V^- = −5V to −15V V^+ = 0V, V_O = −1.5V	82	70 **65**	65 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			15.3	15.20 **15.00**	15.20 **15.00**	V max
A_V	Large Signal Voltage Gain	R_L = 2 kΩ Sourcing (Note 7)	340	80 **40**	80 **40**	V/mV
		Sinking	24	15 **10**	15 **10**	
		R_L = 600Ω Sourcing	300	34	34	V/mV
		(Note 7) Sinking	15	6	6	
C_{IN}	Input Capacitance		3			pF
V_O	Output Swing	V^+ = 15V R_L = 2 kΩ	14.7	14.4 **14.2**	14.4 **14.2**	V min
			0.16	0.32 **0.45**	0.32 **0.45**	V max
		V^+ = 15V R_L = 600Ω	14.1	13.4 **13.0**	13.4 **13.0**	V min
			0.5	1.0 **1.3**	1.0 **1.3**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (Note 9)	50	30 **20**	30 **20**	mA min
		Sinking, V_O = 12V (Note 9)	50	30 **20**	30 **20**	mA min
I_S	Supply Current		0.8	1.50 **1.71**	1.50 **1.71**	mA max

15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 15V, V^- = 0V, V_{CM} = 1.5V, V_O = V^+/2 and R_L = 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7101AI Limit (Note 6)	LMC7101BI Limit (Note 6)	Units
SR	Slew Rate	V^+ = 15V (Note 8)	1.1	0.5 **0.4**	0.5 **0.4**	V/μs min
GBW	Gain-Bandwidth Product	V^+ = 15V	1.1			MHz
ϕ_m	Phase Margin		45			Deg
G_m	Gain Margin		10			dB
e_n	Input-Referred Voltage Noise	F = 1 kHz V_{CM} = 1V	37			$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	F = 1 kHz	1.5			$\frac{fA}{\sqrt{Hz}}$
T.H.D.	Total Harmonic Distortion	F = 10 kHz, A_V = −2 R_L = 10 kΩ, V_O = 8.5 V_{PP}	0.01			%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is PD = $(T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 15V, V_{CM} = 1.5V and R_L connect to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 12.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 8: V^+ = 15V. Connected as a Voltage Follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. R_L = 100 kΩ connected to 7.5V. Amp excited with 1 kHz to produce V_O = 10 V_{PP}.

Note 9: Do not short circuit output to V^+ when V^+ is greater than 12V or reliability will be adversely affected.

National Semiconductor

LMC7111
Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

General Description

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT 23-5 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V^+ supply. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

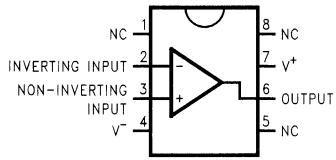
- Tiny SOT23-5 package saves space
- Very wide common mode input range
- Specified at 2.7V, 5V, and 10V
- Typical supply current 25 µA at 5V
- 50 kHz gain-bandwidth at 5V
- Similar to popular LMC6462
- Output to within 20 mV of supply rail at 100k load
- Good capacitive load drive

Applications

- Mobile communications
- Portable computing
- Current sensing for battery chargers
- Voltage reference buffering
- Sensor interface
- Stable bias for GaAs RF amps

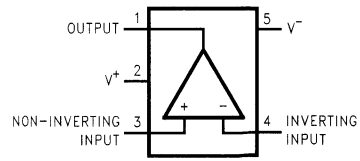
Connection Diagrams

8-Pin DIP



Top View

5-Pin SOT23-5



Top View

Actual Size

Ordering Information

Package	Ordering Information	NSC Drawing Number	Package Marking	Transport Media
8-Pin DIP	LMC7111AIN	N08E	LMC7111AIN	Rails
8-Pin DIP	LMC7111BIN	N08E	LMC7111BIN	Rails
5-Pin SOT23-5	LMC7111BIM5	MA05A	A01B	1k units Tape and Reel
	LMC7111BIM5X	MA05A	A01B	3k Units Tape and Reel

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance SOT23-5 (Note 2)	2000V
ESD Tolerance DIP Package (Note 2)	1500V
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	$(V^+) + 0.3V$, $(V^-) - 0.3V$
Supply Voltage ($V^+ - V^-$)	11V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±30 mA
Current at Power Supply Pin	30 mA
Lead Temp. (Soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.5V \le V^+ \le 11V$
Junction Temperature Range	
LMC7111AI, LMC7111BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	115°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	$V^+ = 2.7V$	0.9	3	7	mV
				5	**9**	max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			µV/°C
I_B	Input Bias Current	(Note 9)	0.1	1	1	pA
				20	**20**	max
I_{OS}	Input Offset Current	(Note 9)	0.01	0.5	0.5	pA
				10	**10**	max
R_{IN}	Input Resistance		>10			Tera Ω
+PSRR	Positive Power Supply Rejection Ratio	$2.7V \le V^+ \le 5.0V$, $V^- = 0V$, $V_O = 2.5V$	60	55	55	dB
				50	**50**	min
−PSRR	Negative Power Supply Rejection Ratio	$-2.7V \le V^- \le -5.0V$, $V^- = 0V$, $V_O = 2.5V$	60	55	55	dB
				50	**50**	min
V_{CM}	Input Common-Mode Voltage Range	$V^+ = 2.7V$ For CMRR ≥ 50 dB	−0.10	0.0	0.0	V
				0.40	**0.40**	min
			2.8	2.7	2.7	V
				2.25	**2.25**	max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	$V^+ = 2.7V$ $R_L = 100\ k\Omega$	2.69	2.68	2.68	V
				2.4	**2.4**	min
			0.01	0.02	0.02	V
				0.08	**0.08**	max
		$V^+ = 2.7V$ $R_L = 10\ k\Omega$	2.65	2.6	2.6	V
				2.4	**2.4**	min
			0.03	0.1	0.1	V
				0.3	**0.3**	max
I_{SC}	Output Short Circuit Current	Sourcing, $V_O = 0V$	7	1	1	mA
				0.7	**0.7**	min
		Sinking, $V_O = 2.7V$	7	1	1	mA
				0.7	**0.7**	min

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
A_{VOL}	Voltage Gain	Sourcing	400			V/mv min
		Sinking	150			V/mv min
I_S	Supply Current	V^+ = +2.7V, V_O = $V^+/2$	20	45 **60**	50 **65**	µA max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.015			V/µs
GBW	Gain-Bandwidth Product		40			kHz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 2.7V, V_{CM} = 1.35V and R_L connected to 1.35V. For Sourcing tests, 1.35V ≤ V_O ≤ 2.7V. For Sinking tests, 0.5V ≤ V_O ≤ 1.35V.

Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, V^+ = 2.7V and R_L = 100 kΩ connected to 1.35V. Amp excited with 1 kHz to produce V_O = 1 V_{PP}.

Note 9: Bias Current guaranteed by design and processing.

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	V^+ = 3V For CMRR ≥ 50 dB	−0.25	0.0	0.0	V min
			3.2	3.0 **2.8**	3.0 **2.8**	V max

3.3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 3.3V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	V^+ = 3.3V For CMRR ≥ 50 dB	−0.25	−0.1 **0.00**	−0.1 **0.00**	V min
			3.5	3.4 **3.2**	3.4 **3.2**	V max

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 5V	0.9			mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			µV/°C
I_B	Input Bias Current	(Note 9)	0.1	1 **20**	1 **20**	pA max
I_{OS}	Input Offset Current	(Note 9)	0.01	0.5 **10**	0.5 **10**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	85	70	60	dB min
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤10V, V^- = 0V, V_O = 2.5V	85	70	60	dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤−10V, V^- = 0V, V_O = −2.5V	85	70	60	dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5V For CMRR ≥ 50 dB	−0.3	−0.20 **0.00**	−0.20 **0.00**	V min
			5.25	5.20 **5.00**	5.20 **5.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ	4.99	4.98	4.98	Vmin
			0.01	0.02	0.02	Vmax
		V^+ = 5V R_L = 10 kΩ	4.98	4.9	4.9	Vmin
			0.02	0.1	0.1	Vmin
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V	7	5 **3.5**	5 **3.5**	mA min
		Sinking, V_O = 3V	7	5 **3.5**	5 **3.5**	mA min
A_{VOL}	Voltage Gain	Sourcing	500			V/mv min
		Sinking	200			V/mv min
I_S	Supply Current	V^+ = +5V, V_O = $V^+/2$	25			µA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	Positive Going Slew Rate (Note 8)	0.027	0.015	0.010	V/μs
GBW	Gain-Bandwidth Product		50			kHz

Note 10: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 11: Human body model, 1.5 kΩ in series with 100 pF.

Note 12: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 13: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 14: Typical Values represent the most likely parametric norm.

Note 15: All limits are guaranteed by testing or statistical analysis.

Note 16: V^+ = 5V, V_{CM} = 2.5V and R_L connected to 2.5V. For Sourcing tests, 2.5V ≤ V_O ≤ 5.0V. For Sinking tests, 0.5V ≤ V_O ≤ 2.5V.

Note 17: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive slew rate. The negative slew rate is faster. Input referred, V^+ = 5V and R_L = 100 kΩ connected to 1.5V. Amp excited with 1 kHz to produce V_O = 1 V_{PP}.

Note 18: Bias Current guaranteed by design and processing.

10V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 10V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage	V^+ = 10V	0.9	3 **5**	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2.0			μV/°C
I_B	Input Bias Current		0.1	1 **20**	1 **20**	pA max
I_{OS}	Input Offset Current		0.01	0.5 **10**	0.5 **10**	pA max
R_{IN}	Input Resistance		>10			Tera Ω
+PSRR	Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤10V, V^- = 0V, V_O = 2.5V	80			dB min
−PSRR	Negative Power Supply Rejection Ratio	−5V ≤ V^- ≤−10V, V^- = 0V, V_O = 2.5V	80			dB min
V_{CM}	Input Common-Mode Voltage Range	V^+ = 10V For CMRR ≥ 50 dB	−0.2	−0.15 **0.00**	−0.15 **0.00**	V min
			10.2	10.15 **10.00**	10.15 **10.00**	V max
C_{IN}	Common-Mode Input Capacitance		3			pF
I_{SC}	Output Short Circuit Current (Note 9)	Sourcing, V_O = 0V	30	20 **7**	20 **7**	mA min
		Sinking, V_O = 10V	30	20 **7**	20 **7**	mA min

10V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 10V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
A_{VOL}	Voltage Gain 100 kΩ Load	Sourcing	500			V/mv min
		Sinking	200			V/mv min
I_S	Supply Current	V^+ = +10V, $V_O = V^+/2$	25	50 **65**	60 **75**	μA max
V_O	Output Swing	V^+ = 10V	9.99	9.98	9.98	Vmin
		R_L = 100 kΩ	0.01	0.02	0.02	Vmax
		V^+ = 10V	9.98	9.9	9.9	Vmin
		R_L = 10 kΩ	0.02	0.1	0.1	Vmin

10V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 10V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7111AI Limit (Note 6)	LMC7111BI Limit (Note 6)	Units
SR	Slew Rate	(Note 8)	0.03			V/μs
GBW	Gain-Bandwidth Product		50			kHz
ϕ_m	Phase Margin		50			deg
G_m	Gain Margin		15			dB
	Input-Referred Voltage Noise	f = 1 kHz V_{CM} = 1V	110			$\frac{nV}{\sqrt{Hz}}$
	Input-Referred Current Noise	f = 1 kHz	0.03			$\frac{pA}{\sqrt{Hz}}$

Note 19: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 20: Human body model, 1.5 kΩ in series with 100 pF.

Note 21: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C.

Note 22: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 23: Typical Values represent the most likely parametric norm.

Note 24: All limits are guaranteed by testing or statistical analysis.

Note 25: V^+ = 10V, V_{CM} = 5V and R_L connected to 5V. For Sourcing tests, 5V ≤ V_O ≤ 10V. For Sinking tests, 0.5V ≤ V_O ≤ 5V.

Note 26: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates. Input referred, V^+ = 10V and R_L = 100 kΩ connected to 5V. Amp excited with 1 kHz to produce $V_O = 2\ V_{PP}$.

Note 27: Operation near absolute maximum limits will adversely affect reliability.

National Semiconductor

LMC8101
Rail-to-Rail Input and Output, 2.7V Op Amp in micro SMD package with Shutdown

General Description

The LMC8101 is a Rail-to-Rail Input and Output high performance CMOS operational amplifier. The LMC8101 is ideal for low voltage (2.7V to 10V) applications requiring Rail-to-Rail inputs and output. The LMC8101 is supplied in the die sized micro SMD as well as the 8 pin MSOP packages. The micro SMD package requires 75% less board space as compared to the SOT23-5 package. The LMC8101 is an upgrade to the industry standard LMC7101.

The LMC8101 incorporates a simple user controlled methodology for shutdown. This allows ease of use while reducing the total supply current to 1nA typical. This extends battery life where power saving is mandated. The shutdown input threshold can be set relative to either V^+ or V^- using the SL pin (see Application Note section for details).

Other enhancements include improved offset voltage limit, three times the output current drive and lower 1/f noise when compared to the industry standard LMC7101 Op Amp. This makes the LMC8101 ideal for use in many battery powered, wireless communication and Industrial applications.

Features

V_S = 2.7V, T_A = 25°C, R_L to $V^+/2$, Typical values unless specified.

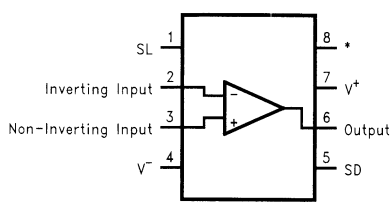
- Rail-to-Rail Inputs
- Rail-to-Rail Output Swing — Within 35mV of Supplies (R_L =2kΩ)
- Packages Offered:
- micro SMD package — 1.39mm x 1.41mm
- MSOP package — 3.0mm x 4.9mm
- Low Supply Current — <1mA (max)
- Shutdown Current — 1µA (max)
- Versatile Shutdown feature — 10µs turn-on
- Output Short Circuit Current — 10mA
- Offset Voltage — ±5 mV (max)
- Gain-Bandwidth — 1MHz
- Supply Voltage Range — 2.7V-10V
- THD — 0.18%
- Voltage Noise — 36 $\frac{nV}{\sqrt{Hz}}$

Applications

- Portable Communication (voice, data)
- Cellular Phone Power Amp Control Loop
- Buffer AMP
- Active Filters
- Battery Sense
- VCO Loop

Connection Diagrams

8-Pin MSOP



* No Internal Connection

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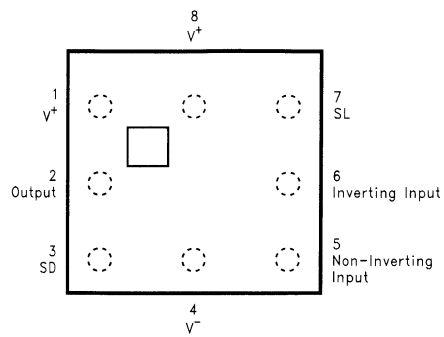
Top View

micro SMD



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Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	2KV (Note 2)
	200V (Note 13)
V_{IN} differential	+/−Supply Voltage
Output Short Circuit Duration	(Notes 3, 11)
Supply Voltage ($V^+ - V^-$)	12V
Voltage at Input/Output pins	V^+ +0.8V, V^- −0.8V
Current at Input Pin	+/−10mA
Current at Output Pin (Notes 3, 12)	+/−80mA
Current at Power Supply pins	+/−80mA
Storage Temperature Range	−65°C to +150°C
Junction Temperature(Note 4)	+150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings (Note 1)

Supply Voltage ($V^+ - V^-$)	2.7V to 10V
Junction Temperature Range (Note 4)	−40°C to +85°C
Package Thermal Resistance (θ_{JA}) (Note 4)	
micro SMD	220°C/W
MSOP pkg. 8 pin Surface Mount	230°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		±0.70	±5 **±7**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		4		µV/°C
I_B	Input Bias Current	(Note 7)	±1	**±64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
$R_{in\ CM}$	Input Common Mode Resistance		10		GΩ
$C_{in\ CM}$	Input Common Mode Capacitance		10		pF
CMRR	Common Mode Rejection Ratio	0V < = V_{CM} < = 2.7V	78	60	dB min
		V_S = 3V 0V < = V_{CM} < = 3V	78	64 **60**	
PSRR	Power Supply Rejection Ratio	V_S = 2.7V to 3V	57	50 **48**	dB min
CMVR	Input Common-Mode Voltage Range	V_S = 2.7V CMRR > = 50dB	0.0	0.0	V max
			3.0	2.7	V min
		V_S = 3V CMRR > = 50dB	−0.2	−0.1	V max
			3.2	3.1	V min

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = V_O = $V^+/2$ and R_L > 1 MΩ to $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 2kΩ to $V^+/2$ V_O = 1.35V to 2.45V	3162	1000 562	V/V min
		Sinking R_L = 2kΩ to $V^+/2$ V_O = 1.35V to 0.25V	3162	804 **562**	
		Sourcing R_L = 10kΩ to $V^+/2$ V_O = 1.35V to 2.65V	4000	1778 **1000**	V/V min
		Sinking R_L = 10kΩ to $V^+/2$ V_O = 1.35V to 0.05V	4000	1778 **1000**	
V_O	Output Swing High	R_L = 2kΩ to $V^+/2$ V_{ID} = 100mV	2.67	2.64 **2.62**	V min
		R_L = 10kΩ to $V^+/2$ V_{ID} = 100mV	2.69	2.68 **2.67**	V min
	Output Swing Low	R_L = 2kΩ to $V^+/2$ V_{ID} = −100mV	32	100 **150**	mV max
		R_L = 10kΩ to $V^+/2$ V_{ID} = −100mV	10	30 **70**	mV max
I_{SC}	Output Short Circuit Current	Sourcing to $V^+/2$ V_{ID} = 100mV (Note 11)	20	14 **6**	mA min
		Sinking to $V^+/2$ V_{ID} = −100mV (Note 11)	10	5 **4**	mA min
I_S	Supply Current	No load, normal operation	0.70	1.0 **1.2**	mA max
		Shutdown mode	0.001	1	μA max
T_{on}	Shutdown Turn-on time	(Note 9)	10	15	μs
T_{off}	Shutdown Turn-off time	(Note 9)	1		μs
I_{in}	'SL' and 'SD' Input Current		±1	**±64**	pA max
SR	Slew Rate (Note 8)	A_V = +1, R_L = 10kΩ to $V^+/2$ V_I= $1V_{PP}$	1	0.8	V/μs min
f_u	Unity Gain-Bandwidth	V_I = 10mV, R_L = 2kΩ to $V^+/2$	750		KHz
GBW	Gain Bandwidth Product	f = 100KHz	1		MHz
e_n	Input-Referred Voltage Noise	f = 10KHz, R_S = 50Ω	36		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10KHz	1.5		$\frac{fA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1KHz, AV = +1, V_O = 2.2Vpp, R_L = 600Ω to $V^+/2$	0.18		%

+/−5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ =5V, V^- = −5V, V_{CM} = V_O = 0V, and R_L > 1 MΩ to gnd. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		±0.7	±5 **±7**	mV max
TCV_{os}	Input Offset Voltage Average Drift		4		µV/°C
I_B	Input Bias Current	(Note 7)	±1	**±64**	pA max
I_{OS}	Input Offset Current		0.5	**32**	pA max
$R_{in\ CM}$	Input Common Mode Resistance		10		GΩ
$C_{in\ CM}$	Input Common Mode Capacitance		10		pF
CMRR	Common-Mode Rejection Ratio	−5V < = V_{CM} < = 5V	87	70 **67**	dB min
PSRR	Power Supply Rejection Ratio	V_S = 5V to 10V	80	76 **72**	dB min
CMVR	Input Common-Mode Voltage Range	CMRR ≥ 50 dB	−5.3	−5.2 **−5.0**	V max
			5.3	5.2 **5.0**	V min
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 600Ω V_O = 0V to 4V	34.5	17.8 **10**	V/mV min
		Sinking R_L = 600Ω V_O = 0V to −4V	34.5	17.8 **3.16**	
		Sourcing R_L = 2kΩ V_O = 0V to 4.6V	138	31.6 **17.8**	V/mV min
		Sinking R_L = 2kΩ V_O = 0V to −4.6V	138	31.6 **10**	
V_O	Output Swing High	R_L = 600Ω V_{ID} = 100mV	4.73	4.60 **4.54**	V min
		R_L = 2kΩ V_{ID} = 100mV	4.90	4.85 **4.83**	V min
	Output Swing Low	R_L = 600Ω V_{ID} = −100mV	−4.85	−4.75 **−4.65**	V max
		R_L = 2kΩ V_{ID} = −100mV	−4.95	4.90 **−4.84**	V max
I_{SC}	Output Short Circuit Current	Sourcing, V_{ID} = 100mV (Note 3),(Note 11)	49	30 **25**	mA min
		Sinking, V_{ID} = −100mV (Note 3),(Note 11)	90	60 **52**	mA min
I_S	Supply Current	No load, normal operation	1.1	1.7 **1.9**	mA max
		Shutdown mode	0.001	1	µA
T_{on}	Shutdown Turn-on time	(Note 9)	10	15	µs
T_{off}	Shutdown Turn-off time	(Note 9)	1		µs
I_{in}	'SL' and 'SD' Input Current		±1	**±64**	pA max

+/−5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ =5V, V^- = -5V, V_{CM} = V_O = 0V, and R_L > 1 MΩ to gnd. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
SR	Slew Rate (Note 8)	A_V = +10, R_L = 10kΩ, V_O = 10Vpp, C_L = 1000pF	1.2		V/μs
f_u	Unity Gain-Bandwidth	V_I = 10mV R_L = 2kΩ	840		KHz
GBW	Gain Bandwidth Product	f = 10KHz	1.3		MHz
e_n	Input-Referred Voltage Noise	f = 10KHz, R_S = 50Ω	33		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 10KHz	1.5		$\frac{fA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 10KHz, AV = +1, V_O =8Vpp, R_L = 600Ω	0.2		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C. Output currents in excess of 40mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Positive current corresponds to current flowing into the device.

Note 8: Slew rate is the slower of the rising and falling slew rates.

Note 9: Shutdown Turn-on and Turn-off times are defined as the time required for the output to reach 90% and 10%, respectively, of its final peak to peak swing when set for Rail to Rail output swing with a 100KHz sine wave, 2KΩ load, and A_V = +10.

Note 10: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 11: Short circuit test is a momentary test. See Note 12.

Note 12: Output short circuit duration is infinite for V_S < 6V. Otherwise, extended period output short circuit may damage the device.

Note 13: machine Model, 0Ω in series with 200pF.

National Semiconductor

LMV301
Low Input Bias Current, 1.8V Op Amp w/Rail-to-Rail Output

General Description

The LMV301 CMOS operational amplifier is ideal for single supply, low voltage operation with a guaranteed operating voltage range from 1.8V to 5V. The low input bias current of less than 0.182pA typical, eliminates input voltage errors that may originate from small input signals. This makes the LMV301 ideal for electrometer applications requiring low input leakage such as sensitive photodetection transimpedance amplifiers and sensor amplifiers. The LMV301 also features a rail-to-rail output voltage swing in addition to a input common-mode range that includes ground. The LMV301 will drive a 600Ω resistive load and up to 1000pF capacitive load in unity gain follower applications. The low supply voltage also makes the LMV301 well suited for portable two-cell battery systems and single cell Li-Ion systems.

The LMV301 exhibits excellent speed-power ratio, achieving 1MHz at unity gain with low supply current. The high DC gain of 100dB makes it ideal for other low frequency applications.

The LMV301 is offered in a space saving SC-70 package, which is only 2.0X2.1X1.0mm. It is also similar to the LMV321 except the LMV301 has a CMOS input.

Key Specifications

(Typical values unless otherwise specified)

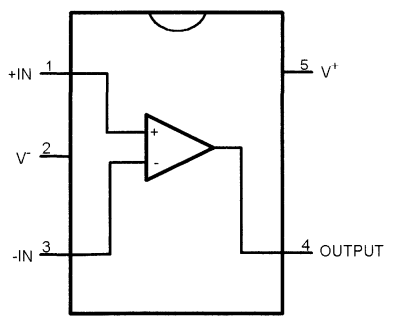
- Input bias current 0.182pA
- Gain bandwidth product 1MHz
- Supply voltage @ 1.8V 1.8V to 5V
- Supply current 150µA
- Input referred voltage noise @ 1kHz 40nV/$\sqrt{Hz}$
- DC Gain (600Ω load) 100dB
- Output voltage range @ 1.8V 0.024 to 1.77V
- Input common-mode voltage range −0.3V to V^+ - 1.2V

Applications

- Thermocouple amplifiers
- Photo current amplifiers
- Transducer amplifiers
- Sample and hold circuits
- Low frequency active filters

Connection Diagram

SC70-5

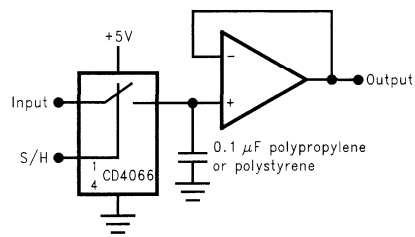


20019301

Top View

Applications Circuit

Low Leakage Sample and Hold



20019307

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70-5	LMV301MG	A48	1k Units Tape and Reel	MAA05A
	LMV301MGX		3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 7)	
Machine Model	200V
Human Body Model	2000V
Differential Input Voltage	±Supply Voltage
Supply Voltage (V^+ - V^-)	5.5V
Output Short Circuit to V^+ (Note 2)	
Output Short Circuit to V^- (Note 2)	
Storage Tempeature Range	−65°C to 150°C
Mounting Temperature	
Infrared or Convection (20 sec)	235°C
Junction Temperature (Note 3)	150°C

Operating Ratings (Note 1)

Supply Voltage	1.8V to 5.0V
Temperature Range	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package	
5-pin Surface Mount	478°C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.4V, V^+ = 1.3V, = V^- = −0.5V			0.9	8 **9**	mV
I_B	Input Bias Current				0.182	35 **50**	pA
I_S	Supply Current	V_{CM} = 0.4V, V^+ = 1.3V, = V^- = −0.5V			150	250 **275**	µA
CMRR	Common Mode Rejection Ratio	0.3V ≤ V_{CM} ≤ 0.9V		62 **60**	108		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V, 0.9 ≤ V_{CM} ≤ 2.5V		67 **62**	110		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.3 **0**		0.6	V
A_V	Large Signal Voltage Gain Sourcing	R_L = 600Ω to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	119		dB
		R_L = 2kΩ to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	111		
	Sinking	R_L = 600Ω to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	94		dB
		R_L = 2kΩ to 0V, V^+ = 1.2V, V^- = −0.6V, V_O = −0.2V to 0.8V, V_{CM} = 0V		80 **75**	96		
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ±100mV	V_{OH}	1.65 **1.63**	1.72		V
			V_{OL}		0.074	0.100	V
		R_L = 2kΩ to 0.9V V_{IN} = ±100mV	V_{OH}	1.75 **1.74**	1.77		V
			V_{OL}		0.024	0.035 **0.040**	V
I_O	Output Short Circuit Current	Sourcing, V_O = 0V, V_{IN} = 100mV		4 **3.3**	8.4		mA
		Sinking, V_O = 1.8V, V_{IN} = −100mV		7	9.8		mA

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Units
SR	Slew Rate	(Note 6)	0.57	V/µs
GBW	Gain Bandwidth Product		1	MHz
ϕm	Phase Margin		60	Deg
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 0.5V f = 100kHz	40 30	nV/$\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 RL = 600kΩ, V_{IN} = $1V_{PP}$	0.089	%

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.35V, V^+ = 1.7V, V^- = −1V			0.9	8 **9**	mV
I_B	Input Bias Current				0.182	35 **50**	pA
I_S	Supply Current	V_{CM} = 0.35V, V^+ = 1.7V, V^- = −1V			153	250 **275**	µA
CMRR	Common Mode Rejection Ratio	−0.15V ≤ V_{CM} ≤ 1.35V		62 **60**	115		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V+ ≤ 5V		67 **62**	110		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.3 **0**		1.5	V
A_V	Large Signal Voltage Gain Sourcing	R_L = 600Ω to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		80 **75**	100		dB
		R_L = 2kΩ to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		83 **77**	114		
	Sinking	R_L = 600Ω to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		80 **75**	98		dB
		R_L = 2kΩ to 0V, V^+ = 1.35V, V^- = −1.35V, V_O = −1V to 1V, V_{CM} = 0V		80 **75**	99		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ±100mV	V_{OH}	2.550 **2.530**	2.62		V
			V_{OL}		0.078	0.100	V
		R_L = 2kΩ to 1.35V V_{IN} = ±100mV	V_{OH}	2.650 **2.640**	2.675		V
			V_{OL}		0.024	0.045	V
I_O	Output Short Circuit Current	Sourcing, V_O = 0V, V_{IN} = 100mV		20 **15**	32		mA
		Sinking, V_O = 2.7V, V_{IN} = −100mV		19 **12**	24		mA

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Units
SR	Slew Rate	(Note 6)	0.60	V/μs
GBW	Gain Bandwidth Product		1	MHz
ϕm	Phase Margin		65	Deg
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 0.5V f = 100kHz	40 30	nV/$\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600kΩ, V_{IN} = $1V_{PP}$	0.077	%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition		Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.5V, V^+ = 3V, V^- = −2V			0.9	8 **9**	mV
I_D	Input Bias Current				0.182	35 **50**	pA
I_S	Supply Current	V_{CM} = 0.5V, V^+ = 3V, V^- = −2V			163	260 **285**	μA
CMRR	Common Mode Rejection Ratio	−1.3V ≤ V_{CM} ≤ 2.5V		62 **61**	111		dB
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V		67 **62**	110		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.3 **0**		3.8	V
A_V	Large Signal Voltage Gain Sourcing	R_L = 600Ω to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		86 **82**	117		dB
		R_L = 2kΩ to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		89 **85**	116		
	Sinking	R_L = 600Ω to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		80 **75**	105		dB
		R_L = 2kΩ to 0V, V^+ = 2.5V, V^- = −2.5V, V_O = −2V to 2V, V_{CM} = 0V		80 **75**	107		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ±100mV	V_{OH}	4.850 **4.840**	4.893		V
			V_{OL}		0.1	0.150 **1.160**	V
		R_L = 2kΩ to 2.5V V_{IN} = ±100mV	V_{OH}	4.935	4.966		V
			V_{OL}		0.034	0.065 **0.075**	V
I_O	Output Short Circuit Current	Sourcing, V_O = 0V, V_{IN} = 100mV		85 **68**	108		mA
		Sinking, V_O = 5V, V_{IN} = −100mV		60 **45**	69		mA

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = 2.5V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Units
SR	Slew Rate	(Note 6)	0.66	V/μs
GBW	Gain Bandwidth Product		1	MHz
ϕm	Phase Margin		70	Deg
G_m	Gain Margin		15	dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 1V f = 100kHz	40 30	nV/$\sqrt{Hz}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_O = $1V_{PP}$	0.069	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Applies to both single supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = $(T_{J(MAX)} - T_A)\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

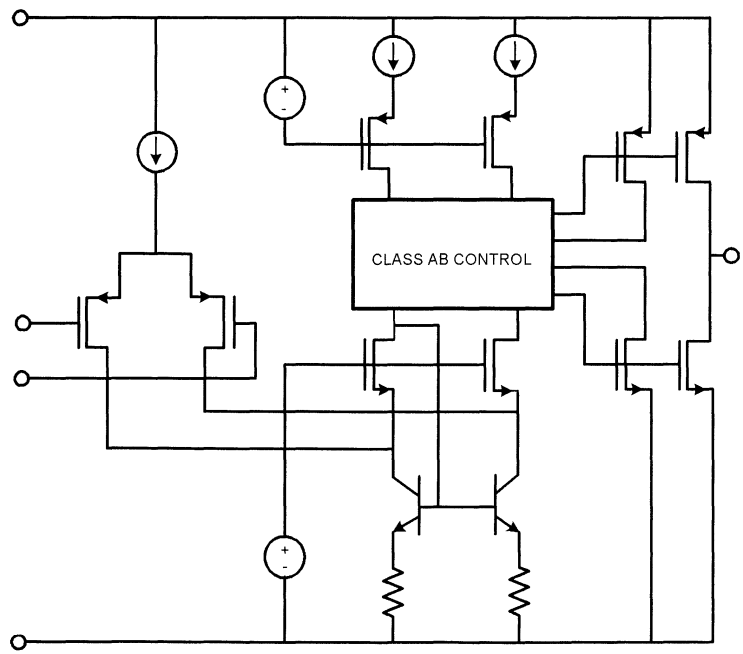
Note 4: Typical value represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Simplified Schematic



20019302

National Semiconductor

LMV321/LMV358/LMV324 Single/Dual/Quad General Purpose, Low Voltage, Rail-to-Rail Output Operational Amplifiers

General Description

The LMV358/324 are low voltage (2.7–5.5V) versions of the dual and quad commodity op amps, LM358/324, which currently operate at 5–30V. The LMV321 is the single version.

The LMV321/358/324 are the most cost effective solutions for the applications where low voltage operation, space saving and low price are needed. They offer specifications that meet or exceed the familiar LM358/324. The LMV321/358/324 have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratio, achieving 1 MHz of bandwidth and 1 V/μs of slew rate with low supply current.

The LMV321 is available in space saving SC70-5, which is approximately half the size of SOT23-5. The small package saves space on pc boards, and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with National's advanced submicron silicon-gate BiCMOS process. The LMV321/358/324 have bipolar input and output stages for improved noise performance and higher output current drive.

Features

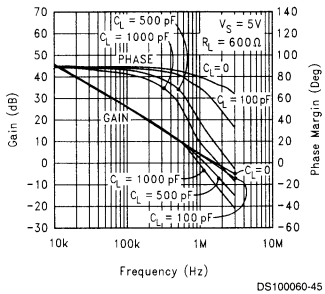
(For V^+ = 5V and V^- = 0V, Typical Unless Otherwise Noted)

- Guaranteed 2.7V and 5V Performance
- No Crossover Distortion
- Space Saving Package — SC70-5 2.0x2.1x1.0mm
- Industrial Temp.Range — −40°C to +85°C
- Gain-Bandwidth Product — 1MHz
- Low Supply Current
  - LMV321 — 130μA
  - LMV358 — 210μA
  - LMV324 — 410μA
- Rail-to-Rail Output Swing @ 10kΩ Load — V^+−10mV, V^-+65mV
- V_{CM} — −0.2V to V^+−0.8V

Applications

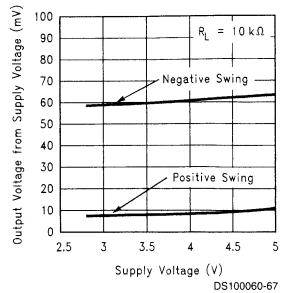
- Active Filters
- General Purpose Low Voltage Applications
- General Purpose Portable Devices

Gain and Phase vs Capacitive Load



DS100060-45

Output Voltage Swing vs Supply Voltage



DS100060-67

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	
LMV358/324	2000V
LMV321	900V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Output Short Circuit to V^+	(Note 3)
Output Short Circuit to V^-	(Note 4)
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temp. Range	−65°C to 150°C
Junction Temp. (T_j, max) (Note 5)	150°C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.5V
Temperature Range	
LMV321, LMV358, LMV324	$-40°C \le T_J \le 85°C$
Thermal Resistance (θ_{JA})(Note 10)	
5-pin SC70-5	478°C/W
5-pin SOT23-5	265°C/W
8-Pin SOIC	190°C/W
8-Pin MSOP	235°C/W
14-Pin SOIC	145°C/W
14-Pin TSSOP	155°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, $V_O = V^+/2$ and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_{OS}	Input Offset Voltage		1.7	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/°C
I_B	Input Bias Current		11	250	nA max
I_{OS}	Input Offset Current		5	50	nA max
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 1.7V$	63	50	dB min
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$, V_O = 1V	60	50	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR≥50dB	−0.2	0	V min
			1.9	1.7	V max
V_O	Output Swing	R_L = 10kΩ to 1.35V	V^+ -10	V^+ -100	mV min
			60	180	mV max
I_S	Supply Current	LMV321	80	170	µA max
		LMV358 Both amplifiers	140	340	µA max
		LMV324 All four amplifiers	260	680	µA max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
GBWP	Gain-Bandwidth Product	C_L = 200 pF	1		MHz
Φ_m	Phase Margin		60		Deg
G_m	Gain Margin		10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	46		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.17		$\frac{pA}{\sqrt{Hz}}$

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_{OS}	Input Offset Voltage		1.7	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/°C
I_B	Input Bias Current		15	250 **500**	nA max
I_{OS}	Input Offset Current		5	50 **150**	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	65	50	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V V_{CM} = 1V	60	50	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR≥50dB	−0.2	0	V min
			4.2	4	V max
A_V	Large Signal Voltage Gain (Note 8)	R_L = 2kΩ	100	15 **10**	V/mV min
V_O	Output Swing	R_L = 2kΩ to 2.5V	V^+ -40	V^+ -300 **V^+ -400**	mV min
			120	300 **400**	mV max
		R_L = 10kΩ to 2.5V	V^+ -10	V^+ -100 **V^+ -200**	mV min
			65	180 **280**	mV max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V	60	5	mA min
		Sinking, V_O = 5V	160	10	mA min
I_S	Supply Current	LMV321	130	250 **350**	µA max
		LMV358 Both amplifiers	210	440 **615**	µA max
		LMV324 All four amplifiers	410	830 **1160**	µA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
SR	Slew Rate	(Note 9)	1		V/μs
GBWP	Gain-Bandwidth Product	C_L = 200 pF	1		MHz
Φ_m	Phase Margin		60		Deg
G_m	Gain Margin		10		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz,	39		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.21		$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 200 pF.

Note 3: Shorting output to V^+ will adversely affect reliability.

Note 4: Shorting output to V^- will adversely affect reliability.

Note 5: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 6: Typical values represent the most likely parametric norm.

Note 7: All limits are guaranteed by testing or statistical analysis.

Note 8: R_L is connected to V^-. The output voltage is $0.5V \le V_O \le 4.5V$.

Note 9: Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Note 10: All numbers are typical, and apply for packages soldered directly onto a PC board in still air.

National Semiconductor

LMV710 and LMV711
Low Power, RRIO Operational Amplifiers with High Output Current Drive and Shutdown Option

General Description

The LMV710 and LMV711 are BiCMOS operational amplifiers with a CMOS input stage. Both devices have greater than RR input common mode voltage range, rail-to-rail output and high output current drive. They offer a bandwidth of 5MHz and a slew rate of 5V/µs.

On the LMV711, a separate shutdown pin can be used to disable the device and reduces the supply current to 0.2µA (typical). The LMV711 features a turn on time of less than 10µs. It is an ideal solution for power sensitive applications, such as cellular phone, pager, palm computer, etc.

The LMV710 is offered in the space saving SOT23-5 Tiny package. The LMV711 is offered in the space saving SOT23-6 Tiny package.

The LMV710/711 are designed to meet the demands of low power, low cost, and small size required by cellular phones and similar battery powered portable electronics.

Features

(For 5 Supply, Typical Unless Otherwise Noted).

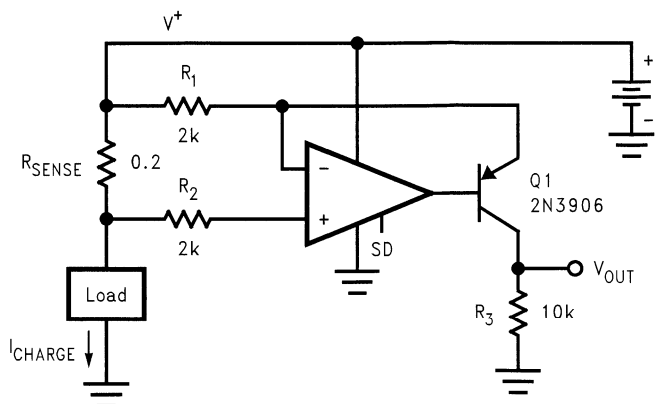
- Low offset voltage 3mV, max
- Gain-bandwidth product 5MHz, typ
- Slew rate 5V/µs, typ
- Space saving packages SOT23-5 and SOT23-6
- Turn on time from shutdown <10µs
- Industrial temperature range −40°C to +85°C
- Supply current in shutdown mode 0.2µA, typ
- Guaranteed 2.7V and 5V Performance
- Unity gain stable
- Rail-to-rail input and output
- Capable of driving 600Ω load

Applications

- Wireless phones
- GSM/TDMA/CDMA power amp control
- AGC, RF power detector
- Temperature compensation
- Wireless LAN
- Bluetooth
- HomeRF

Typical Application

High Side Current Sensing



$$V_{OUT} = \frac{R_{SENSE} \bullet R_3}{R_1} \bullet I_{Charge} = 1\Omega \bullet I_{Charge}$$

DS101325-13

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Voltage at Input/Output Pin	(V^+) + 0.4V (V^-) − 0.4V
Supply Voltage $(V^+ - V^-)$	5.5V
Output Short Circuit to V^+	(Note 3)
Output Short Circuit to V^-	(Note 4)
Current at Input Pin	± 10mA
Mounting Temp.	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature(T_{JMAX}) (Note 5)	150°C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.0V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal Resistance (θ_{JA})	
MF05A Package, 5-Pin SOT23-5	265 °C/W
MF06A package, 6-Pin SOT23-6	265 °C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 6)	Limits (Note 7)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V & V_{CM} = 1.85V	0.4	3 **3.2**	mV max
I_B	Input Bias Current		4		pA
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 2.7V$	75	50 **45**	dB min
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$, V_{CM} = 0.85V	110	70 **68**	dB min
		$2.7V \le V^+ \le 5V$, V_{CM} = 1.85V	95	70 **68**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V
			3	2.9	
I_{SC}	Output Short Circuit Current	Sourcing V_O =0V	28	15 **12**	mA min
		Sinking V_O = 2.7V	40	25 **22**	mA min
V_O	Output Swing	R_L = 10kΩ to 1.35V	2.68	2.62 **2.60**	V min
			0.01	0.12 **0.15**	V max
		R_L = 600Ω to 1.35V	2.55	2.52 **2.50**	V min
			0.05	0.23 **0.30**	V max
V_O (SD)	Output Voltage Level in Shutdown Mode		50	200	mV
I_S	Supply Current	ON Mode	1.22	1.7 **1.9**	mA max
		Shutdown Mode, V_{SD} = 0V	0.002	10	µA

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 6)	Limits (Note 7)	Units
A_V	Large Signal Voltage	Sourcing R_L = 10kΩ V_O = 1.35V to 2.3V	115	80 **76**	dB min
		Sinking R_L = 10kΩ V_O = 0.4V to 1.35V	113	80 **76**	dB min
		Sourcing R_L = 600Ω V_O = 1.35V to 2.2V	110	80 **76**	dB min
		Sinking R_L = 600Ω V_O = 0.5V to 1.35V	100	80 **76**	dB min
SR	Slew Rate	(Note 8)	5		V/μs
GBWP	Gain-Bandwidth Product		5		MHz
ϕ_m	Phase Margin		60		Deg
T_{ON}	Turn-on Time from Shutdown		<10		μs
V_{SD}	Shutdown Pin Voltage Range	On Mode	1.5 to 2.7	2.4 to 2.7	V
		Shutdown Mode	0 to 1	0 to 0.8	V
e_n	Input-Referred Voltage Noise	f = 1kHz	20		$\frac{nV}{\sqrt{Hz}}$

3.2V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 3.2V, V^- = 0V, V_{CM} = 1.6V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_O	Output Swing	I_O = 6.5mA	3.0	2.95 **2.92**	V min
			0.01	0.18 **0.25**	V max

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 6)	Limits (Note 7)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V & V_{CM} = 1.85V	0.4	3 **3.2**	mV max
I_B	Input Bias Current		4		pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	70	50 **48**	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 0.85V	110	70 **68**	dB min
		2.7V ≤ V^+ ≤ 5V, V_{CM} = 1.85V	95	70 **68**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	–0.2	V
			5.3	5.2	

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.5V, and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 6)	Limits (Note 7)	Units
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V	35	25 **21**	mA min
		Sinking V_O = 5V	40	25 **21**	mA min
V_O	Output Swing	R_L = 10kΩ to 2.5V	4.98	4.92 **4.90**	V min
			0.01	0.12 **0.15**	V max
		R_L = 600Ω to 2.5V	4.85	4.82 **4.80**	V min
			0.05	0.23 **0.3**	V max
V_O (SD)	Output Voltage Level in Shutdown Mode		50	200	mV
I_S	Supply Current	On Mode	1.17	1.7 **1.9**	mA max
		Shutdown Mode	0.2	10	µA
A_V	Large Signal Voltage Gain	Sourcing R_L = 10kΩ V_O = 2.5V to 4.6V	123	80 **76**	dB min
		Sinking R_L = 10kΩ V_O = 0.4V to 2.5V	120	80 **76**	dB min
		Sourcing R_L = 600Ω V_O = 2.5V to 4.5V	110	80 **76**	dB min
		Sinking R_L = 600Ω V_O = 0.5V to 2.5V	118	80 **76**	dB min
SR	Slew Rate	(Note 8)	5		V/µs
GBWP	Gain-Bandwidth Product		5		MHz
ϕ_m	Phase Margin		60		Deg
T_{ON}	Turn-on Time from Shutdown		<10		µs
V_{SD}	Shutdown Pin Voltage Range	ON Mode	2 to 5	2.4 to 5	V
		Shutdown Mode	0 to 1.5	0 to 0.8	
e_n	Input-Referred Voltage Noise	f = 1kHz	20		$\frac{nV}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100pF. Machine model, 0Ω in series with 100pF.

Note 3: Shorting circuit output to V^+ will adversely affect reliability.

Note 4: Shorting circuit output to V^- will adversely affect reliability.

Note 5: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 6: Typical values represent the most likely parametric norm.

Note 7: All limits are guaranteed by testing or statistical analysis.

Note 8: Number specified is the slower of the positive and negative slew rates.

National Semiconductor

LMV712
Low Power, Low Noise, High Output, RRIO Dual Operational Amplifier with Independent Shutdown

General Description

The LMV712 duals are high performance BiCMOS operational amplifiers intended for applications requiring Rail-to-Rail inputs combined with speed and low noise. They offer a bandwidth of 5MHz and a slew rate of 5V/µs and can handle capacitive loads of up to 200pF without oscillation.

The LMV712 offers two independent shutdown pins. This feature allows disabling of each device separately and reduces the supply current to less than 1µA typical. The output voltage rapidly ramps up smoothly with no glitch as the amplifier comes out of the shutdown mode.

The LMV712 with the shutdown feature is offered in space saving 10-Bump micro SMD and 10 pin Leadless Leadframe Package (LLP) packages. It is also offered in 10 lead MSOP package. These packages are designed to meet the demands of small size, low power, and low cost required by cellular phones and similar battery operated portable electronics.

Features

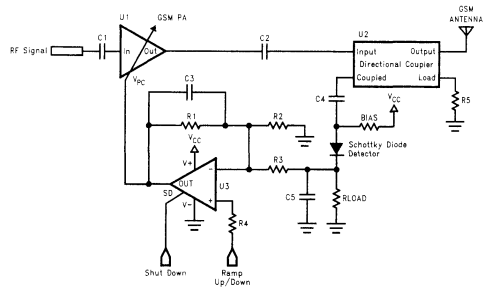
(Typical Unless Otherwise Noted)

- 5 MHz GBP
- Slew rate 5 V/µs
- Low noise 20nV/ $\sqrt{Hz}$
- Supply current 1.22mA/channel
- V_{OS} < 3mV max.
- Low supply voltage 2.7V to 5V.
- Rail-to-Rail inputs and outputs.
- Unity gain stable.
- Small package: 10-Pin LLP, 10-Pin MSOP and 10-Bump micro SMD
- 1.5µA shutdown I_{CC}
- 2.2µs turn on

Applications

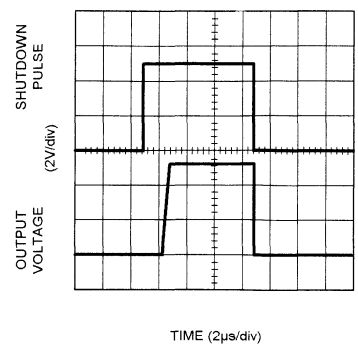
- Power amplifier control loop
- Cellular phones
- Portable equipment
- Wireless LAN
- Radio systems
- Cordless phones

Typical Application Circuit



P.A. Control Loop

Output Waveform vs. Shutdown Pulse



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	150V
Human Body Model	1.5kV
Differential Input Voltage	±Supply Voltage
Voltage at Input/Output Pin	(V^+) +0.4V to (V^-) −0.4V
Supply Voltage $(V^+ - V^-)$	5.5V
Output Short Circuit V^+	(Note 3)
Output Short Circuit V^-	(Note 3)
Current at Input Pin	±10mA
Current at Output Pin	±50mA
Storage Temp Range	−65°C to 150°C
Mounting Temperature	
Infrared or Convection (20 sec)	235°C
Junction Temperature T_{JMAX} (Note 4)	150°C

Recommended Operating Conditions (Note 1)

Supply Voltage	2.7V to 5V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal Resistance	
10-Pin MSOP	235°C/W
10-Pin LLP	53.4°C/W
10-Bump micro SMD	196°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.35V$ and $T_A = 25°C$ and $R_L > 1M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	$V_{CM} = 0.85V$ and $V_{CM} = 1.85V$		0.4	3 **3.2**	mV
I_B	Input Bias Current			5.5	115 **130**	pA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$	50 **45**	75		dB
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$, $V_{CM} = 0.85V$	70 **68**	90		dB
		$2.7V \le V^+ \le 5V$, $V_{CM} = 1.85V$	70 **68**	90		dB
CMVR	Common Mode Voltage Range	For CMRR ≥ 50dB		−0.3	−0.2	V
			2.9	3		V
I_{SC}	Output Short Circuit Current	Sourcing $V_O = 0V$	15 **12**	25		mA
		Sinking $V_O = 2.7V$	25 **22**	50		mA
V_O	Output Swing	$R_L = 10k\Omega$ to 1.35V	2.62 **2.60**	2.68		V
				0.01	0.12 **0.15**	V
		$R_L = 600\Omega$ to 1.35V	2.52 **2.50**	2.55		V
				0.05	0.23 **0.30**	V
V_O(SD)	Output Voltage in Shutdown			10	200	mV
I_S	Supply Current per Channel	On Mode		1.22	1.7 **1.9**	mA
		Shutdown Mode		0.12	1.5 **2.0**	uA

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes. (Continued)

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 10kΩ V_O = 1.35V to 2.3V	80 **76**	115		dB
		Sinking R_L = 10kΩ V_O = 0.4V to 1.35V	80 **76**	113		dB
		Sourcing R_L = 600Ω V_O = 1.35V to 2.2V	80 **76**	97		dB
		Sinking R_L = 600Ω V_O = 0.5V to 1.35V	80 **76**	100		dB
V_{SD}	Shutdown Pin Voltage Range	On Mode	2.4 to 2.7	2.0 to 2.7		V
		Shutdown Mode	0 to 0.8	0 to 1		V
GBWP	Gain-Bandwidth Product			5		MHz
SR	Slew Rate	(Note 7)		5		V/µs
ϕ_m	Phase Margin			60		Deg
e_n	Input Referred Voltage Noise	f = 1kHz		20		nV/$\sqrt{Hz}$
T_{ON}	Turn-On Time from Shutdown			2.2	4 **4.6**	µs
	Turn-On Time from Shutdown (micro SMD)		6 **8**			µs

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for V^+ =5V, V^- = 0V, V_{CM} = 2.5V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0.85V and V_{CM} = 1.85V		0.4	3 **3.2**	mV
I_B	Input Bias Current			5.5	115 **130**	pA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 5V	50 **45**	80		dB
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V, V_{CM} = 0.85V	70 **68**	90		dB
		2.7V ≤ V^+ ≤ 5V, V_{CM} = 1.85V	70 **68**	90		dB
CMVR	Common Mode Voltage Range	For CMRR ≥ 50dB		−0.3	−0.2	V
			5.2	5.3		V
I_{SC}	Output Short Circuit Current	Sourcing V_O = 0V	20 **18**	35		mA
		Sinking V_O = 5V	25 **21**	50		mA

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for V^+ =5V, V^- = 0V, V_{CM} = 2.5V and T_A = 25°C and R_L > 1MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_O	Output Swing	R_L = 10kΩ to 2.5V	4.92 **4.90**	4.98		V
				0.01	0.12 **0.15**	V
		R_L = 600Ω to 2.5V	4.82 **4.80**	4.85		V
				0.05	0.23 **0.30**	V
V_O(SD)	Output Voltage in Shutdown			10	200	mV
I_S	Supply Current per Channel	On Mode		1.17	1.7 **1.9**	mA
		Shutdown Mode		0.12	1.5 **2.0**	uA
A_{VOL}	Large Signal Voltage Gain	Sourcing R_L = 10kΩ V_O = 2.5V to 4.6V	80 **76**	130		dB
		Sinking R_L = 10kΩ V_O = 0.4V to 2.5V	80 **76**	130		dB
		Sourcing R_L = 600Ω V_O = 2.5V to 4.6V	80 **76**	110		dB
		Sinking R_L = 600Ω V_O = 0.4V to 2.5V	80 **76**	107		dB
V_{SD}	Shutdown Pin Voltage Range	On Mode	4.5 to 5	3.5 to 5		V
		Shutdown Mode	0 to 0.8	0 to 1.5		V
GBWP	Gain-Bandwidth Product			5		MHz
SR	Slew Rate	(Note 7)		5		V/µs
ϕ_m	Phase Margin			60		Deg
e_n	Input Referred Voltage Noise	f = 1kHz		20		nV/$\sqrt{Hz}$
T_{ON}	Turn-On Time for Shutdown			1.6	4 **4.6**	µs
	Turn-On Time for Shutdown (micro SMD)		6 **8**			µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model: 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 100pF.

Note 3: Shorting circuit output to either V^+ or V^- will adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Number specified is the slower of the positive and negative slew rates.

National Semiconductor

LMV721/LMV722
10MHz, Low Noise, Low Voltage, and Low Power Operational Amplifier

General Description

The LMV721 (Single) and LMV722 (Dual) are low noise, low voltage, and low power op amps, that can be designed into a wide range of applications. The LMV721/LMV722 has a unity gain bandwidth of 10MHz, a slew rate of 5V/us, and a quiescent current of 930uA/amplifier at 2.2V.

The LMV721/722 are designed to provide optimal performance in low voltage and low noise systems. They provide rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5mV (Over Temp.) for the LMV721/LMV722. Their capacitive load capability is also good at low supply voltages. The operating range is from 2.2V to 5.5V.

The chip is built with National's advanced Submicron Silicon-Gate BiCMOS process. The single version, LMV721, is available in 5 pin SOT23-5 and a SC-70 (new) package. The dual version, LMV722, is available in a SO-8, MSOP-8 and 8-pin LLP package.

Features

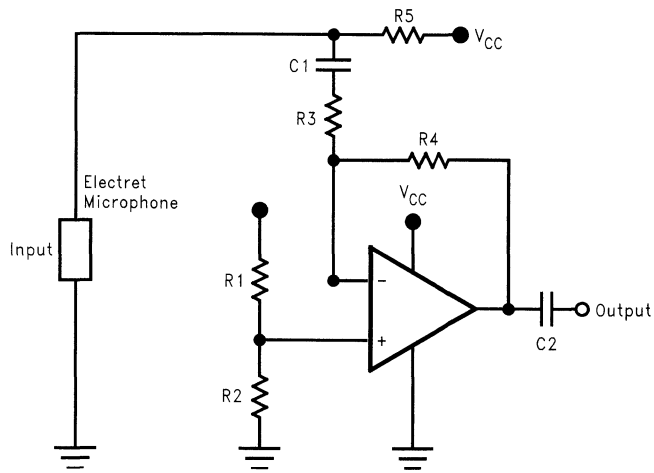
(For Typical, 5 V Supply Values; Unless Otherwise Noted)

- Guaranteed 2.2V and 5.0V Performance
- Low Supply Current LMV721/2 930µA/amplifier @2.2V
- High Unity-Gain Bandwidth 10MHz
- Rail-to-Rail Output Swing
  @600Ω load 120mV from either rail at 2.2V
  @2kΩ load 50mV from either rail at 2.2V
- Input Common Mode Voltage Range Includes Ground
- Silicon Dust™, SC70-5 Package 2.0x2.0x1.0 mm
- Miniature packaging: LLP-8 2.5mm x 3mm x 0.8mm
- Input Voltage Noise 9 nV/$\sqrt{Hz}$ @ f = 1KHz

Applications

- Cellular an Cordless Phones
- Active Filter and Buffers
- Laptops and PDAs
- Battery Powered Electronics

A Battery Powered Microphone Preamplifier



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2000V
Machine Model	200V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Storage Temp. Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 3)

Supply Voltage	2.2V to 5.0V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal Resistance (θ_{JA})	
Silicon Dust SC70-5 Pkg	440°C/W
Tiny SOT23-5 Pkg	265 °C/W
SO Pkg, 8-pin Surface Mount	190°C/W
MSOP Pkg, 8-Pin Mini Surface Mount	235 °C/W
SO Pkg, 14-Pin Surface Mount	145°C/W
LLP pkg, 8-Pin	58.2°C/W

2.2V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.2V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1$ MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		0.02	3 **3.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		0.6		µV/°C
I_B	Input Bias Current		260		nA
I_{OS}	Input Offset Current		25		nA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 1.3V$	88	70 **64**	dB min
PSRR	Power Supply Rejection Ratio	$2.2V \le V^+ \le 5V$, V_O = 0 V_{CM} = 0	90	70 **64**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	−0.30		V
			1.3		V
A_V	Large Signal Voltage Gain	R_L=600Ω V_O = 0.75V to 2.00V	81	75 **60**	dB min
		R_L= 2kΩ V_O = 0.50V to 2.10V	84	75 **60**	dB min
V_O	Output Swing	R_L = 600Ω to $V^+/2$	2.125	2.090 **2.065**	V min
			0.061	0.110 **0.135**	V max
		R_L = 2kΩ to $V^+/2$	2.177	2.150 **2.125**	V min
			0.026	0.050 **0.075**	V max
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ± 0.5V	14.9	10.0 **5.0**	mA min
		Sinking, V_O = 2.2V V_{IN}(diff) = ± 0.5V	23.8	15.0 **5.0**	mA min
I_S	Supply Current	LMV721	0.93	1.2 **1.5**	mA max
		LMV722	1.64	2.2 **2.6**	

2.2V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.2V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	4.9	V/μs
GBW	Gain-Bandwidth Product		10	MHz
Φ_m	Phase Margin		67.4	Deg
G_m	Gain Margin		-9.8	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	9	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.3	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz A_V = 1 R_L = 600Ω, V_O = 500 mV_{PP}	0.004	%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		-0.08	3 **3.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		0.6		μV/°C
I_B	Input Bias Current		260		nA
I_{OS}	Input Offset Current		25		nA
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.1V	89	70 **64**	dB min
PSRR	Power Supply Rejection Ratio	2.2V ≤ V^+ ≤ 5.0V, V_O = 0 V_{CM} = 0	90	70 **64**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.30		V
			4.1		V
A_V	Large Signal Voltage Gain	R_L = 600Ω V_O = 0.75V to 4.80V	87	80 **70**	dB min
		R_L = 2kΩ, V_O = 0.70V to 4.90V,	94	85 **70**	dB min
V_O	Output Swing	R_L = 600Ω to $V^+/2$	4.882	4.840 **4.140**	V min
			0.105	0.160 **0.185**	V max
		R_L = 2kΩ to $V^+/2$	4.962	4.940 **4.915**	V min
			0.046	0.080 **0.105**	V max
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	52.6	25.0 **12.0**	mA min
		Sinking, V_O = 5V V_{IN}(diff) = ±0.5V	23.7	15.0 **8.5**	mA min
I_S	Supply Current	LMV721	1.03	1.4 **1.7**	mA max
		LMV722	1.83	2.4 **2.8**	

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	5.25	V/μs min
GBW	Gain-Bandwidth Product		10.0	MHz
Φ_m	Phase Margin		72	Deg
G_m	Gain Margin		−11	dB
e_n	Input-Related Voltage Noise	f = 1 kHz	8.5	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.2	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = 1 R_L = 600Ω, V_O = 1 V_{PP}	0.001	%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Connected as voltage follower with 1V step input. Number specified is the slower of the positive and negative slew rate.

National Semiconductor

LMV751
Low Noise, Low Vos, Single Op Amp

General Description

The LMV751 is a high performance CMOS operational amplifier intended for applications requiring low noise and low input offset voltage. It offers modest bandwidth of 4.5MHz for very low supply current and is unity gain stable.

The output stage is able to drive high capacitance, up to 1000pF and source or sink 8mA output current.

It is supplied in the space saving SOT23-5 Tiny package.

The LMV751 is designed to meet the demands of small size, low power, and high performance required by cellular phones and similar battery operated portable electronics.

Features

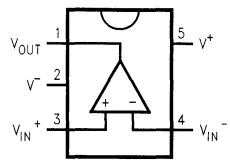
- Low Noise 6.5nV Rt-Hz typ.
- Low Vos (0.05mV typ.)
- Wideband 4.5MHz GBP typ.
- Low Supply Current 500uA typ.
- Low Suppy Voltage 2.7V to 5.0V
- Ground-referenced Inputs
- Unity gain stable
- Small Package

Applications

- Cellular Phones
- Portable Equipment
- Radio Systems

Connection Diagram

SOT23-5

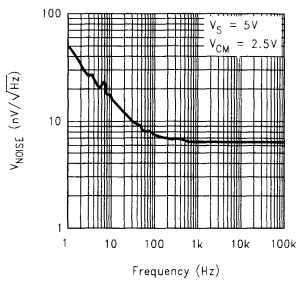


Top View

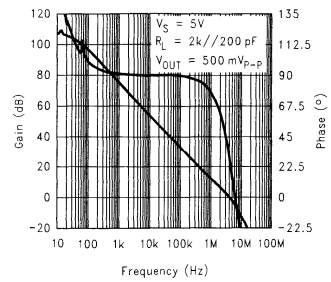
Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
5-Pin SOT23-5	LMV751M5	A32A	1k Units Tape and Reel	MA05B
	LMV751M5X	A32A	3k units Tape and Reel	MA05B

Voltage Noise



Gain/Phase



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD tolerance (Note 3)	
Human Body Model	2000V
Machine Model	200V
Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Lead Temperature (Soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (T_J) (Note 4)	150°C

Recommended Operating Conditions

Supply Voltage	2.7V to 5.0V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal resisance (θ_{JA}) (Note 6)	
M5 Package, SOT23-5	274°C/W

2.7V Electrical Characteristics

$V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = 1.35V$, $T_A = 25°C$ unless otherwise stated. **Boldface limits** apply over theTemperature Range.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 2)	Units
V_{OS}	Input Offset Voltage		0.05	1.0 **1.5**	mV max
V_{CM}	Input common-Mode Voltage Range	For CMRR ≥ 50dB		0	V min
			1.4	1.3	V max
CMRR	Common Mode Rejection Ratio	$0V < V_{CM} < 1.3V$	100	85 **70**	dB min
PSRR	Power Supply Rejection Ratio	V^+ =2.7V to 5.0V	107	85 **70**	dB min
I_S	Supply Current		0.5	0.7 **0.75**	mA max
I_{IN}	Input Current		1.5	100	pA max
I_{OS}	Input Offset Current		0.2		pA
A_{VOL}	Voltage Gain	R_L = 10k Connect to $V^+/2$ V_O = 0.2V to 2.2V	120	110 **95**	dB min
		R_L = 2k Connect to $V^+/2$ V_O = 0.2V to 2.2V	120	100 **85**	
V_O	Positive Voltage Swing	R_L = 10k Connect to $V^+/2$	2.62	2.54 **2.52**	V min
		R_L = 2k Connect to $V^+/2$	2.62	2.54 **2.52**	
V_O	NegativeVoltage Swing	R_L = 10k Connect to $V^+/2$	78	140 **160**	mV max
		R_L = 2k Connect to $V^+/2$	78	140 **160**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN}(diff) = ±0.5V	12	6.0 **1.5**	mA min
		Sinking,V_O = 2.7V V_{IN}(diff) = ±0.5V	11	6.0 **1.5**	
e_n (10Hz)	Input Referred Voltage Noise		15.5		$nV/\sqrt{Hz}$
e_n (1kHz)	Input Referred Voltage Noise		7		$nV/\sqrt{Hz}$

2.7V Electrical Characteristics (Continued)

V^+ = 2.7V, V^- = 0V, V_{CM} = 1.35V, T_A = 25°C unless otherwise stated. **Boldface limits** apply over theTemperature Range.

Symbol	Parameter	Condition	Typ (Note 5)	Limit (Note 2)	Units
e_n (30kHz)	Input Referred Voltage Noise		7	10	nV/$\sqrt{Hz}$ max
I_N(1kHz)	Input Referred Current Noise		0.01		pA/$\sqrt{Hz}$
GBW	Gain-Bandwidth Product		4.5	2	MHZ min
SR	Slew Rate		2		V/μs

5.0V Electrical Characteristics

V^+ = 5.0V, V^- = 0V, V_{CM} = 2.5V, T_A = 25°C unless otherwise stated.**Boldface limits** apply over theTemperature Range.

Symbol	Parameter		Typ (Note 5)	Limit (Note 2)	Units
V_{OS}	Input Offset Voltage		0.05	1.0 **1.5**	mV max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 3.6V	103	85 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		0	V min
			3.7	3.6	V max
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5.0V	107	85 **70**	dB min
I_S	Supply Current		0.6	0.8 **0.85**	mA max
I_{IN}	Input Current		1.5	100	pA max
I_{OS}	Input offset Current		0.2		pA
A_{VOL}	Voltage Gain	R_L = 10k Connect to $V^+/2$ V_O = 0.2V to 4.5V	120	110 **95**	db min
		R_L = 2k Connect to $V^+/2$ V_O = 0.2V to 4.5V	120	100 **85**	
V_O	Positive Voltage Swing	R_L = 10k Connect to $V^+/2$	4.89	4.82 **4.80**	V min
		R_L = 2k Connect to $V^+/2$	4.89	4.82 **4.80**	
V_O	Negative Voltage Swing	R_L = 10k Connect to $V^+/2$	86	160 **180**	mV max
		R_L = 2k Connect to $V^+/2$	86	160 **180**	
I_O	Output Current	Sourcing, V_O = 0V V_{IN} (diff) = ±0.5V	15	8.0 **2.5**	mA min
		Sinking, V_O = 5V V_{IN} (diff) = ±0.5V	20	8.0 **2.5**	
e_n (10Hz)	Input Referred Voltage Noise		15		nV/$\sqrt{Hz}$
e_n (1kHz)	Input Referred Voltage Noise		6.5		nV/$\sqrt{Hz}$

5.0V Electrical Characteristics (Continued)

V^+ = 5.0V, V^- = 0V, V_{CM} = 2.5V, T_A = 25°C unless otherwise stated. **Boldface limits** apply over theTemperature Range.

Symbol	Parameter		Typ (Note 5)	Limit (Note 2)	Units
e_n (30kHz)	Input Referred Voltage Noise		6.5	10	$nV/\sqrt{Hz}$ max
I_N (1kHz)	Input Referred Current Noise		0.01		$pA/\sqrt{Hz}$
GBW	Gain-Bandwidth Product		5	2	MHz min
SR	Slew Rate		2.3		V/μs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: All limits are guaranteed by testing or statistical analysis

Note 3: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 1000pF.

Note 4: The maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All numbers are typical, and apply to packages soldered directly onto PC board in still air.

National Semiconductor

LMV821 Single/LMV822 Dual/LMV824 Quad Low Voltage, Low Power, R-to-R Output, 5 MHz Op Amps

General Description

The LMV821/LMV822/LMV824 bring performance and economy to low voltage / low power systems. With a 5 MHz unity-gain frequency and a guaranteed 1.4 V/µs slew rate, the quiescent current is only 220 µA/amplifier (2.7 V). They provide rail-to-rail (R-to-R) output swing into heavy loads (600 Ω Guarantees). The input common-mode voltage range includes ground, and the maximum input offset voltage is 3.5mV (Guaranteed). They are also capable of comfortably driving large capacitive loads (refer to the application notes section).

The LMV821 (single) is available in the ultra tiny SC70-5 package, which is about half the size of the previous title holder, the SOT23-5.

Overall, the LMV821/LMV822/LMV824 (Single/Dual/Quad) are low voltage, low power, performance op amps, that can be designed into a wide range of applications, at an economical price.

Features

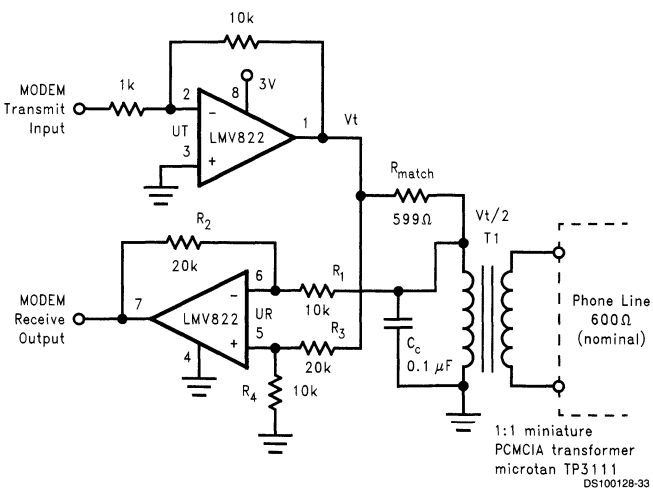
(For Typical, 5 V Supply Values; Unless Otherwise Noted)

- Ultra Tiny, SC70-5 Package 2.0 x 2.0 x 1.0 mm
- Guaranteed 2.5 V, 2.7 V and 5 V Performance
- Maximum VOS 3.5 mV (Guaranteed)
- VOS Temp. Drift 1 uV/° C
- GBW product @ 2.7 V 5 MHz
- I_{Supply} @ 2.7 V 220 µA/Amplifier
- Minimum SR 1.4 V/us (Guaranteed)
- CMRR 90 dB
- PSRR 85 dB
- Rail-to-Rail (R-to-R) Output Swing
  - — @600 Ω Load 160 mV from rail
  - — @10 kΩ Load 55 mV from rail
- V_{CM} @ 5 V -0.3 V to 4.3 V
- Stable with High Capacitive Loads (Refer to Application Section)

Applications

- Cordless Phones
- Cellular Phones
- Laptops
- PDAs
- PCMCIA

Telephone-line Transceiver for a PCMCIA Modem Card



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	
LMV822/824	2000V
LMV821	1500V
Differential Input Voltage	± Supply Voltage
Supply Voltage (V^+–V^-)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	2.5V to 5.5V
Temperature Range	
LMV821, LMV822, LMV824	−40°C ≤T_J ≤85°C
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package 5-Pin Surface Mount	440 °C/W
Tiny SOT23-5 Package 5-Pin Surface Mount	265 °C/W
SO Package, 8-Pin Surface Mount	190 °C/W
MSOP Package, 8-Pin Mini Surface Mount	235 °C/W
SO Package, 14-Pin Surface Mount	145 °C/W
TSSOP Package, 14-Pin	155 °C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3.5 **4**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		30	90 **140**	nA max
I_{OS}	Input Offset Current		0.5	30 **50**	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.7V	85	70 **68**	dB min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V	85	75 **70**	dB min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V	85	73 **70**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V max
			2.0	1.9	V min
A_V	Large Signal Voltage Gain	Sourcing, R_L = 600Ω to 1.35V, V_O = 1.35V to 2.2V	100	90 **85**	dB min
		Sinking, R_L = 600Ω to 1.35V, V_O = 1.35V to 0.5V	90	85 **80**	dB min
		Sourcing, R_L = 2kΩ to 1.35V, V_O = 1.35V to 2.2V	100	95 **90**	dB min
		Sinking, R_L = 2kΩ to 1.35, V_O = 1.35 to 0.5V	95	90 **85**	dB min

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_O	Output Swing	V^+ = 2.7V, R_L= 600Ω to 1.35V	2.58	2.50	V
				2.40	min
			0.13	0.20	V
				0.30	max
		V^+ = 2.7V, R_L= 2kΩ to 1.35V	2.66	2.60	V
				2.50	min
			0.08	0.120	V
				0.200	max
I_O	Output Current	Sourcing, V_O = 0V	16	12	mA
					min
		Sinking, V_O = 2.7V	26	12	mA
					min
I_S	Supply Current	LMV821 (Single)	0.22	0.3	mA
				0.5	max
		LMV822 (Dual)	0.45	0.6	mA
				0.8	max
		LMV824 (Quad)	0.72	1.0	mA
				1.2	max

2.5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.5V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.25V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3.5	mV
				4	max
V_O	Output Swing	V^+ = 2.5V, R_L = 600Ω to 1.25V	2.37	2.30	V
				2.20	min
			0.13	0.20	V
				0.30	max
		V^+ = 2.5V, R_L = 2kΩ to 1.25V	2.46	2.40	V
				2.30	min
			0.08	0.12	V
				0.20	max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	1.5		V/μs
GBW	Gain-Bandwdth Product		5		MHz
Φ_m	Phase Margin		61		Deg.
G_m	Gain Margin		10		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V	28		$\frac{nV}{\sqrt{Hz}}$

2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
i_n	Input-Referred Current Noise	f = 1 kHz	0.1		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01		%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 **Limit** (Note 6)	Units
V_{OS}	Input Offset Voltage		1	3.5	mV
				4.0	max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		40	100	nA
				150	max
I_{OS}	Input Offset Current		0.5	30	nA
				50	max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4.0V	90	72	dB
				70	min
+PSRR	Positive Power Supply Rejection Ratio	1.7V ≤ V^+ ≤ 4V, V^- = 1V, V_O = 0V, V_{CM} = 0V	85	75	dB
				70	min
−PSRR	Negative Power Supply Rejection Ratio	-1.0V ≤ V^- ≤ -3.3V, V^+ = 1.7V, V_O = 0V, V_{CM} = 0V	85	73	dB
				70	min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2	V
					max
			4.3	4.2	V
					min
A_V	Large Signal Voltage Gain	Sourcing, R_L = 600Ω to 2.5V, V_O = 2.5 to 4.5V	105	95	dB
				90	min
		Sinking, R_L = 600Ω to 2.5V, V_O = 2.5 to 0.5V	105	95	dB
				90	min
		Sourcing, R_L = 2kΩ to 2.5V, V_O = 2.5 to 4.5V	105	95	dB
				90	min
		Sinking, R_L = 2kΩ to 2.5, V_O = 2.5 to 0.5V	105	95	dB
				90	min
V_O	Output Swing	V^+ = 5V, R_L = 600Ω to 2.5V	4.84	4.75	V
				4.70	min
			0.17	0.250	V
				.30	max
		V^+ = 5V, R_L = 2kΩ to 2.5V	4.90	4.85	V
				4.80	min
			0.10	0.15	V
				0.20	max

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
I_O	Output Current	Sourcing, V_O = 0V	45	20	mA
				15	min
		Sinking, V_O = 5V	40	20	mA
				15	min
I_S	Supply Current	LMV821 (Single)	0.30	0.4	mA
				0.6	max
		LMV822 (Dual)	0.5	0.7	mA
				0.9	max
		LMV824 (Quad)	1.0	1.3	mA
				1.5	max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = 2V, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMV821/822/824 Limit (Note 6)	Units
SR	Slew Rate	(Note 7)	2.0	1.4	V/μs min
GBW	Gain-Bandwdth Product		5.6		MHz
Φ_m	Phase Margin		67		Deg.
G_m	Gain Margin		15		dB
	Amp-to-Amp Isolation	(Note 8)	135		dB
e_n	Input-Related Voltage Noise	f = 1 kHz, V_{CM} = 1V	24		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.25		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = −2, R_L = 10 kΩ, V_O = 4.1 V_{PP}	0.01		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series wth 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 5V. Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Note 8: Input referred, V^+ = 5V and R_L = 100kΩ connected to 2.5V. Each amp excited in turn with 1 kHz to produce V_O = 3 V_{PP}.

National Semiconductor

LMV921/LMV922/LMV924
Single, Dual and Quad 1.8V, 1MHz, Low Power Operational Amplifiers with Rail-To-Rail Input and Output

General Description

The LMV921 Single/LMV922 Dual/LMV924 Quad are guaranteed to operate from +1.8V to +5.0V supply voltages and have rail-to-rail input and output. This rail-to-rail operation enables the user to make full use of the entire supply voltage range. The input common mode voltage range extends 300mV beyond the supplies and the output can swing rail-to-rail unloaded and within 100mV from the rail with 600Ω load at 1.8V supply. The LMV921/LMV922/LMV924 are optimized to work at 1.8V which make them ideal for portable two-cell battery-powered systems and single cell Li-Ion systems.

The LMV921/LMV922/LMV924 exhibit excellent speed-power ratio, achieving 1MHz gain bandwidth product at 1.8V supply voltage with very low supply current. The LMV921/LMV922/LMV924 are capable of driving 600Ω load and up to 1000pF capacitive load with minimal ringing. The LMV921/LMV922/LMV924's high DC gain of 100dB makes them suitable for low frequency applications.

The LMV921 (Single) is offered in a space saving SC70–5 and SOT23–5 packages. The SC70–5 package is only 2.0X2.1X1.0mm. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellphones and PDAs.

Features

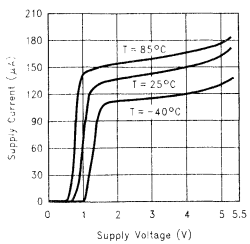
(Typical 1.8V Supply Values; Unless Otherwise Noted)

- Guaranteed 1.8V, 2.7V and 5V specifications
- Rail-to-Rail input & output swing
  - — w/600Ω load — 100 mV from rail
  - — w/2kΩ load — 30 mV from rail
- V_{CM} — 300mV beyond rails
- Supply current — 145µA/amplifier
- Gain bandwidth product — 1MHz
- LMV921 Maximum V_{OS} — 6mV
- 90dB gain w/600Ω load
- LMV921 available in Ultra Tiny, SC70-5 package
- LMV922 available in MSOP-8 package
- LMV924 available in TSSOP-14 package

Applications

- Cordless/cellular phones
- Laptops
- PDAs
- PCMCIA
- Portable/battery-powered electronic Equipment
- Supply current Monitoring
- Battery monitoring

Supply Current vs. Supply Voltage (LMV921)



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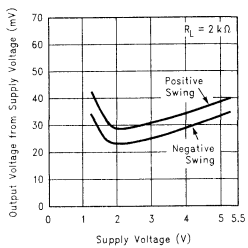
Output Voltage Swing vs. Supply Voltage



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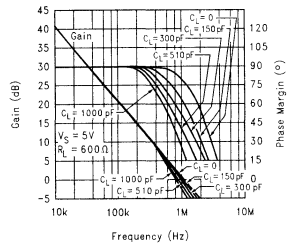
Gain and Phase Margin vs. Frequency



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C
Mounting Temp.	
Infrared or Convection (20 sec)	235°C

Operating Ratings (Note 1)

Supply Voltage	1.5V to 5.0V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal Resistance (θ_{JA})	
Ultra Tiny SC70-5 Package	
5-Pin Surface Mount	440 °C/W
Tiny SOT23-5 Package	
5-Pin Surface Mount	265 °C/W
MSOP Package	
8-Pin Surface Mount	235°C/W
TSSOP Package	
14-Pin Surface Mount	155°C/W
SOIC Package	
8-Pin Surface Mount	175°C/W
14-Pin Surface Mount	127°C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25°C$. $V^+ = 1.8V$, $V^- = 0V$, $V_{CM} = V^+/2$, $V_O = V^+/2$ and $R_L > 1\ M\Omega$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage	LMV921 (Single)	−1.8	6 **8**	mV max
		LMV922 (Dual) LMV924 (Quad)	−1.8	8 **9.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		12	35 **50**	nA max
I_{OS}	Input Offset Current		2	25 **40**	nA max
I_S	Supply Current	LMV921 (Single)	145	185 **205**	µA max
		LMV922 (Dual)	330	400 **550**	
		LMV924 (Quad)	560	700 **850**	
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 0.6V$	82	62 **60**	dB min
		$-0.2V \le V_{CM} \le 0V$ $1.8V \le V_{CM} \le 2.0V$	74	50	
PSRR	Power Supply Rejection Ratio	$1.8V \le V^+ \le 5V$, $V_{CM} = 0.5V$	78	67 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 **0**	V min
			2.15	2.0 **1.8**	V max

1.8V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
A_V	Large Signal Voltage Gain LMV921 (Single)	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	91	77 **73**	dB min
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	95	80 **75**	
	Large Signal Voltage Gain LMV922 (Dual) LMV924 (Quad)	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	79	65 **61**	dB min
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	83	68 **63**	
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ± 100mV	1.7	1.65 **1.63**	V min
			0.075	0.090 **0.105**	V max
		R_L = 2kΩ to 0.9V V_{IN} = ± 100mV	1.77	1.75 **1.74**	V min
			0.025	0.035 **0.040**	V max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	6	4 **3.3**	mA min
		Sinking, V_O = 1.8V V_{IN} = −100mV	10	7 **5**	mA min

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.39	V/μs
GBW	Gain-Bandwidth Product		1	MHz
Φ_m	Phase Margin		60	Deg
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 0.5V	45	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.1	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600kΩ, V_{IN} = 1 V_{PP}	0.089	%
	Amp-to-Amp Isolation	(Note 8)	140	dB

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage	LMV921 (Single)	−1.6	6 **8**	mV max
		LMV922 (Dual) LMV924 (Quad)	−1.6	8 **9.5**	mV max

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		12	35 **50**	nA max
I_{OS}	Input Offset Current		2	25 **40**	nA max
I_S	Supply Current	LMV921 (Single)	147	190 **210**	uA max
		LMV922 (Dual)	380	450 **600**	
		LMV924 (Quad)	580	750 **900**	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 1.5V	84	62 **60**	dB min
		−0.2V ≤ V_{CM} ≤ 0V 2.7V ≤ V_{CM} < 2.9V	73	50	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V, V_{CM} = 0.5V	78	67 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 **0**	V min
			3.050	2.9 **2.7**	V max
A_V	Large Signal Voltage Gain LMV921 (Single)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V	98	80 **75**	dB min
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V	103	83 **77**	
	Large Signal Voltage Gain LMV922 (Dual) LMV924 (Quad)	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V	86	68 **63**	dB min
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V	91	71 **65**	
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ± 100mV	2.62	2.550 **2.530**	V min
			0.075	0.095 **0.115**	V max
		R_L = 2kΩ to 1.35V V_{IN} = ± 100mV	2.675	2.650 **2.640**	V min
			0.025	0.040 **0.045**	V max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	27	20 **15**	mA min
		Sinking, V_O = 2.7V V_{IN} = −100mV	28	22 **16**	mA min

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.41	V/µs

2.7V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
GBW	Gain-Bandwidth Product		1	MHz
Φ_m	Phase Margin		65	Deg.
G_m	Gain Margin		10	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 0.5V	45	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.1	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600kΩ, V_{IN} = 1 V_{PP}	0.077	%
	Amp-to-Amp Isolation	(Note 8)	140	dB

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ.**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage	LMV921 (Single)	−1.5	6 **8**	mV max
		LMV922 (Dual) LMV924 (Quad)	−1.5	8 **9.5**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		1		µV/°C
I_B	Input Bias Current		12	35 **50**	nA max
I_{OS}	Input Offset Current		2	25 **40**	nA max
I_S	Supply Current	LMV921 (Single)	160	210 **230**	µA max
		LMV922 (Dual)	400	500 **700**	
		LMV924 (Quad)	750	850 **980**	
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 3.8V	86	62 **61**	dB min
		−0.2V ≤ V_{CM} ≤ 0V 5.0V ≤ V_{CM} ≤ 5.2V	72	50	
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V	78	67 **62**	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	-0.3	-0.2 **0**	V min
			5.350	5.2 **5.0**	V max

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
A_V	Voltage Gain LMV921 (Single)	R_L = 600Ω to 2.5V V_O = 0.2V to 4.8V	104	86 **82**	dB min
		R_L = 2kΩ to 2.5V V_O = 0.2V to 4.8V	108	89 **85**	dB min
	Voltage Gain LMV922 (Dual) LMV924 (Quad)	R_L = 600Ω to 2.5V V_O = 0.2V to 4.8V	90	72 68	dB min
		R_L = 2kΩ to 2.5V V_O = 0.2V to 4.8V	96	77 73	dB min
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ± 100mV	4.895	4.865 **4.840**	V min
			0.1	0.135 **0.160**	V max
		R_L = 2kΩ to 2.5V V_{IN} = ± 100mV	4.965	4.945 **4.935**	V min
			0.035	0.065 **0.075**	V max
I_O	Output Short Circuit Current	LMV921 Sourcing, V_O = 0V V_{IN} = 100mV	98	85 **68**	mA min
		LMV922, LMV924 Sourcing, V_O = 0V V_{IN} = 100mV	60	35	mA min
		Sinking, V_O = 5V V_{IN} = −100mV	75	65 **45**	mA min

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Units
SR	Slew Rate	(Note 7)	0.45	V/μs
GBW	Gain-Bandwidth Product		1	MHz
Φ_m	Phase Margin		70	Deg
G_m	Gain Margin		15	dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 1V	45	$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.1	$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600Ω, V_O = 1 V_{PP}	0.069	%
	Amp-to-Amp Isolation	(Note 8)	140	dB

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100pF. Machine model, 200Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

Note 8: Input referred, V^+ = 5V and R_L = 100kΩ connected to 2.5V. Each amp excited in turn with 1kHz to produce $V_O = 3V_{PP}$.

National Semiconductor

LMV931
Single, 1.8V, 1MHz, Operational Amplifier with Rail-To-Rail Input and Output

General Description

The LMV931 is a single low voltage, low power operational amplifier. LMV931 is guaranteed to operate from +1.8V to +5.0V supply voltages and have rail-to-rail input and output. LMV931 input common mode voltage extends 200mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail-to-rail unloaded and within 100mV from the rail with 600Ω load at 1.8V supply. The LMV931 is optimized to work at 1.8V which make them ideal for portable two-cell battery powered systems and single cell Li-Ion systems.

The LMV931 exhibits excellent speed-power ratio, achieving 1.4MHz gain bandwidth product at 1.8V supply voltage with very low supply current. The LMV931 is capable of driving a 600Ω load and up to 1000pF capacitive load with minimal ringing. The LMV931 has a high DC gain of 101dB, making it suitable for low frequency applications.

The LMV931 is offered in space saving SC70-5 and SOT23-5 packages. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellular phones and PDAs.

Features

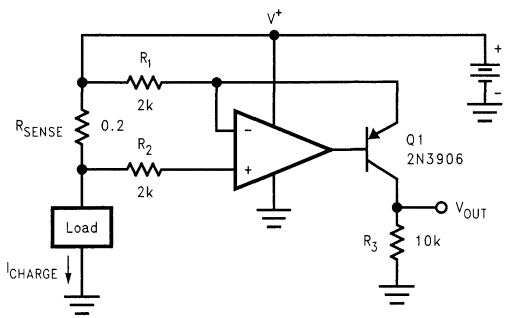
(Typical 1.8V Supply Values; Unless Otherwise Noted)

- Guaranteed 1.8V, 2.7V and 5V specifications
- Output swing
  - — w/600Ω load 84mV from rail
  - — w/2kΩ load 26mV from rail
- V_{CM} 200mV beyond rails
- Supply current 100µA
- Gain bandwidth product 1.4MHz
- Maximum V_{OS} 4.0mV
- Gain w/600Ω load 101dB

Applications

- Consumer communication
- Consumer computing
- PDAs
- PCMCIA
- Portable/battery-powered electronic equipment
- Supply current monitoring
- Battery monitoring

Typical Application



$$V_{OUT} = \frac{R_{SENSE} \cdot R_3}{R_1} \cdot I_{Charge} = 1\Omega \cdot I_{Charge}$$

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	200V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C
Mounting Temp.	
Infrared or Convection (20 sec)	235°C

Operating Ratings (Note 1)

Supply Voltage Range	1.8V to 5.0V
Temperature Range	−40°C to 85°C
Thermal Resistance (θ_{JA})	
SC70-5	414°C/W
SOT23-5	265°C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1.0	4 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C
I_B	Input Bias Current			15	35 **50**	nA
I_{OS}	Input Offset Current			13	25 **40**	nA
I_S	Supply Current			103	185 **205**	µA
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 0.6V$ $1.4V \le V_{CM} \le 1.8V$	60 **55**	78		dB
		$-0.2V \le V_{CM} \le 0V$ $1.8V \le V_{CM} \le 2.0V$	50	72		
PSRR	Power Supply Rejection Ratio	$1.8V \le V^+ \le 5V$	75 **70**	100		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.2 2.1	−0.2 2.0 **0.0** **1.8**	V
A_V	Large Signal Voltage Gain	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	77 **73**	101		dB
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	80 **75**	105		
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ± 100mV	1.65 **1.63**	1.72		V
				0.077	0.09 **0.105**	
		R_L = 2kΩ to 0.9V V_{IN} = ± 100mV	1.75 **1.74**	1.77		
				0.024	0.035 **0.04**	

1.8V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	4 **3.3**	8		mA
		Sinking, V_O = 1.8V V_{IN} = −100mV	7 **5**	9		

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.42		V/μs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		Deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 0.5V		60		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1kHz		0.06		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.023		%

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1.0	4 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		μV/°C
I_B	Input Bias Current			15	35 **50**	nA
I_{OS}	Input Offset Current			8	25 **40**	nA
I_S	Supply Current			105	190 **210**	μA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 1.5V 2.3V ≤ V_{CM} ≤ 2.7V	60 **55**	81		dB
		−0.2V ≤ V_{CM} ≤ 0V 2.7V ≤ V_{CM} ≤ 2.9V	50	74		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V	75 **70**	100		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.2 3.0	−0.2 2.9 **0.0** **2.7**	V

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_V	Large Signal Voltage Gain	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V	87 **86**	104		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V	92 **91**	110		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ± 100mV	2.55 **2.53**	2.62		V
				0.083	0.095 **0.115**	
		R_L = 2kΩ to 1.35V V_{IN} = ± 100mV	2.65 **2.64**	2.675		
				0.025	0.04 **0.045**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	20 **15**	30		mA
		Sinking, V_O = 2.7V V_{IN} = −100mV	22 **16**	25		

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.46		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		Deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 0.5V		57		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz		0.082		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600kΩ, V_{IN} = 1 V_{PP}		0.022		%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1.0	4 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C
I_B	Input Bias Current			14	35 **50**	nA
I_{OS}	Input Offset Current			9	25 **40**	nA

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_S	Supply Current			116	210 **230**	µA
		In Shutdown		0.201	1 **2**	µA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3.8V 4.6V ≤ V_{CM} ≤ 5.0V	60 **55**	86		dB
		−0.2V ≤ V_{CM} ≤ 0V 5.0V ≤ V_{CM} ≤ 5.2V	50	78		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V	75 70	100		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.2 5.3	−0.2 5.2 **0.0** **5.0**	V
A_V	Large Signal Voltage Gain	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V	88 **87**	102		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V	94 **93**	112		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ± 100mV	4.855 4.835	4.890 4.88		V
				0.120	1.145 **0.165**	
		R_L = 2kΩ to 2.5V V_{IN} = ± 100mV	4.945 **4.935**	4.967		
				0.037	0.065 **0.075**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	80 **68**	100		mA
		Sinking, V_O = 5V V_{IN} = −100mV	58 **45**	65		

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.48		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			79		Deg
G_m	Gain Margin			12		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 1V		50		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz		0.07		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600Ω, V_O = 1 V_{PP}		0.022		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

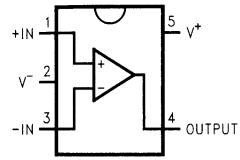
Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 5V$. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

Connection Diagram

5-Pin SC70-5/SOT23-5



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Top View

Ordering Information

Package	Part Number	Packaging Marking	Transport Media	NSC Drawing
5-Pin SC70	LMV931MG	A74	1k Units Tape and Reel	MAA05A
	LMV931MGX		3k Units Tape and Reel	
5-Pin SOT23	LMV931MF	A79A	1k Units Tape and Reel	MF05A
	LMV931MFX		3k Units Tape and Reel	

National Semiconductor

LMV981
RRIO, 1.8V, Operational Amplifier in micro SMD with Shutdown

General Description

The LMV981 is a single low voltage, low power operational amplifier. LMV981 is guaranteed to operate from +1.8V to +5.0V supply voltages and have rail-to-rail input and output. LMV981 input common mode voltage extends 200mV beyond the supplies which enables user enhanced functionality beyond the supply voltage range. The output can swing rail-to-rail unloaded and within 100mV from the rail with 600Ω load at 1.8V supply. The LMV981 is optimized to work at 1.8V which make them ideal for portable two-cell battery powered systems and single cell Li-Ion systems.

The LMV981 offers a shutdown pin that can be used to disable the device and reduce the supply current.

The LMV981 exhibits excellent speed-power ratio, achieving 1.4MHz gain bandwidth product at 1.8V supply voltage with very low supply current. The LMV981 is capable of driving a 600Ω load and up to 1000pF capacitive load with minimal ringing. The LMV981 has a high DC gain of 101dB, making it suitable for low frequency applications.

The LMV981 is offered in space saving 6-Bump micro SMD, SC70-6 and SOT23-6 packages. The 6-Bump micro SMD package has only a 1.006mm x 1.514mm x 0.945mm footprint. These small packages are ideal solutions for area constrained PC boards and portable electronics such as cellular phones and PDAs.

Features

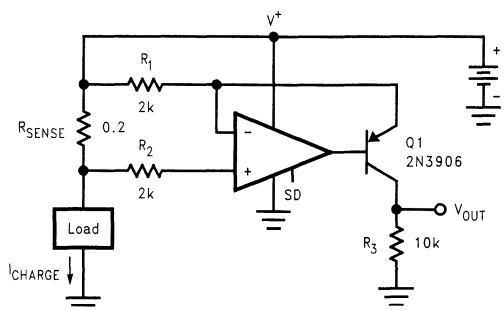
(Typical 1.8V Supply Values; Unless Otherwise Noted)

- Guaranteed 1.8V, 2.7V and 5V specifications
- Output swing
  - — w/600Ω load 84mV from rail
  - — w/2kΩ load 26mV from rail
- V_{CM} 200mV beyond rails
- Supply current 100µA
- Gain bandwidth product 1.4MHz
- Maximum V_{OS} 4.0mV
- Gain w/600Ω load 101dB
- Ultra tiny packages 1.0mm x 1.5mm
- Turn-on time from shutdown <13µs max
- Temperature range −40°C to 125°C

Applications

- Industrial and automotive
- Consumer communication
- Consumer computing
- PDAs
- PCMCIA
- Portable/battery-powered electronic equipment
- Supply current monitoring
- Battery monitoring

Typical Application



$$V_{OUT} = \frac{R_{SENSE} \cdot R_3}{R_1} \cdot I_{Charge} = 1\Omega \cdot I_{Charge}$$

200214H0

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	200V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^+ (Note 3)	
Output Short Circuit to V^- (Note 3)	
Storage Temperature Range	−65°C to 150°C
Junction Temperature (Note 4)	150°C
Mounting Temp.	
Infrared or Convection (20 sec)	235°C

Operating Ratings (Note 1)

Supply Voltage Range	1.8V to 5.0V
Temperature Range	−40°C to 125°C
Thermal Resistance (θ_{JA})	
6-Bump micro SMD	286°C/W
SC70-6	414°C/W
SOT23-6	265°C/W

1.8V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, $V_{CM} = V^+/2$, $V_O = V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1.0	4 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C
I_B	Input Bias Current			15	35 **50**	nA
I_{OS}	Input Offset Current			13	25 **40**	nA
I_S	Supply Current			103	185 **205**	µA
		In Shutdown		0.156	1 **2**	
CMRR	Common Mode Rejection Ratio	$0 \le V_{CM} \le 0.6V$ $1.4V \le V_{CM} \le 1.8V$ (Note 8)	60 **55**	78		dB
		$-0.2V \le V_{CM} \le 0V$ $1.8V \le V_{CM} \le 2.0V$ (Note 8)	50	72		
PSRR	Power Supply Rejection Ratio	$1.8V \le V^+ \le 5V$	75 **70**	100		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB (Note 8)		−0.2 2.1	−0.2 2.0 **0.0** **1.8**	V
A_V	Large Signal Voltage Gain	R_L = 600Ω to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	77 **73**	101		dB
		R_L = 2kΩ to 0.9V, V_O = 0.2V to 1.6V, V_{CM} = 0.5V	80 **75**	105		
V_O	Output Swing	R_L = 600Ω to 0.9V V_{IN} = ± 100mV (Note 8)	1.65 **1.63**	1.72		V
				0.077	0.09 **0.105**	
		R_L = 2kΩ to 0.9V V_{IN} = ± 100mV	1.75 **1.74**	1.77		
				0.024	0.035 **0.04**	

1.8V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	4 **3.3**	8		mA
		Sinking, V_O = 1.8V V_{IN} = −100mV	7 **5**	9		
Ton	Turn-on Time from Shutdown			19		µs

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 1.8V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.42		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			67		Deg
G_m	Gain Margin			7.5		dB
e_n	Input-Referred Voltage Noise	f = 1kHz, V_{CM} = 0.5V		60		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1kHz		0.06		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1kHz, A_V = +1 R_L = 600Ω, V_{IN} = 1 V_{PP}		0.023		%

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1.0	4 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C
I_B	Input Bias Current			15	35 **50**	nA
I_{OS}	Input Offset Current			8	25 **40**	nA
I_S	Supply Current			105	190 **210**	µA
		In Shutdown		0.061	1 **2**	
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 1.5V 2.3V ≤ V_{CM} ≤ 2.7V (Note 8)	60 **55**	81		dB
		−0.2V ≤ V_{CM} ≤ 0V 2.7V ≤ V_{CM} ≤ 2.9V (Note 8)	50	74		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V	75 **70**	100		dB

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB (Note 8)		−0.2 3.0	−0.2 2.9 **0.0** **2.7**	V
A_V	Large Signal Voltage Gain	R_L = 600Ω to 1.35V, V_O = 0.2V to 2.5V	87 **86**	104		dB
		R_L = 2kΩ to 1.35V, V_O = 0.2V to 2.5V	92 **91**	110		
V_O	Output Swing	R_L = 600Ω to 1.35V V_{IN} = ± 100mV (Note 8)	2.55 **2.53**	2.62		V
				0.083	0.095 **0.115**	
		R_L = 2kΩ to 1.35V V_{IN} = ± 100mV	2.65 **2.64**	2.675		
				0.025	0.04 **0.045**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	20 **15**	30		mA
		Sinking, V_O = 2.7V V_{IN} = −100mV	22 **16**	25		
Ton	Turn-on Time from Shutdown			12.5		µs

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = 1.35V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.46		V/µs
GBW	Gain-Bandwidth Product			1.4		MHz
Φ_m	Phase Margin			70		Deg
G_m	Gain Margin			8		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 0.5V		57		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz		0.082		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600kΩ, V_{IN} = 1 V_{PP}		0.022		%

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = $V^+/2$ and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage			1.0	4 **6**	mV
TCV_{OS}	Input Offset Voltage Average Drift			2		µV/°C

5V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
I_B	Input Bias Current			14	35 **50**	nA
I_{OS}	Input Offset Current			9	25 **40**	nA
I_S	Supply Current			116	210 **230**	µA
		In Shutdown		0.201	1 **2**	µA
CMRR	Common Mode Rejection Ratio	0 ≤ V_{CM} ≤ 3.8V 4.6V ≤ V_{CM} ≤ 5.0V (Note 8)	60 **55**	86		dB
		−0.2V ≤ V_{CM} ≤ 0V 5.0V ≤ V_{CM} ≤ 5.2V (Note 8)	50	78		
PSRR	Power Supply Rejection Ratio	1.8V ≤ V^+ ≤ 5V V_{CM} = 0.5V	75 70	100		dB
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB		−0.2 5.3	−0.2 5.2 **0.0** **5.0**	V
A_V	Large Signal Voltage Gain	R_L = 600Ω to 2.5V, V_O = 0.2V to 4.8V	88 **87**	102		dB
		R_L = 2kΩ to 2.5V, V_O = 0.2V to 4.8V	94 **93**	112		
V_O	Output Swing	R_L = 600Ω to 2.5V V_{IN} = ± 100mV (Note 8)	4.855 4.835	4.890 4.88		V
				0.120	1.145 **0.165**	
		R_L = 2kΩ to 2.5V V_{IN} = ± 100mV	4.945 **4.935**	4.967		
				0.037	0.065 **0.075**	
I_O	Output Short Circuit Current	Sourcing, V_O = 0V V_{IN} = 100mV	80 **68**	100		mA
		Sinking, V_O = 5V V_{IN} = −100mV	58 **45**	65		
Ton	Turn-on Time from Shutdown			8.4		µs

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = V^+/2, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
SR	Slew Rate	(Note 7)		0.48		V/µs
GBW	Gain-Bandwidth Product			1.5		MHz
Φ_m	Phase Margin			79		Deg
G_m	Gain Margin			12		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz, V_{CM} = 1V		50		$\frac{nV}{\sqrt{Hz}}$

5V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$, V_O = 2.5V and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
i_n	Input-Referred Current Noise	f = 1 kHz		0.07		$\frac{pA}{\sqrt{Hz}}$
THD	Total Harmonic Distortion	f = 1 kHz, A_V = +1 R_L = 600Ω, V_O = 1 V_{PP}		0.022		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

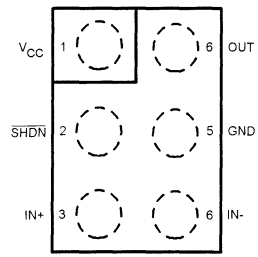
Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: V^+ = 5V. Connected as voltage follower with 5V step input. Number specified is the slower of the positive and negative slew rates.

Note 8: Max temperature guarantee range (−40°C to 85°C).

Connection Diagrams

6-Bump micro SMD



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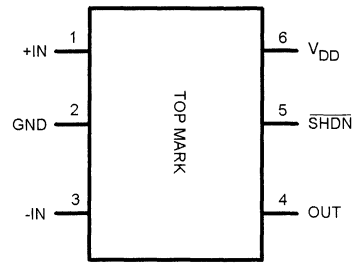
Top View

6-Pin SC70-6/SOT23-6



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Top View

Ordering Information

Package	Part Number	Packaging Marking	Transport Media	NSC Drawing
6-Bump micro SMD	LMV981BL	A	250 Units Tape and Reel	BLA006AAB
	LMV981BLX		3k Units Tape and Reel	
6-Pin SC70	LMV981MG	A77	1k Units Tape and Reel	MAA06A
	LMV981MGX		3k Units Tape and Reel	
6-Pin SOT23	LMV981MF	A78A	1k Units Tape and Reel	MF06A
	LMV981MFX		3.5k Units Tape and Reel	

National Semiconductor

LP324/LP2902
Micropower Quad Operational Amplifier

General Description

The LP324 series consists of four independent, high gain internally compensated micropower operational amplifiers. These amplifiers are specially suited for operation in battery systems while maintaining good input specifications, and extremely low supply current drain. In addition, the LP324 has an input common mode range, and output source range which includes ground, making it ideal in single supply applications.

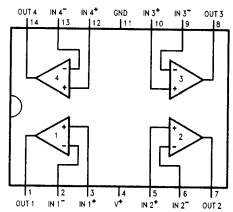
These amplifiers are ideal in applications which include portable instrumentation, battery backup equipment, and other circuits which require good DC performance and low supply current.

Features

- Low supply current: 85µA (typ)
- Low offset voltage: 2mV (typ)
- Low input bias current: 2nA (typ)
- Input common mode to GND
- Interfaces to CMOS logic
- Wide supply range: 3V < V^+ < 32V
- Small Outline Package available
- Pin-for-pin compatible with LM324

Connection Diagrams

Dual-In-Line (N) and SO (M)



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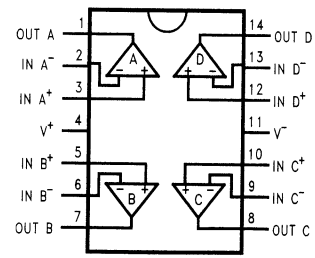
Order Number LP324M or LP2902M
See NS Package Number M14A
Order Number LP324N or LP2902N
See NS Package Number N14A

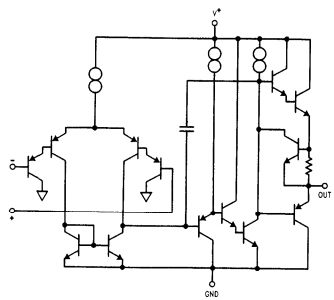
14-Pin TSSOP



00856240

Order Number LP324MT and LP324MTX
See NS Package Number MTC14

Simplified Schematic



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
LP324	32V or ± 16V
LP2902	26V or ± 13V
Differential Input Voltage	
LP324	32V
LP2902	26V
Input Voltage (Note 2)	
LP324	−0.3V to 32V
LP2902	−0.3V to 26V
Output Short-Circuit to GND (One Amplifier) (Note 3)	Continuous
$V^+ < 15V$ and $T_A = 25^\circ C$ ESD Susceptibility (Note 10)	±500V

Operating Conditions

T_{JMAX}	150°C
θ_{JA} (Note 4)	
MT Package	154°C/W
N Package	90°C/W
M Package	140°C/W
Operating Temp. Range	(Note 5)
Storage Temp. Range	$-65^\circ C \le T_J \le 150^\circ C$
Soldering Information	
Wave Soldering(10sec)	260°C(lead temp.)
Convection or Infrared(20sec)	235°C

Electrical Characteristics (Note 6)

Symbol	Parameter	Conditions	LP2902 (Note 9)			LP324			Units Limits
			Typ	Tested Limit (Note 7)	Design Limit (Note 8)	Typ	Tested Limit (Note 7)	Design Limit (Note 8)	
V_{OS}	Input Offset Voltage		2	4	**10**	2	4	**9**	mV (Max)
I_B	Input Bias Current		2	20	**40**	2	10	**20**	nA (Max)
I_{OS}	Input Offset Current		0.5	4	**8**	0.2	2	**4**	nA (Max)
A_{VOL}	Voltage Gain	R_L = 10k to GND V^+ = 30V	70	40	**30**	100	50	**40**	V/mV (Min)
CMRR	Common Mode Rej. Ratio	V^+ = 30V, 0V ≤ V_{CM} < V^+− 1.5	90	80	**75**	90	80	**75**	dB (Min)
PSRR	Power Supply Rej. Ratio	V^+ = 5V to 30V	90	80	**75**	90	80	**75**	dB (Min)
I_S	Supply Current	$R_L = \infty$	85	150	**250**	85	150	**250**	µA (Max)
V_O	Output Voltage Swing	I_L = 350µA to GND V_{CM} = 0V	3.6	3.4	**V^+−1.9V**	3.6	3.4	**V^+−1.9V**	V (Min)
		I_L = 350µA to V^+ V_{CM} = 0V	0.7	0.8	**1.0**	0.7	0.8	**1.0**	V (Max)
I_{OUT} Source	Output Source Current	V_O = 3V V_{IN} (diff) = 1V	10	7	**4**	10	7	**4**	mA (Min)
I_{OUT} Sink	Output Sink Current	V_O = 1.5V V_{IN} (diff) = 1V	5	4	**3**	5	4	**3**	mA (Min)
I_{OUT} Sink	Output Sink Current	V_O = 1.5V V_{CM} = 0V	4	2	**1**	4	2	**1**	mA (Min)
I_{SOURCE}	Output Short to GND	V_{IN} (diff) = 1V	20	25 **35**	**35**	20	25 **35**	**35**	mA (Max)
I_{SINK}	Output Short to V^+	V_{IN} (diff) = 1V	15	30	**45**	15	30	**45**	mA (Max)
V_{OS} Drift			10			10			µV/C°
I_{OS} Drift			10			10			pA/C°

Electrical Characteristics (Note 6) (Continued)

Symbol	Parameter	Conditions	LP2902 (Note 9)			LP324			Units Limits
			Typ	Tested Limit (Note 7)	Design Limit (Note 8)	Typ	Tested Limit (Note 7)	Design Limit (Note 8)	
GBW	Gain Bandwidth Product		100			100			KHz
SR	Slew Rate		50			50			V/mS

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: The input voltage is not allowed to go more than −0.3V below V^- (GND) as this will turn on a parasitic transistor causing large currents to flow through the device.

Note 3: Short circuits from the output to GND can cause excessive heating and eventual destruction. The maximum sourcing output current is approximately 30 mA independent of the magnitude of V^+. At values of supply voltage in excess of 15 V_{DC}, continuous short-circuit to GND can exceed the power dissipation ratings (particularly at elevated temperatures) and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 4: For operation at elevated temperatures, these devices must be derated based on a thermal resistance of θ_{JA} and T_J max. $T_J = T_A + \theta_{JA}P_D$.

Note 5: The LP2902 may be operated from $-40^\circ C \le T_A \le +85^\circ C$, and the LP324 may be operated from $0^\circ C \le T_A \le +70^\circ C$.

Note 6: Boldface numbers apply at temperature extremes. All other numbers apply only at $T_A = T_J = 25^\circ C$, $V^+ = 5V$, $V_{cm} = V/2$, and R_L =100k connected to GND unless otherwise specified.

Note 7: Guaranteed and 100% production tested.

Note 8: Guaranteed (but not 100% production tested) over the operating supply voltage range (3.0V to 32V for the LP324, LP324, and 3.0V to 26V for the LP2902), and the common mode range (0V to V^+ −1.5V), unless otherwise specified. These limits are not used to calculate outgoing quality levels.

Note 9: The LP2902 operating supply range is 3V to 26V, and is not tested above 26V.

Note 10: The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

National Semiconductor

LPC660
Low Power CMOS Quad Operational Amplifier

General Description

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltages from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier and LPC661 datasheet for a single CMOS operational amplifier with these same features.

Applications

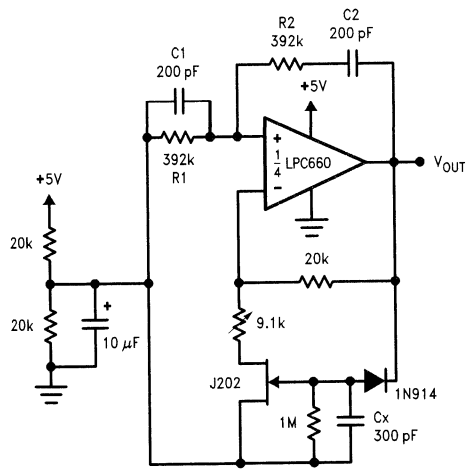
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation: (1 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain: 120 dB
- Low input offset voltage: 3 mV
- Low offset voltage drift: 1.3 µV/°C
- Ultra low input bias current: 2 fA
- Input common-mode includes V^-
- Operation range from +5V to +15V
- Low distortion: 0.01% at 1 kHz
- Slew rate: 0.11 V/µs
- Full military temp. range available

Application Circuit

Sine-Wave Oscillator



Oscillator frequency is determined by R1, R2, C1, and C2:

$f_{OSC} = 1/2\pi RC$

where R = R1 = R2 and C = C1 = C2.

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 2)	150°C
ESD Rating	
(C = 100 pF, R = 1.5 kΩ)	1000V
Power Dissipation	(Note 2)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) − 0.3V
Current at Power Supply Pin	35 mA

Operating Ratings (Note 3)

Temperature Range	
LPC660AM	$-55°C \le T_J \le +125°C$
LPC660AI	$-40°C \le T_J \le +85°C$
LPC660I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}), (Note 10)	
14-Pin Ceramic DIP	90°C/W
14-Pin Molded DIP	85°C/W
14-Pin SO	115°C/W
14-Pin Side Brazed Ceramic DIP	90°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (Notes 4, 8)	Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				µV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 12.0V V^+ = 15V	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	5V ≤ V^+ ≤ 15V	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	0V ≤ V^- ≤ −10V	94	84	84	74	dB
			82	**83**	**73**	min
Input Common Mode Voltage Range	V^+ = 5V & 15V For CMRR > 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		V^+ − 1.9	V^+ − 2.3	V^+ − 2.3	V^+ − 2.3	V
			V^+ − 2.6	**V^+ − 2.5**	**V^+ − 2.5**	min
Large Signal Voltage Gain	R_L = 100 kΩ (Note 5) Sourcing	1000	400	400	300	V/mV
			250	**300**	**200**	min
	Sinking	500	180	180	90	V/mV
			70	**120**	**70**	min
	R_L = 5 kΩ (Note 5) Sourcing	1000	200	200	100	V/mV
			150	**160**	**80**	min
	Sinking	250	100	100	50	V/mV
			35	**60**	**40**	min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (Notes 4, 8)	Limit (Note 4)	Limit (Note 4)	
Output Swing	V^+ = 5V	4.987	4.970	4.970	4.940	V
	R_L = 100 kΩ to $V^+/2$		**4.950**	**4.950**	**4.910**	min
		0.004	0.030	0.030	0.060	V
			0.050	**0.050**	**0.090**	max
	V^+ = 5V	4.940	4.850	4.850	4.750	V
	R_L = 5 kΩ to $V^+/2$		**4.750**	**4.750**	**4.650**	min
		0.040	0.150	0.150	0.250	V
			0.250	**0.250**	**0.350**	max
	V^+ = 15V	14.970	14.920	14.920	14.880	V
	R_L = 100 kΩ to $V^+/2$		**14.880**	**14.880**	**14.820**	min
		0.007	0.030	0.030	0.060	V
			0.050	**0.050**	**0.090**	max
	V^+ = 15V	14.840	14.680	14.680	14.580	V
	R_L = 5 kΩ to $V^+/2$		**14.600**	**14.600**	**14.480**	min
		0.110	0.220	0.220	0.320	V
			0.300	**0.300**	**0.400**	max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	16	13	mA
			12	**14**	**11**	min
	Sinking, V_O = 5V	21	16	16	13	mA
			12	**14**	**11**	min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19	28	23	mA
			19	**25**	**20**	min
	Sinking, V_O = 13V	39	19	28	23	mA
	(Note 11)		**19**	**24**	**19**	min
Supply Current	All Four Amplifiers	160	200	200	240	µA
	V_O = 1.5V		**250**	**230**	**270**	max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5, and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC660AM LPC660AMJ/883	LPC660AI	LPC660I	Units
			Limit (Notes 4, 8)	**Limit** (Note 4)	**Limit** (Note 4)	
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs
			0.04	**0.05**	**0.03**	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				$nV/\sqrt{Hz}$
Input Referred Current Noise	F = 1 kHz	0.0002				$pA/\sqrt{Hz}$
Total Harmonic Distortion	F = 1 kHz, A_V = −10 R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 100 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.

Note 9: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J-T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to $V^+$when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LPC661
Low Power CMOS Operational Amplifier

General Description

The LPC661 CMOS operational amplifier is ideal for operation from a single supply. It features a wide range of operating supply voltage from +5V to +15V, rail-to-rail output swing and an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the supply current requirement is typically 55 µA.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier or the LPC662 data sheet for a Dual CMOS operational amplifier with these same features.

Features

(Typical unless otherwise noted)

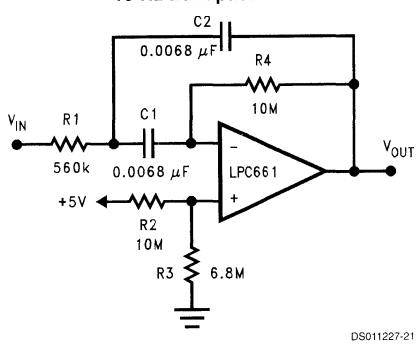
- Rail-to-rail output swing
- Low supply current 55 µA
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 µV/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/µs

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

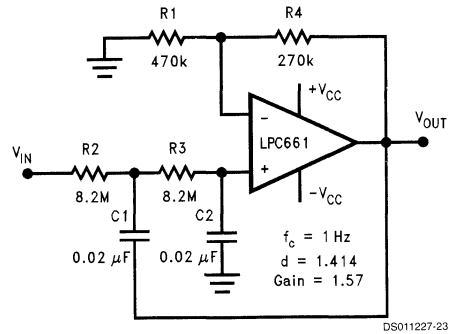
Application Circuits

10 Hz Bandpass Filter



f_O = 10 Hz
Q = 2.1
Gain = 18.9 dB

1 Hz Low-Pass Filter
(Maximally Flat, Dual Supply Only)



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$)	16V
Differential Input Voltage	±Supply Voltage
Output Short Circuit to V^+	(Notes 2, 9)
Output Short Circuit to V^-	(Note 2)
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	260°C
Junction Temperature (Note 3)	150°C
Power Dissipation	(Note 3)
ESD Rating	
(C=100 pF, R=1.5 kΩ)	1000V
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Voltage Input/Output Pin	(V^+) +0.3V, (V^-) −0.3V
Current at Power Supply Pin	35 mA

Operating Ratings (Note 1)

Supply Voltage	$4.75V \le V^+ \le 15.5V$
Junction Temperature Range	
LPC661AM	$-55°C \le T_J \le +125°C$
LPC661AI	$-40°C \le T_J \le +85°C$
LPC661I	$-40°C \le T_J \le +85°C$
Power Dissipation	(Note 7)
Thermal Resistance (θ_{JA}) (Note 8)	
8-Pin DIP	101°C/W
8-Pin SO	165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25°C$.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_{OS}	Input Offset Voltage		1	3	3	6	mV
				3.5	**3.3**	**6.3**	
TCV_{OS}	Input Offset Voltage Average Drift		1.3				µV/°C
I_B	Input Bias Current		0.002	20			pA
				100	**4**	**4**	max
I_{OS}	Input Offset Current		0.001	20			pA
				100	**2**	**2**	max
R_{IN}	Input Resistance		>1				Tera Ω
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$, $V^+ = 15V$	83	70	70	63	dB
				68	**68**	**61**	min
+PSRR	Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$	83	70	70	63	dB
				68	**68**	**61**	min
−PSRR	Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB
				82	**83**	**73**	min
V_{CM}	Input Common Mode Voltage Range	$V^+ = 5V$ and 15V for CMRR ≥ 50 dB	−0.4	−0.1	−0.1	−0.1	V
				0	**0**	**0**	max
			$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
				$V^+ - 2.6$	**$V^+ - 2.5$**	**$V^+ - 2.5$**	min
A_V	Large Signal Voltage Gain	Sourcing $R_L = 100 kΩ$ (Note 5)	1000	400	400	300	V/mV
				250	**300**	**200**	min
		Sinking $R_L = 100 kΩ$ (Note 5)	500	180	180	90	V/mV
				70	**120**	**70**	min
		Sourcing $R_L = 5 kΩ$ (Note 5)	1000	200	200	100	V/mV
				150	**160**	**80**	min
		Sinking $R_L = 5 kΩ$ (Note 5)	250	100	100	50	V/mV
				35	**60**	**40**	min

DC Electrical Characteristics (Continued)

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
V_O	Output Swing	V^+ = 5V R_L = 100 kΩ to 2.5V	4.987	4.970 **4.950**	4.970 **4.950**	4.940 **4.910**	V min
			0.004	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		V^+ = 5V R_L = 5 kΩ to 2.5V	4.940	4.850 **4.750**	4.850 **4.750**	4.750 **4.650**	V min
			0.040	0.150 **0.250**	0.150 **0.250**	0.250 **0.350**	V max
		V^+ = 15V R_L = 100 kΩ to 7.5V	14.970	14.920 **14.880**	14.920 **14.880**	14.880 **14.820**	V min
			0.007	0.030 **0.050**	0.030 **0.050**	0.060 **0.090**	V max
		V^+ = 15V R_L = 5 kΩ to 7.5V	14.840	14.680 **14.600**	14.680 **14.600**	14.580 **14.480**	V min
			0.110	0.220 **0.300**	0.220 **0.300**	0.320 **0.400**	V max
I_O	Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **12**	16 **14**	13 **11**	mA min
		Sinking, V_O = 5V	21	16 **12**	16 **14**	13 **11**	mA min
I_O	Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19 **19**	28 **25**	23 **20**	mA min
		Sinking, V_O = 13V (Note 9)	39	19 **19**	28 **24**	23 **19**	mA min
I_S	Supply Current	V^+ = 5V, V_O = 1.5V	55	60 **70**	60 **70**	70 **85**	μA max
		V^+ = 15V, V_O = 1.5V	58	75 **85**	75 **85**	90 **105**	μA max

AC Electrical Characteristics

The following specifications apply for V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V, and R_L = 1M unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits T_J = 25°C.

Symbol	Parameter	Conditions	Typ	LPC661AM Limit (Note 4)	LPC661AI Limit (Note 4)	LPC661I Limit (Note 4)	Units (Limit)
SR	Slew Rate	(Note 6)	0.11	0.07 **0.04**	0.07 **0.05**	0.05 **0.03**	V/μs min
GBW	Gain-Bandwidth Product		350				kHz
ϕm	Phase Margin		50				Deg
G_M	Gain Margin		17				dB
e_n	Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{Hz}$
i_n	Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{Hz}$
T.H.D.	Total Harmonic Distortion	F = 1 kHz, A_V = −10 R_L = 100 kΩ, V_O = 8 V_{PP} V^+ = 15V	0.01				%

AC Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: V+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J-T_A)/\theta_{JA}$.

Note 8: All numbers apply for packages soldered directly into a PC board.

Note 9: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LPC662
Low Power CMOS Dual Operational Amplifier

General Description

The LPC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V, rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain (into 100 kΩ and 5 kΩ) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier and LPC661 for a single CMOS operational amplifier with these same features.

Applications

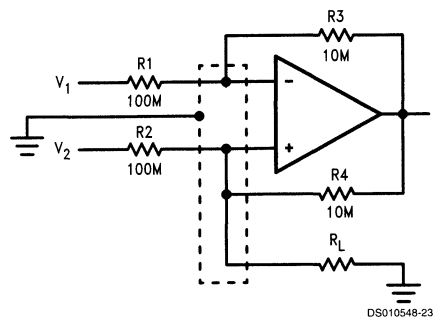
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (<0.5 mW)
- Specified for 100 kΩ and 5 kΩ loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μV/°C
- Ultra low input bias current 2 fA
- Input common-mode includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/μs
- Full military temperature range available

Application Circuit

Howland Current Pump



Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage ($V^+ - V^-$)	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature	
(Soldering, 10 sec.)	260°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
ESD Rating	
(C = 100 pF, R = 1.5 kΩ)	1000V
Power Dissipation	(Note 2)
Current at Input Pin	±5 mA
Current at Output Pin	±18 mA
Current at Power Supply Pin	35 mA
Voltage at Input/Output Pin	(V^+) + 0.3V, (V^-) −0.3V

Operating Ratings (Note 3)

Temperature Range	
LPC662AMJ/883	$-55°C \le T_J \le +125°C$
LPC662AM	$-55°C \le T_J \le +125°C$
LPC662AI	$-40°C \le T_J \le +85°C$
LPC662I	$-40°C \le T_J \le +85°C$
Supply Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
8-Pin Ceramic DIP	100°C/W
8-Pin Molded DIP	101°C/W
8-Pin SO	165°C/W
8-Pin Side Brazed Ceramic DIP	100°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Input Offset Voltage		1	3	3	6	mV
			3.5	**3.3**	**6.3**	max
Input Offset Voltage Average Drift		1.3				µV/°C
Input Bias Current		0.002	20			pA
			100	**4**	**4**	max
Input Offset Current		0.001	20			pA
			100	**2**	**2**	max
Input Resistance		>1				Tera Ω
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70	70	63	dB
			68	**68**	**61**	min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ V_O = 2.5V	83	70	70	63	dB
			68	**68**	**61**	min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84	84	74	dB
			82	**83**	**73**	min
Input Common-Mode Voltage Range	V^+ = 5V and 15V For CMRR ≥ 50 dB	−0.4	−0.1	−0.1	−0.1	V
			0	**0**	**0**	max
		$V^+ - 1.9$	$V^+ - 2.3$	$V^+ - 2.3$	$V^+ - 2.3$	V
			$V^+ - 2.6$	**$V^+ - 2.5$**	**$V^+ - 2.5$**	min
Large Signal Voltage Gain	R_L = 100 kΩ (Note 5) Sourcing	1000	400	400	300	V/mV
			250	**300**	**200**	min
	Sinking	500	180	180	90	V/mV
			70	**120**	**70**	min
	R_L = 5 kΩ (Note 5) Sourcing	1000	200	200	100	V/mV
			150	**160**	**80**	min
	Sinking	250	100	100	50	V/mV
			35	**60**	**40**	min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Output Swing	V^+ = 5V	4.987	4.970	4.970	4.940	V
	R_L = 100 kΩ to $V^+/2$		**4.950**	**4.950**	**4.910**	min
		0.004	0.030	0.030	0.060	V
			0.050	**0.050**	**0.090**	max
	V^+ = 5V	4.940	4.850	4.850	4.750	V
	R_L = 5 kΩ to $V^+/2$		**4.750**	**4.750**	**4.650**	min
		0.040	0.150	0.150	0.250	V
			0.250	**0.250**	**0.350**	max
	V^+ = 15V	14.970	14.920	14.920	14.880	V
	R_L = 100 kΩ to $V^+/2$		**14.880**	**14.880**	**14.820**	min
		0.007	0.030	0.030	0.060	V
			0.050	**0.050**	**0.090**	max
	V^+ = 15V	14.840	14.680	14.680	14.580	V
	R_L = 5 kΩ to $V^+/2$		**14.600**	**14.600**	**14.480**	min
		0.110	0.220	0.220	0.320	V
			0.300	**0.300**	**0.400**	max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16	16	13	mA
			12	**14**	**11**	min
	Sinking, V_O = 5V	21	16	16	13	mA
			12	**14**	**11**	min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	19	28	23	mA
			19	**25**	**20**	min
	Sinking, V_O = 13V	39	19	28	23	mA
	(Note 11)		**19**	**24**	**19**	min
Supply Current	Both Amplifiers	86	120	120	140	μA
	V_O = 1.5V		**145**	**140**	**160**	max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Parameter	Conditions	Typ	LPC662AM LPC662AMJ/883 Limit (Notes 4, 8)	LPC662AI Limit (Note 4)	LPC662I Limit (Note 4)	Units
Slew Rate	(Note 6)	0.11	0.07	0.07	0.05	V/μs
			0.04	**0.05**	**0.03**	min
Gain-Bandwidth Product		0.35				MHz
Phase Margin		50				Deg
Gain Margin		17				dB
Amp-to-Amp Isolation	(Note 7)	130				dB
Input Referred Voltage Noise	F = 1 kHz	42				nV/$\sqrt{\text{Hz}}$
Input Referred Current Noise	F = 1 kHz	0.0002				pA/$\sqrt{\text{Hz}}$
Total Harmonic Distortion	F = 1 kHz, A_V = −10, V^+ = 15V R_L = 100 kΩ, V_O = 8 V_{PP}	0.01				%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation of any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: V^+ = 15V, V_{CM} = 7.5V and R_L connected to 7.5V. For Sourcing tests, 7.5V ≤ V_O ≤ 11.5V. For Sinking tests, 2.5V ≤ V_O ≤ 7.5V.

Note 6: V^+ = 15V. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. V^+ = 15V and R_L = 100 kΩ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce V_O = 13 V_{PP}.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC662AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC662AMJ/883 may also be procured to a Standard Military Drawing specification.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to $V^+$when V^+ is greater than 13V or reliability may be adversely affected.

National Semiconductor

LPV321 Single/LPV358 Dual/LPV324 Quad General Purpose, Low Voltage, Low Power, Rail-to-Rail Output Operational Amplifiers

General Description

The LPV321/358/324 are low power (9µA per channel at 5.0V) versions of the LMV321/358/324 op amps. This is another addition to the LMV321/358/324 family of commodity op amps.

The LPV321/358/324 are the most cost effective solutions for the applications where low voltage, low power operation, space saving and low price are needed. The LPV321/358/324 have rail-to-rail output swing capability and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratio, achieving 152 KHz of bandwidth with a supply current of only 9µA.

The LPV321 is available in space saving SC70-5, which is approximately half the size of SOT23-5. The small package saves space on pc boards, and enables the design of small portable electronic devices. It also allows the designer to place the device closer to the signal source to reduce noise pickup and increase signal integrity.

The chips are built with National's advanced submicron silicon-gate BiCMOS process. The LPV321/358/324 have bipolar input and output stages for improved noise performance and higher output current drive.

Features

(For V^+ = 5V and V^- = 0V, Typical Unless Otherwise Noted)

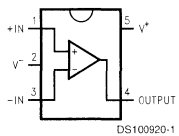
- Guaranteed 2.7V and 5V Performance
- No Crossover Distortion
- Space Saving Package — SC70-5 2.0x2.1x1.0mm
- Industrial Temp.Range — −40°C to +85°C
- Gain-Bandwidth Product — 152KHz
- Low Supply Current
  - LPV321 — 9µA
  - LPV358 — 15µA
  - LPV324 — 28µA
- Rail-to-Rail Output Swing @ 100kΩ Load — V^+−3.5mV; V^-+90mV
- V_{CM} — −0.2V to V^+−0.8V

Applications

- Active Filters
- General Purpose Low Voltage Applications
- General Purpose Portable Devices

Connection Diagrams

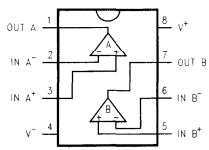
5-Pin SC70-5/SOT23-5



DS100920-1

Top View

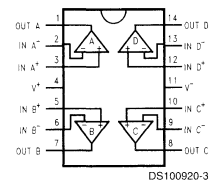
8-Pin SO/MSOP



DS100920-2

Top View

14-Pin SO/TSSOP



DS100920-3

Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Model	100V
Human Body Model	2000V
Differential Input Voltage	± Supply Voltage
Supply Voltage ($V^+ - V^-$)	5.5V
Output Short Circuit to V^+	(Note 3)
Output Short Circuit to V^-	(Note 4)
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temp. Range	−65°C to 150°C
Junction Temp. (T_j, max) (Note 5)	150°C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5V
Temperature Range	$-40°C \le T_J \le 85°C$
Thermal Resistance (θ_{JA})(Note 10)	
5-pin SC70-5	478°C/W
5-pin SOT23-5	265°C/W
8-Pin SOIC	190°C/W
8-Pin MSOP	235°C/W
14-Pin SOIC	145°C/W
14-Pin TSSOP	155°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, $V_O = V^+/2$ and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_{OS}	Input Offset Voltage		1.2	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2		µV/°C
I_B	Input Bias Current		1.7	50	nA max
I_{OS}	Input Offset Current		0.6	40	nA max
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 1.7V$	70	50	dB min
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 5V$ V_O = 1V, V_{CM} = 1V	65	50	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	−0.2	0	V min
			1.9	1.7	V max
V_O	Output Swing	R_L = 100kΩ to 1.35V	V^+ -3	V^+ -100	mV min
			80	180	mV max
I_S	Supply Current	LPV321	4	8	µA max
		LPV358 Both amplifiers	8	16	µA max
		LPV324 All four amplifiers	16	24	µA max

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, V_{CM} = 1.0V, V_O = V^+/2 and R_L > 1 MΩ.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
GBWP	Gain-Bandwidth Product	C_L = 22 pF	112		KHz
Φ_m	Phase Margin		97		Deg
G_m	Gain Margin		35		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz	178		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.50		$\frac{pA}{\sqrt{Hz}}$

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
V_{OS}	Input Offset Voltage		1.5	7 **10**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		2		µV/°C
I_B	Input Bias Current		2	50 **60**	nA max
I_{OS}	Input Offset Current		0.6	40 **50**	nA max
CMRR	Common Mode Rejection Ratio	0V ≤ V_{CM} ≤ 4V	71	50	dB min
PSRR	Power Supply Rejection Ratio	2.7V ≤ V^+ ≤ 5V V_O = 1V, V_{CM} = 1V	65	50	dB min
V_{CM}	Input Common-Mode Voltage Range	For CMRR ≥ 50dB	−0.2	0	V min
			4.2	4	V max
A_V	Large Signal Voltage Gain (Note 8)	R_L = 100kΩ	100	15 **10**	V/mV min
V_O	Output Swing	R_L = 100kΩ to 2.5V	V^+ −3.5	V^+ −100 **V^+ −200**	mV min
			90	180 **220**	mV max
I_O	Output Short Circuit Current	Sourcing, V_O = 0V	17	2	mA min
		Sinking, V_O = 5V	72	20	mA min
I_S	Supply Current	LPV321	9	12 **15**	µA max
		LPV358 Both amplifiers	15	20 **24**	µA max
		LPV324 All four amplifiers	28	42 **46**	µA max

5V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = 2.0V, V_O = V^+/2 and R_L > 1 MΩ. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 6)	Limit (Note 7)	Units
SR	Slew Rate	(Note 9)	0.1		V/μs
GBWP	Gain-Bandwidth Product	C_L = 22 pF	152		KHz
Φ_m	Phase Margin		87		Deg
G_m	Gain Margin		19		dB
e_n	Input-Referred Voltage Noise	f = 1 kHz,	146		$\frac{nV}{\sqrt{Hz}}$
i_n	Input-Referred Current Noise	f = 1 kHz	0.30		$\frac{pA}{\sqrt{Hz}}$

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. Machine model, 0Ω in series with 200 pF.

Note 3: Shorting output to V^+ will adversely affect reliability.

Note 4: Shorting output to V^- will adversely affect reliability.

Note 5: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}-T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 6: Typical values represent the most likely parametric norm.

Note 7: All limits are guaranteed by testing or statistical analysis.

Note 8: R_L is connected to V^-. The output voltage is $0.5V \le V_O \le 4.5V$.

Note 9: Connected as voltage follower with 3V step input. Number specified is the slower of the positive and negative slew rates.

Note 10: All numbers are typical, and apply for packages soldered directly onto a PC board in still air.

National Semiconductor

TL082
Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

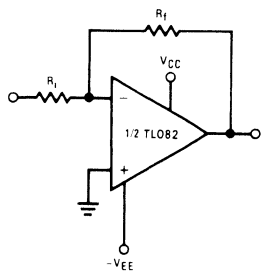
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Features

- Internally trimmed offset voltage: 15 mV
- Low input bias current: 50 pA
- Low input noise voltage: 16nV/√Hz
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 4 MHz
- High slew rate: 13 V/μs
- Low supply current: 3.6 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

Typical Connection



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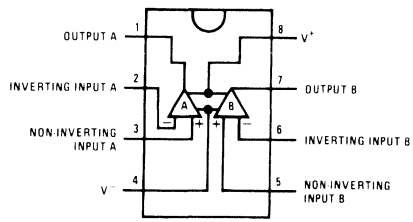
Connection Diagram

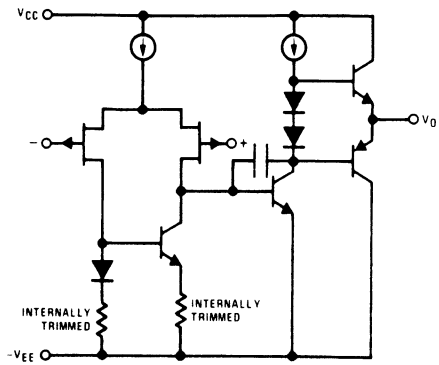
DIP/SO Package (Top View)



DS008357-3

Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

Simplified Schematic



DS008357-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	±18V
Power Dissipation	(Note 2)
Operating Temperature Range	0°C to +70°C
$T_{j(MAX)}$	150°C
Differential Input Voltage	±30V
Input Voltage Range (Note 3)	±15V
Output Short Circuit Duration	Continuous
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	260°C

ESD rating to be determined.

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

DC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	R_S = 10 kΩ, T_A = 25°C		5	15	mV
		Over Temperature			20	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S = 10 kΩ		10		µV/°C
I_{OS}	Input Offset Current	T_j = 25°C, (Notes 5, 6)		25	200	pA
		$T_j \leq$ 70°C			4	nA
I_B	Input Bias Current	T_j = 25°C, (Notes 5, 6)		50	400	pA
		$T_j \leq$ 70°C			8	nA
R_{IN}	Input Resistance	T_j = 25°C		10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S = ±15V, T_A = 25°C	25	100		V/mV
		V_O = ±10V, R_L = 2 kΩ				
		Over Temperature	15			V/mV
V_O	Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range	V_S = ±15V	±11	+15		V
				−12		V
CMRR	Common-Mode Rejection Ratio	$R_S \leq$ 10 kΩ	70	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 7)	70	100		dB
I_S	Supply Current			3.6	5.6	mA

AC Electrical Characteristics (Note 5)

Symbol	Parameter	Conditions	TL082C			Units
			Min	Typ	Max	
	Amplifier to Amplifier Coupling	T_A = 25°C, f = 1Hz-20 kHz (Input Referred)		−120		dB
SR	Slew Rate	V_S = ±15V, T_A = 25°C	8	13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15V, T_A = 25°C		4		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C, R_S = 100Ω, f = 1000 Hz		25		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01		pA/√Hz
THD	Total Harmonic Distortion	A_V = +10, R_L = 10k, V_O = 20 Vp − p, BW = 20 Hz–20 kHz		<0.02		%

Note 2: For operating at elevated temperature, the device must be derated based on a thermal resistance of 115°C/W junction to ambient for the N package.

Note 3: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 4: The power dissipation limit, however, cannot be exceeded.

Note 5: These specifications apply for V_S = ±15V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. V_S = ±6V to ±15V.

Section 2
Amplifiers - High Speed

Section 2 Contents

National Semiconductor

CLC High Speed Amplifier Obsolescence

Dear CLC Customer,

It is with our sincere regret that we must inform you that we will be issuing a Life Time Buy Notice (LTB) in February 2002 on all National's CLC Amplifier products and the LM7131. This LTB does not include National's Data Acquisition and Serial Digital Interface CLC products or the CLC5506. The reason for this LTB and in particular the short notice is that we have been informed by Agere (Sept 2001), the outside fab that produces our CBIC wafers, that they no longer will be supporting us and they require we place our final orders by February 2002. In response we have stepped up our efforts to transfer the CLC products to National's recently released (Sept 2000) internal VIP10 bipolar process. The LM7131 has already been superceded by the LMH6642 with superior performance and lower cost. In transferring these CLC products, we will be assigning new part numbers with National's LMH prefix. Since our VIP10 complimentary bipolar process is a 'state of the art' complimentary bipolar process, specifically designed for optimizing high-speed amplifiers, as well as being completely internal to National, these new products will offer you superior performance with National's superior delivery and lower prices.

In April 2001 we debuted the VIP10 process with the first seven new LMH prefixed products. These products were designed in National's two new high-speed amplifier design centers. Future products will be supported by National's three dedicated high-speed design centers including one located in Fort Collins, Colorado that includes some of the original CLC amplifier engineers. Unfortunately, the sudden notice from Agere forces us to issue the LTB before we can fully complete the transfer. To lessen the impact on you, we will handle this as a normal obsolescence with a one-year (February 2002 to February 2003) window to accept delivery on LTB orders. Since VIP10 is a much faster process with much lower parasitic, the transferred parts may have slight differences in performance. Typically we are finding we can match or improve performance while reducing the required input power. We will try to minimize the differences between the CLC and LMH products so there will be little or no impact on your designs. Pin outs for these single, dual and quad amplifiers will also remain in the same standard configurations.

Again we apologize for any inconvenience and look forward to supporting you in the future.

Sincerely,

Amplifiers High Speed Marketing

National Semiconductor

High Speed Amplifiers/Buffers/Multiplexers/Variable Gain Amplifiers Selection Guide

TABLE 1. HISPEED

Part Number	Number of Channels	Features	Mode	BW (MHz)	Slew (V/ns)	I_{CC} mA/Ch typ	I_{OUT} mA	2nd/3rd HD (dBc)	NTSC Diff G/P %/deg	Settling Time (2V step) ns/%
LM6165	1	Low Noise, A_VC_L>25	VFB	725	300	5	65	N/A	0.1/0.1	80ns to 0.1%
LMH6654	1	V_{CM} to V−, High Output Drive	VFB	260	200	4.5	186	−80/−85 at 1MHz	0.1/0.025	14ns to 0.1%
LMH6655	2	V_{CM} to V−, High Output Drive	VFB	260	200	4.5	186	−80/−85 at 1MHz	0.1/0.025	14ns to 0.1%
LM7171	1	High Output Drive, Fast Slew, A_VC_L>2	VFB	200	4100	6.5	100	−7.5/−55 at 5MHz	0.01/0.02	42ns to 0.1%
LM6164	1	A_VC_L>5	VFB	175	300	5	65	N/A	0.1/0.1	100ns to 0.1%
LM7121	1	Fast Slew	VFB	175	1300	4.8	52	N/A	0.3/0.65	65ns to 0.1%
LMH6622	2	Low Noise, A_VC_L>2	VFB	160	80	4.3	90	−90/−100 at 1MHz	0.03/0.03	40ns to 0.1%
LMH6642	1	R-R Out, High Output Drive, Low Voltage	VFB	130	135	2.7	115	−80/−65 at 1MHz	0.01/0.01	68ns to 0.1%
LMH6643	2	R-R Out, High Output Drive, Low Voltage	VFB	130	135	2.7	115	−80/−65 at 1MHz	0.01/0.01	68ns to 0.1%
LMH6644	4	R-R Out, High Output Drive, Low Voltage	VFB	130	135	2.7	115	−80/−65 at 1MHz	0.01/0.01	68ns to 0.1%
LMH6672	2	V_{CM} to V−, High Output Drive, A_VC_L>2	VFB	130	170	6.2	200	−92/−95 at 1MHz	N/A	N/A
LM7372	2	High Output Drive, Fast Slew, A_VC_L>2	VFB	120	3000	6.5	250	−84/−94 at 1MHz	0.01/0.02	70ns to 0.1%
LM6162	1	A_VC_L>2	VFB	100	300	5	65	N/A	0.1/0.1	100ns to 0.1%
LM6171	1	High Output Drive, Fast Slew	VFB	100	3600	2.5	135	−50/−50 at 5MHz	0.03/0.5	48ns to 0.1%
LM6172	2	Fast Slew	VFB	100	3000	2.3	85	−50/−50 at 5MHz	0.28/0.6	65ns to 0.1%
LM6181	1	High Output Drive, Fast Slew	CFB	100	1400	7.5	130	−50/−55 at 10MHz	0.05/0.04	50ns to 0.1%
LMH6645	1	R-R In and Out, Low Voltage	VFB	55	40	0.725	20	−62/−72 at 1MHz	N/A	125ns to 0.1%
LMH6646	2	R-R In and Out, Low Voltage	VFB	55	40	0.725	20	−62/−72 at 1MHz	N/A	125ns to 0.1%
LMH6647	1	R-R In and Out, Disable, Low Voltage	VFB	55	40	0.725	20	−62/−72 at 1MHz	N/A	125ns to 0.1%
LM6121	1	High Output Drive	FGB	50	800	14	300	N/A	N/A	N/A
LM6125	1	Disable, High Output Drive	FGB	50	800	14	300	N/A	N/A	N/A
LM6161	1	High- Speed	VFB	50	200	5	65	N/A	0.1/0.1	120ns to 0.1%

TABLE 2. HISPEED

Part Number	V_{os} mV Typ/Temp Limit	Spec. Supply Voltage	Voltage Noise ($nV/\sqrt{Hz}$)	Current Noise ($pA/\sqrt{Hz}$)	Temp Range	Package	Eval Board	SPICE Model
LM6165	1/4	5V to 36V	5	1.5	M	J08, WG10	A	Y
LMH6654	1/4	4.5V to 12V	4.5	1.7	I	M08	A	Y
LMH6655	1/4	4.5V to 12V	4.5	1.7	I	M08, MM08	B, V	Y
LM7171	0.2/4, 0.2/7	5.5V to 36V	14	1.8	I, M	J08, M08, N08, W10, WG10	A	Y
LM6164	2/6	5V to 36V	8	1.5	M	J08, W10, WG10	A	Y
LM7121	1.5/8	4.5V to 33V	17	1.9	I	M08, MF05	A, L	Y
LMH6622	0.2/2	5V to 12V	1.6	1.5	I	M08, MM08	B, V	Y
LMH6642	1/7	2.7V to 12V	17	0.9	I	M08, MF05	A, L	Y
LMH6643	1/7	2.7V to 12V	17	0.9	I	M08	B, V	Y
LMH6644	1/7	2.7V to 12V	17	0.9	I	M14, MT14	E	Y
LMH6672	0.2/5.5	5V to 12V	4.5	1.7	I	M08, MP08	X	Y
LM7372	3/10	9V to 36V	14	1.5	I	L08, M16, MP08	Q, X	Y
LM6162	3/8	5V to 36V	10	1.2	M	J08, WG10	A	Y
LM6171	1.5/5, 1.5/8	5.5V to 36V	12	1	I	M08, N08	A	Y
LM6172	0.4/3.5, 0.4/4	5.5V to 36V	12	1	I	J08, M08, N08, WG16	B	Y
LM6181	3.5/5.5	7V to 32V	4	16	I	M08, M16, N08	A	Y
LMH6645	1/4	2.5V to 12V	17	0.75	I	M08, MF05	A, L	Y
LMH6646	1/4	2.5V to 12V	17	0.75	I	M08, MM08	B, L	Y
LMH6647	1/4	2.5V to 12V	17	0.75	I	M08, MF06	A, P	Y
LM6121	15/50	10V to 36V	N/A	N/A	M	H08, J08	-	Y
LM6125	15/50	10V to 36V	N/A	N/A	M	H08	-	Y
LM6161	5/10	4.75V to 36V	15	1.5	M	E20, J08, W10, WG10	A	Y

TABLE 3. RF/IF AMPLIFIER PRODUCT

Device	Single/Dual/ Triple/Quad	Signal Channel BW (MHz)	Control Channel BW (MHz)	Gain Adjust Range (dB)	Supply Voltage V_S (V)	Supply Current I_S (mA)	Noise Figure (dB)	Output IP3 (dBm)	Step Size (dB)	Temp Range	Pkg	Eval Board	Comments
CLC5506	S	600	600	26	+5	75	4.8	22	0.25	I	E	L	Gain Linear In dB

See Legend Information following these Selection Guides.

Legend Description

Temperature Range Codes

C	Commercial (0°C to + 70°C)
I	Industrial (–40°C to + 85°C)
M	Military (–55°C to +125°C)

All values are typical at room temperature unless otherwise specified.

Note 1: (Letter = Pkg. Type, Number = # of pins)

Package Codes

Code Letter	Package Type
BP	microSMD
E	LCC
H/G	Metal Can
J/D	Ceramic Dual-In-Line
K	Metal Can (TO-3)
M	SOIC
MF	TSSOP
MM	MSOP
M3	SOT23-3
M5	SOT23-5
M6	SOT23-6
N	Plastic Dual-In-Line (PDIP)
T	TO-220
V	PLCC
W	Flatpack
WG	Ceramic SOIC
Z	TO-92

Evaluation Board Codes

Code	DIP	SOIC		Code	DIP	SOIC
A	CLC730013	CLC730027		F	CLC730055	CLC730060
B	CLC730038	CLC730036		J	CLC730065	CLC730066
E	CLC730024	CLC730031		K	CLC730075	CLC730074

Code	Demo Board	Package
L	CLC730068	SOT-23-5
P	CLC730116	SOT-23-6
Q	CLC730114	LLP-8
U	CLC730102	CLC5506
V	CLC730123	MSOP-8
X	CLC730121	EPAD-8

Amplifier/Buffer Mode

CFB	Current Feedback
VFB	Voltage Feedback
FGB	Fixed Gain Buffer
PGB	Programmable Gain Buffer

Note 2: Closed Loop Gain used to specify most parameters.

Note 3: Spec. Supply Range is the range of total supply voltage where operation is possible but parameters are not necessarily guaranteed. Refer to datasheets for more details.

Note 4: Crosstalk tested at 10MHz, $2V_{pp}$.

Note 5: Harmonic Distortion at 5MHz, $2V_{pp}$.

National Semiconductor

High Speed Op Amp Definition Of Terms

Mode:

Voltage Feedback: The traditional Op Amp topology where an output signal is generated in response to the voltage difference between the two inputs.

Current Feedback: Op amp which generates an output signal in response to the current flowing into the inverting input node (transimpedance gain function). This topology offers operational advantages in certain areas, compared to the traditional voltage feedback.

Close Loop Buffer: High input impedance and low output impedance amplifier with a fixed gain of +1 used for isolation, or increased output drive, or capacitive load drive, etc. usually, no gain setting resistor are required.

Programmable Gain Buffer: Op Amp with gain setting resistors integrated on the die with possible gains of +1, +2, or −1 using simple external connections. Ideal for minimizing external component count, minimizing signal lead lengths, and simplifying designs.

Gain:

Open Loop Gain

Voltage feedback Op Amp: The open loop gain is specified at DC and is defined as the ratio of an output voltage change to an input voltage change. Also referred to as differential voltage gain (no feedback or input networks added). When specified using a sinusoidal waveform, it varies in magnitude and phase relative to frequency.

Current Feedback Op Amp: Ratio of output voltage change to Inverting input current change (transimpedance gain). When specified using a sinusoidal waveform, it varies in magnitude and phase relative to frequency.

Closed Loop Gain: Defined as the ratio of an output voltage change to an input voltage change after feedback and input networks are added. Usually, external resistors are used to set this parameter.

Frequency Domain Response:

−3dB Bandwidth (or small signal bandwidth (ssbw)): The frequency at which the closed loop amplifier small signal magnitude response is 3dB below its nominal value at low frequency. Sometimes specified for various signal amplitudes.

Gain Bandwidth Product: Arithmetic Product of a given input frequency and the op amp open loop gain at that frequency (usually specified in MHz, voltage feedback amplifiers only.) For an ideal op amp, this is a constant for all frequency after the dominant pole frequency, but other poles and zeroes in the forward path could make the number vary with frequency.

Unity Gain Frequency: The frequency at which a voltage feedback op amp gain is 1 (0dB). For an ideal op amp, this is equal to the Gain Bandwidth product.

Gain Flatness: Specified as "Peaking" and "Rolloff" numbers in dB over a given frequency band, its a measure of an op amp's closed loop frequency response gain flatness. Phase margin, Gain margin, and sufficient loop gain are the most important parameters affecting these specifications.

Linear Phase Deviation: Specified over a given frequency band, it is a measure of how close an op amp's closed loop phase response follows a linear relationship with respect to frequency.

Differential Gain and Phase: Differential Gain refers to change in gain with level and differential Phase refers to change in phase with level. Both parameters are used in video broadcast applications as a measure of consistency of video signal relative to changes in illumination.

Time Domain Response:

Rise an Fall Times: The time it takes the output voltage to change between 10% and 90% voltage levels when driven with a small signal step input. Correlates to frequency domain small signal bandwidth.

Overshoot: Related to Rise and Fall time measurement. Specified in percentage.

Slew Rate: Maximum rate at which an overdriven op amp can change its output. Overdriving an op amp means exceeding its input voltage amplitude and/or frequency thresholds.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Distortion and Noise Response:

Harmonic Distortion: Unwanted spurious signals generated at the output of an amplifier due to nonlinearity in the signal flow path. With sinusoidal input, these spurs will occur at integer multiples of the input frequency.

Intercept point: The fundamental output power where the specified distortion term (2^{nd},3^{rd}, or 3^{rd} order Intermodulation) is equal in power to this fundamental value power.

Input Voltage Noise (e_n) & Input Current Noise (i_n): Input referred noise sources used to model the noise behavior of an Op Amp.

Static DC Performance:

Supply Current (I_{CC}): The current required from the power supply to operate the op amp with no load and its output midway between the supplies.

Output Current: the current available at the output of the op amp to drive a load. Usually a function of input over-drive, output voltage relative to supplies, and temperature. Sourcing and Sinking characteristics could be different.

Static DC Performance: (Continued)

Input Offset Voltage (V_{OS}): The voltage which must be applied between the input terminals to obtain zero output voltage.

Specified Supply Range: Specified supply range are the power supply voltages required to power the op amp.

National Semiconductor

CLC5506
Gain Trim Amplifier (GTA)

General Description

The CLC5506 is a low noise amplifier with programmable gain for use in cellular base stations, WLL, radar and RF/IF subsystems where gain control is required to increase the dynamic range. The CLC5506 allows designers to compensate for manufacturing component tolerances and temperature variations in receiver front ends. Maximum amplifier gain is set at 26dB . A three-line MICROWIRE serial interface allows 16dB of attenuation from the max gain setting in precise 0.25dB steps.

The CLC5506 uses a differential input and output, allowing large output swings on a single 5V rail. The differential output is well suited for impedance matching networks driving SAW filters or directly driving differential input analog to digital converters (ADC). The differential output also makes it possible to drive transformers allowing designers the ability to match a wide variety of transmission lines. The output amplifier has excellent output drive with low distortion.

Digital control of the CLC5506 is accomplished using MICROWIRE Interface. Data Out and a Load Enable are incorporated so that more than one CLC5506/channel may be programmed per system.

The CLC5506 maintains a 600MHz performance bandwidth over its entire gain and attenuation range from +10dB to +26dB. Gain control is divided into 64 equal steps of 0.25dB and is dB-linear. Output drive and distortion performance are excellent; In a 50Ω system, the third-order output intercept point is +22dBm at nominal gain of 18dB at 25°C. The CLC5506 operates over the industrial temperature range of −40°C to +85°C.

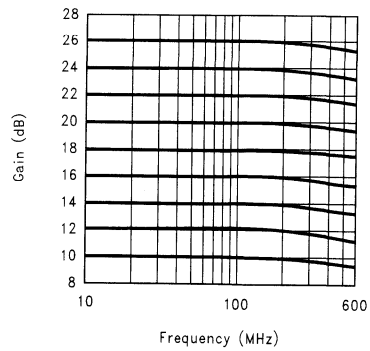
Features

- 600MHz bandwidth
- 26dB maximum gain @ 150MHz
- 16dB gain control range
- Attenuation step size: 0.25dB
- 4.8dB noise figure @ 26dB
- +22dBm output IP3 @ 18dB gain
- Digital 'dB Linear' gain control
- Supply voltage: 5V
- Supply current: 75mA
- Supply shutdown: 35µA
- Package: SOIC-14
- Typical at 25°C

Applications

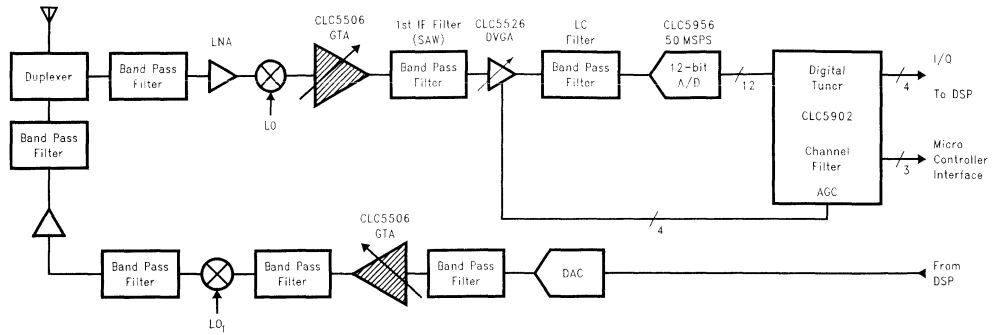
- Cellular base-stations
- Base station repeater
- Wireless Local Loop
- Radar
- Receivers
- IF amplifiers
- Digital IF receiver
- Software radio
- Satellite communications

Frequency Response vs. Gain Setting



DS101050-1

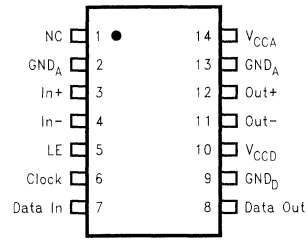
Typical Application



DS101050-2

Connection Diagram

CLC5506 Pin Diagram



DS101050-3

Top View

Pin #	Pin Name	Description
1	NC	No connection
2	GND_A	Analog ground
3	In+	Positive differential input
4	In−	Negative differential input
5	LE	MICROWIRE load enable input. High impedance CMOS input with Schmitt trigger
6	Clock	MICROWIRE clock input. High impedance CMOS input with Schmitt trigger. Data is clocked in on the rising edge of clock.
7	Data In	MICROWIRE data input. High impedance CMOS input with Schmitt trigger. Binary serial data. Data entered Power Down first.
8	Data Out	MICROWIRE data output. High impedance CMOS input with Schmitt trigger.
9	GND_D	Digital ground
10	V_{CCD}	Digital supply voltage
11	Out−	Negative differential Output
12	Out+	Positive differential output
13	GND_A	Analog ground
14	V_{CCA}	Analog supply voltage

Ordering Information

Package	Temperature Range	Part Number	Package Marking	NSC Drawing
SO-14	–40°C to +85°C	CLC5506IM	CLC5506IM	M14a
		CLC5506IMX	CLC5506IM	
N/A	–40°C to +85°C	CLC5506PCASM	N/A	Fully loaded evaluation board

National Semiconductor

LM6121/LM6221/LM6321
High Speed Buffer

General Description

These high speed unity gain buffers slew at 800 V/µs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

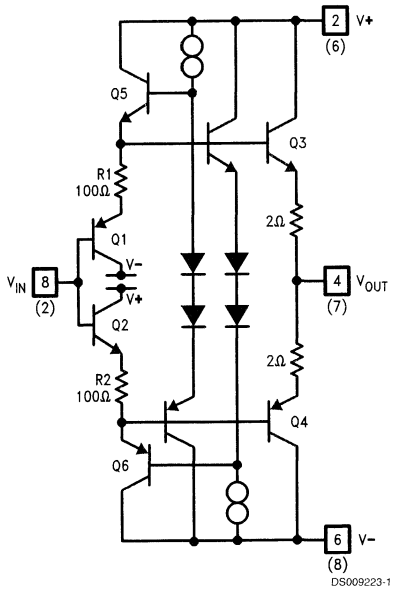
Features

- High slew rate: 800 V/µs
- Wide bandwidth: 50 MHz
- Slew rate and bandwidth 100% tested
- Peak output current: ±300 mA
- High input impedance: 5 MΩ
- LH0002H pin compatible
- No oscillations with capacitive loads
- 5V to ±15V operation guaranteed
- Current and thermal limiting
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

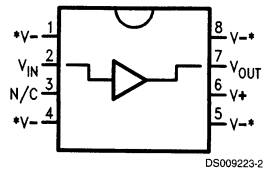
Simplified Schematic



Numbers in ( ) are for 8-pin N DIP.

Connection Diagrams

Plastic DIP

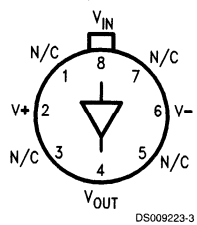


DS009223-2

*Heat-sinking pins. See Application section on heat sinking requirements.

Order Number LM6221N, LM6321N or LM6121J/883
See NS Package Number J08A or N08E

Metal Can

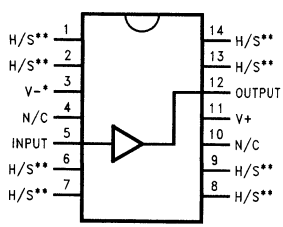


DS009223-3

Note: Pin 6 connected to case.

Top View
Order Number LM6221H or LM6121H/883
See NS Package Number H08C

Plastic SO



DS009223-7

*Pin 3 must be connected to the negative supply.
**Heat-sinking pins. See Application section on heat-sinking requirements.
These pins are at V^- potential.

Order Number LM6321M
See NS Package Number M14A

National Semiconductor

LM6125/LM6225/LM6325
High Speed Buffer

General Description

The LM6125 family of high speed unity gain buffers slew at 800 V/µs and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive ±300 mA peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

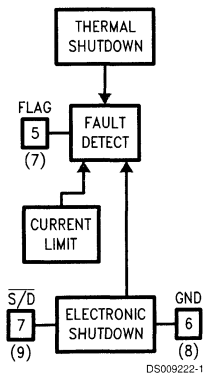
Features

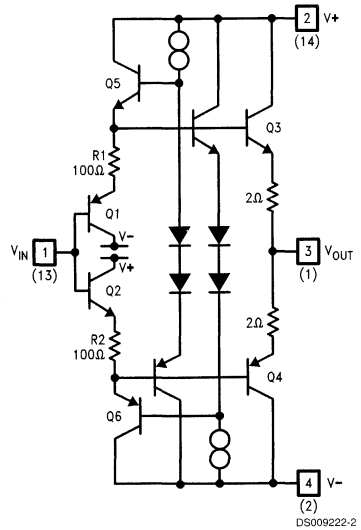
- High slew rate: 800 V/µs
- High output current: ±300 mA
- Stable with large capacitive loads
- Current and thermal limiting
- Electronic shutdown
- 5V to ±15V operation guaranteed
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

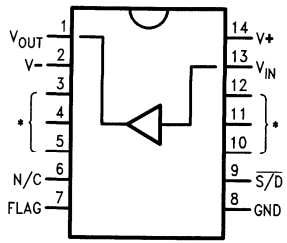
Simplified Schematic and Block Diagram





Numbers in () are for 14-pin N DIP.

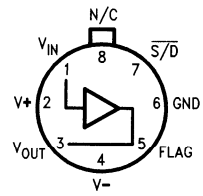
Pin Configurations



DS009222-3

*Heat sinking pins.
Internally connected to V−.

Order Number LM6225N
or LM6325N
See NS Package Number N14A



DS009222-4

Note: Pin 4 connected to case

Top View
Order Number LM6125H/883 (Note 1)
or LM6125H
See NS Package Number H08C

Note 1: Available per 5962-9081501

National Semiconductor

LM6161/LM6261/LM6361
High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/μs and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

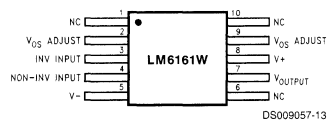
- High slew rate 300 V/μs
- High unity gain freq 50 MHz
- Low supply current 5 mA
- Fast settling 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase 0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

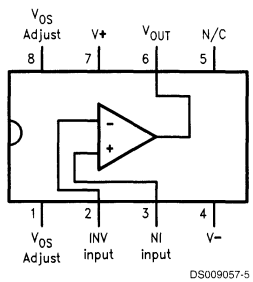
- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams

10–Lead Flatpak



See NS Package Number W10A



See NS Package Number J08A, N08E or M08A

Temperature Range			Package	NSC Drawing
Military $-55°C \le T_A \le +125°C$	Industrial $-25°C \le T_A \le +85°C$	Commercial $0°C \le T_A \le +70°C$		
	LM6261N	LM6361N	8-Pin Molded DIP	N08E
LM6161J/883 5962-8962101PA		LM6361J	8-Pin Ceramic DIP	J08A
	LM6261M	LM6361M	8-Pin Molded Surface Mt.	M08A
LM6161WG/883 5962-8962101XA			10-Lead Ceramic SOIC	WG10A
LM6161W/883 5962-8962101HA			10-Pin Ceramic Flatpak	W10A

National Semiconductor

LM6162
High Speed Operational Amplifier

General Description

The LM6162 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/µs and 100 MHz gain-bandwidth product (stable for gains as low as +2 or −1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

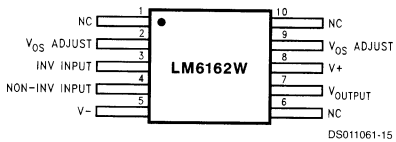
- High slew rate: 300 V/µs
- High gain-bandwidth product: 100 MHz
- Low supply current: 5 mA
- Fast settling time: 120 ns to 0.1%
- Low differential gain: <0.1%
- Low differential phase: <0.1°
- Wide supply range: 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

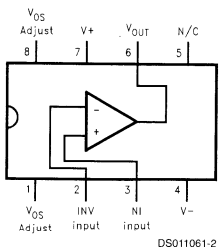
- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

Connection Diagrams

10-Pin Ceramic Flatpak



Top View
See NS Package Number W10A



See NS Package Number N08E or J08A

Ordering Information

Temperature Range			Package	NSC Drawing
Military $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	Industrial $-25^{\circ}C \leq T_A \leq +85^{\circ}C$	Commercial $0^{\circ}C \leq T_A \leq +70^{\circ}C$		
LM6162N			8-Pin Molded DIP	N08E
LM6162J/883 5962-9216501PA			8-Pin Ceramic DIP	J08A
LM6162WG/883 5962-9216501XA			10-Lead Ceramic SOIC	WG10A
LM6162W/883 5962-9216501HA			10-Pin Ceramic Flatpak	W10A

National Semiconductor

LM6164/LM6264/LM6364
High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per µs and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

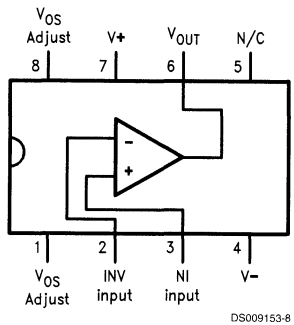
Features

- High slew rate: 300 V/µs
- High GBW product: 175 MHz
- Low supply current: 5 mA
- Fast settling: 100 ns to 0.1%
- Low differential gain: <0.1%
- Low differential phase: <0.1°
- Wide supply range: 4.75V to 32V
- Stable with unlimited capacitive load

Applications

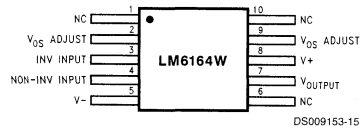
- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams



NS Package Number J08A, M08A or N08E

10-Lead Flatpak



Top View
NS Package Number W10A

Ordering Information

Temperature Range			Package	NSC Drawing
Military $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	Industrial $-25^{\circ}C \leq T_A \leq +85^{\circ}C$	Commercial $0^{\circ}C \leq T_A \leq +70^{\circ}C$		
	LM6264N	LM6364N	8-Pin Molded DIP	N08E
LM6164J/883 5962-8962401PA			8-Pin Ceramic DIP	J08A
		LM6364M	8-Pin Molded Surface Mt.	M08A
LM6164WG/883 5962-8962401XA			10-Lead Ceramic SOIC	WG10A
LM6164W/883 5962-8962401HA			10-Pin Ceramic Flatpak	W10A

National Semiconductor

LM6165/LM6265/LM6365
High Speed Operational Amplifier

General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/µs and 725 MHz GBW (stable for gains as low as +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIP™ (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

- High GBW product: 725 MHz
- Low supply current: 5 mA
- Fast settling: 80 ns to 0.1%
- Low differential gain: <0.1%
- Low differential phase: <0.1°
- Wide supply range: 4.75V to 32V
- Stable with unlimited capacitive load

Applications

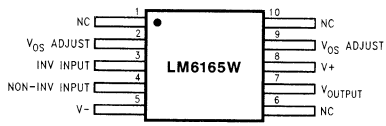
- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Features

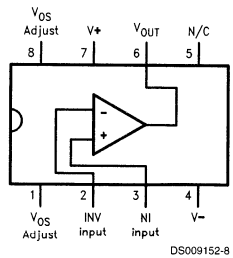
- High slew rate: 300 V/µs

Connection Diagrams

10-Lead Flatpak
Top View



Order Number LM6165W/883
See NS Package Number W10A



Order Number LM6165J/883
See NS Package Number J08A
Order Number LM6365M
See NS Package Number M08A
Order Number LM6265N or LM6365N
See NS Package Number N08E

Ordering Information

Temperature Range			Package	NSC Drawing
Military $-55^{\circ}C \leq T_A \leq +125^{\circ}C$	Industrial $-25^{\circ}C \leq T_A \leq +85^{\circ}C$	Commercial $0^{\circ}C \leq T_A \leq +70^{\circ}C$		
	LM6265N	LM6365N	8-Pin Molded DIP	N08E
LM6165J/883 5962-8962501PA			8-Pin Ceramic DIP	J08A
		LM6365M	8-Pin Molded Surface Mt.	M08A
LM6165WG/883 5962-8962501XA			10-Lead Ceramic SOIC	WG10A
LM6165W883 5962-8962501HA			10-Pin Ceramic Flatpak	W10A

National Semiconductor

LM6171
High Speed Low Power Low Distortion Voltage Feedback Amplifier

General Description

The LM6171 is a high speed unity-gain stable voltage feedback amplifier. It offers a high slew rate of 3600V/µs and a unity-gain bandwidth of 100 MHz while consuming only 2.5 mA of supply current. The LM6171 has very impressive AC and DC performance which is a great benefit for high speed signal processing and video applications.

The ±15V power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM6171 has high output current drive, low SFDR and THD, ideal for ADC/DAC systems. The LM6171 is specified for ±5V operation for portable applications.

The LM6171 is built on National's advanced VIP™ III (Vertically Integrated PNP) complementary bipolar process.

Features

(Typical Unless Otherwise Noted)

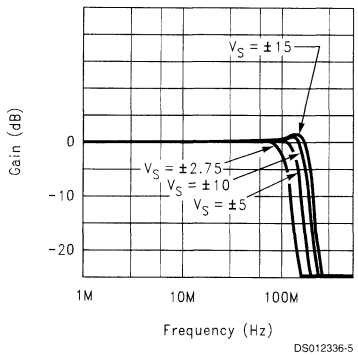
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate: 3600V/µs
- Wide Unity-Gain-Bandwidth Product: 100 MHz
- −3 dB Frequency @ A_V = +2: 62 MHz
- Low Supply Current: 2.5 mA
- High CMRR: 110 dB
- High Open Loop Gain: 90 dB
- Specified for ±15V and ±5V Operation

Applications

- Multimedia Broadcast Systems
- Line Drivers, Switchers
- Video Amplifiers
- NTSC, PAL® and SECAM Systems
- ADC/DAC Buffers
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- Instrumentation Amplifier
- Active Filters

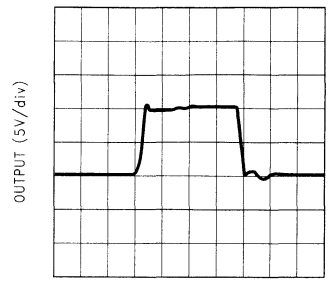
Typical Performance Characteristics

Closed Loop Frequency Response vs Supply Voltage (A_V = +1)



DS012336-5

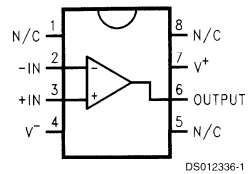
Large Signal Pulse Response A_V = +1, V_S = ±15



DS012336-9

Connection Diagram

8-Pin DIP/SO



Top View

Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	Transport Media	NSC Drawing
8-Pin Molded DIP	LM6171AIN LM6171BIN	Rails	N08E
8-Pin Small Outline	LM6171AIM, LM6171BIM	Rails	M08A
	LM6171AIMX, LM6171BIMX	Tape and Reel	

National Semiconductor

LM6172
Dual High Speed, Low Power, Low Distortion, Voltage Feedback Amplifiers

General Description

The LM6172 is a dual high speed voltage feedback amplifier. It is unity-gain stable and provides excellent DC and AC performance. With 100 MHz unity-gain bandwidth, 3000V/µs slew rate and 50 mA of output current per channel, the LM6172 offers high performance in dual amplifiers; yet it only consumes 2.3 mA of supply current each channel.

The LM6172 operates on ±15V power supply for systems requiring large voltage swings, such as ADSL, scanners and ultrasound equipment. It is also specified at ±5V power supply for low voltage applications such as portable video systems.

The LM6172 is built with National's advanced VIP™ III (Vertically Integrated PNP) complementary bipolar process. See the LM6171 datasheet for a single amplifier with these same features.

Features

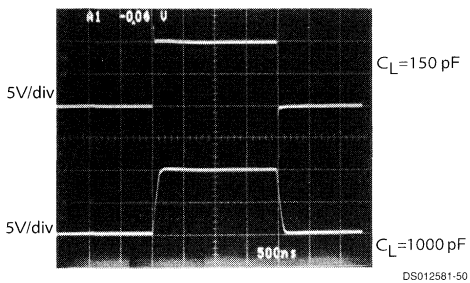
(Typical Unless Otherwise Noted)

- Easy to Use Voltage Feedback Topology
- High Slew Rate 3000V/µs
- Wide Unity-Gain Bandwidth 100 MHz
- Low Supply Current 2.3 mA/Channel
- High Output Current 50 mA/channel
- Specified for ±15V and ±5V Operation

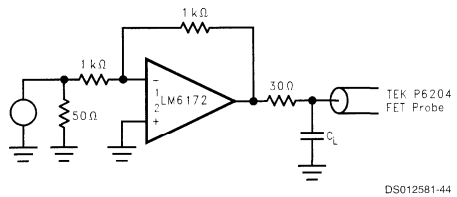
Applications

- Scanner I-to-V Converters
- ADSL/HDSL Drivers
- Multimedia Broadcast Systems
- Video Amplifiers
- NTSC, PAL® and SECAM Systems
- ADC/DAC Buffers
- Pulse Amplifiers and Peak Detectors

LM6172 Driving Capacitive Load



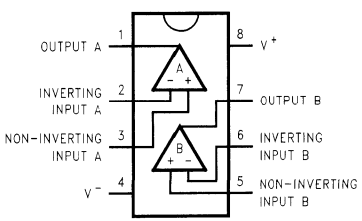
DS012581-50



DS012581-44

Connection Diagram

8-Pin DIP/SO



DS012581-1

Top View

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40°C to +85°C	Military −55°C to +125°C		
8-Pin DIP	LM6172IN		Rails	N08E
8-Pin CDIP	LM6172AMJ-QML	5962-95604	Rails	J08A
10-Pin Ceramic SOIC	LM6172AMWG-QML	5962-95604	Trays	WG10A
8-Pin Small Outline	LM6172IM		Rails	M08A
	LM6172IMX		Tape and Reel	

National Semiconductor

LM6181
100 mA, 100 MHz Current Feedback Amplifier

General Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin DIP high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at A_V = −1, 60 MHz at A_V = −10. With a slew rate of 2000V/µs, 2nd harmonic distortion of −50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

Features

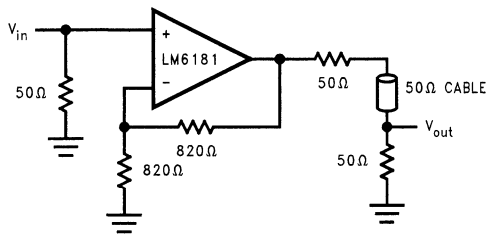
(Typical unless otherwise noted)

- Slew rate: 2000 V/µs
- Settling time (0.1%): 50 ns
- Characterized for supply ranges: ±5V and ±15V
- Low differential gain and phase error: 0.05%, 0.04°
- High output drive: ±10V into 100Ω
- Guaranteed bandwidth and slew rate
- Improved performance over EL2020, OP160, AD844, LT1223 and HA5004

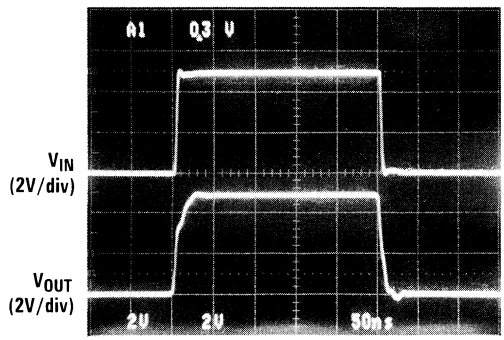
Applications

- Coax cable driver
- Video amplifier
- Flash ADC buffer
- High frequency filter
- Scanner and Imaging systems

Typical Application



Cable Driver



National Semiconductor

LM7121
235 MHz Tiny Low Power Voltage Feedback Amplifier

General Description

The LM7121 is a high performance operational amplifier which addresses the increasing AC performance needs of video and imaging applications, and the size and power constraints of portable applications.

The LM7121 can operate over a wide dynamic range of supply voltages, from 5V (single supply) up to ±15V (see the Application Information section for more details). It offers an excellent speed-power product delivering 1300V/µs and 235 MHz Bandwidth (−3 dB, A_V = +1). Another key feature of this operational amplifier is stability while driving unlimited capacitive loads.

Due to its Tiny SOT23-5 package, the LM7121 is ideal for designs where space and weight are the critical parameters. The benefits of the Tiny package are evident in small portable electronic devices, such as cameras, and PC video cards. Tiny amplifiers are so small that they can be placed anywhere on a board close to the signal source or near the input to an A/D converter.

Features

(Typical unless otherwise noted) V_S = ±15V

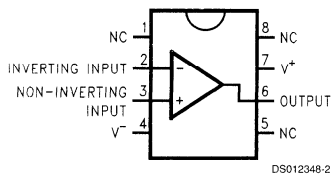
- Easy to use voltage feedback topology
- Stable with unlimited capacitive loads
- Tiny SOT23-5 package—typical circuit layout takes half the space of SO-8 designs
- Unity gain frequency: 175 MHz
- Bandwidth (−3 dB, A_V = +1, R_L = 100Ω): 235 MHz
- Slew rate: 1300V/µs
- Supply Voltages SO-8: 5V to ±15V
  SOT23-5: 5V to ±5V
- Characterized for: +5V, ±5V, ±15V
- Low supply current: 5.3 mA

Applications

- Scanners, color fax, digital copiers
- PC video cards
- Cable drivers
- Digital cameras
- ADC/DAC buffers
- Set-top boxes

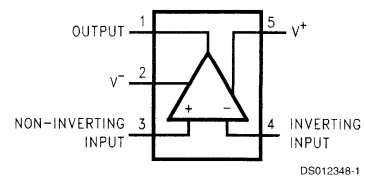
Connection Diagrams

8-Pin SO-8



Top View

5-Pin SOT23



Top View

Ordering Information

Package	Ordering Information	NSC Drawing Number	Package Marking	Supplied As
8-Pin SO-8	LM7121IM	M08A	LM7121IM	Rails
	LM7121IMX	M08A	LM7121IM	2.5k Tape and Reel
5-Pin SOT23-5	LM7121IM5	MA05A	A03A	1k Tape and Reel
	LM7121IM5X	MA05A	A03A	3k Tape and Reel

National Semiconductor

LM7171
Very High Speed, High Output Current, Voltage Feedback Amplifier

General Description

The LM7171 is a high speed voltage feedback amplifier that has the slewing characteristic of a current feedback amplifier; yet it can be used in all traditional voltage feedback amplifier configurations. The LM7171 is stable for gains as low as +2 or −1. It provides a very high slew rate at 4100V/µs and a wide unity-gain bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as HDSL and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for ±5V operation for portable applications.

The LM7171 is built on National's advanced VIP™ III (Vertically integrated PNP) complementary bipolar process.

Features

(Typical Unless Otherwise Noted)

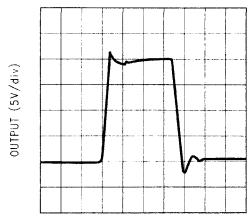
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate: 4100V/µs
- Wide Unity-Gain Bandwidth: 200 MHz
- −3 dB Frequency @ A_V = +2: 220 MHz
- Low Supply Current: 6.5 mA
- High Open Loop Gain: 85 dB
- High Output Current: 100 mA
- Differential Gain and Phase: 0.01%, 0.02°
- Specified for ±15V and ±5V Operation

Applications

- HDSL and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

Typical Performance

Large Signal Pulse Response
A_V = +2, V_S = ±15V



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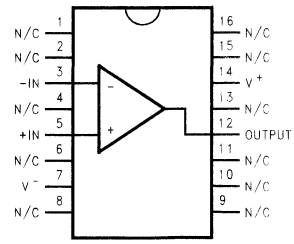
16-Pin Wide Body SO

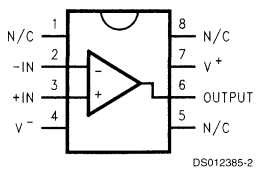


DS012385-3

Top View

Connection Diagrams

8-Pin DIP/SO



DS012385-2

Top View

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40°C to +85°C	Military −55°C to +125°C		
8-Pin DIP	LM7171AIN, LM7171BIN		Rails	N08E
8-Pin CDIP	LM7171AMJ-QML LM7171AMJ-QMLV	5962-95536	Rails	J08A
10-Pin Ceramic SOIC	LM7171AMWG-QML LM7171AMWG-QMLV	5962-95536	Trays	WG10A
8-Pin Small Outline	LM7171AIM, LM7171BIM		Rails	M08A
	LM7171AIMX, LM7171BIMX		Tape and Reel	
16-Pin Small Outline	LM7171AIWM, LM7171BIWM		Rails	M16B
	LM7171AWMX, LM7171BWMX		Tape and Reel	

National Semiconductor

LM7372
High Speed, High Output Current, Dual Operational Amplifier

General Description

The LM7372 is a high speed dual voltage feedback amplifier that has the slewing characteristic of current feedback amplifiers; yet it can be used in all traditional voltage feedback amplifier configurations.

The LM7372 is stable for gains as low as +2 or −1. It provides a very high slew rate at 3000V/µs and a wide gain bandwidth product of 120MHz, while consuming only 6.5mA/per amplifier of supply current. It is ideal for video and high speed signal processing applications such as xDSL and pulse amplifiers. With 150mA output current, the LM7372 can be used for video distribution, as a transformer driver or as a laser diode driver.

Operation on ±15V power supplies allows for large signal swings and provides greater dynamic range and signal-to-noise ratio. The LM7372 offers high SFDR and low THD, ideal for ADC/DAC systems. In addition, the LM7372 is specified for ±5V operation for portable applications.

The LM7372 is built on National's Advance VIP™ III (Vertically integrated PNP) complementary bipolar process.

Features

- −80dBc highest harmonic distortion @1MHz, $2V_{PP}$
- Very high slew rate: 3000V/µs
- Wide gain bandwidth product: 120MHz
- −3dB frequency @ A_V = +2: 200MHz
- Low supply current: 13mA (both amplifiers)
- High open loop gain: 85dB
- High output current: 150mA
- Differential gain and phase: 0.01%, 0.02°

Applications

- HDSL and ADSL Drivers
- Multimedia broadcast systems
- Professional video cameras
- CATV/Fiber optics signal processing
- Pulse amplifiers and peak detectors
- HDTV amplifiers

Typical Application

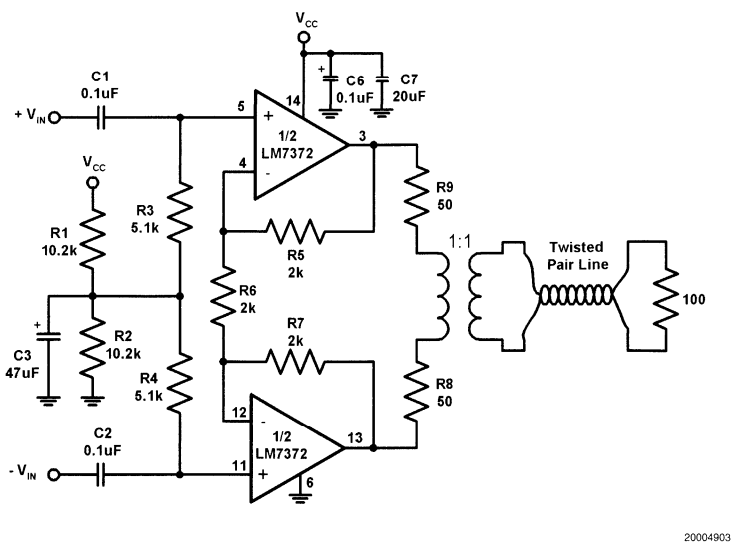
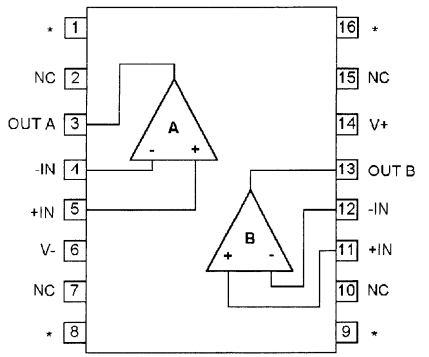


FIGURE 1. Single Supply Application (SOIC-16)

Connection Diagrams

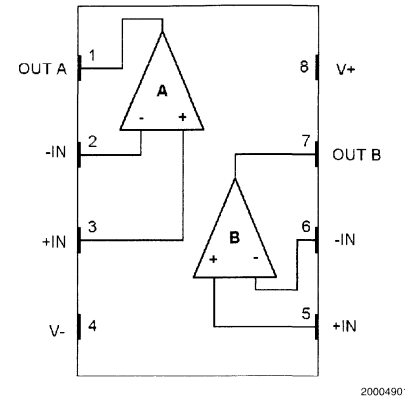
16-Pin SOIC



Top View

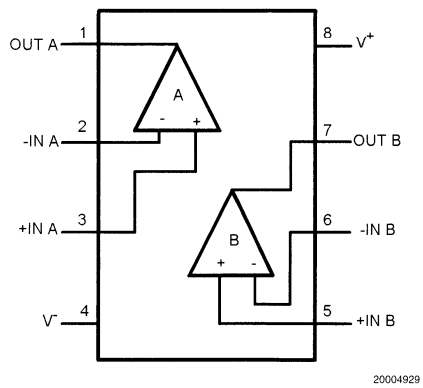
* Heatsink Pins. See note 4

8-Contact LLP



Top View

8-Pin PSOP



Top View

For PSOP SOIC-8 the exposed pad should be tied either to V^- or left electrically floating. (die attach material is conductive and is internally tied to V^-)

Ordering Information

Symbol	Temperature Range	Package Markiing	Transport Media	NSC Drawing
	−40˚C to +85˚C			
16-Pin SOIC	LM7372IMA	LM7372IMA	Rails	M16A
	LM7372IMAX	LM7372IMA	2.5k Units Tape and Reel	
8-Pin LLP	LM7372ILD	L7372	1k Units Tape and Reel	LDC08A
	LM7372ILDX	L7372	4.5k Units Tape and Reel	
8-Pin PSOP	LM7372MR	LM7372MR	Rails	MRA08A
	LM7372MRX	LM7372MR	2.5k Units Tape and Reel	

National Semiconductor

LMH6622
Dual Wideband, Low Noise, 160MHz, Operational Amplifiers

General Description

The LMH6622 is a dual high speed voltage feedback operational amplifier specifically optimized for low noise. A voltage noise specification of 1.6nV/ $\sqrt{Hz}$, a current noise specification 1.5pA/ $\sqrt{Hz}$, a bandwidth of 160MHz, and a harmonic distortion specification that exceeds 90dBc combine to make the LMH6622 an ideal choice for the receive channel amplifier in ADSL, VDSL, or other xDSL designs. The LMH6622 operates from ±2.5V to ±6V in dual supply mode and from +5V to +12V in single supply configuration. The LMH6622 is stable for $A_V \geq 2$ or $A_V \leq -1$. The fabrication of the LMH6622 on National Semiconductor's advanced VIP10 process enables excellent (160MHz) bandwidth at a current consumption of only 4.3mA/amplifier. Packages for this dual amplifier are the 8-lead SOIC and the 8-lead MSOP.

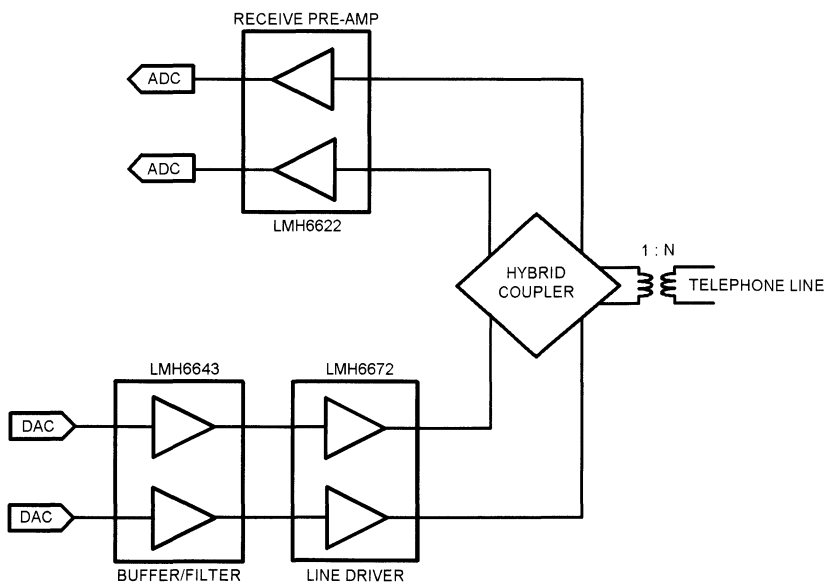
Features

V_S = ±6V, T_A = 25°C, Typical values unless specified

- Bandwidth (A_V = +2) 160MHz
- Supply Voltage Range ±2.5V to ±6V +5V to +12
- Slew rate 85V/µs
- Supply current 4.3mA/amp
- Input common mode voltage −4.75V to +5.7V
- Output Voltage Swing (R_L = 100Ω) ±4.6V
- Input voltage noise 1.6nV/ $\sqrt{Hz}$
- Input current noise 1.5pA/ $\sqrt{Hz}$
- Linear output current 90mA
- Excellent harmonic distortion 90dBc

Applications

- xDSL receiver
- Low noise instrumentation front end
- Ultrasound preamp
- Active filters
- Cellphone basestation



xDSL Analog Front End

National Semiconductor

LMH6642/6643/6644
3V, Low Power, 130MHz, 75mA Rail-to-Rail Output Amplifiers

General Description

The LMH664X family true single supply voltage feedback amplifiers offer high speed (130MHz), low distortion (−62dBc), and exceptionally high output current (approximately 75mA) at low cost and with reduced power consumption when compared against existing devices with similar performance.

Input common mode voltage range extends to 0.5V below V^- and 1V from V^+. Output voltage range extends to within 40mV of either supply rail, allowing wide dynamic range especially desirable in low voltage applications. The output stage is capable of approximately 75mA in order to drive heavy loads. Fast output Slew Rate (130V/µs) ensures large peak-to-peak output swings can be maintained even at higher speeds, resulting in exceptional full power bandwidth of 40MHz with a 3V supply. These characteristics, along with low cost, are ideal features for a multitude of industrial and commercial applications.

Careful attention has been paid to ensure device stability under all operating voltages and modes. The result is a very well behaved frequency response characteristic (0.1dB gain flatness up the 12MHz under 150Ω load and A_V = +2) with minimal peaking (typically 2dB maximum) for any gain setting and under both heavy and light loads. This along with fast settling time (68ns) and low distortion allows the device to operate well in ADC buffer, and high frequency filter applications as well as other applications.

This device family offers professional quality video performance with low DG (0.01%) and DP (0.01°) characteristics. Differential Gain and Differential Phase characteristics are also well maintained under heavy loads (150Ω) and throughout the output voltage range. The LMH664X family is offered in single (LMH6642), dual (LMH6643), and quad (LMH6644) options. See ordering information for packages offered.

Features

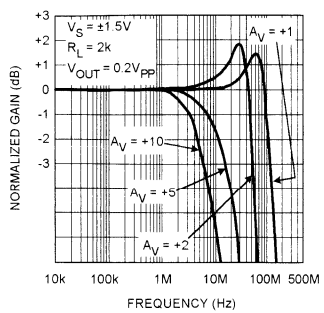
(V_S = ±5V, T_A = 25°C, R_L = 2kΩ, A_V = +1. Typical values unless specified).

- −3dB BW (A_V = +1) 130MHz
- Supply voltage range 3V to 12.8V
- Slew rate (Note 8), (A_V = −1) 130V/µs
- Supply current (no load) 2.7mA/amp
- Output short circuit current +115mA/−145mA
- Linear output current ±75mA
- Input common mode volt. 0.5V beyond V^-, 1V from V^+
- Output voltage swing 40mV from rails
- Input voltage noise (100kHz) 17nV/$\sqrt{Hz}$
- Input current noise (100kHz) 0.9pA/$\sqrt{Hz}$
- THD (5MHz, R_L = 2kΩ, V_O = $2V_{PP}$, A_V = +2) −62dBc
- Settling time 68ns
- Fully characterized for 3V, 5V, and ±5V
- Overdrive recovery 100ns
- Output short circuit protected (Note 11)
- No output phase reversal with CMVR exceeded

Applications

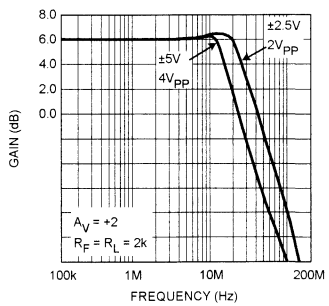
- Active filters
- CD/DVD ROM
- ADC buffer amp
- Portable video
- Current sense buffer

Closed Loop Gain vs. Frequency for Various Gain



20018535

Large Signal Frequency Response



20018547

National Semiconductor

LMH6645/46/47
2.7V, 650µA, 55MHz, Rail-to-Rail Input and Output Amplifiers with Shutdown Option

General Description

The LMH6645 (single) and LMH6646 (dual), rail-to-rail input and output voltage feedback amplifiers, offer high speed (55MHz), and low voltage operation (2.7V) in addition to micro-power shutdown capability (LMH6647, single).

Input common mode voltage range exceeds either supply by 0.3V, enhancing ease of use in multitude of applications where previously only inferior devices could be used. Output voltage range extends to within 20mV of either supply rails, allowing wide dynamic range especially in low voltage applications. Even with low supply current of 650µA/amplifier, output current capability is kept at a respectable ±20mA for driving heavier loads. Important device parameters such as BW, Slew Rate and output current are kept relatively independent of the operating supply voltage by a combination of process enhancements and design architecture.

In portable applications, the LMH6647 provides shutdown capability while keeping the turn-off current to less than 50µA. Both turn-on and turn-off characteristics are well behaved with minimal output fluctuations during transitions. This allows the part to be used in power saving mode, as well as multiplexing applications. Miniature packages (SOT23, MSOP-8, and SO-8) are further means to ease the adoption of these low power high speed devices in applications where board area is at a premium.

Features

(V_S = 2.7V, T_A = 25°C, R_L = 1kΩ to $V^+/2$, A_V = +1. Typical values unless specified).

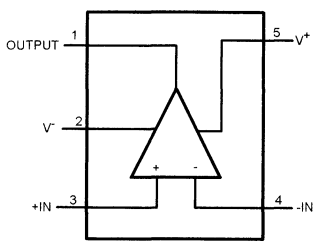
■ –3dB BW	55MHz
■ Supply voltage range	2.5V to 12V
■ Slew rate	22V/µs
■ Supply current	650µA/channel
■ Output short circuit current	42mA
■ Linear output current	±20mA
■ Input common mode voltage	0.3V beyond rails
■ Output voltage swing	20mV from rails
■ Input voltage noise	17nV/ $\sqrt{Hz}$
■ Input current noise	0.75pA/ $\sqrt{Hz}$

Applications

- Active filters
- High speed portable devices
- Multiplexing applications (LMH6647)
- Current sense buffer
- High speed transducer amp

Connection Diagrams

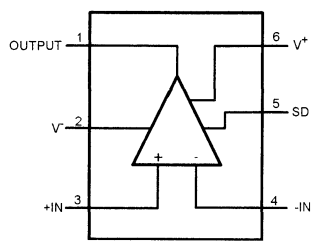
SOT23-5 (LMH6645)



20020259

Top View

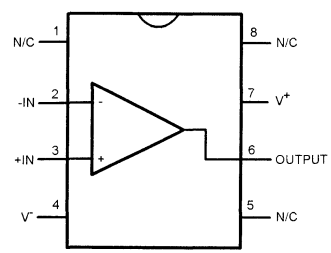
SOT23-6 (LMH6647)



20020260

Top View

SOIC-8 (LMH6645)

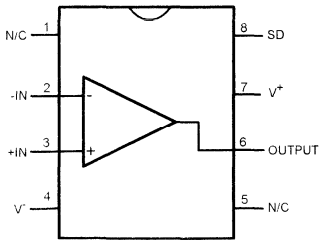


20020261

Top View

Connection Diagrams (Continued)

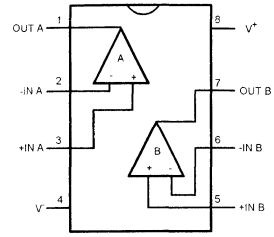
SOIC-8 (LMH6647)



20020262

Top View

SOIC-8 and MSOP-8 (LMH6646)



20020263

Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LMH6645MF	A68A	1k Units Tape and Reel	MF05A
	LMH6645MFX		3k Units Tape and Reel	
6-Pin SOT-23	LMH6647MF	A69A	1k Units Tape and Reel	MF06A
	LMH6647MFX		3k Units Tape and Reel	
SOIC-8	LMH6645MA	LMH6645MA	95 Units Rails	M08A
	LMH6645MAX		2.5k Units Tape and Reel	
	LMH6646MA	LMH6646MA	95 Units Rails	
	LMH6646MAX		2.5k Units Tape and Reel	
	LMH6647MA	LMH6647MA	95 Units Rails	
	LMH6647MAX		2.5k Units Tape and Reel	
MSOP-8	LMH6646MM	A70A	1k Units Tape and Reel	MUA08A
	LMH6646MMX		3.5k Units Tape and Reel	

National Semiconductor

LMH6654/55
Single/Dual Low Power, 250 MHz, Low Noise Amplifiers

General Description

The LMH6654/55 single and dual high speed, voltage feedback amplifiers are designed to have unity-gain stable operation with a bandwidth of 250MHz. They operate from ±2.5V to ±6V and each channel consumes only 4.5mA. The amplifiers feature very low voltage noise and wide output swing to maximize signal-to-noise ratio.

The LMH6654/55 have a true single supply capability with input common mode voltage range extending 150 mV below negative rail and within 1.3V of the positive rail.

LMH6654/55 high speed and low power combination make these products an ideal choice for many portable, high speed application where power is at a premium.

The LMH6654 is packaged in SOT23-5 and SOIC-8. The LMH6655 is packaged in MSOP-8 and SOIC-8.

The LMH6654/55 are built on National's Advance VIP10™ (Vertically Integrated PNP) complementary bipolar process.

Features

(V_S = ±5V, T_J = 25°C, Typical values unless specified).

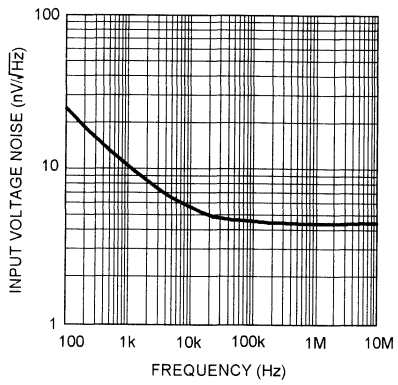
- Voltage feedback architecture
- Unity gain bandwidth — 250MHz
- Supply voltage range — ±2.5V to ±6V
- Slew rate — 200V/µsec
- Supply current — 4.5mA/channel
- Input common mode voltage — −5.15V to +3.7V
- Output voltage swing (R_L = 100Ω) — −3.6V to 3.4V
- Input voltage noise — 4.5nV/$\sqrt{Hz}$
- Input current noise — 1.7pA/$\sqrt{Hz}$
- Settling Time to 0.01% — 25ns

Applications

- ADC drivers
- Consumer video
- Active filters
- Pulse delay circuits
- xDSL receiver
- Pre-amps

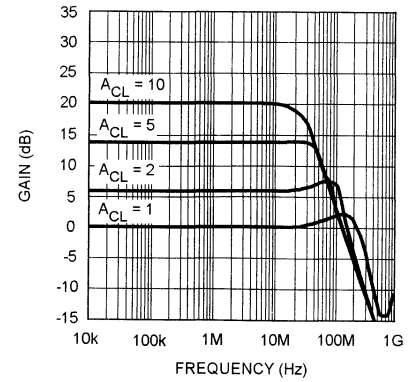
Typical Performance Characteristics

Input Voltage Noise vs. Frequency



20016560

Closed Loop Gain vs. Frequency



20016558

National Semiconductor

LMH6672
Dual, High Output Current, High Speed Op Amp

General Description

The LMH6672 is a low cost, dual high speed op amp capable of driving signals to within 1V of the power supply rails. It features the high output drive with low distortion required for the demanding application of a single supply xDSL line driver.

When connected as a differential output driver, the LMH6672 can drive a 50Ω load to 16.8V_{PP} swing with only −93dBc distortion, fully supporting the peak upstream power levels for upstream full-rate ADSL. The LMH6672 is fully specified for operation with 5V and 12V supplies. Ideal for PCI modem cards and xDSL modems.

Applications

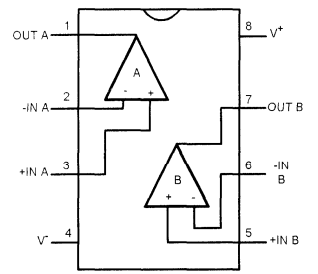
- ADSL PCI modem cards
- xDSL external modems
- Line drivers

Features

- **High Output Drive**
  19.2V_{PP} differential output voltage, R_L = 50Ω
  9.6V_{PP} single-ended output voltage, R_L = 25Ω
- **High Output Current**
  ±200mA @ V_O = 9$_{VPP}$, V_S = 12V
- **Low Distortion**
  93dB SFDR @ 100KHz, V_O = 8.4V_{PP}, R_L = 25Ω
  92dB SFDR @ 1MHz, V_O = 2V_{PP}, R_L = 100Ω
- **High Speed**
  130MHz 3dB bandwidth (G = 2)
  160V/µs slew rate
- **Low Noise**
  4.5nV/ $\sqrt{Hz}$: input noise voltage
  1.7pA/ $\sqrt{Hz}$: input noise current
- Low supply current: 6.2mA/amp
- Single-supply operation: 5V to 12V
- Available in 8-pin SOIC, PSOP and LLP

Connection Diagram

8-Pin SOIC/PSOP/LLP



Top View

Typical Application

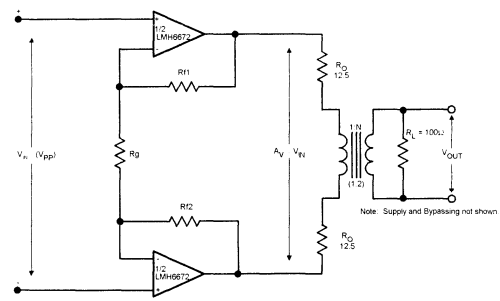


Figure 1

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LMH6672MA	LMH6672MA	Rails	M08A
	LMH6672MAX	LMH6672MA	2.5k Units Tape and Reel	
8-Pin PSOP	LMH6672MR	LMH6672MR	Rails	MRA08A
	LMH6672MRX	LMH6672MR	2.5k Units Tape and Reel	
8-Pin LLP	LMH6672LD	L6672LD	1k Units Tape and Reel	LDC08A
	LMH6672LDX	L6672LD	4.5k Units Tape and Reel	

Section 3
Analog Microcontrollers

Section 3 Contents

3

National Semiconductor

The 8-Bit COP8™ Family: Optimized for Value

CPU/Instruction Set Features

- 10 MHz, 15 MHz or 20 MHz from 10 MHz oscillator
- 0.5, 0.67, or 1 µs instruction cycle time
- Up to 14 multi-sourced vectored interrupt servicing each interrupt source with independent vector
- Versatile and easy to use instruction set
- 8-bit stack pointer (SP)—(Stack in RAM)
- Two 8-bit register indirect memory pointers (B,X)
- High code efficiency with majority of instructions being single byte/single cycle (77%)
- True bit manipulation
- BCD arithmetic instructions

Peripheral Features (Vary by Device)

- On-chip Flash up to 32 kbytes
- On-chip ROM from 768 bytes to 32 kbytes
- On-chip OTP EPROM up to 32 kbytes
- On-chip RAM from 64 to 1 kbytes
- On-chip EEPROM up to 512 bytes
- Virtual EEPROM on Flash devices
- Up to three 16-bit multi-function timers, each with two 16-bit registers supporting
  - — Processor independent PWM mode
  - — External event counter mode
  - — Input capture mode
- Idle timer
- Multi-Input Wakeup (up to 8 wakeup pins) with optional interrupts (8)
- Full duplex USART
- CAN interface
- A/D (8 or 10 bit)
- Analog function block with single-scope A/D capability
- Analog comparators
- WATCHDOG™ and clock monitor logic
- MICROWIRE/PLUS™ serial I/O
- Brown out detection
- Power-On-Reset
- Multiply/Divide function

I/O Features

- Memory mapped I/O
- Software selectable I/O
  - — TRI-STATE® outputs
  - — Push-Pull outputs
  - — Weak Pull-Up input
  - — High impedance input
- Schmitt trigger inputs
- High current outputs
- Pin efficient (i.e., 40 pins in 44-pin package are devoted to useful I/O)
- Packing:
- 16 to 68 pins
- SOIC, DIP, PLCC, and QFP
- Chip-Scale and µSMD

Fully Static CMOS

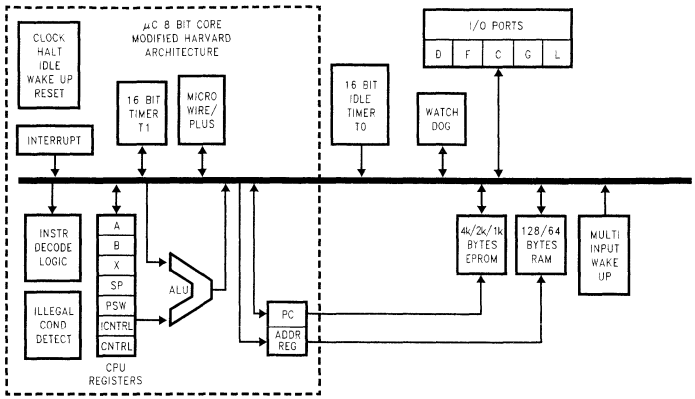
- Low current drain (typically < 1 µA in HALT)
- Two power saving modes: HALT and IDLE
- Single supply operation: 2.3V to 6.0V
- Temperature ranges: 0°C to +70°C, −40°C to +85°C, and −55°C to +125°C

Development Support

- Eraseable, OTP and Flash devices
- Real time emulation and full program debug offered by MetaLink Development System

Development Support (Continued)

An Example of COP888 Block Diagram (COP8SAx7)



MS000073-3

Embedded Control: Practical Solutions to Real Problems

Microcontrollers have played an important role in the semiconductor industry for quite some time. Unlike microprocessors, which typically address a range of more computation intensive, general purpose applications, microcontrollers are based on a central processing unit, data memory and input/output circuitry that are designed primarily for specific, single function applications.

During the 1970s, microcontrollers were initially used in simple applications such as calculators and digital watches, but the combination of decreasing costs and increasing integration and performance has created many new application opportunities over the years. Even as the bulk of application growth occurs in the 8-bit arena, the same issues that system designers were concerned with in the 4-bit world continue in force today. These include cost/performance tradeoffs, low power and low voltage capabilities, time to market, space/pin efficiency, and ease of design.

- **Cost/Performance.** A price difference of just a few pennies can be the gating factor in today's 8-bit design decisions. Manufacturers must offer a wide range of cost/performance options in order to meet customer demands.
- **Low Power and Low Voltage.** The increasing range of mobile and/or battery-powered applications is placing a premium on low-power, low-voltage, CMOS and BiCMOS embedded control solutions.
- **Time to Market.** The microcontroller's architecture, functionality, and feature set have a major influence on product design cycles in today's competitive market, with its shrinking windows of opportunity.
- **Space/Pin Efficiency.** Real estate and board configuration considerations demand maximum space and I/O pin efficiency, particularly given today's high integration and small product form factors.
- **Ease of Design.** A familiar and easy to use application design environment—including complete development tool support—is one of the driving factors affecting today's 8-bit microcontroller design decisions.

All of these issues must be considered when searching for the appropriate 8-bit microcontroller to meet specific application needs.

National Semiconductor has been a prominent player in the worldwide microcontroller market, and its COP8 family of products spans today's range of applications, providing customers with a wealth of options at every price/performance point in the 8-bit microcontroller market.

Designers can select from a variety of building blocks centered around a common memory-mapped core and modified Harvard architecture. These building blocks include ROM, RAM, user programmable memory, USART, comparator, A/D, and I/O functions.

The COP8 family incorporates 0.5/0.67/1 μs instruction cycle times, WATCHDOG and clock monitors, multi-input wake up circuitry and National's MICROWIRE/PLUS interface. In addition, National's COP8 microcontrollers are available in a wide variety of temperature range configurations from −55°C through +125°C—optimizing them for rugged industrial and military applications.

COP8 Benefits

The COP8 family provides designers with a number of features that result in substantial benefits. These include a code-efficient instruction set, low power/voltage features, efficient I/O, a flexible and configurable design methodology, robust design tools, and electromagnetic interference (EMI) control.

The COP8 family's compact, efficient and easy-to-program instruction set enables designers to reduce time to market for their products. Thanks to the instruction set, efficient ROM utilization lowers costs while providing the opportunity to integrate additional functionality on-chip. Low voltage operation, low current drain, multi-input wakeup and several power saving modes reduce power consumption for today's increasing range of handheld, battery-driven applications. An array of user-friendly development tools—including hardware from MetaLink, and state-of-the-industry assemblers, and C compilers help design engineers save valuable development time.

COP8 Benefits (Continued)

National's Configurable Controller Methodology (CCM) for the COP8 family creates "whole products" that are bug-free, fully tested and characterized, and supported by a range of documentation and hardware/software tools. National developed CCM because the majority of customer requests for new products have typically called for reconfigurations of existing proven blocks—such as RAM, ROM, timers, comparators, USARTs, and I/O.

EMI Reduction Technology

COP8 products incorporate circuitry that guards against electromagnetic interference—an increasing problem in todays microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, EMI-optimized pinouts, gradual turn-on outputs (GTO), and on-chip choke device to help customers circumvent many of the EMI issues influencing embedded control designs.

In-System Programming And Virtual EEPROM

TheFlash based devices include a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize the in system software update capability if MICROWIRE/PLUS is not desired.

Additional functions will copy blocks of data between the RAM and the Flash Memory. These functions provide a virtual EEPROM capability by allowing the user to emulate a variable amount of EEPROM by initializing nonvolatile variables from the Flash Memory and occasionally restoring these variables to the Flash Memory.

The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins.

Dual Clock And Clock Doubler

Some devices include a versatile clocking system and two oscillator circuits designed to drive a crystal or ceramic resonator. The primary oscillator operates at high speed up to 10 MHz. The secondary oscillator is optimized for operation at 32.768 kHz.

The user can, through specified transition sequences, switch execution between the high speed and low speed oscillators. The unused oscillator can then be turned off to minimize power dissipation. If the low speed oscillator is not used, the pins are available as general purpose bidirectional ports.

The operation of the CPU will use a clock at twice the frequency of the selected oscillator (up to 20 MHz for high speed operation and 65.536 kHz for low speed operation).

True In-System Emulation

On-chip emulation capability has been added to Flash based devices which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

Core Architecture

All COP8 devices use a modified Harvard architecture, which means that program memory and data memory are accessed separately using independent address/data buses. This type of architecture offers the advantage of faster operation because the next instruction can be fetched from program memory while the current data memory transfer operation is carried out. The COP8 architecture is a "modified" Harvard version because data tables can be accessed from program memory by using a special instruction, Load Accumulator Indirect (LAID).

The core CPU has an 8-bit accumulator (A), a 15-bit program counter (PC), two 8-bit data pointers (B and X), an 8-bit stack pointer (SP), an 8-bit processor status word (PSW), an 8-bit control register (CNTRL), and a bank of general-purpose 8-bit registers. All RAM, I/O ports, and registers (except for the accumulator and program counter) are mapped into the data memory address space.

The COP8 device communicates with other devices through several configurable I/O ports or through the MICROWIRE/PLUS serial I/O interface. The I/O ports are designated by letter names such as Port C, Port D, Port G, Port I, and Port L. The number of ports and port pins vary with the device type and package type.

All COP8 devices have at least one 16-bit, general-purpose timer that can be programmed to operate in any of three modes: Pulse Width Modulation (PWM), external event counter, or input capture mode. Many COP8 devices have two or more of these timers and/or special-purpose timers such as the IDLE mode timer.

Peripheral Blocks

Several different on-chip peripheral devices are available in different COP8 devices, with multiple peripherals available in some versions of COP8 devices. Some of the peripheral blocks available are:

- Comparator
- Analog-to-Digital Converter
- Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
- Controller Area Network (CAN) Interface
- Hardware Multiply/Divide

Typically, the inputs and outputs of the peripherals are "alternate functions" of the programmable I/O ports of the COP8 device. In other words, the port pins can be programmed to operate as general-purpose inputs and outputs or as special-purpose inputs and outputs for the supported peripheral device.

Instruction Set

The COP8 offers a powerful and efficient instruction set. Most instructions are one byte long and take one instruction cycle to execute, resulting in compact, efficient programs. Several single-byte instructions are available that carry out multiple operations. For example, the single-byte DRSZ instruction decrements a specified register and skips the next instruction if the result is zero.

Instruction Set (Continued)

The instruction set offers a variety of addressing modes. For reading or writing data, the device offers the following addressing modes: direct, register B or X indirect, register B or X indirect with post-incrementing/decrementing, immediate, immediate short, and indirect from program memory. For transfer of program control, the device offers the following addressing modes: jump relative, jump absolute, jump absolute long, and jump indirect.

The COP8 allows any individual bit in data memory address space to be set, reset, and tested, including bits in the memory-mapped I/O ports and registers.

COP8 Families

The COP8 line of 8-bit microcontrollers is divided into two families called the "Basic Core" and "Feature Core." The Basic Core devices are for lower-end, lower-cost applications that require less memory and simpler peripheral devices; whereas the Feature Core devices are for applications that require more memory and more-advanced peripheral devices. However, both families share the same basic architecture and basic instruction set.

Basic Core devices have from 768 bytes to 4k bytes of ROM, EPROM or Flash and 64 or 128 bytes of RAM; and one 16-bit timer. A HALT mode is available to shut down the device during periods of inactivity. Devices typically have 20 or 28 pins. Simple peripheral devices such as a comparator are offered in the family.

Feature Core devices have from 2k to 32 kbytes of ROM and 128 to 1 kbytes of RAM; and at least two 16-bit timers. The Feature instruction set offers nine additional instructions to support vectored interrupts, pushing/popping the stack, and additional types of logic operations. In addition to the HALT mode, another power-down mode is available called the IDLE mode, which allows certain time-monitoring sections to operate while the rest of the device is shut down. All Feature Core devices offer Multi-Input Wakeup, which provides separate inputs for edge-triggered maskable interrupts or for exiting from the HALT or IDLE mode. Devices typically have 28, 40, or 44 pins. Advanced peripheral devices such as an A/D Converter, USART, and/or CAN Interface are offered in the family.

One-Time Programmable (OTP) Devices

All COP8 devices are supported by One-Time Programmable (OTP) devices of the same or increased capability. OTP devices are field-programmable using standard programming equipment. They are useful not only for prototypes and limited-production runs, but for the shortest time to market and for the ability to quickly make revisions or correct bugs, OTP COP8 devices offer an attractive choice for final production.

OTP COP8 devices offer low-voltage operation and program memory security. Security is achieved by programming a bit in the device that makes the program memory unreadable from outside the chip.

COP8SAx7, and COP8SGx7 OTP Devices

Recent additions to the COP8 Feature Family are the COP8SAx7 and COP8SGx7 OTP devices: the COP8SAA7, COP8SAB7, COP8SAC7, COP8SGE7, and COP8SGR7.

These devices offer an unusual combination of OTP memory, low price, and a rich set of features:

- Low cost 8-bit OTP microcontroller
- Very small packaging
- Quiet Design (low radiated emissions)
- Multi-Input Wakeup pins with optional interrupts
- 1k to 32k OTP program memory
- 8 bytes of user storage space in EPROM
- User selectable clock options
- Zero external component operation
- Internal Power-On Reset—user selectable
- WATCHDOG and Clock Monitor Logic—user selectable
- Up to 12 high current outputs

COP8 Features/Benefits Analysis

	Key Features	Benefits
Instruction Set	• Efficient Instruction Set (77% Single Byte/Single Cycle) • Easy To Program • Compact Instruction Set • Multi Function Instructions • Ten Addressing Modes	• Efficient ROM Utilization (compact code) • Low Cost Microcontroller (small ROM size) • Fast Time To Market
Low Power	• Low Voltage Operation • Lower Current Drain • Multi-Input Wakeup • Power Savings Modes (HALT/IDLE)	• Lower Power Consumption for Hand Held Battery Driven Applications
Efficient I/O	• Software Programmable I/O • Efficient Pin Utilization • Breadth of Available Packages • Package Types Including Variety of Low Pin Count Devices • High Current Outputs • Schmitt Trigger Inputs	• Multiple Use of I/O Pins • Economical Use of External Components (lower system cost) • Cleaner Hardware Design • Choice of Optimum Package Type (price/outline/pinout)
Flexible/Powerful On-Board Features	• Smart 16-Bit Timers (processor independent PWM) • A/D • Comparators • Analog Function Block (low cost A/D) • UART • Multi-Input Wakeup • Multi-Source Hardware Interrupts • MICROWIRE/PLUS Serial Interface • Application Specific Features (CAN, Motor Control Timers, etc.)	• Timers Allow Less Software/Process Overhead for Frequency • Measurement (capture) and PWM • Cleaner Hardware (eliminating the need for external components) • Overall Cost Reduction
Safety/Software-Runaway Protection	• WATCHDOG • Software Interrupt • Clock Monitor • Brown Out Detection	• No Need for External ProtectionCircuitry • Brown Out Detection Allows the Use of Low Cost Power Supply
Development Tools	• A range of software and hardware tools options to meet every need and budget	• Saves Engineering Development Time—Fast Time to Market

National Semiconductor

ROM Products

National Semiconductor

COP912C
8-Bit Microcontroller

General Description

Note: COP8SA devices are instruction set and pinout compatible supersets of the COP912C devices, and are replacements for these in new designs when possible.

The COP912C ROM based microcontrollers are integrated COP8(tm) Base core devices with smaller memory (768 bytes), and fewer on-board features. These single-chip CMOS devices are suited for lower-functionality applications where system cost is of prime consideration. Pin and software compatible (different Vcc range) 4k/32k OTP versions are available (COP87LxxCJ/RJ Family). Erasable windowed versions are available for use with a range of COP8(tm) software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10MHz CKI with 2.5us(912C) or 2us(912CH) instruction cycle, one multi-function 16-bit timer/counter with PWM, MICROWIRE/PLUS(tm) serial I/O, power saving HALT mode, three clock modes, high current outputs, software selectable I/O options, multi-volt operation and 20 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP912C	768 ROM	64	16	20 DIP/SOIC	0 to +70˚C	2.3v - 4.0v
COP912CH	768ROM	64	16	20 DIP/SOIC	0 to +70˚C	4.0v - 5.5v

Key Features

- Lowest cost COP8 microcontroller
- 16-bit multi-function timer supporting
  - — PWM mode
  - — External event counter mode
  - — Input capture mode
- 768 bytes of ROM
- 64 bytes of RAM

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- Schmitt trigger inputs on Port G
- MICROWIRE/PLUS™ Serial I/O
- Packages: 20 DIP/SO with 16 I/O pins

CPU/Instruction Set Features

- Instruction cycle time of 2 µs for COP912CH and 2.5 µs for COP912C
- Three multi-sourced interrupts servicing
  - — External Interrupt with selectable edge
  - — Timer interrupt
  - — Software interrupt
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP) — stack in RAM
- Two 8-bit Register Indirect Memory Pointers (B, X)

Fully Static CMOS

- Low current drain (typically < 1 µA)
- Single supply operation: 2.3V to 4.0V or 4.0V to 5.5V
- Temperature range: 0˚C to +70˚C

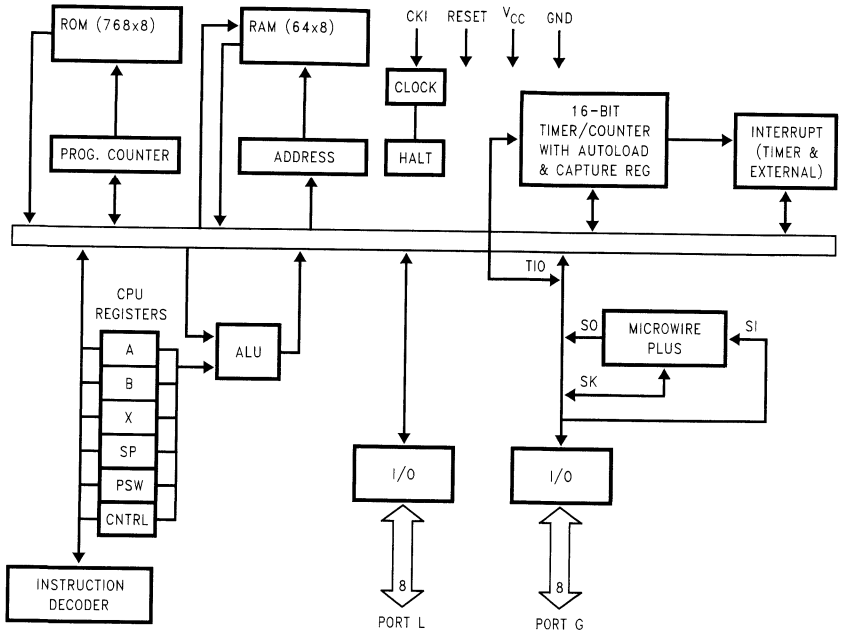
Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Applications

- Electronic keys and switches
- Remote Control
- Timers
- Alarms
- Small industrial control units
- Low cost slave controllers
- Temperature meters
- Small domestic appliances
- Toys and games

Block Diagram



National Semiconductor

COP820C/840C Family
8-Bit CMOS ROM Based Microcontrollers with 1k or 2k Memory

General Description

Note: COP8SA devices are instruction set and pinout compatible supersets of the COP800C Family devices, and are replacements for these in new designs when possible.

The COP820C/840C Family ROM based microcontrollers are integrated COP8™ Base core devices with smaller memory (1k/2k), and fewer on-board features. These single-chip CMOS devices are suited for lower-functionality applications where system cost is of prime consideration. Pin and software compatible (different V_{CC} range) 4k/32k OTP versions are available (COP87LxxCJ/RJ Family). Erasable windowed versions are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 Hz CKI with 1µs instruction cycle, one multi-function 16-bit timer/counter with PWM, MICROWIRE/PLUS™ serial I/O, power saving HALT mode, three clock modes, high current outputs, software selectable I/O options, 2.3v-6.0v operation and 20/28 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP620C	1k ROM	64	24	28 DIP/SOIC	-55 to +125˚C	4.5v - 5.5v
COP820C	1k ROM	64	24	28 DIP/SOIC	-40 to +85˚C	
COP920C	1k ROM	64	24	28 DIP/SOIC	0 to +70˚C	2.3v-4.0v, CH=4.0v-6.0v
COP622C	1k ROM	64	16	20 DIP/SOIC	-55 to +125˚C	4.5v - 5.5v
COP822C	1k ROM	64	16	20 DIP/SOIC	-40 to +85˚C	
COP922C	1k ROM	64	16	20 DIP/SOIC	0 to +70˚C	2.3v-4.0v, CH=4.0v-6.0v
COP640C	2k ROM	128	24	28 DIP/SOIC	-55 to +125˚C	4.5v - 5.5v
COP840C	2k ROM	128	24	28 DIP/SOIC	-40 to +85˚C	
COP940C	2k ROM	128	24	28 DIP/SOIC	0 to +70˚C	2.3v-4.0v, CH=4.0v-6.0v
COP642C	2k ROM	128	16	20 DIP/SOIC	-55 to +125˚C	4.5v - 5.5v
COP842C	2k ROM	128	16	20 DIP/SOIC	-40 to +85˚C	
COP942C	2k ROM	128	16	20 DIP/SOIC	0 to +70˚C	2.3v-4.0v, CH=4.0v-6.0v

Key Features

- 16-bit multi-function timer supporting
  - — PWM mode
  - — External event counter mode
  - — Input capture mode
- 1024 bytes ROM/64 bytes RAM-COP820C
- 2048 bytes ROM/128 bytes RAM-COP840C

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- High current outputs
- Schmitt trigger inputs on Port G
- MICROWIRE/PLUS serial I/O
- Packages:
  - — 20 DIP/SO with 16 I/O pins
  - — 28 DIP/SO with 24 I/O pins

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Three multi-source interrupts servicing
  - — External interrupt with selectable edge
  - — Timer interrupt
  - — Software interrupt
- Versatile and easy to use instruction set
- 8-bit Stack point (SP) — stack in RAM
- Two 8-bit Register Indirect Memory Pointers (B, X)

Fully Static CMOS

- Low current drain (typically < 1 µA)
- Single supply operation: 2.5V to 6.0V
- Temperature range: 0˚C to +70˚C, –40˚C to +85˚C, –55˚C to +125˚C

Development Support

- Emulation and OTP devices

Development Support (Continued)

- Real time emulation and full program debug offered by MetaLink's Development System

Block Diagram

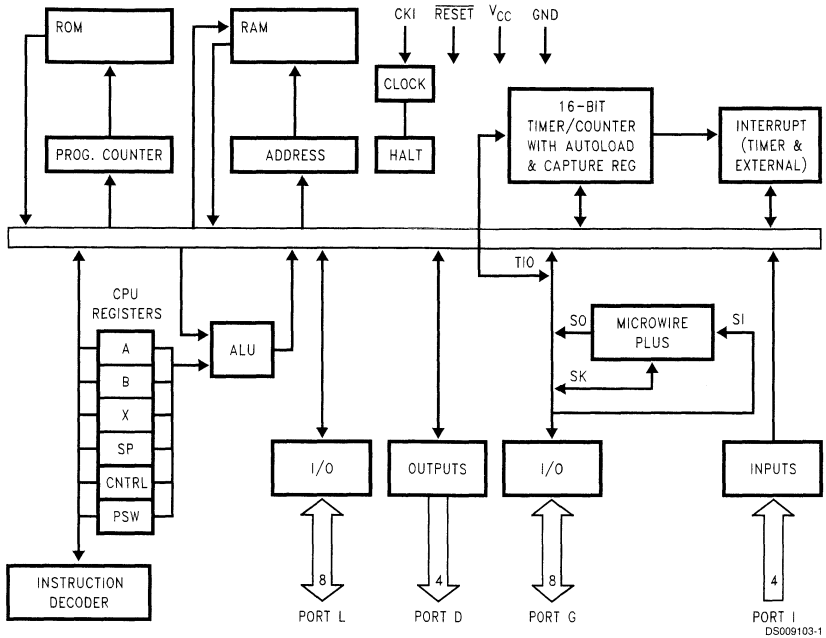


FIGURE 1.

National Semiconductor

COP880C Microcontrollers

General Description

The following part numbers are pin count and temperature variations of the COP880C: COP680C/COP681C/ COP682C/COP881C /COP882C/COP980C/ COP981C/COP982C.

The COP880C devices are members of the COP8 microcontroller family. They are fully static parts, fabricated using double-metal silicon gate microCMOS technology. This low cost microcontroller is a complete microcomputer containing all system timing, interrupt logic, ROM, RAM, and I/O necessary to implement dedicated control functions in a variety of applications. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS™ serial I/O, a 16-bit timer/counter with capture register and a multi-sourced interrupt. Each I/O pin has software selectable options to adapt the device to the specific application. The part operates over a voltage range of 2.5 to 6.0V. High throughput is achieved with an efficient, regular instruction set operating at a 1 microsecond per instruction rate.

Key Features

- —16-bit multi-function timer supporting
  - —PWM mode
  - —External event counter mode
  - —Input capture mode
- 4 kbytes of ROM
- 128 bytes of RAM

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE®, Push-Pull, Weak Pull-Up Input, High Impedance Input)
- High current outputs (8 pins)
- Schmitt trigger inputs on Port G
- MICROWIRE PLUS serial I/O
- Packages:
  - —20 DIP/SO with 16 I/O pins
  - —28 DIP/SO with 24 I/O pins
  - —40 DIP, 36 I/O pins
  - —44 PLCC, 36 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Three multi-source interrupts servicing
  - —External interrupt with selectable edge
  - —Timer interrupt
  - —Software interrupt
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Low current drain (typically < 1 µA)
- Single supply operation: 2.5V to 6.0V
- Temperature ranges: 0°C to 70°C, −40°C to +85°C, −55°C to +125°C.

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink's development system

Block Diagram

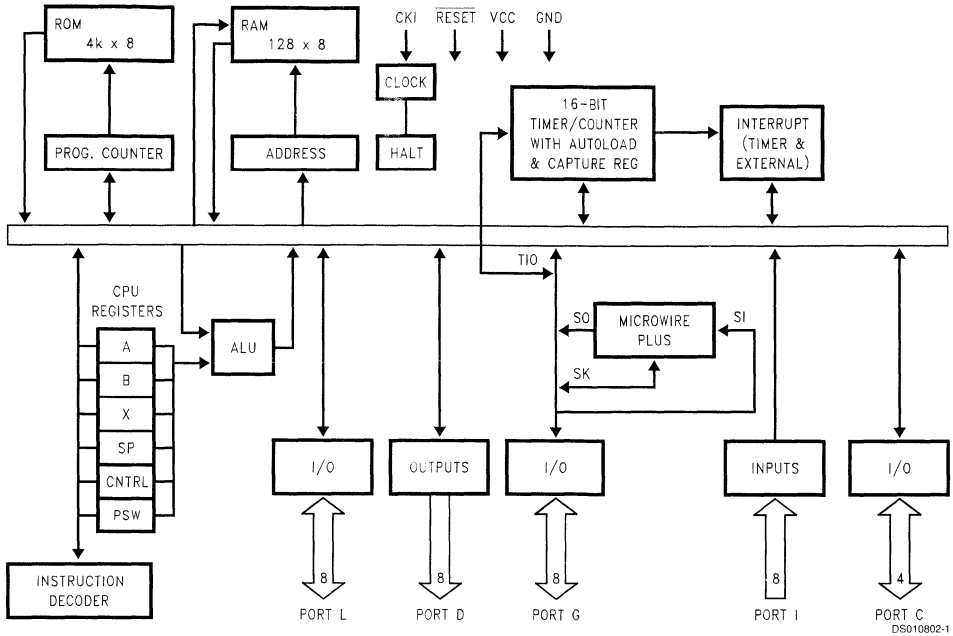
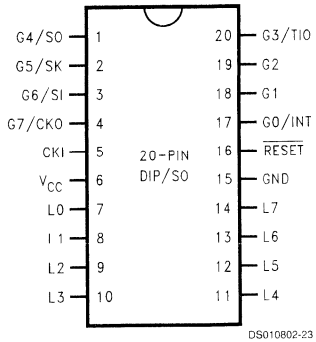


FIGURE 1.

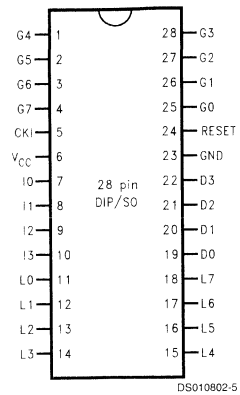
Connection Diagrams

Dual-In-Line Package



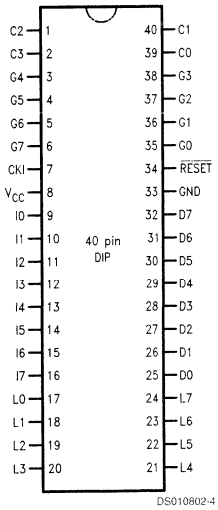
Top View
Order Number COP882C-XXX/N, COP982C-XXX/N, COP882C-XXX/WM, COP982C-XXX/WM, COP982C-XXX/N or COP982CH-XXX/WM

Dual-In-Line Package (N) and 28 Wide SO (WM)



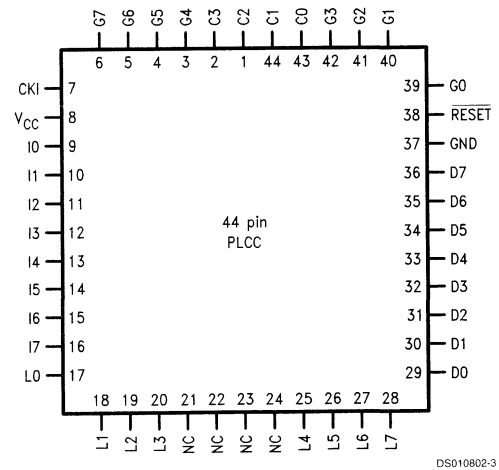
Top View
Order Number COP881C-XXX/N, COP981C-XXX/N, COP881C-XXX/WM, COP981C-XXX/WM, COP981CH-XXX/N or COP981CH-XXX/WM

Dual-In-Line Package



Top View
Order Number COP680C-XXX/N, COP880C-XXX/N, COP980C-XXX/N or COP980CH-XXX/N

Plastic Chip Carrier



Top View
Order Number COP680C-XXX/V, COP880C-XXX/V, COP980C-XXX/V or COP980CH-XXX/V

FIGURE 2. Connection Diagrams

National Semiconductor

COP820CJ/COP840CJ Family 8-Bit CMOS ROM Based Microcontrollers with 1k or 2k Memory, Comparator and Brown Out Detector

General Description

The COP820CJ/840CJ Family ROM based microcontrollers are integrated COP8™ Base core devices with 1k or 2k memory, an Analog comparator and Brownout detection. These single-chip CMOS devices are suited for lower-functionality applications where power and voltage fluctuations are a consideration. Pin and software compatible (no Brownout; different Vcc range) 4k/32k OTP versions are available (COP87LxxCJ/RJ Family) for pre-production, and for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10MHz CKI with 1us instruction cycle, one multi-function 16-bit timer/counter, MICROWIRE/PLUS™ serial I/O, one analog comparator, power saving HALT mode, MIWU, on-chip R/C oscillator capacitor (COP840CJ), high current outputs, software selectable I/O options, WATCHDOG™ timer, modulator/timer, Brownout detector, Power on Reset, 2.5v-6.0v operation, and 16/20/28 pin packages.

In this datasheet, the term COP820CJ refers to packages including the COP820CJ, COP822CJ, and COP823CJ; and COP840CJ refers to COP840CJ, COP842CJ, COP940CJ, and COP942CJ.

Devices included in this data sheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP820CJ	1k ROM	64	24	28 DIP/SOIC	-40 to +85˚C	
COP822CJ	1k ROM	54	16	20 DIP/SOIC	-40 to +85˚C	
COP823CJ	1k ROM	64	12	16 SOIC	-40 to +85˚C	
COP840CJ	2k ROM	128	24	28 DIP/SOIC	-40 to +85˚C	Low EMI
COP940CJ	2k ROM	128	24	28 DIP/SOIC	-0 to +70˚C	2.5V-4.5V, CJH = 4V-6V
COP842CJ	2k ROM	128	16	20 DIP/SOIC	-40 to +85˚C	
COP942CJ	2k ROM	128	16	20 DIP/SOIC	-0 to +70˚C	2.5V-4.5V, CJH = 4V-6V

Key Features

- Multi-Input Wake Up (on the 8-bit Port L)
- Brown out detector
- Analog comparator
- Modulator/timer (High speed PWM for IR transmission)
- 16-bit multi-function timer supporting
  - — PWM mode
  - — External event counter mode
  - — Input capture mode
- 1024 or 2048 bytes of ROM
- 64 or 128 bytes of RAM
- Quiet design (low radiated emissions)
- Integrated capacitor for the R/C oscillator for COP840CJ

I/O Features

- Software selectable I/O options (TRI-STATE® output, push-pull output, weak pull-up input, high impedance input)
- High current outputs (8 pins)
- Packages
  - — 16 SO with 12 I/O pins for COP820CJ
  - — 20 DIP/SO with 16 I/O pins
  - — 28 DIP/SO with 24 I/O pins
- Schmitt trigger inputs on Port G
- MICROWIRE/PLUS serial I/O

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Three multi-source vectored interrupts servicing
  - — External interrupt with selectable edge
  - — Timer interrupt
  - — Software interrupt
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit register indirect data memory pointers (B, X)

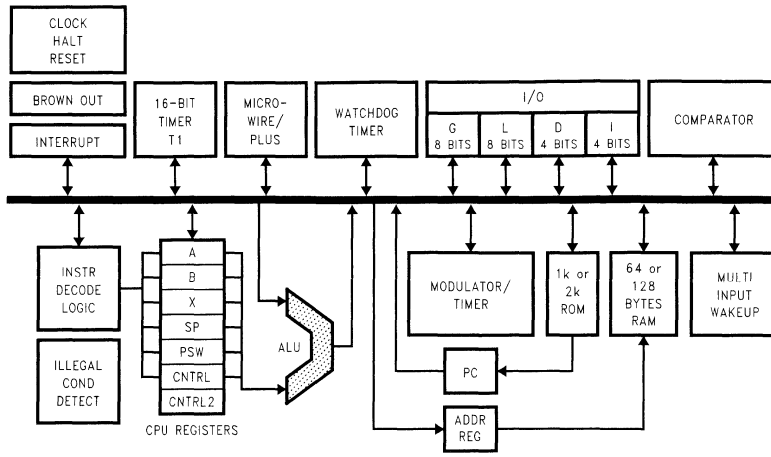
Fully Static CMOS

- Low current drain (typically < 1 µA)
- Single supply operation: 2.5V to 6.0V
- Temperature ranges: –0˚C to +70˚C and –40˚C to +85˚C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

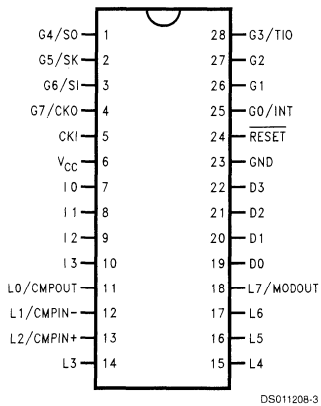
Block Diagram



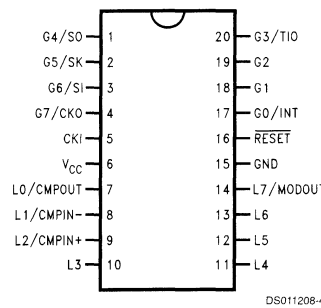
2k ROM and 128 Bytes RAM for COP840CJ

FIGURE 1. Block Diagram

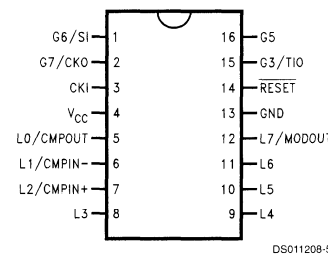
Connection Diagrams



Top View
Order Number COPCJ820-XXX/N or COPCJ820-XXX/M,
Order Number COPCJ840-XXX/N or COPCJ840-XXX/M,
Order Number COPCJ940-XXX/N or COPCJ940-XXX/M
See NS Package Number N28B or M28B



Top View
Order Number COPCJ822-XXX/N or COPCJ822-XXX/M
Order Number COPCJ842-XXX/N or COPCJ842-XXX/M
Order Number COPCJ942-XXX/N or COPCJ942-XXX/M
See NS Package Number N20A or M20B



Top View
Order Number COPCJ823-XXX/WM
See NS Package Number M16B

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

COP820CJ/COP840CJ Pin Assignment

Port Pin	Typ.	ALT Function	16-Pin	20-Pin	28-Pin
L0	I/O	MIWU/CMPOUT	5	7	11
L1	I/O	MIWU/CMPIN−	6	8	12
L2	I/O	MIWU/CMPIN+	7	9	13
L3	I/O	MIWU	8	10	14
L4	I/O	MIWU	9	11	15
L5	I/O	MIWU	10	12	16
L6	I/O	MIWU	11	13	17
L7	I/O	MIWU/MODOUT	12	14	18
G0	I/O	INTR		17	25
G1	I/O			18	26
G2	I/O			19	27
G3	I/O	TIO	15	20	28
G4	I/O	SO		1	1
G5	I/O	SK	16	2	2
G6	I	SI	1	3	3
G7	I	CKO	2	4	4
I0	I				7
I1	I				8
I2	I				9
I3	I				10
D0	O				19
D1	O				20
D2	O				21
D3	O				22
V_{CC}			4	6	6
GND			13	15	23
CKI			3	5	5
$\overline{\text{RESET}}$			14	16	24

National Semiconductor

COP888CL
8-Bit Microcontroller

General Description

The following part numbers are pin count and temperature variations of the COP888CL: COP688CL, COP684CL, COP884CL, COP988CL, COP984CL.

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888CL is a member of this expandable 8-bit core processor family of microcontrollers.

It is a fully static part, fabricated using double-metal silicon gate microCMOS technology. Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS serial I/O, two 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture mode capabilities), and two power savings modes (HALT and IDLE), both with a multi-sourced wakeup/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes. Each I/O pin has software selectable configurations. The device operates over a voltage range of 2.5V to 6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 µs per instruction rate.

Key Features

- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 4 kbytes of on-chip ROM
- 128 bytes of on-chip RAM

Additional Peripheral Features

- Idle Timer
- Multi-input Wake Up (MIWU) with optional interrupts (8)
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS™ serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- High current outputs
- Schmitt trigger inputs on port G
- Packages:
  - — 44 PLCC with 40 I/O pins
  - — 40 DIP with 36 I/O pins
  - — 28 DIP with 24 I/O pins
  - — 28 SO with 24 I/O pins

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Ten multi-source vectored interrupts servicing
  - — External Interrupt with selectable edge
  - — Idle Timer T0
  - — Timers (Each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B, X)

Fully Static CMOS

- Low current drain (typically < 1 µA)
- Single supply operation: 2.5V to 6.0V
- Temperature ranges: 0°C to +70°C, −40°C to +85°C, −55°C to +125°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

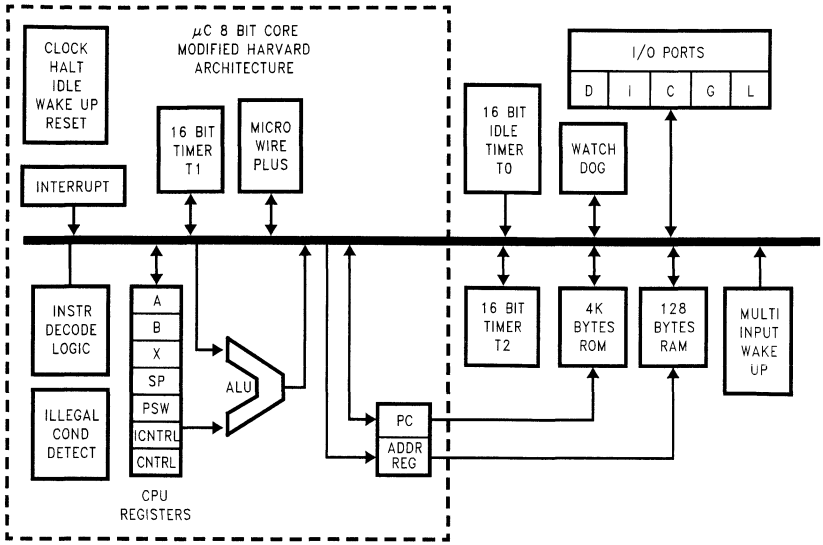
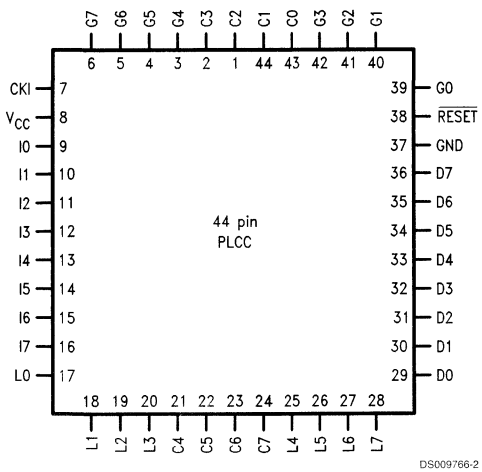


FIGURE 1. Block Diagram

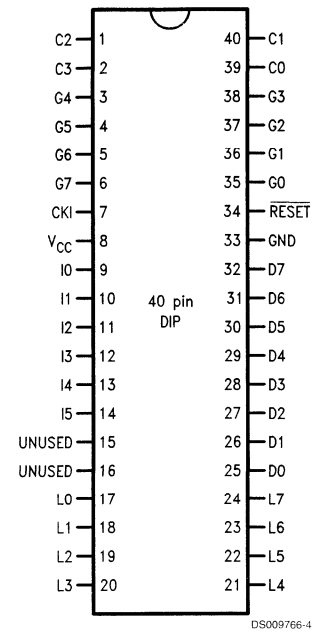
Connection Diagrams

Plastic Chip Carrier



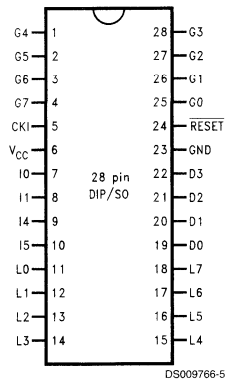
Top View
Order Number COP688CL-XXX/V, COP888CL-XXX/V, COP988CL-XXX/V or COP988CLH-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View
Order Number COP688CL-XXX/N, COP888CL-XXX/N, COP988CL-XXX/N or COP988CLH-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



Top View
Order Number COP688CL-XXX/N, COP884CL-XXX/N, COP984CL-XXX/N or COP984CLH-XXX/N
See NS Molded Package Number N28B
Order Number COP684CL-XXX/WM, COP884CL-XXX/WM, COP984CL-XXX/WM, or COP984CLHXXX/WM
See NS Surface Mount Package Number M28B

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin	40-Pin	44-Pin
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU		12	18	18
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT		4	6	6
		RESTART				
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I			7	9	9
I1	I			8	10	10
I2	I				11	11
I3	I				12	12
I4	I			9	13	13
I5	I			10	14	14
I6	I					15
I7	I					16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
Unused (Note 1)					16	
Unused (Note 1)					15	
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

Note 1: On the 40-pin package Pins 15 and 16 must be connected to GND.

National Semiconductor

COP8SE Family
8-Bit CMOS ROM Based and OTP Microcontrollers with 4k Memory and 128 Bytes EEPROM

General Description

The COP8SEx5 Family ROM based microcontrollers are highly integrated COP8™ Feature core devices with 4k memory and advanced features including EEPROM. COP8SER7 devices are pin and software compatible (different V_{CC} range), 32k OTP (One Time Programmable) versions for engineering development use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1µs instruction cycle, 128 bytes of EEPROM for non-volatile data storage, one multi-function 16-bit timer/counter, idle timer with MIWU, MICROWIRE/PLUS™, serial I/O, crystal or R/C oscillator, two power saving HALT/IDLE modes, Schmitt trigger inputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, Low EMI 2.7V to 5.5V operation, and 16/20 pin packages.

Devices included in this data sheet are:

Device	OSC	Memory (bytes)	RAM (bytes)	EERAM	I/O Pins	Package	Temperature
COP8SEC5		4k ROM	128	128 bytes	12/16	16/20 SOIC	-40 to +85°C, -40 to +135°C
COP8SER7-XE	xtal	32k OTP EPROM	128	128 bytes	16	20 SOIC	-40 to +85°C, Engineering
COP8SER7-RE	R/C	32k OTP EPROM	128	128 bytes	16	20 SOIC	-use only

Key Features

- 256 bytes data memory
  - — 128 bytes RAM
  - — 128 bytes EEPROM
- OTP with security feature (SER7)
- Quiet Design (low radiated emissions)
- Multi-Input Wakeup pins with optional interrupts (8 pins)
- User selectable clock options:
  - — R/C oscillator
  - — Crystal oscillator

Other Features

- Fully static CMOS, with low current drain
- Available with Crystal (-XE) or RC (-RE) oscillator
- Two power saving modes: HALT and IDLE
- 1 µs instruction cycle time
- 4k bytes on-board masked ROM or 32k bytes OTP
- Single supply operation: 2.7V — 5.5V
- MICROWIRE/PLUS Serial Peripheral Interface Compatible
- Nine multi-source vectored interrupts servicing
  - — EEPROM write complete
  - — External interrupt
  - — Idle Timer T0
  - — One Timer (with 2 Interrupts)
  - — MICROWIRE/PLUS Serial Interface
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS
- Idle Timer with programmable interrupt interval
- One 16 bit timer with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- Versatile instruction set
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options:
  - — TRI-STATE® Output:
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Temperature ranges:
  - — -40°C to +85°C
  - — -40°C to +135°C (SEC5 only)
- Packaging: 16, and 20 SO (SEC5); 20 SO (SER7)
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

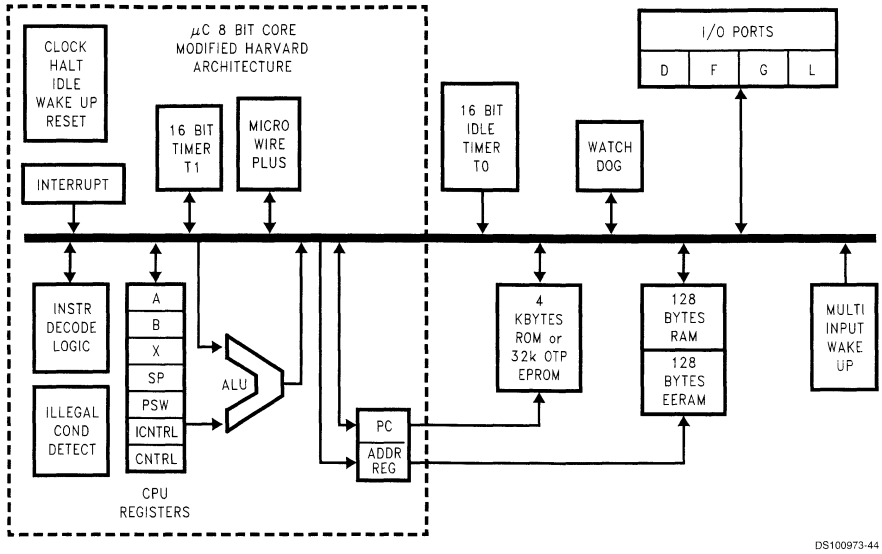


FIGURE 1. Block Diagram

1.0 Device Description

1.1 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. Non-volatile memory for the storage of data variables is provided by the EEPROM in the COP8SEC5 and COP8SER7. In a Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.2 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set—one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM/OTP). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.2.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.2.2 Many Single-Byte, Multifunction Instructions

The COP8 instruction set utilizes many single-byte, multifunction instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction; decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

1.0 Device Description (Continued)

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (analogous to "FOR NEXT" in higher level languages).

1.2.3 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.2.4 Register Set

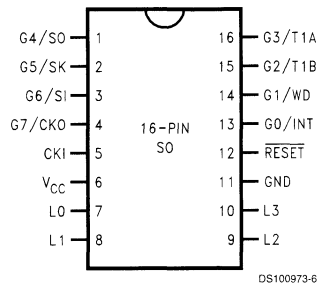
Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-maped registers allow designers to optimize the precise implementation of certain specific instructions.

1.3 PACKAGING/PIN EFFICIENCY

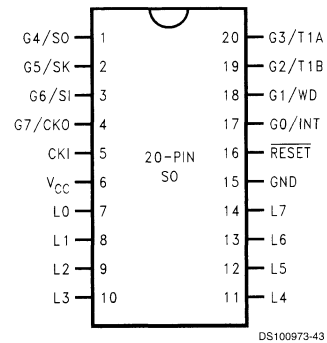
Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increase device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins: up to 90.9% (or 40 pins in the 44-pin package, these packages are not available on all COP8 devices) are devoted to useful I/O.

Connection Diagrams



Top View
Order Number COP8SEC516M
See NS Package Number M16B



Top View
Order Number COP8SEC520M or COP8SER720M
See NS Package Number M20B

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 16-, and 20-Pin Packages

Port	Type	Alt. Fun	20-Pin SO	16-Pin SO
L0	I/O	MIWU	7	7
L1	I/O	MIWU	8	8
L2	I/O	MIWU	9	9
L3	I/O	MIWU	10	10
L4	I/O	MIWU	11	
L5	I/O	MIWU	12	
L6	I/O	MIWU	13	
L7	I/O	MIWU	14	
G0	I/O	INT	17	13
G1	I/O	WDOUT*	18	14
G2	I/O	T1B	19	15
G3	I/O	T1A	20	16
G4	I/O	SO	1	1
G5	I/O	SK	2	2
G6	I	SI	3	3
G7	I	CKO	4	4
D0	O			
D1	O			
D2	O			
D3	O			
F0	I/O			
F1	I/O			
F2	I/O			
F3	I/O			
V_{CC}			6	6
GND			15	11
CKI	I		5	5
$\overline{\text{RESET}}$	I		16	12

* G1 operation as WDOUT is controlled by Mask Option.

2.1 Ordering Information

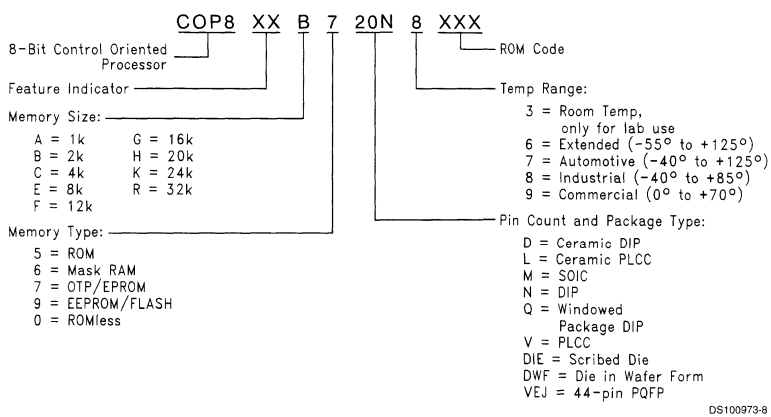


FIGURE 3. Part Numbering Scheme

National Semiconductor

COP888FH
8-Bit CMOS ROM Based Microcontrollers with 12k Memory, Comparators, USART and Hardware Multiply/Divide

General Description

The COP888FH Family of ROM based microcontrollers are highly integrated COP8™ Feature core devices with 12k memory and advanced features including Analog comparators, and Hardware Multiply/Divide. These single-chip CMOS devices are suited for more complex applications requiring a full featured controller, low EMI, two comparators, a full-duplex USART, and hardware multiply/divide functions. COP87L88FH devices are pin and software compatible (different V_{CC} range) 16k OTP (One Time Programmable) versions for pre-production , and for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1µs instruction cycle, hardware multiply/divide functions, three multi-function 16-bit timer/counters with PWM, full duplex USART, MICROWIRE/PLUS™, two Analog comparators, two power saving HALT/IDLE modes, MIWU, idle timer, high current outputs, software selectable options WATCHDOG™ and clock/oscillator mode, low EMI 2.5V to 5.5V operation, and 28/40/44 pin packages.

Devices included in this data sheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP684FH	12k ROM	512	24	28 DIP/SOIC	-55 to +125°C	4.5V to 5.5V
COP884FH	12k ROM	512	24	28 DIP/SOIC	-40 to +85°C	
COP984FH	12k ROM	512	24	28 DIP/SOIC	0 to +70°C	2.5V to 4.0V, FHH=4.0V to 6.0V
COP688FH	12k ROM	512	36/40	40 DIP, 44 PLCC	-55 to +125°C	4.5V to 5.5V
COP888FH	12k ROM	512	36/40	40 DIP, 44 PLCC	-40 to +85°C	
COP988FH	12k ROM	512	36/40	40 DIP, 44 PLCC	0 to +70°C	2.5V to 4.0V, FHH=4.0V to 6.0V

Key Features

- Hardware Multiply/Divide Functions
- Full duplex USART
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Quiet design (low radiated emissions)
- 12 kbytes on-board ROM
- 512 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Two analog comparators
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE®, Push-Pull, Weak Pull-Up, and High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Packages:
  - — 40 DIP with 36 I/O pins
  - — 44 PLCC with 40 I/O pins
  - — 28 DIP/SO with 24 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Fourteen multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Three Timers (Each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — USART (2)
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

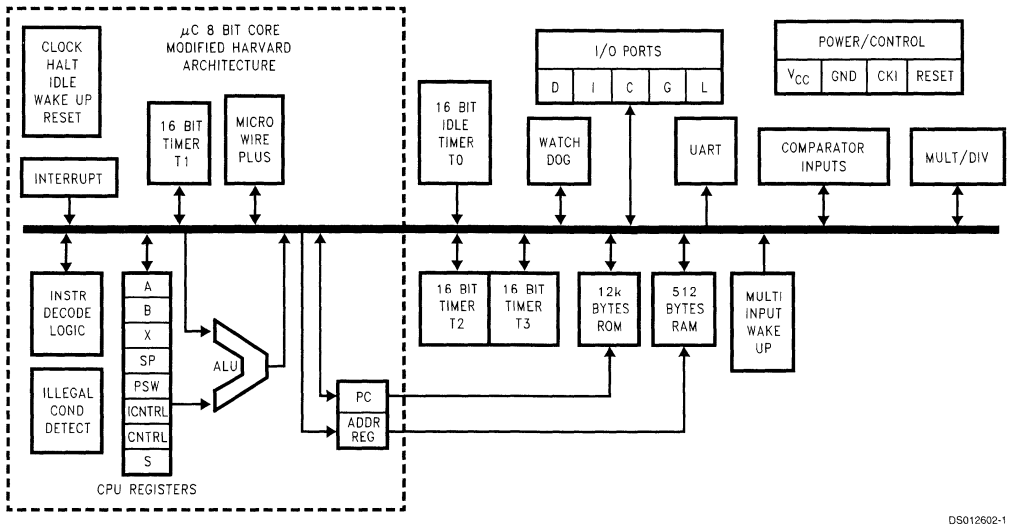
Fully Static CMOS

- Low current drain (typically < 5 µA)
- Two power saving modes: HALT and IDLE
- Single supply operation: 2.5V–5.5V
- Temperature ranges: 0°C to +70°C,
  −40°C to +85°C
  −55°C to +125°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

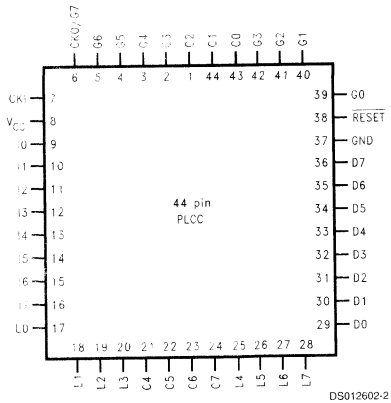


DS012602-1

FIGURE 1. COP888FH Block Diagram

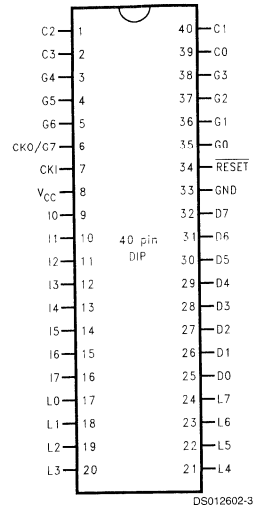
Connection Diagrams

Plastic Chip Carrier



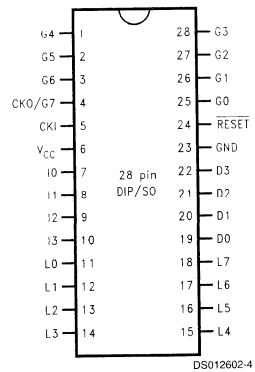
Top View
Order Number COP688FH-XXX/V,
COP888FH-XXX/V or COP988FH-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View Order
Number COP688FH-XXX/N,
COP888FH-XXX/N or COP988FH-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



Order Number COP684FH-XXX/M, COP884FH-XXX/M,
COP984FH-XXX/M, COP684FH-XXX/N,
COP884FH-XXX/N or COP984FH-XXX/N
See NS Molded Package Number M28B or N28B

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU	CKX	12	18	18
L2	I/O	MIWU	TDX	13	19	19
L3	I/O	MIWU	RDX	14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU	T3A	17	23	27
L7	I/O	MIWU	T3B	18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
I0	I			7	9	9
I1	I	COMP1IN−		8	10	10
I2	I	COMP1IN+		9	11	11
I3	I	COMP1OUT		10	12	12
I4	I	COMP2IN−			13	13
I5	I	COMP2IN+			14	14
I6	I	COMP2OUT			15	15
I7	I				16	16
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

National Semiconductor

COP888xG/CS Family
8-Bit CMOS ROM Based Microcontrollers with 4k to 24k Memory, Comparators and USART

General Description

Note: COP8SG devices are form-fit-function compatible supersets of the COP888xG/CL/CS Family devices, and are replacements for these in new designs, and design upgrades with minimum effort.

The COP888xG ROM based microcontrollers are highly integrated COP8™ Feature core devices with larger memory (4k to 24k) and advanced features including two Analog comparators. These single-chip CMOS devices are suited for more complex applications requiring a full featured controller with a range of memory sizes, low EMI (except EG), comparators, and a full-duplex USART. Pin and software compatible (different V_{CC} range) 8k toor 32k OTP (One Time Programmable) versions are available (COP8SGx7 Family). Erasable windowed versions are available for use with a range of software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1µs instruction cycle, three multi-function 16-bit timer/counters, full-duplex USART, MICROWIRE/PLUS™ serial I/O, two Analog comparators, two power saving HALT/IDLE modes, idle timer, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, low EMI 2.5V to 5.5V operation, and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP684CS	4k ROM	192	24	28 DIP/SOIC	-55 to +125˚C	4.5V - 5.5V
COP884CS	4k ROM	192	24	28 DIP/SOIC	-40 to +85˚C	
COP984CS	4k ROM	192	24	28 DIP/SOIC	-0 to +70˚C	2.5V - 4.0V, CSH=4.0V - 6.0V
COP688CS	4k ROM	192	36/40	40 DIP, 44 PLCC	-55 to +125˚C	4.5V - 5.5V
COP888CS	4k ROM	192	36/40	40 DIP, 44 PLCC	-40 to +85˚C	
COP988CS	4k ROM	192	36/40	40 DIP, 44 PLCC	-0 to +70˚C	2.5V - 4.0V, CSH=4.0V - 6.0V
COP884CG	4k ROM	128	24	28 DIP/SOIC	-40 to +85˚C	2.5V - 6.0V
COP888CG	4k ROM	128	34/38	40 DIP, 44 PLCC	-40 to +85˚C	2.5V - 6.0V
COP684EG	4k ROM	256	24	28 DIP, SOIC	-55 to +125˚C	4.5V - 5.5V
COP884EG	4k ROM	256	24	28 DIP, SOIC	-40 to +85˚C	
COP984EG	4k ROM	256	24	28 DIP, SOIC	0 to +70˚C	2.5V - 4.0V, EGH=4.0 - 6.0V
COP688EG	8k ROM	256	36/40	40 DIP, 44 PLCC	-55 to +125˚C	4.5V - 5.5V
COP888EG	8k ROM	256	36/40	40 DIP, 44 PLCC/PQFP	-40 to +85˚C	
COP988EG	8k ROM	256	36/40	40 DIP, 44 PLCC	0 to +70˚C	2.5V - 4.0V, EGH=4.0 - 6.0V
COP688GG	16k ROM	512	36/40	40 DIP, 44 PLCC/PQFP	-55 to +125˚C	4.5V - 5.5V
COP888GG	16k ROM	512	36/40	40 DIP, 44 PLCC/PQFP	-40 to +85˚C	
COP688HG	20k ROM	512	36/40	40 DIP, 44 PLCC	-55 to +125˚C	4.5V - 5.5V
COP888HG	20k ROM	512	36/40	40 DIP, 44 PLCC	-40 to +85˚C	
COP688KG	24k ROM	512	36/40	40 DIP, 44 PLCC	-55 to +125˚C	4.5V - 5.5V
COP888KG	24k ROM	512	36/40	40 DIP, 44 PLCC	-40 to +85˚C	

Key Features

- Full duplex USART
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Quiet design (low radiated emissions)
- 4 to 24 kbytes on-board ROM
- 128 to 512 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake-Up (MIWU) with optional interrupts (8)
- Two analog comparators (one for the CS series)

Additional Peripheral Features

(Continued)

- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- Up to 8 high current outputs
- Schmitt trigger inputs on ports G and L
- Packages:
  - — 44 PQFP with 40 I/O pins
  - — 44 PLCC with 40 I/O pins
  - — 40 DIP with 36 I/O pins
  - — 28 DIP/SOIC with 24 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Versatile and easy to use instruction set
- Up to fourteen multi-source vectored interrupts servicing
  - — External Interrupt with selectable edge
  - — Idle Timer T0
  - — Three Timers (one timer for the CS series)(each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake-Up
  - — Software Trap
  - — USART (2)
  - — Default VIS (default interrupt)
- 8-bit Stack Pointer SP—(stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Low current drain (typically <1 µA)
- Single supply operation: 2.5V–5.5V (COP88x)
- Temperature ranges: 0°C to +70°C, −40°C to +85°C, and −55°C to +125°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink's Development System

Block Diagram

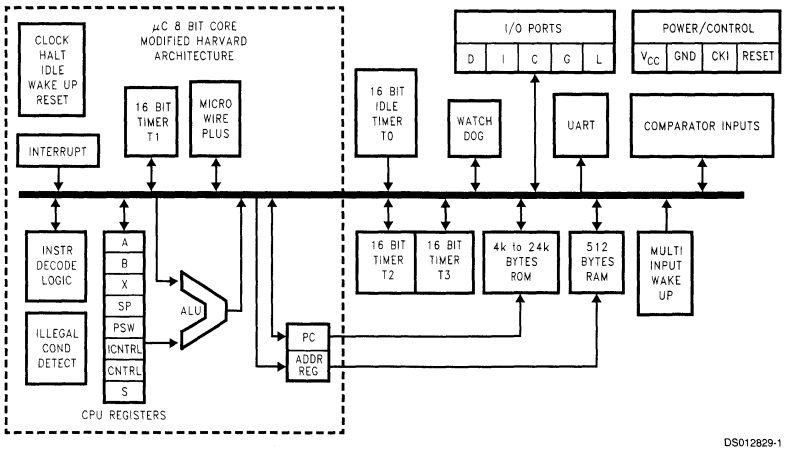
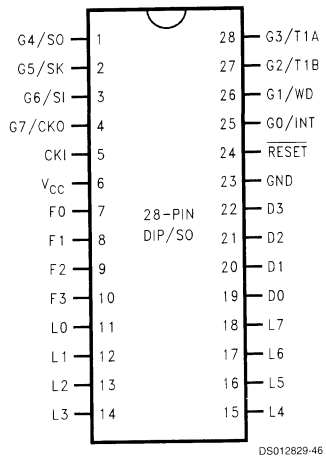


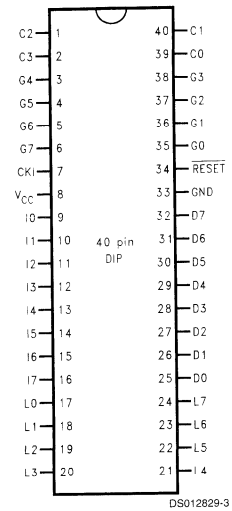
FIGURE 1. COP888xG Block Diagram

Connection Diagrams



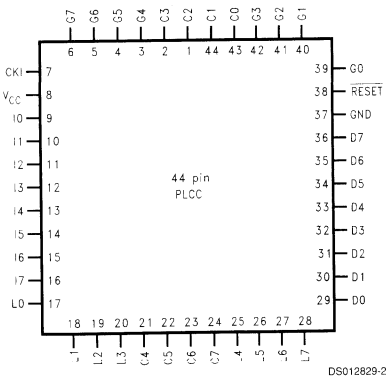
Top View
Order Number COP884CS-XXX/WM, COP984CS-XXX/WM, COP984CSH-XXX/WM, COP684CS-XXX/WM, COP884CG-XXX/WM, COP884EG-XXX/WM or COP884CS-XXX/N, COP984CS-XXX/N, COP984CSH-XXX/N, COP884CG-XXX/N, COP884EG-XXX/N
See NS Package Number M28B or N28A

Dual-In-Line Package

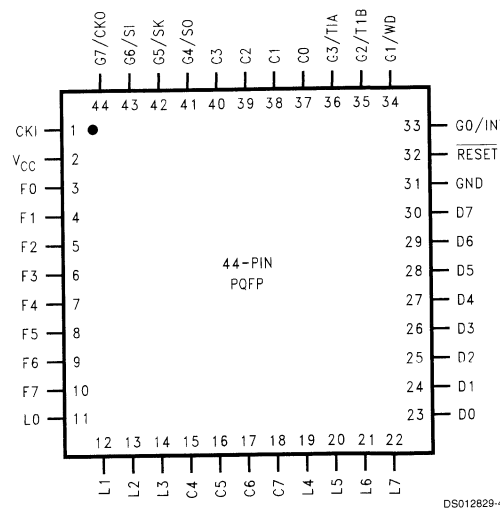


Top View
Order Number COP888CS-XXX/N, COP988CS-XXX/N, COP688CS-XXX/N, COP988CSH-XXX/N, COP888CG-XXX/N, COP688EG-XXX/N, COP888GG-XXX/N, COP688GG-XXX/N, COP888GG-XXX/N, COP688HG-XXX/N, COP888HG-XXX/N, COP688KG-XXX/N, or COP888KG-XXX/N
See NS Package Number N40A

Plastic Chip Carrier



Top View
Order Number COP688CS-XXX/V, COP888CS-XXX/V, COP988CS/CSH-XXX/V, COP688EG-XXX/V, COP888EG-XXX/V, COP988EG-XXX/V, COP888CG-XXX/V, COP688GG-XXX/V, COP888GG-XXX/V, COP688HG-XXX/V, COP888HG-XXX/V, COP688KG-XXX/V, or COP888KG-XXX/V
See NS Package Number V44A



Top View
Order Number COP888EG-XXX/VEJ, COP688GG-XXX/VEJ, COP888GG-XXX/VEJ,
See NS Package Number VEJ44A

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin DIP/SO	40-Pin DIP	44-Pin PLCC	44-Pin PQFP
L0	I/O	MIWU		11	17	17	11
L1	I/O	MIWU	CKX	12	18	18	12
L2	I/O	MIWU	TDX	13	19	19	13
L3	I/O	MIWU	RDX	14	20	20	14
L4	I/O	MIWU	T2A*	15	21	25	19
L5	I/O	MIWU	T2B*	16	22	26	20
L6	I/O	MIWU	T3A*	17	23	27	21
L7	I/O	MIWU	T3B*	18	24	28	22
G0	I/O	INT		25	35	39	33
G1	WDOUT			26	36	40	34
G2	I/O	T1B		27	37	41	35
G3	I/O	T1A		28	38	42	36
G4	I/O	SO		1	3	3	41
G5	I/O	SK		2	4	4	42
G6	I	SI		3	5	5	43
G7	I/CKO	HALT Restart		4	6	6	44
D0	O			19	25	29	23
D1	O			20	26	30	24
D2	O			21	27	31	25
D3	O			22	28	32	26
D4	O				29	33	7
D5	O				30	34	8
D6	O				31	35	9
D7	O				32	36	10
I0	I			7	9	9	27
I1	I	COMP1IN−		8	10	10	28
I2	I	COMP1IN+		9	11	11	29
I3	I	COMP1OUT		10	12	12	30
I4	I	COMP2IN−*			13	13	3
I5	I	COMP2IN+*			14	14	4
I6	I	COMP2OUT*			15	15	5
I7	I				16	16	6
C0	I/O				39	43	37
C1	I/O				40	44	38
C2	I/O				1	1	39
C3	I/O				2	2	40
C4	I/O					21	15
C5	I/O					22	16
C6	I/O					23	17
C7	I/O					24	18
V_{CC}				6	8	8	2
GND				23	33	37	31
CKI				5	7	7	1
$\overline{\text{RESET}}$				24	34	38	32

Note 1: * Not available on the CS series

National Semiconductor

COP884BC
8-Bit CMOS ROM Based Microcontrollers with 2k Memory, Comparators, and CAN Interface

General Description

The following part number is a pin count and temperature variation of the COP884BC: COP885BC.

The COP884BC ROM based microcontrollers are highly integrated COP8™ Feature core devices with 2k memory and advanced features including a CAN 2.0B (passive) interface and two Analog comparators. These single-chip CMOS devices are suited for applications requiring a full featured controller with a CAN interface, low EMI, and an 8-bit 39 kHz PWM timer. COP87L84BC devices are pin and software compatible 16k OTP (One Time Programmable) versions for pre-production, and for use with a range of COP8 software and hardware development tools.

Features include an 8-bit memory mapped architecture, 10 MHz CKI (crystal osc) with 1μs instruction cycle, one multi-function 16-bit timer/counter, 8-bit 39 kHz PWM timer with 2 outputs, CAN 2.0B (passive) interface, MICROWIRE/PLUS™ serial I/O, two Analog comparators, two power saving HALT/IDLE modes, idle timer, MIWU, software selectable I/O options, Power on Reset, low EMI 4.5V to 5.5V operation, and 20/28 pin packages.

Note: A companion device with CAN interface, more I/O and memory, A/D, and USART is the COP888EB.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP684BC	2k ROM	64	18	28 SOIC	-55 to +125°C
COP884BC	2k ROM	64	18	28 SOIC	-40 to +85°C
COP685BC	2k ROM	64	10	20 SOIC	-55 to +125°C
COP885BC	2k ROM	64	10	20 SOIC	-40 to +85°C

Key Features

- CAN 2.0B (passive) Interface
- Power On Reset (selectable)
- One 16-bit timer, with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- High speed, constant resolution 8-bit PWM/frequency monitor timer with 2 output pins
- 2048 bytes on-board ROM
- 64 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake Up (MIWU) with optional interrupts (7)
- Two analog comparators
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Packages: 28 SO with 18 I/O pins and 20 SO with 10 I/O pins

CPU/Instruction Set Features

- 1 μs instruction cycle time
- Eleven multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Timer T1 (with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — PWM Timer
  - — CAN Interface (with 3 interrupts)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Low current drain (typically <1 μA)
- Single supply operation: 4.5V–5.5V
- Temperature ranges: –40°C to +85°C, –55°C to +125°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development Systems

Block Diagram

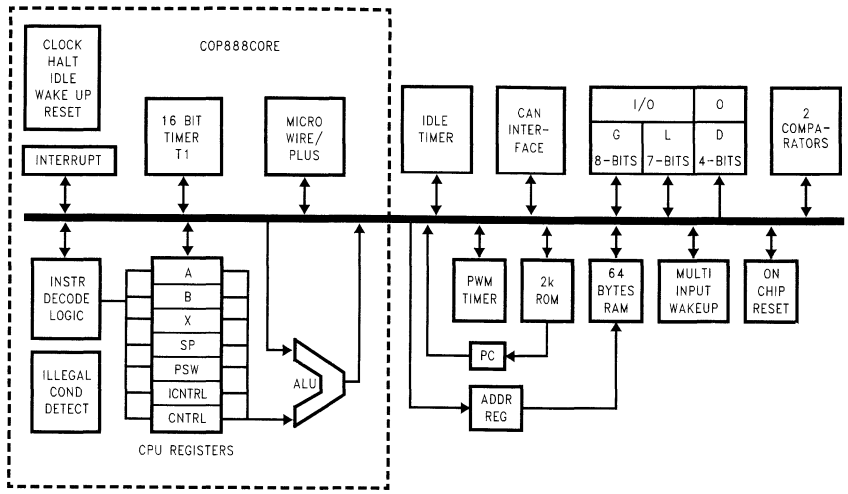
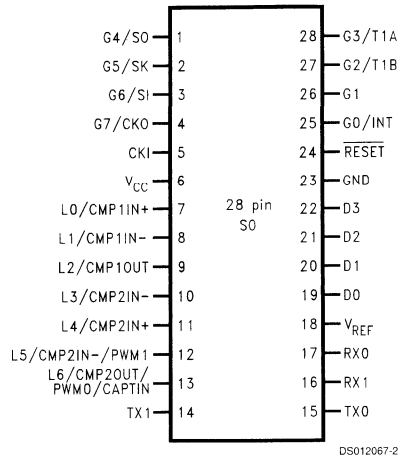
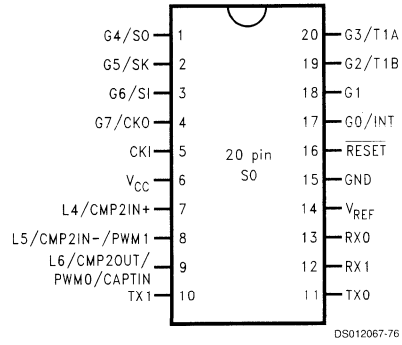


FIGURE 1. Block Diagram

Connection Diagrams



Top View
Order Number COP884BC-xxx/WM or COP684BC-xxx/WM
See NS Package Number M28B



Top View
Order Number COP885BC-xxx/WM or COP685BC-xxx/WM
See NS Package Number M20B

FIGURE 2. Connection Diagrams

Pinouts for 28-SO Package

Port Pin	Type	Alt. Function	20-Pin SO	28-Pin SO
G0	I/O	INTR	17	25
G1	I/O		18	26
G2	I/O	T1B	19	27
G3	I/O	T1A	20	28
G4	I/O	SO	1	1
G5	I/O	SK	2	2
G6	I	SI	3	3
G7	I	CKO	4	4
L0	I/O	CMP1IN+/MIWU		7
L1	I/O	CMP1IN-/MIWU		8
L2	I/O	CMP10UT/MIWU		9
L3	I/O	CMP2IN-/MIWU		10
L4	I/O	CMP2IN+/MIWU	7	11
L5	I/O	CMP2IN-/PWM1/MIWU	8	12
L6	I/O	CMP2OUT/PWM0/ CAPTIN/MIWU	9	13
D0	O			19
D1	O			20
D2	O			21
D3	O			22
CAN V_{REF}			14	18
CAN Tx0	O		11	15
CAN Tx1	O		10	14
CAN Rx0	I	MIWU (Note 1)	13	17
CAN Rx1	I	MIWU	12	16
V_{CC}			6	6
GND			15	23
CKI	I		5	5
$\overline{\text{RESET}}$	I		16	24

Note 1: The MIWU function for the CAN interface is internal (see CAN interface block diagram)

National Semiconductor

COP888EB
8-Bit CMOS ROM Based Microcontrollers with 8k Memory, CAN Interface, 8-Bit A/D, and USART

General Description

The COP888EB ROM based microcontrollers are highly integrated COP8™ Feature core devices with 8k memory and advanced features including a CAN 2.0B (passive) interface, A/D and USART. These single-chip CMOS devices are suited for applications requiring a full featured controller with a CAN interface, low EMI, and versatile communications interfaces. COP87L8EB/RB devices are pin and software compatible 16k or 32k OTP (One Time Programmable) versions for pre-production, and for use with a range of COP8 software and hardware development tools.

Features include an 8-bit memory mapped architecture, 10 MHz CKI with 1μs instruction cycle, two multi-function 16-bit timer/counters, WATCHDOG™ and Clock Monitor, CAN 2.0B (passive) interface, MICROWIRE/PLUS™ serial I/O, SPI master/slave interface, fully buffered USART, 8-bit A/D with 8 channels, two power saving HALT/IDLE modes, MIWU, idle timer, software selectable I/O options, low EMI 4.5V to 5.5V operation, and 44/68 pin packages.

Note: A companion device with CAN interface, less I/O and memory, and PWM timer is the COP888BC.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP688EB	8k ROM	192	31	44 PLCC	-55 to +125°C
COP888EB	8k ROM	192	31	44 PLCC	-40 to +85°C
COP689EB	8k ROM	192	58	68 PLCC	-55 to +125°C
COP889EB	8k ROM	192	58	68 PLCC	-40 to +85°C

Key Features

- CAN bus interface, with Software Power save mode
- 8-bit A/D Converter with 8 channels
- Fully buffered USART
- Multi-input wake up (MIWU) on both Port L and M
- SPI Compatible Master/Slave Interface
- Quiet Design (Low Radiated Emissions)
- 8096 bytes of on-board ROM
- 192 bytes of on-board RAM

Additional Peripheral Features

- Idle timer (programmable)
- Two 16-bit timer, with two 16-bit registers supporting
  - — Processor independent PWM mode
  - — External Event counter mode
  - — Input capture mode
- WATCHDOG and Clock Monitor
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE® outputs, Push pull outputs, Weak pull up input, High impedance input)
- Schmitt trigger inputs on Port G, L and M
- Packages: 44 PLCC with 31 I/O pins
  68 PLCC with 58 I/O pins

CPU/Instruction Set Features

- 1 μs instruction cycle time
- Fourteen multi-sourced vectored interrupts servicing
  - — External interrupt
  - — Idle Timer T0
  - — Timers (T1 and T2) (4 Interrupts)
  - — MICROWIRE/PLUS and SPI
  - — Multi-input Wake up
  - — Software Trap
  - — CAN interface (3 interrupts)
  - — USART (2 Inputs)
- Versatile easy to use instruction set
- 8-bit stack pointer (SP) (Stack in RAM)
- Two 8-bit Register Indirect Memory Pointers (B, X)

Fully Static CMOS

- Two power saving modes: HALT, IDLE
- Single supply operation: 4.5V to 5.5V
- Temperature ranges: −40°C to +85°C and −55°C to +125°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Basic Functional Description

- CAN I/F—CAN serial bus interface block as described in the CAN specification part 2.0B (Passive)
  - — Interface rates up to 250k bit/s are supported utilizing standard message identifiers
- Programmable double buffered USART
- A/D—8-bit, 8 channel, 1-LSB Resolution, with improved Source Impedance and improved channel to channel cross talk immunity
- Multi-Input-Wake-Up (MIWU)—edge selectable wake-up and interrupt capability via input port and CAN interface (Port L, Port M and CAN I/F); supports Wake-Up capability on SPI, USART, and T2 capture
- Port C—8-bit bi-directional I/O port
- Port D—8-bit Output port with high current drive capability (10 mA)
- Port F—8-bit bidirectional I/O
- Port G—8-bit bidirectional I/O port, including alternate functions for:
  - — MICROWIRE™ Input and Output
  - — Timer 1 Input or Output (Depending on mode selected)
  - — External Interrupt input
  - — WATCHDOG Output
- Port I—8-bit input port combining either digital input, or up to eight A/D input channels
- Port L—8-bit bidirectional I/O port, including alternate functions for:
  - — USART Transmit/Receive I/O
  - — Multi-input-wake up (MIWU on all pins)
- Port M—8-bit I/O port, with the following alternate function
  - — SPI Interface
  - — MIWU
  - — CAN Interface Wake-up (MSB)
  - — Timer 2 Input or Output (Depending on mode selected)
- Port N—8-bit bidirectional I/O
  - — SPI Slave Select Expander
- Two 16-bit multi-function Timer counters (T1 and T2) plus supporting registers
  - — (I/P Capture, PWM and Event Counting)
- Idle timer—Provides a basic time-base counter, (with interrupt) and automatic wake up from IDLE mode programmable
- MICROWIRE/PLUS—MICROWIRE serial peripheral interface, supporting both Master and Slave operation
- HALT and IDLE—Software programmable low current modes
  - — HALT—Processor stopped, Minimum current
  - — IDLE—Processor semi-active more than 60% power saving
- 8 kBytes ROM and 192 bytes of on board static RAM
- SPI Master/Slave interface includes 12 bytes Transmit and 12 bytes Receive FIFO Buffers. Operates up to 1M Bit/S
- On board programmable WATCHDOG and CLOCK Monitor

Applications

- Automobile Body Control and Comfort System
- Integrated Driver Informaiton Systems
- Steering Wheel Control
- Car Radio Control Panel
- Sensor/Actuator Applications in Automotive and Industrial Control

Block Diagram

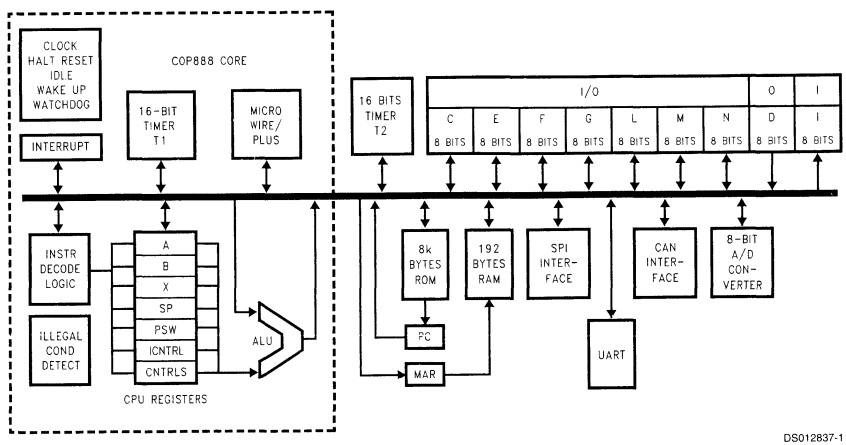
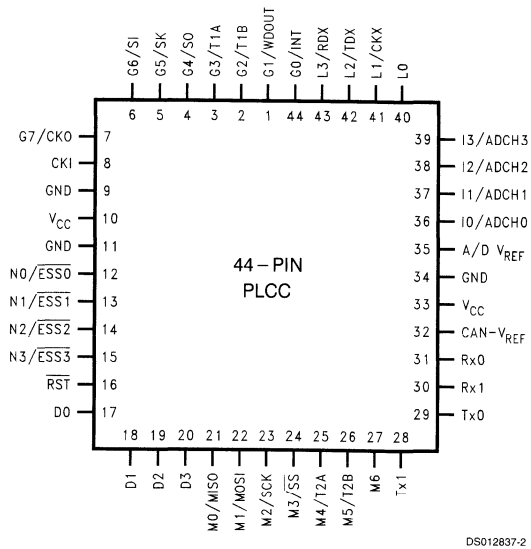


FIGURE 1. Block Diagram

Connection Diagrams

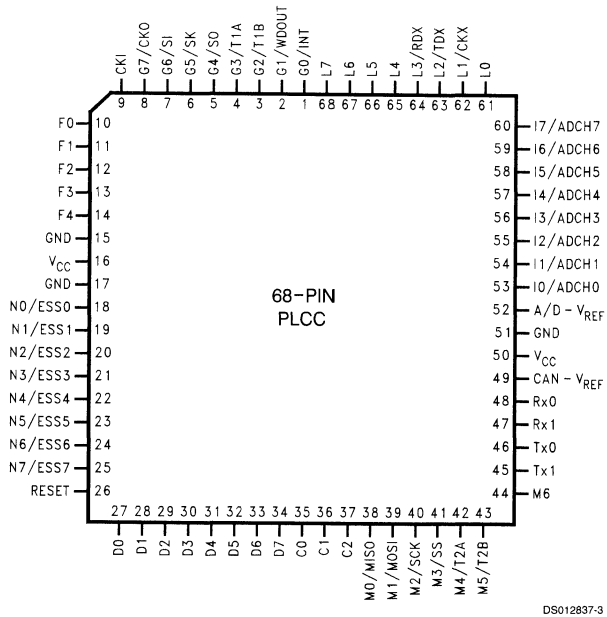
Plastic Chip Carrier



DS012837-2

Top View
Order Number COP888EB-XXX/V, COP688EB-XXX/V
See NS Plastic Chip Package Number V44A

Plastic Leaded Chip Carrier



DS012837-3

Top View
Order Number COP889EB-XXX/V, COP689EB-XXX/V
See NS Plastic Chip Package Number V68A

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 44-Pin and 68-Pin Packages

Port Pin	Type	ALT Function	44-Pin PLCC	68-Pin PLCC
G0	I/O	INT	44	1
G1	I/O	WDOUT	1	2
G2	I/O	T1B	2	3
G3	I/O	T1A	3	4
G4	I/O	SO	4	5
G5	I/O	SK	5	6
G6	I	SI	6	7
G7	I	CKO	7	8
D0	O		17	27
D1	O		18	28
D2	O		19	29
D3	O		20	30
D4	O			31
D5	O			32
D6	O			33
D7	O			34
I0	I	ADCH0	36	53
I1	I	ADCH1	37	54
I2	I	ADCH2	38	55
I3	I	ADCH3	39	56
I4	I	ADCH4		57
I5	I	ADCH5		58
I6	I	ADCH6		59
I7	I	ADCH7		60
L0	I/O	MIWU	40	61
L1	I/O	MIWU;CKX	41	62
L2	I/O	MIWU;TDX	42	63
L3	I/O	MIWU;RDX	43	64
L4	I/O	MIWU		65
L5	I/O	MIWU		66
L6	I/O	MIWU		67
L7	I/O	MIWU		68
M0	I/O	MIWU;MISO	21	38
M1	I/O	MIWU;MOSI	22	39
M2	I/O	MIWU;SCK	23	40
M3	I/O	MIWU;$\overline{SS}$	24	41
M4	I/O	MIWU;T2A	25	42
M5	I/O	MIWU;T2B	26	43
M6	I/O	MIWU	27	44
N0	I/O	ESS0	12	18
N1	I/O	ESS1	13	19
N2	I/O	ESS2	14	20
N3	I/O	ESS3	15	21
N4	I/O	ESS4		22
N5	I/O	ESS5		23
N6	I/O	ESS6		24
N7	I/O	ESS7		25

Port Pin	Type	ALT Function	44-Pin PLCC	68-Pin PLCC
F0	I/O			10
F1	I/O			11
F2	I/O			12
F3	I/O			13
F4	I/O			14
C0	I/O			35
C1	I/O			36
C2	I/O			37
RX0	I		31	48
RX1	I		30	47
TX0	O		29	46
TX1	O		28	45
$CANV_{REF}$			32	49
CKI			8	9
RESET			16	26
DV_{CC}			10, 33	16, 50
GND			9, 11, 34	15, 17, 51
A/D V_{REF}			35	52

National Semiconductor

COP888CF
8-Bit CMOS ROM Based Microcontrollers with 4k Memory and A/D Converter

General Description

The COP888CF ROM based microcontrollers are highly integrated COP8™ Feature core devices with 4k memory and advanced features including an A/D Converter. These single-chip CMOS devices are suited for applications requiring a full featured controller with an 8-bit A/D converter. Pin and software compatible (different V_{CC} range) 16k/32k OTP (One Time Programmable) versions are available (COP87L88CF Family) for pre-production, and for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1 µs instruction cycle, two multi-function 16-bit timer/counters, MICROWIRE/PLUS™ serial I/O, one 8-bit/8-channel A/D converter with prescaler and both differential and single ended modes, crystal or R/C oscillator, two power saving HALT/IDLE modes, idle timer, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, 2.5V to 6.0V operation and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory	RAM	I/O Pins	Packages	Temperature
COP884CF	4k bytes ROM	128 bytes	22	28 DIP/SOIC	-40 to +85˚C
COP984CF	4k bytes ROM	128 bytes	22	28 DIP/SOIC	-0 to +70˚C
COP888CF	4k bytes ROM	128 bytes	34/38	40 DIP, 44 PLCC	-40 to +85˚C
COP988CF	4k bytes ROM	128 bytes	34/38	40 DIP, 44 PLCC	-0 to +70˚C

Key Features

- A/D converter (8-bit, 8-channel, with prescaler and both differential and single ended modes)
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 4 kbytes of on-chip ROM
- 128 bytes of on-chip RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake Up (MIWU) with optional interrupts (8)
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE®Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- High current outputs
- Packages:
  - — 44 PLCC with 38 I/O pins
  - — 40 DIP with 34 I/O pins
  - — 28 DIP/SO with 22 I/O pins
- Schmitt trigger inputs on Port G

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Ten multi-source vectored interrupts servicing
  - — External interrupt with selectable edge
  - — Idle Timer T0
  - — Two Timers (Each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B, X)

Fully Static CMOS

- Low current drain (typically < 1 µA)
- Single supply operation: 2.5V to 6.0V
- Temperature ranges: 0˚C to +70˚C, and -40˚C to +85˚C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

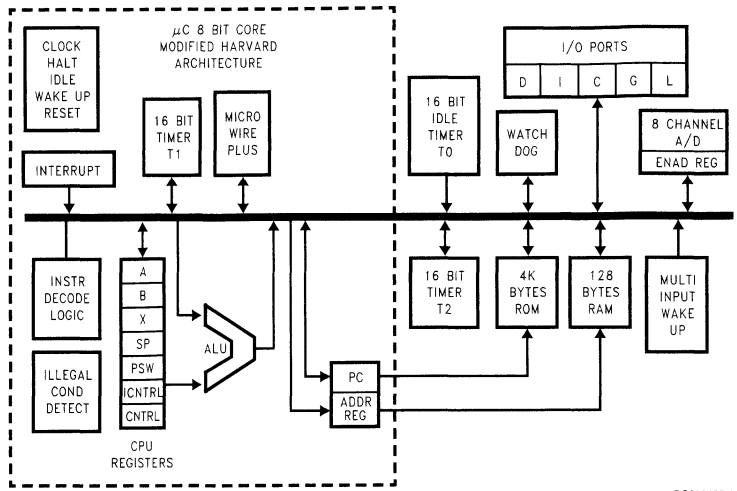
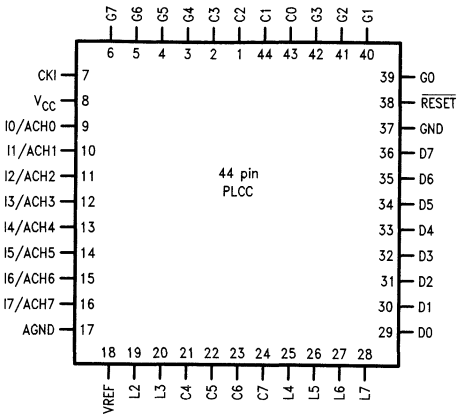


FIGURE 1. Block Diagram

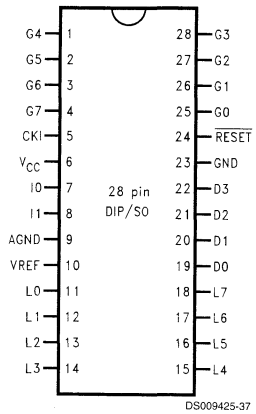
Connection Diagrams

Plastic Chip Carrier



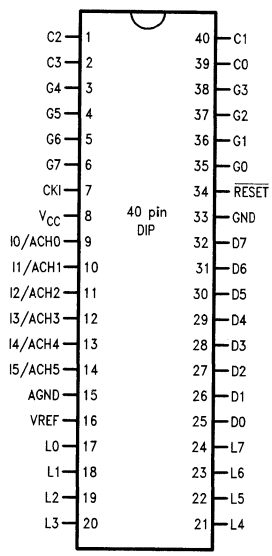
Top View
Order Number COP888CF-XXX/V
COP988CF-XXX/V or COP988CFH-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View
Order Number COP884CF-XXX/N,
COP884CF-XXX/WM, COP984CF-XXX/N,
COP984CFH-XXX/N, COP984CFH-XXX/WM
or COP984CFH-XXX/WM
See NS Package Number N28B or M28B

Dual-In-Line Package



Top View
Order Number COP888CF-XXX/N,
COP988CF-XXX/N or COP988CFH-XXX/N
See NS Molded Package Number N40A

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	—
L1	I/O	MIWU		12	18	—
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
I0	I	ACH0		7	9	9
I1	I	ACH1		8	10	10
I2	I	ACH2			11	11
I3	I	ACH3			12	12
I4	I	ACH4			13	13
I5	I	ACH5			14	14
I6	I	ACH6				15
I7	I	ACH7				16
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{REF}	$+V_{REF}$			10	16	18
AGND	AGND			9	15	17
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

National Semiconductor

COP888GD
8-Bit CMOS ROM Based Microcontrollers with 16k Memory and 8-Channel A/D

General Description

The COP888GD ROM based microcontrollers are highly integrated COP8™ Feature core devices with 16k memory and advanced features including an A/D Converter. These multi-chip CMOS devices are suited for applications requiring a full featured controller with an 8-bit A/D converter, and as pre-production devices for a masked ROM design. Pin and software compatible 16k or 32k OTP EPROM versions are available (COP87L88GD/RD Family) for pre-production, and for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1µs instruction cycle, three multi-function 16-bit timer/counters, MICROWIRE/PLUS™ serial I/O, one 8-bit/8-channel A/D converter with prescaler and both differential and single ended modes, two power saving HALT/IDLE modes, MIWU, idle timer, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, 2.5V to 5.5V operation, program code security, and 44 pin package.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP688GD	16k ROM	256	40	44 PLCC	-55 to +125°C	4.5V to 5.5V
COP888GD	16k ROM	256	40	44 PLCC	-40 to +85°C	2.5V to 5.5V
COP988GD	16k ROM	256	40	44 PLCC	0 to +70°C	2.5V to 4.0V, GDH = 4.0V to 6.0V

Key Features

- 8-channel A/D converter with prescaler and both differential and single ended modes
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Quiet design (low radiated emissions)
- 16 kbytes on-board ROM
- 256 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- WATCHDOG and clock monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull Up Input, High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Package:
  - — 44 PLCC with 40 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Twelve multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Three Timers (each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP) – stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.5V to 5.5V
- Temperature range: –0°C to +70°C and –40°C to +85°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

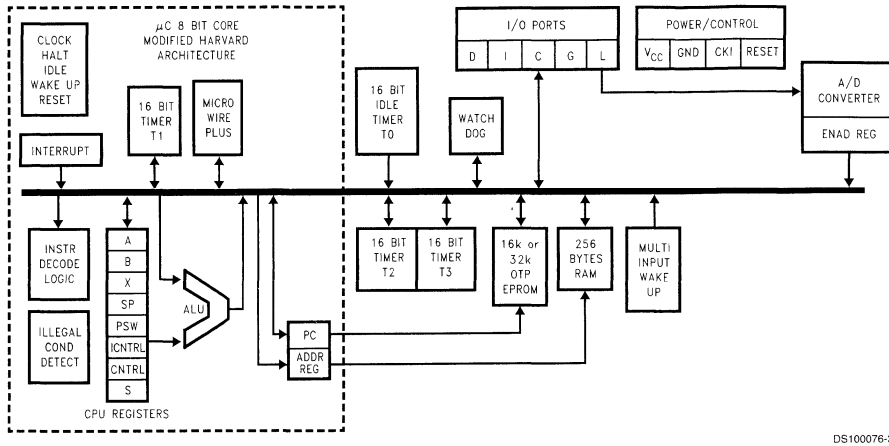
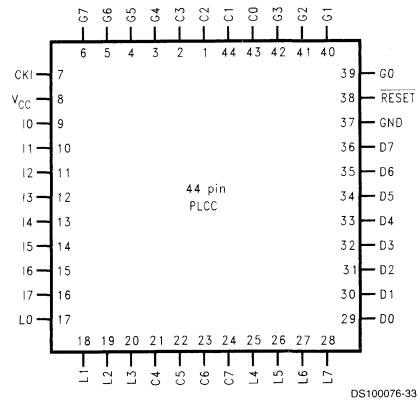


FIGURE 1. Block Diagram

Connection Diagram

Plastic Chip Carrier



Top View
Order Number COP888GD-XXXV, COP988GD-XXX/V
See NS Plastic Chip Package Number V44A

FIGURE 2. Connection Diagram

Connection Diagram (Continued)

Pinouts for 44-Pin Package

Port	Type	Alt. Fun	Alt. Fun	44-Pin Pack.
L0	I/O	MIWU		17
L1	I/O	MIWU		18
L2	I/O	MIWU		19
L3	I/O	MIWU		20
L4	I/O	MIWU	T2A	25
L5	I/O	MIWU	T2B	26
L6	I/O	MIWU	T3A	27
L7	I/O	MIWU	T3B	28
G0	I/O	INT		39
G1	WDOUT			40
G2	I/O	T1B		41
G3	I/O	T1A		42
G4	I/O	SO		3
G5	I/O	SK		4
G6	I	SI		5
G7	I/CKO	HALT Restart		6
D0	O			29
D1	O			30
D2	O			31
D3	O			32
D4	O			33
D5	O			34
D6	O			35
D7	O			36
I0	I	ACH0		9
I1	I	ACH1		10
I2	I	ACH2		11
I3	I	ACH3		12
I4	I	ACH4		13
I5	I	ACH5		14
I6	I	ACH6		15
I7	I	ACH7		16
C0	I/O			43
C1	I/O			44
C2	I/O			1
C3	I/O			2
C4	I/O			21
C5	I/O			22
C6	I/O			23
C7	I/O			24
V_{CC}				8
GND				37
CKI				7
$\overline{\text{RESET}}$				38

National Semiconductor

COP8ACC Family
8-Bit CMOS ROM Based and OTP Microcontrollers with 4k or 16k Memory and High Resolution A/D

General Description

The COP8ACC Family ROM based microcontrollers are highly integrated COP8™ Feature core devices with 4k memory and advanced features including a High-Resolution A/D. These single-chip CMOS devices are suited for applications requiring a full featured, low EMI controller with an A/D (only one external capacitor required). COP8ACC7 devices are pin and software compatible (different V_{CC} range) 16k OTP EPROM versions for pre-production. Erasable windowed versions are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 4 MHz CKI with 2.5μs instruction cycle, 6 channel A/D with 12-bit resolution, analog capture timer, analog current source and $V_{CC}/2$ reference, one multi-function 16-bit timer/counter, MICROWIRE/PLUS serial I/O, two power saving HALT/IDLE modes, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, Low EMI 2.5V to 5.5V operation and 20/28 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP8ACC5xxx9	4k ROM	128	15/23	20 SOIC, 28 DIP/SOIC	0 to +70˚C
COP8ACC5xxx8	4k ROM	128	15/23	20 SOIC, 28 DIP/SOIC	-40 to +85˚C
COP8ACC7xxx9	16k OTP EPROM	128	15/23	20 SOIC, 28 DIP/SOIC	0 to +70˚C
COP8ACC7xxx8	16k OTP EPROM	128	15/23	20 SOIC, 28 DIP/SOIC	-40 to +85˚C

Key Features

- Analog Function Block with 12-bit A/D including
  - — Analog comparator with seven input mux
  - — Constant Current Source and $V_{CC/2}$ Reference
  - — 16-bit capture timer (upcounter) clocked from CKI with auto reset on timer startup
- Quiet design (reduced radiated emissions)
- 4096 bytes on-board ROM or 16,384 OTP EPROM with security feature
- 128 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- One 16-bit timer with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Multi-Input Wake-Up (MIWU) with optional interrupts
- WATCHDOG and clock monitor logic
- MICROWIRE/PLUS™ serial I/O with programmable shift clock-polarity

I/O Features

- Software selectable I/O options (Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- High current outputs
- Schmitt Trigger inputs on ports G and L
- Packages: 28 DIP/SO with 23 I/O pins, 20 SO with 15 I/O pins

CPU/Instruction Set Features

- 2.5 μs instruction cycle time
- Eight multi-source vectored interrupt servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Timer T1 associated Interrupts
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS
  - — A/D (Capture Timer)
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Registers Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.5V to 5.5V for COP8ACC5
- Single supply operation: 2.7V to 5.5V for COP8ACC7
- Temperature ranges: 0˚C to +70˚C, −40˚C to +85˚C

Development System

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink development system

Applications

- Battery Chargers
- Appliances
- Data Acquisition systems

Block Diagram

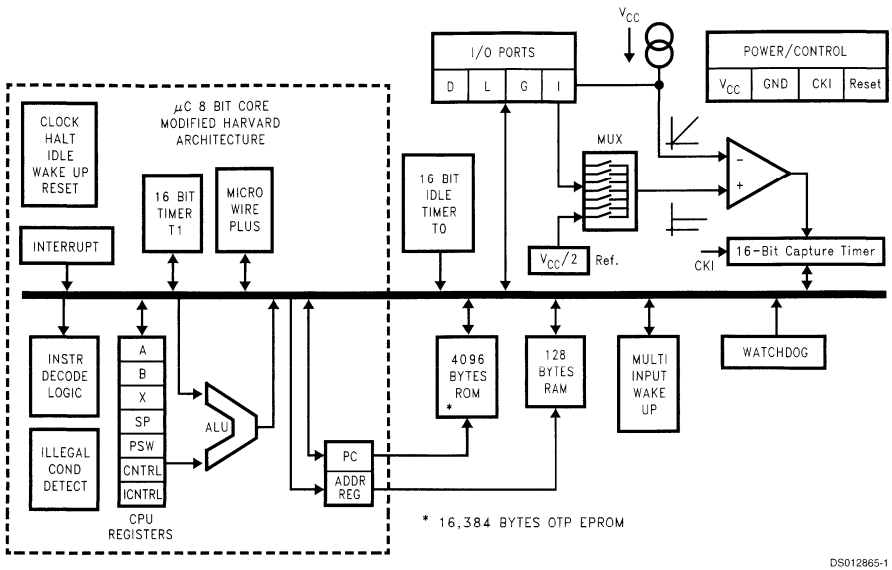
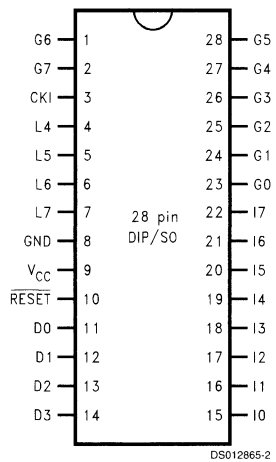
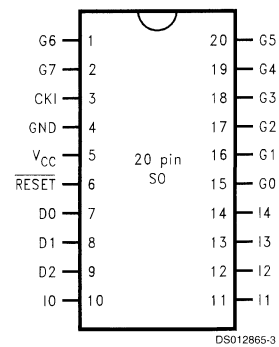


FIGURE 1. Block Diagram

Connection Diagrams



Top View
Order Number COP8ACC528N9 or COP8ACC528N8
See NS Molded Package Number N28A
Order Number COP8ACC528M9 or COP8ACC528M8
Order Number COP8ACC728N9-XE or COP8ACC728N8-XE
Order Number COP8ACC728M9-XE or COP8ACC728M8-XE
See NS Molded Package Number M28B



Note: -X Crystal Oscillator
Note: -E Halt Enable

Top View
Order Number COP8ACC520M9 or COP8ACC520N8
Order Number COP8ACC720M9-XE or COP8ACC720N8-XE
See NS Molded Package Number M20B

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-Pin, 20-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin DIP/SO	20-Pin SO
L4	I/O	MIWU	Ext. Int.	4	
L5	I/O	MIWU	Ext. Int.	5	
L6	I/O	MIWU	Ext. Int.	6	
L7	I/O	MIWU	Ext. Int.	7	
G0	I/O	INT		23	15
G1	WDOUT			24	16
G2	I/O	T1B		25	17
G3	I/O	T1A		26	18
G4	I/O	SO		27	19
G5	I/O	SK		28	20
G6	I	SI		1	1
G7	I/CKO	HALT Restart		2	2
D0	O			11	7
D1	O			12	8
D2	O			13	9
D3	O			14	
I0	I	Analog CH1		15	10
I1	I	I_{SRC}		16	11
I2	I	Analog CH2		17	12
I3	I	Analog CH3		18	13
I4	I	Analog CH4		19	14
I5	I	Analog CH5		20	
I6	I	Analog CH6		21	
I7	I	C_{OUT}		22	
V_{CC}				9	5
GND				8	4
CKI				3	3
$\overline{\text{RESET}}$				10	6

Ordering Information

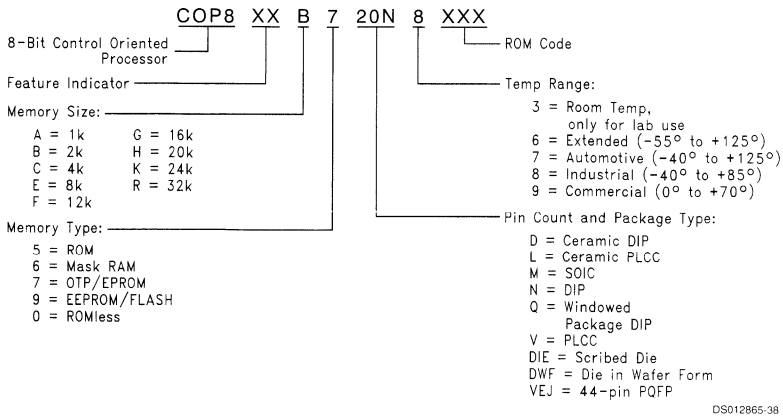


FIGURE 3. Part Numbering Scheme

National Semiconductor

COP888EK
8-Bit CMOS ROM Based Microcontrollers with 8k Memory, Comparator, and Single-slope A/D Capability

General Description

The COP888EK ROM based microcontrollers are highly integrated COP8™ Feature core devices with 8k memory and advanced features including a Multi-Input Comparator and Single-slope A/D capability. These single-chip CMOS devices are suited for applications requiring a full featured, low EMI controller with an analog comparator, current source, and voltage reference. The COP87L88EK/RK Family devices are pin and software compatible (different V_{CC} range) 16k or 32k OTP (One Time Programmable) versions for pre-production, and for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1µs instruction cycle, three multi-function 16-bit timer/counters with PWM, MICROWIRE/PLUS™ serial I/O, one analog comparator with seven input multiplexor, an analog current source and V_{CC} reference, two power saving HALT/IDLE modes, idle timer, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, Low EMI 2.5V to 6.0V operation and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP684EK	8k ROM	256	24	28 DIP/SOIC	-55 to +125°C	4.5V - 5.5V
COP884EK	8k ROM	256	24	28 DIP/SOIC	-40 to +85°C	
COP984EK	8k ROM	256	24	28 DIP/SOIC	0 to +70°C	2.5V - 4.0V, EKH=4.0V - 6.0V
COP688EK	8k ROM	256	36/40	40 DIP, 44 PLCC	-55 to +125°C	4.5V - 5.5V
COP888EK	8k ROM	256	36/40	40 DIP, 44 PLCC	-40 to +85°C	
COP988EK	8k ROM	256	36/40	40 DIP, 44 PLCC	0 to +70°C	2.5V - 4.0V, EKH=4.0V - 6.0V

Key Features

- Analog function block with
  - — Analog comparator with seven input multiplexor
  - — Constant current source and $V_{CC}/2$ reference
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8 kbytes of on-chip ROM
- 256 bytes of on-chip RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake Up (MIWU) with optional interrupts (8)
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE™ Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- High current outputs
- Schmitt trigger inputs on Port G and L
- Packages: 44 PLCC with 40 I/O pins, 40 DIP with 36 I/O pins, and 28 DIP/SO with 24 I/O pins

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Twelve multi-source vectored interrupts servicing
  - — External Interrupt with selectable edge
  - — Idle Timer T0
  - — Three Timers (Each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B, X)

Fully Static CMOS

- Single supply operation: 2.5V to 6.0V
- Temperature ranges: 0°C to +70°C, −40°C to +85°C, and −55°C to +125°C

Development Support

- Emulation and OTP devices
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

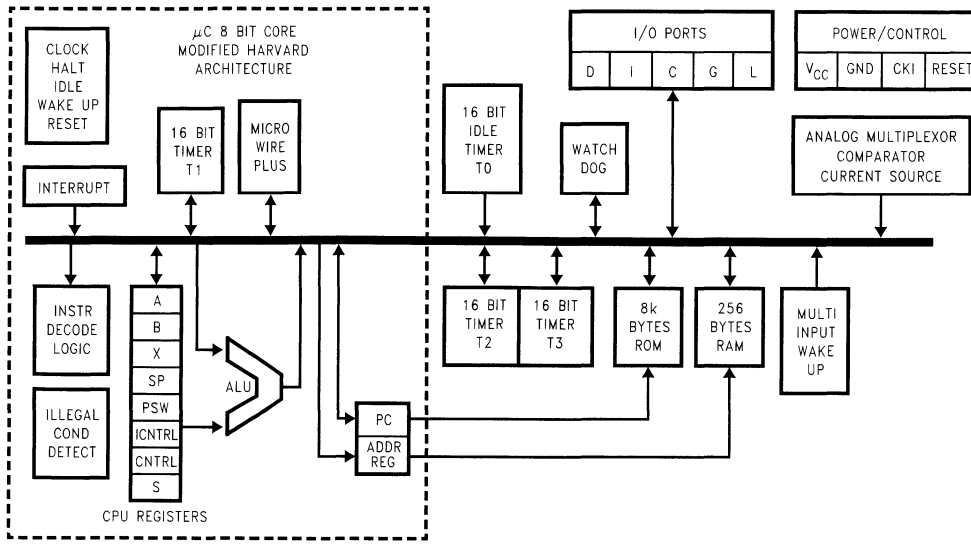
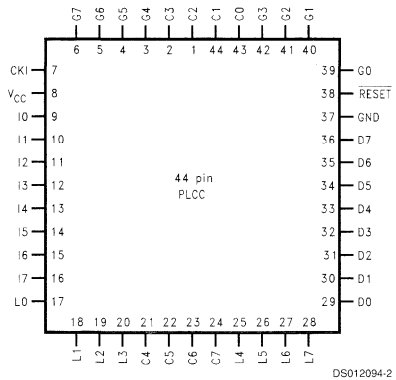


FIGURE 1. Block Diagram

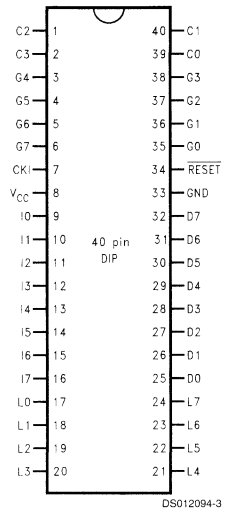
Connection Diagrams

Plastic Chip Carrier



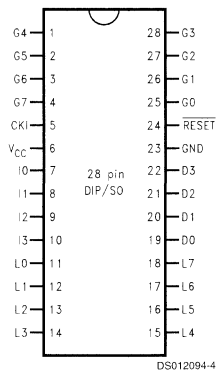
Top View
Order Number COP688EK-XXX/V, COP888EK-XXX/V, COP988EK-XXX/V or COP988EKH-XXX/V
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View
Order Number COP688EK-XXX/N, COP888EK-XXX/N, COP988EK-XXX/N or COP988EKH-XXX/N
See NS Molded Package Number N40A

Dual-In-Line Package



Top View
Order Number COP684EK-XXX/N, COP884EK-XXX/N, COP984EK-XXX/N or COP984EKH-XXX/N
See NS Molded Package Number N28B
Order Number COP684EK-XXX/WM, COP884EK-XXX/WM, COP984EK-XXX/WM or COP984EKH-XXX/WM
See NS Molded Package Number M28B

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU		12	18	18
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU	T3A	17	23	27
L7	I/O	MIWU	T3B	18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I	COMPIN1+		7	9	9
I1	I	COMPIN−/Current Source Out		8	10	10
I2	I	COMPIN0+		9	11	11
I3	I	COMPOUT/COMPIN2+		10	12	12
I4	I	COMPIN3+			13	13
I5	I	COMPIN4+			14	14
I6	I	COMPIN5+			15	15
I7	I	COMPOUT			16	16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

National Semiconductor

PRELIMINARY

COP888GW
8-Bit Microcontroller with Pulse Train Generators and Capture Modules

General Description

The COP888 family of microcontrollers uses an 8-bit single chip core architecture fabricated with National Semiconductor's M²CMOS™ process technology. The COP888GW is a member of this expandable 8-bit core processor family of microcontrollers. It is a fully static part, fabricated using double-metal silicon gate microCMOS technology.

Features include an 8-bit memory mapped architecture, MICROWIRE/PLUS™ serial I/O, two 16-bit timer/counters supporting three modes (Processor Independent PWM generation, External Event counter and Input Capture mode capabilities), four independent 16-bit pulse train generators with 16-bit prescalers, two independent 16-bit input capture modules with 8-bit prescalers, multiply and divide functions, full duplex UART, and two power savings modes (HALT and IDLE), both with a multi-sourced wake up/interrupt capability. This multi-sourced interrupt capability may also be used independent of the HALT or IDLE modes.

Each I/O pin has software selectable configurations. The devices operate over a voltage range of 2.5V–6V. High throughput is achieved with an efficient, regular instruction set operating at a maximum of 1 µs per instruction rate. The device has low EMI emissions. Low radiated emissions are achieved by gradual turn-on output drivers and internal I_{CC} filters on the chip logic and crystal oscillator. The device is available in 68-pin PLCC package.

Key Features

- Two 16-bit input capture modules with 8-bit prescalers
- Four Pulse Train Generators with 16-bit prescalers
- Full duplex UART
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor independent PWM mode
  - — External event counter mode
  - — Input capture mode
- Quiet design (low radiated emissions)
- 16 kbytes on-board ROM
- 512 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake-Up (MIWU) with optional interrupts (8)
- MICROWIRE/PLUS™ serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- Schmitt trigger inputs on port G
- Package: 68-pin PLCC

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Fourteen multi-source vectored interrupts servicing:
  - — External Interrupt with selectable edge
  - — Idle Timer T0
  - — Two Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake-Up
  - — Software Trap
  - — UART (2)
  - — Capture Timers
  - — Counters (one vector for all four counters)
  - — Default VIS (default interrupt)
- Versatile and easy-to-use instruction set
- 8-bit Stack Pointer SP—(stack in RAM)
- Two 8-bit register indirect data memory pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Low current drain (typically <1 µA)
- Single supply operation: 2.5V–5.5V
- Temperature range: −40°C to +85°C

Development Support

- Emulation and OTP device
- Real time emulation and full program debug offered by MetaLink's Development System

Block Diagram

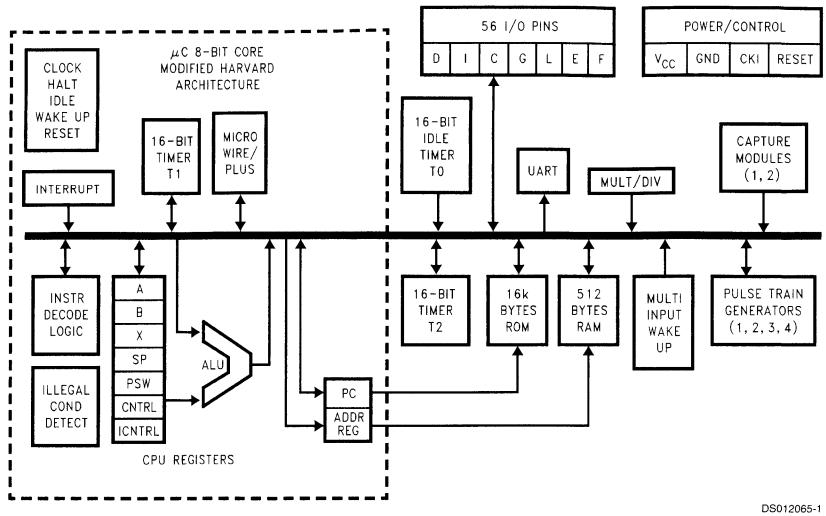
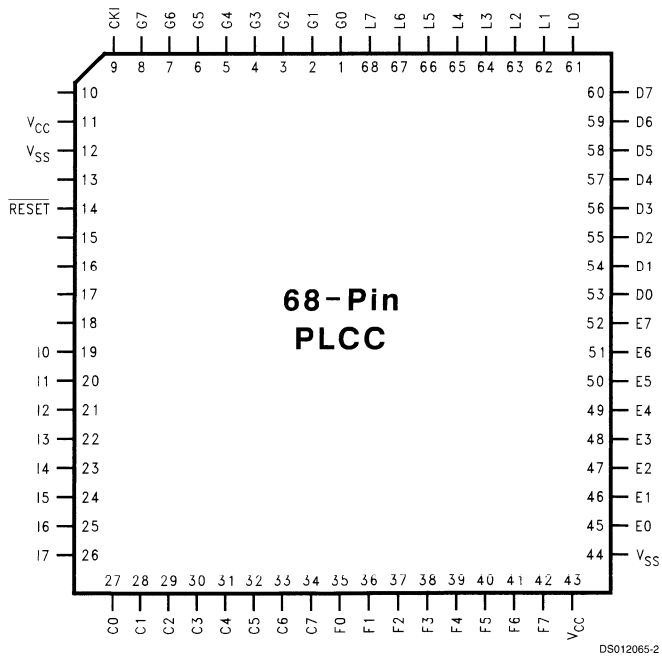


FIGURE 1. COP888GW Block Diagram

Connection Diagram



Top View
Order Number COP888GW-XXX/V
See NS Package Number V68A

National Semiconductor

OTP Products

National Semiconductor

PRELIMINARY

COP87LxxCJ/RJ Family
8-Bit CMOS OTP Microcontrollers with 4k or 32k Memory and Comparator

General Description

The COP87LxxCJ/RJ Family OTP (One Time Programmable) microcontrollers are integrated COP8™ Base core devices with 4k or 32k memory, and an Analog comparator (no brownout). These multi-chip CMOS devices are suited for lower-functionality applications, and as pre-production devices for a ROM design. Low cost, pin and software compatible (plus Brownout) 1k or 2k ROM versions are available (COP820CJ/840CJ Family). Versions are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1µs instruction cycle, three clock options (-1 = crystal; -2 = external; -3 = internal RC), one multi-function 16-bit timer/counter, MICROWIRE/PLUS™ serial I/O, one analog comparator, power saving HALT mode with multi-sourced wakeup/interrupt capability, on-chip R/C oscillator capacitor, high current outputs, software selectable I/O options, WATCHDOG™ timer, modulator/timer, Power on Reset, program code security, 2.7V to 5.5V operation and 20/28 pin packages.

In this datasheet, the term COP87L20CJ refers to the COP87L20CJ, and COP87L22CJ. COP840CJ refers to the COP87L40CJ, COP87L42CJ, COP87L40RJ, and COP87L42RJ.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L20CJ	4k OTP EPROM	64	24	28 DIP/SOIC	-40 to +85˚C
COP87L22CJ	4k OTP EPROM	64	16	20 DIP/SOIC	-40 to +85˚C
COP87L40CJ	4k OTP EPROM	128	24	28 DIP/SOIC	-40 to +85˚C
COP87L42CJ	4k OTP EPROM	128	16	20 DIP/SOIC	-40 to +85˚C
COP87L40RJ	32k OTP EPROM	128	24	28 DIP/SOIC	-40 to +85˚C
COP87L42RJ	32k OTP EPROM	128	16	20 DIP/SOIC	-40 to +85˚C

Key Features

- Multi-Input Wakeup (on the 8-bit Port L)
- Analog comparator
- Modulator/Timer (high speed PWM timer for IR transmission)
- 16-bit multi-function timer supporting
  - — PWM mode
  - — External event counter mode
  - — Input capture mode
- Integrated capacitor for the R/C oscillator
- 4 or 32 kbyte on-board OTP EPROM with security feature
- 64 or 128 bytes on-chip RAM

I/O Features

- Software selectable I/O options (TRI-STATE®, Push-Pull, Weak Pull-Up Input, High Impedance Input)
- High current outputs (8 pins)
- Schmitt trigger inputs on Port G
- MICROWIRE/PLUS serial I/O
- Packages:
  - — 20 DIP/SO with 16 I/O pins
  - — 28 DIP/SO with 24 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Three multi-source interrupts servicing
  - — External interrupt with selectable edge
  - — Timer interrupt
  - — Software interrupt
- Versatile and easy to use instruction set
- 8-bit stack pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Low current drain (typically <1 µA)
- Single supply operation: 2.7V to 5.5V
- Temperature range: −40˚C to +85˚C

Development Support

- Emulation device for the COP820CJ/COP840CJ
- Real time emulation and full program debug offered by MetaLink Development Systems

Block Diagram

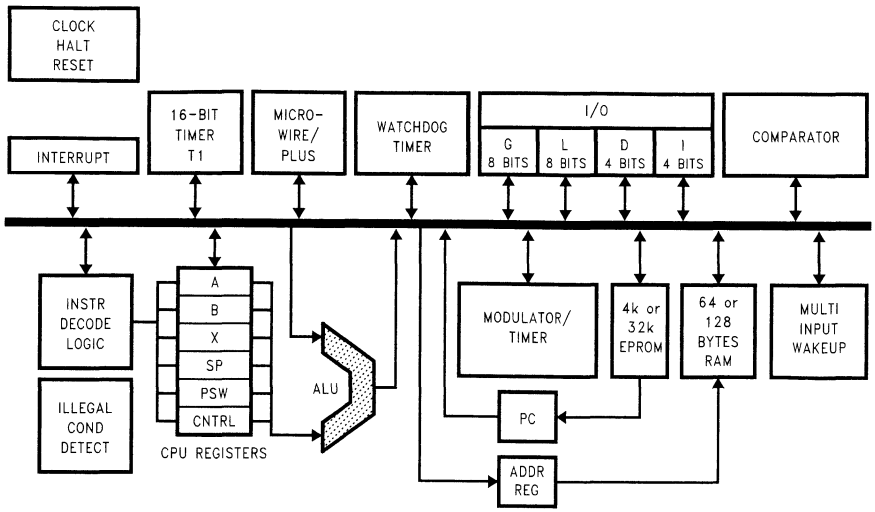
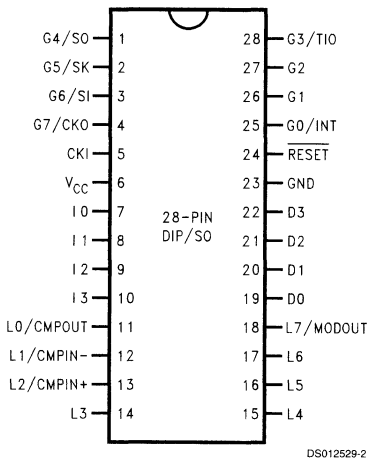
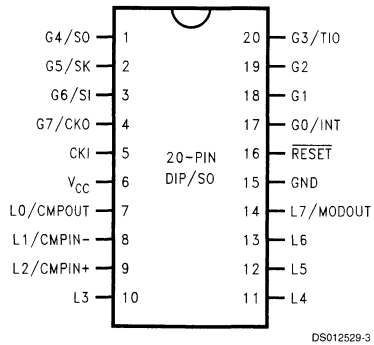


FIGURE 1. Block Diagram

Connection Diagrams



Top View
Order Number
COP87L20CJN (-1N, -2N, -3N), or
COP87L20CJM(-1N, -2N, -3N), or
COP87L40CJN (-1N, -2N, -3N), or
COP87L40CJM (-1N, -2N, -3N), or
COP87L40RJN (-1N, -2N, -3N), or
COP87L40RJM (-1N, -2N, -3N)
See NS Package Number N28B or M28B



Top View
Order Number
COP87L22CJN (-1N, -2N, -3N), or
COP87L22CJM(-1N, -2N, -3N), or
COP87L42CJN (-1N, -2N, -3N), or
COP87L42CJM (-1N, -2N, -3N), or
COP87L42RJN (-1N, -2N, -3N), or
COP87L42RJM (-1N, -2N, -3N)
See NS Package Number N20A or M20B

FIGURE 2. Connection Diagrams

Note: -1 Crystal Oscillator N - Brown out disabled
-2 External Oscillator
-3 R/C Oscillator

Pin Assignment

Port Pin	Typ	ALT Funct.	20 Pin	28 Pin
L0	I/O	MIWU/CMPOUT	7	11
L1	I/O	MIWU/CMPIN–	8	12
L2	I/O	MIWU/CMPIN+	9	13
L3	I/O	MIWU	10	14
L4	I/O	MIWU	11	15
L5	I/O	MIWU	12	16
L6	I/O	MIWU	13	17
L7	I/O	MIWU/MODOUT	14	18
G0	I/O	INTR	17	25
G1	I/O		18	26
G2	I/O		19	27
G3	I/O	TIO	20	28
G4	I/O	SO	1	1
G5	I/O	SK	2	2
G6	I	SI	3	3
G7	I	CKO	4	4
I0	I			7
I1	I			8
I2	I			9
I3	I			10
D0	O			19
D1	O			20
D2	O			21
D3	O			22
V_{CC}			6	6
GND			15	23
CKI			5	5
$\overline{\text{RESET}}$			16	24

National Semiconductor

COP8SA Family
8-Bit CMOS ROM Based and One-Time Programmable (OTP) Microcontroller with 1k to 4k Memory, Power On Reset, and Very Small Packaging

General Description

Note: COP8SAx devices are instruction set and pin compatible supersets of the COP800 Family devices, and are replacements for these in new designs when possible.

The COPSAx Rom based and OTP microcontrollers are highly integrated COP8™ feature core devices, with 1k to 4k memory and advanced features including low EMI. These single-chip CMOS devices are suited for low cost applications requiring a full featured controller, low EMI, and POR. 100% form-fit-function compatible OTP versions are available with 1k, 2k, and 4k memory, and in a variety of packages including 28-pin CSP. Erasable windowed versions are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI with 1 µs instruction cycle, one multi-function 16-bit timer/counter with PWM output, MICROWIRE/PLUS™ serial I/O, two power saving HALT/IDLE modes, MIWU, idle timer, on-chip R/C oscillator, 12 high current outputs, user selectable options (WATCHDOG™, 4 clock/oscillator modes, power-on-reset), low EMI 2.7V to 5.5V operation, and 16/20/28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP8SAA5	1k ROM	64	12/16/24	16/20/28 DIP/SOIC, 28 CSP	0 to +70˚C, -40 to +85˚C, -40 to +125˚C
COP8SAB5	2k ROM	128	16/24	20/28 DIP/SOIC, 28 CSP	0 to +70˚C, -40 to +85˚C, -40 to +125˚C
COP8SAC5	4k ROM	128	16/24/36/40	20/28 DIP/SOIC, 28 CSP, 40 DIP, 44 PLCC/QFP	0 to +70˚C, -40 to +85˚C, -40 to +125˚C
COP8SAA7	1k OTP EPROM	64	12/16/24	16/20/28 DIP/SOIC, 28 CSP	0 to +70˚C, -40 to +85˚C, -40 to +125˚C
COP8SAB7	2k OTP EPROM	128	16/24	20/28 DIP/SOIC, 28 CSP	0 to +70˚C, -40 to +85˚C, -40 to +125˚C
COP8SAC7	4k OTP EPROM	128	16/24	20/28 DIP/SOIC, 28 CSP, 40 DIP, 44 PLCC/QFP	0 to +70˚C, -40 to +85˚C, -40 to +125˚C
COP8SAC7-Q3	4k EPROM	128	16/24/36	20/28/40 DIP	Room Temp. Only
COP8SAC7-J3	4k EPROM	128	40	44 PLCC	Room Temp. Only

Key Features

- Low cost 8-bit OTP microcontroller
- OTP program space with read/write protection (fully secured)
- Quiet Design (low radiated emissions)
- Multi-Input Wakeup pins with optional interrupts (4 to 8 pins)
- 8 bytes of user storage space in EPROM
- User selectable clock options
  - — Crystal/Resonator options
  - — Crystal/Resonator option with on-chip bias resistor
  - — External oscillator
  - — Internal R/C oscillator
- Internal Power-On Reset—user selectable
- WATCHDOG and Clock Monitor Logic—user selectable
- Up to 12 high current outputs

CPU Features

- Versatile easy to use instruction set
- 1 µs instruction cycle time
- Eight multi-source vectored interrupts servicing
  - — External interrupt
  - — Idle Timer T0
  - — One Timer (with 2 interrupts)
  - — MICROWIRE/PLUS Serial Interface
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- Memory mapped I/O
- BCD arithmetic instructions

Peripheral Features

- Multi-Input Wakeup Logic
- One 16-bit timer with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Idle Timer
- MICROWIRE/PLUS Serial Interface (SPI Compatible)

I/O Features

- Software selectable I/O options
  - — TRI-STATE® Output
  - — Push-Pull Output
  - — Weak Pull Up Input
  - — High Impedance Input
- Schmitt trigger inputs on ports G and L
- Up to 12 high current outputs
- Pin efficient (i.e., 40 pins in 44-pin package are devoted to useful I/O)

Fully Static CMOS Design

- Low current drain (typically < 4 µA)
- Single supply operation: 2.7V to 5.5V
- Two power saving modes: HALT and IDLE

Temperature Ranges

0°C to +70°C, −40°C to +85°C, and −40°C to +125°C

Development Support

- Windowed packages for DIP and PLCC
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

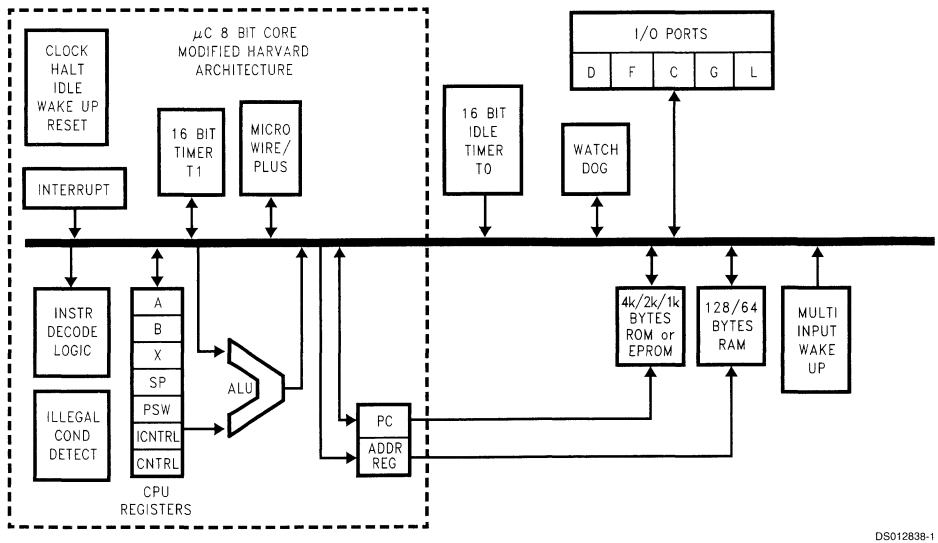


FIGURE 1. COP8SAx Block Diagram

General Description (Continued)

Key features include an 8-bit memory mapped architecture, a 16-bit timer/counter with two associated 16-bit registers supporting three modes (Processor Independent PWM generation, External Event counter, and Input Capture capabilities), two power saving HALT/IDLE modes with a multi-sourced wakeup/interrupt capability, on-chip R/C oscillator, high current outputs, user selectable options such as WATCHDOG, Oscillator configuration, and power-on-reset.

1.1 EMI REDUCTION

The COP8SAx family of devices incorporates circuitry that guards against electromagnetic interference—an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal I_{CC} smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 ARCHITECTURE

The COP8SAx family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently data tables usually need to be contained in ROM or EPROM, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8SAx family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.3 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why COP8 family offers a unique and code-efficient instruction set—one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM/OTP). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.3.1 Key Instruction Set Features

The COP8SAx family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.3.2 Many Single-Byte, Multifunction Instructions

The COP8SAx instruction set utilizes many single-byte, multifunction instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, and LOAD/EXCHANGE instructions with post-incrementing and post-decrementing, to name just a few examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction; decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (analogous to "FOR NEXT" in higher level languages).

1.3.3 Bit-Level Control

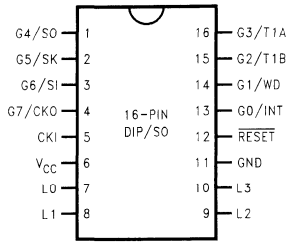
Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers. Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-maped registers allow designers to optimize the precise implementation of certain specific instructions.

1.4 PACKAGING/PIN EFFICIENCY

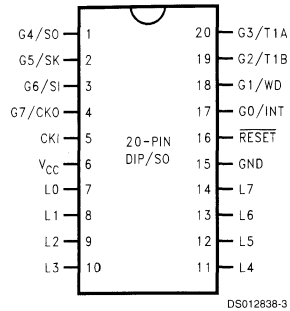
Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increases device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and do not waste pins: up to 90.9% (or 40 pins in the 44-pin package) are devoted to useful I/O.

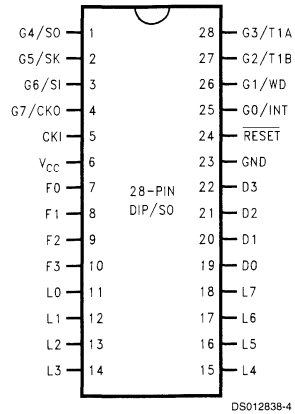
Connection Diagrams



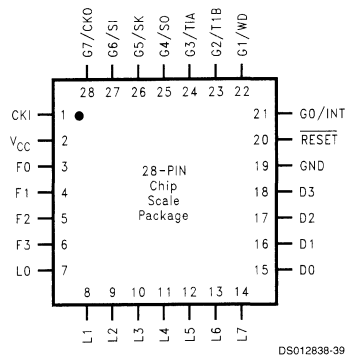
Top View



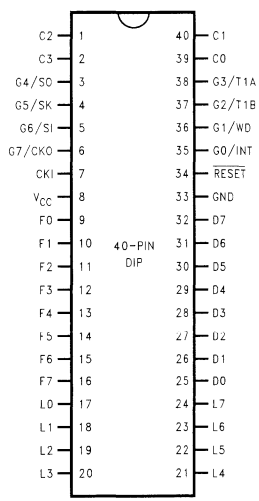
Top View



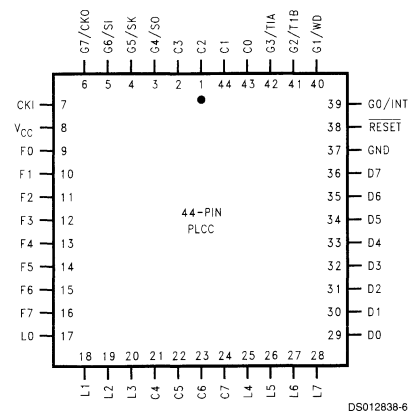
Top View



Top View



Top View



Top View

FIGURE 2. Connection Diagrams

Ordering Information

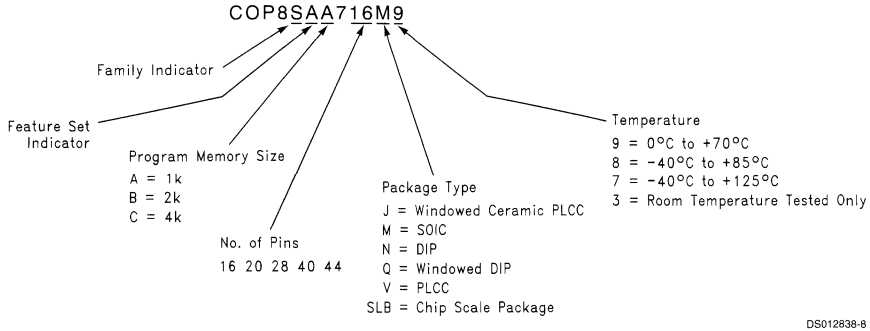


FIGURE 3. Part Numbering Scheme

	1k EPROM		2k EPROM		4k EPROM		4k EPROM	
Temperature	Order Number	Package	Order Number	Package	Order Number	Package	Windowed Device Order Number	Package
0°C to +70°C	COP8SAA716M9	16M						
	COP8SAA720M9	20M	COP8SAB720M9	20M	COP8SAC720M9	20M		
	COP8SAA728M9	28M	COP8SAB728M9	28M	COP8SAC728M9	28M		
	COP8SAA716N9	16N						
	COP8SAA720N9	20N	COP8SAB720N9	20N	COP8SAC720N9	20N	COP8SAC720Q3	20Q
	COP8SAA728N9	28N	COP8SAB728N9	28N	COP8SAC728N9	28N	COP8SAC728Q3	28Q
					COP8SAC740N9	40N	COP8SAC740Q3	40Q
					COP8SAC744V9	44V	COP8SAC744J3	44J
−40°C to +85°C	COP8SAA716M8	16M						
	COP8SAA720M8	20M	COP8SAB720M8	20M	COP8SAC720M8	20M		
	COP8SAA728M8	28M	COP8SAB728M8	28M	COP8SAC728M8	28M		
	COP8SAA716N8	16N						
	COP8SAA720N8	20N	COP8SAB720N8	20N	COP8SAC720N8	20N		
	COP8SAA728N8	28N	COP8SAB728N8	28N	COP8SAC728N8	28N		
					COP8SAC740N8	40N		
					COP8SAC744V8	44V		
	COP8SAA7SLB8	SLB	COP8SAB7SLB8	SLB	COP8SAC7SLB8	SLB		
−40°C to +125°C					COP8SAC720M7	20M		
					COP8SAC728M7	28M		
					COP8SAC720N7	20N		
					COP8SAC728N7	28N		
					COP8SAC740N7	40N		
					COP8SAC744V7	44V		

National Semiconductor

COP87L88CL
8-Bit One-Time Programmable (OTP) Microcontroller

General Description

COP8SG devices are form-fit-function compatible supersets of the COP87L88CL Family devices, and are replacements for these in new designs, and design upgrades with minimum effort.

The COP87L88CL OTP microcontrollers are larger memory (16k), highly integrated COP8™ Feature core devices, with advanced features. These multi-chip CMOS devices are suited for applications requiring a full featured controller with a high I/O pincount, and as pre-production devices for a masked ROM design. Lower cost pin and software compatible 4k ROM versions are available (COP888CL/988CL).

Family features include an 8-bit memory mapped architecture, 10MHz CKI with 1 µs instruction cycle, two multi-function 16-bit timer/counters, MICROWIRE/PLUS™ serial I/O, two power saving HALT/IDLE modes, idle timer, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, 2.7v-5.5v operation, program code security, and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature	Comments
COP87L84CL	16k OTP	128	24	28 DIP/SOIC	-40 to +85°C	Use COP8SGx7
COP87L88CL	16k OTP	128	36/40	40 DIP, 44 PLCC	-40 to +85°C	Use COP8SGx7

Key Features

- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor independent PWM mode
  - — External event counter mode
  - — Input capture mode
- 4 kbytes on-board EEPROM with security feature
- 128 bytes on-board RAM

Additional Peripheral Features

- Idle timer
- Multi-Input Wake-Up (MIWU) with optional interrupts (8)
- WATCHDOG™ and clock monitor logic
- MICROWIRE/PLUS™ serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® output, push-pull output, weak pull-up input, high impedance input)
- Schmitt trigger inputs on ports G and L
- Packages:
  - — 44 PLCC with 39 I/O pins
  - — 40 DIP with 33 I/O pins
  - — 28 DIP with 24 I/O pins
  - — 28 SO with 24 I/O pins (contact local sales office for availability)

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Ten multi-source vectored interrupts servicing
  - — External interrupt
  - — Idle timer T0
  - — Two timers (each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer SP—stack in RAM
- Two 8-bit register indirect data memory pointers (B and X)

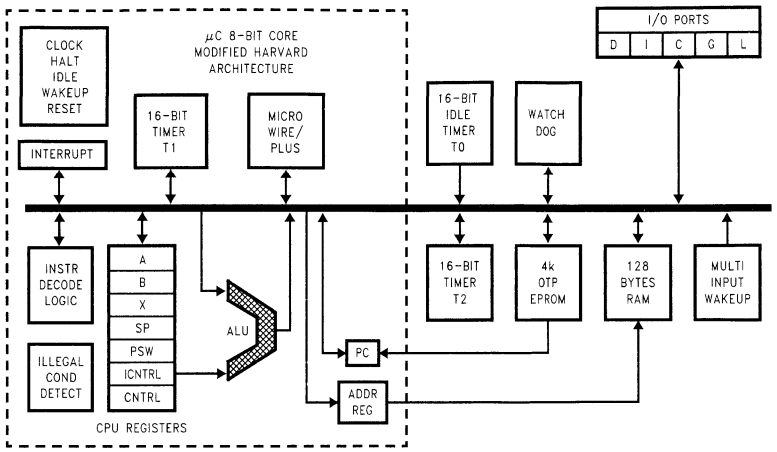
Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.7V–5.5V
- Temperature range: –40°C to +85°C

Development Support

- Emulation device for the COP888CL/COP884CL
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram



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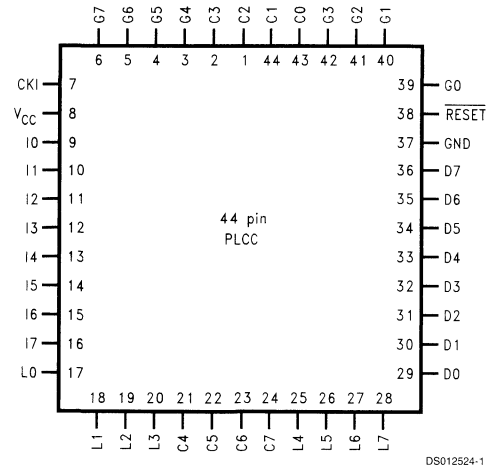
Connection Diagrams

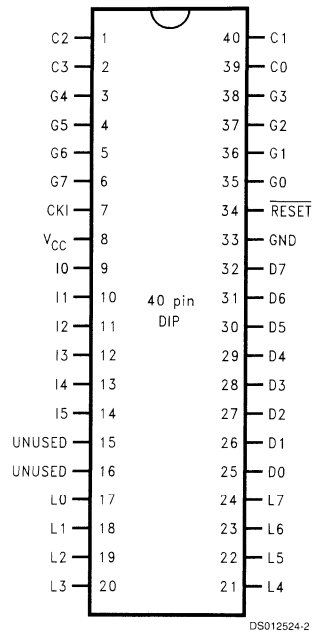
Plastic Chip Carrier



Note: -X Crystal Oscillator
Note: -E Halt Enable

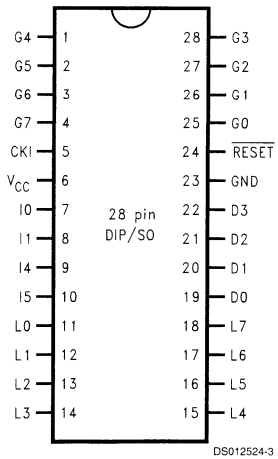
Top View
Order Number COP87L88CLV-XE
See NS Package Number V44A

Dual-In-Line Package



Top View
Order Number COP87L84CLN-XE
See NS Package Number N40A

Dual-In-Line Package



Top View
Order Number COP87L84CLN-XE
or COP87L84CLM-XE
See NS Package Number M28B or N28B

FIGURE 1. COP87L88CL/COP87L84CL Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pkg.	40-Pin Pkg.	44-Pin Pkg.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU		12	18	18
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	Halt Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I			7	9	9
I1	I			8	10	10
I2	I				11	11
I3	I				12	12
I4	I			9	13	13
I5	I			10	14	14
I6	I					15
I7	I					16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
Unused*					16	
Unused					15	
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

* = On the 40-pin package, Pins 15 and 16 must be connected to GND.

National Semiconductor

COP8SG Family
8-Bit CMOS ROM Based and OTP Microcontrollers with 8k to 32k Memory, Two Comparators and USART

General Description

The COP8SG Family ROM and OTP based microcontrollers are highly integrated COP8™ Feature core devices with 8k to 32k memory and advanced features including Analog comparators, and zero external components. These single-chip CMOS devices are suited for more complex applications requiring a full featured controller with larger memory, low EMI, two comparators, and a full-duplex USART. COP8SGx7 devices are 100% form-fit-function compatible OTP (One Time Programmable) versions for use in production or development of the COP8SGx5 ROM.

Erasable windowed versions (Q3) are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 15 MHz CKI with 0.67 µs instruction cycle, 14 interrupts, three multi-function 16-bit timer/counters with PWM, full duplex USART, MICROWIRE/PLUS™, two analog comparators, two power saving HALT/IDLE modes, MIWU, idle timer, on-chip R/C oscillator, high current outputs, user selectable options (WATCHDOG™, 4 clock/oscillator modes, power-on-reset), 2.7V to 5.5V operation, program code security, and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP8SGE5	8k ROM	256	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGG5	16k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGH5	20k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGK5	24k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGR5	32k ROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGE7	8k OTP EPROM	256	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGR7	32k OTP EPROM	512	24/36/40	28 DIP/SOIC, 40 DIP, 44 PLCC/QFP/CSP	-40 to +85˚C, -40 to +125˚C
COP8SGR7-Q3	32k EPROM	512	24/36/40	28 DIP, 40 DIP, 44 PLCC	Room Temp.

Key Features

- Low cost 8-bit microcontroller
- Quiet Design (low radiated emissions)
- Multi-Input Wakeup pins with optional interrupts (8 pins)
- Mask selectable clock options
  - — Crystal oscillator
  - — Crystal oscillator option with on-chip bias resistor
  - — External oscillator
  - — Internal R/C oscillator
- Internal Power-On-Reset—user selectable
- WATCHDOG and Clock Monitor Logic—user selectable
- Eight high current outputs
- 256 or 512 bytes on-board RAM
- 8k to 32k ROM or OTP EPROM with security feature

CPU Features

- Versatile easy to use instruction set
- 0.67 µs instruction cycle time
- Fourteen multi-source vectored interrupts servicing
  - — External interrupt / Timers T0 — T3
  - — MICROWIRE/PLUS Serial Interface
  - — Multi-Input Wake Up
  - — Software Trap
  - — USART (2; 1 receive and 1 transmit)
  - — Default VIS (default interrupt)
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- BCD arithmetic instructions

Peripheral Features

- Multi-Input Wakeup Logic
- Three 16-bit timers (T1 — T3), each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event Counter mode
  - — Input Capture mode
- Idle Timer (T0)

Peripheral Features (Continued)

- MICROWIRE/PLUS Serial Interface (SPI Compatible)
- Full Duplex USART
- Two Analog Comparators

I/O Features

- Software selectable I/O options (TRI-STATE® Output,Push-Pull Output, Weak Pull-Up Input, and High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Eight high current outputs
- Packages: 28 SO with 24 I/O pins, 40 DIP with 36 I/O pins, 44 PLCC, PQFP and CSP with 40 I/O pins

Fully Static CMOS Design

- Low current drain (typically < 4 µA)
- Two power saving modes: HALT and IDLE

Temperature Range

- −40˚C to +85˚C, −40˚C to +125˚C

Development Support

- Windowed packages for DIP and PLCC
- Real time emulation and debug tools available

Block Diagram

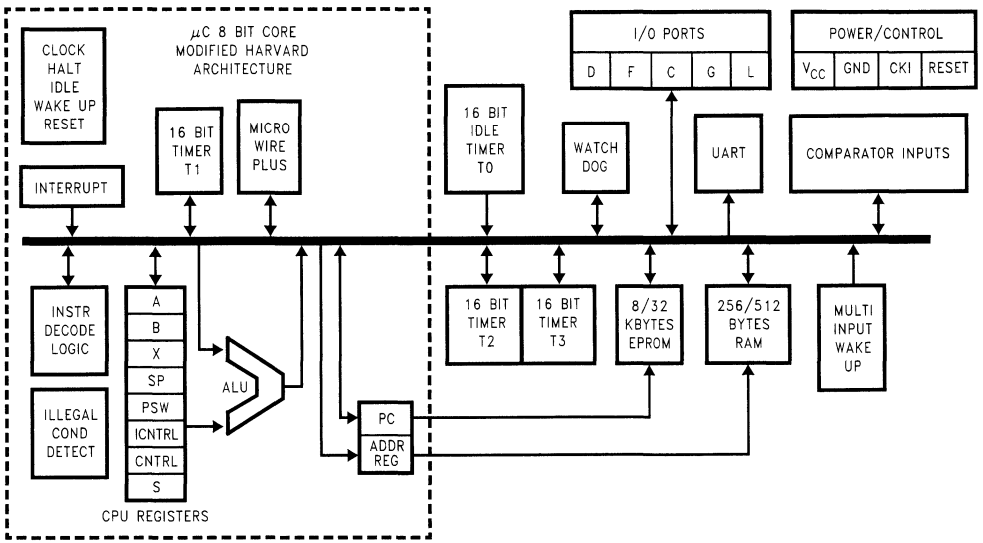


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FIGURE 1. COP8SGx Block Diagram

1.0 Device Description

1.1 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.2 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why COP8 family offers a unique and code-efficient instruction set—one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space. Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.2.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.2.2 Many Single-Byte, Multifunction Instructions

The COP8 instruction set utilizes many single-byte, multifunction instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction; decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (analogous to "FOR NEXT" in higher level languages).

1.2.3 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.2.4 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-maped registers allow designers to optimize the precise implementation of certain specific instructions.

1.3 EMI REDUCTION

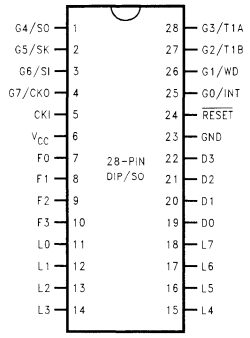
The COP8SGx5 family of devices incorporates circuitry that guards against electromagnetic interference—an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal I_{CC} smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.4 PACKAGING/PIN EFFICIENCY

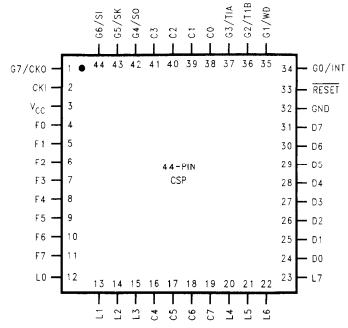
Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increases device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and do not waste pins: up to 90.9% (or 40 pins in the 44-pin package) are devoted to useful I/O.

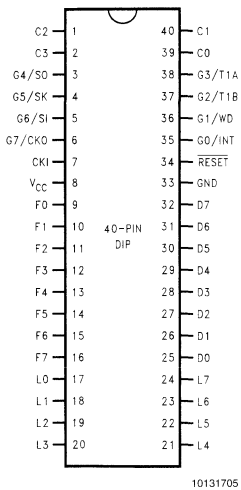
Connection Diagrams



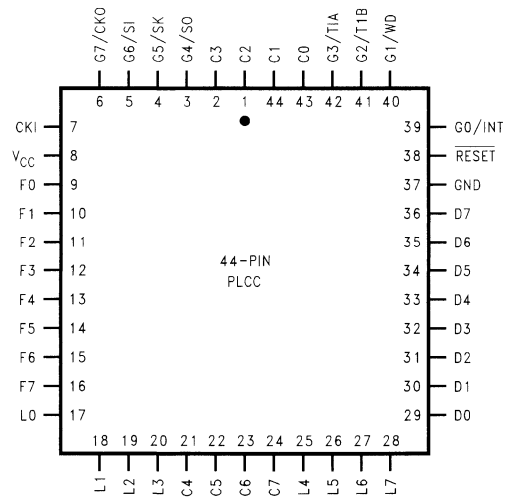
Top View
Order Number COP8SGXY28M8
See NS Package Number M28B
Order Number COP8SGXY28N8
See NS Package Number N28B
Order Number COP8SGR728Q3
See NS Package Number D28JQ



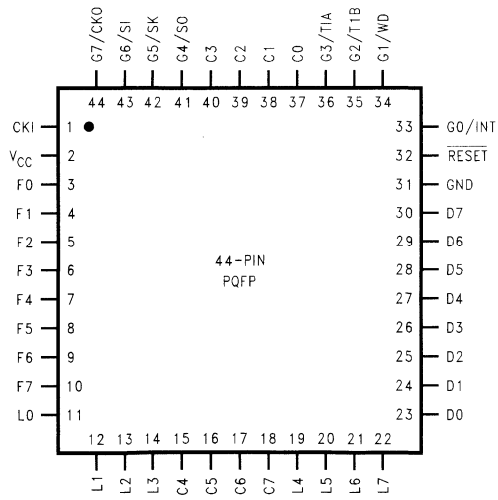
Top View
Order Number COP8SGR7HLQ8
See NS Package Number LQA44A



Top View
Order Number COP8SGXY40N8
See NS Package Number N40A
Order Number COP8SGR5740Q3
See NS Package Number D40KQ



Top View
Order Number COP8SGXY44V8
See NS Package Number V44A
Order Number COP8SGR744J3
See NS Package Number EL44C



Top View
Order Number COP8SGXYVEJ8
See NS Package Number VEJ44A

Note 1: X = E for 8k, G for 16k,
H for 20k, K for 24k, R for 32k
Y = 5 for ROM, 7 for OTP

Pinouts for 28 -, 40- and 44-Pin Packages

Port	Type	Alt. Fun	28-Pin SO	40-Pin DIP	44-Pin PLCC	44-Pin PQFP	44-Pin CSP
L0	I/O	MIWU	11	17	17	11	12
L1	I/O	MIWU or CKX	12	18	18	12	13
L2	I/O	MIWU or TDX	13	19	19	13	14
L3	I/O	MIWU or RDX	14	20	20	14	15
L4	I/O	MIWU or T2A	15	21	25	19	20
L5	I/O	MIWU or T2B	16	22	26	20	21
L6	I/O	MIWU or T3A	17	23	27	21	22
L7	I/O	MIWU or T3B	18	24	28	22	23
G0	I/O	INT	25	35	39	33	34
G1	I/O	WDOUT*	26	36	40	34	35
G2	I/O	T1B	27	37	41	35	36
G3	I/O	T1A	28	38	42	36	37
G4	I/O	SO	1	3	3	41	42
G5	I/O	SK	2	4	4	42	43
G6	I	SI	3	5	5	43	44
G7	I	CKO	4	6	6	44	1
D0	O		19	25	29	23	24
D1	O		20	26	30	24	25
D2	O		21	27	31	25	26
D3	O		22	28	32	26	27
D4	O			29	33	27	28
D5	O			30	34	28	29
D6	O			31	35	29	30
D7	O			32	36	30	31
F0	I/O		7	9	9	3	4
F1	I/O	COMP1IN−	8	10	10	4	5
F2	I/O	COMP1IN+	9	11	11	5	6
F3	I/O	COMP1OUT	10	12	12	6	7
F4	I/O	COMP2IN−		13	13	7	8
F5	I/O	COMP2IN+		14	14	8	9
F6	I/O	COMP2OUT		15	15	9	10
F7	I/O			16	16	10	11
C0	I/O			39	43	37	38
C1	I/O			40	44	38	39
C2	I/O			1	1	39	40
C3	I/O			2	2	40	41
C4	I/O				21	15	16
C5	I/O				22	16	17
C6	I/O				23	17	18
C7	I/O				24	18	19
V_{CC}			6	8	8	2	3
GND			23	33	37	31	32
CKI	I		5	7	7	1	2
$\overline{\text{RESET}}$	I		24	34	38	32	33

* G1 operation as WDOUT is controlled by ECON bit 2.

2.1 Ordering Information

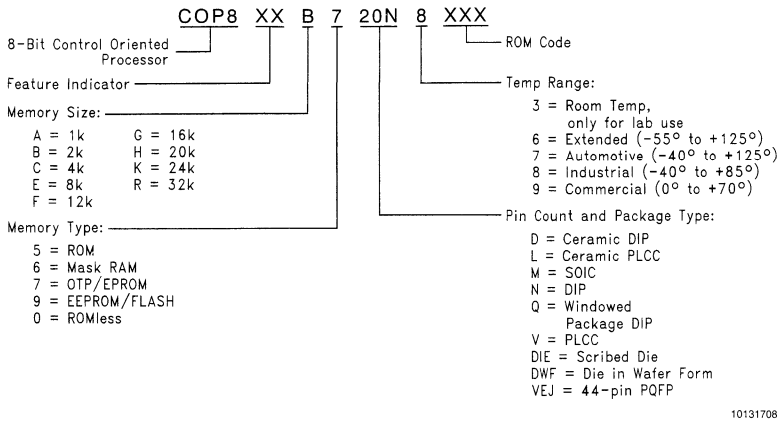


FIGURE 2. Part Numbering Scheme

National Semiconductor

COP87L88FH
8-Bit CMOS OTP Microcontrollers with 16k Memory, Comparators, USART and Hardware Multiply/Divide

General Description

The COP87L88FH OTP (One Time Programmable) microcontrollers are highly integrated COP8™ Feature core devices with 16k memory and advanced features including Analog comparators, and Hardware Multiply/Divide. These multi-chip CMOS devices are suited for applications requiring a full featured controller with comparators, a full-duplex USART, and hardware multiply/divide functions, and as pre-production devices for a masked ROM design. Lower cost pin and software compatible 12k ROM versions are available (COP888FH), as well as a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI (-XE = crystal oscillator; -TE = external clock) with 1µs instruction cycle, hardware multiply/divide functions, three multi-function 16-bit timer/counters with PWM, full duplex USART, MICROWIRE/PLUS™, two Analog comparators, two power saving HALT/IDLE modes, MIWU, idle timer, WATCHDOG™ and clock monitor logic, low EMI 2.7V to 5.5V operation, and 28/40/44 pin packages.

Devices included in this data sheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L84FH	16k OTP EPROM	512	24	28 DIP/SOIC	-40 to +85˚C
COP87L88FH	16k OTP EPROM	512	36/40	40 DIP, 44 PLCC	-40 to +85˚C

Key Features

- Hardware Multiply/Divide Functions
- Full duplex USART
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 16 kbytes on-board EPROM with security features
- 512 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- Two analog comparators
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE®, Push-Pull, Weak Pull-Up, and High Impedance)
- Schmitt trigger inputs on ports G and L
- Packages:
  - — 40 DIP with 36 I/O pins
  - — 44 PLCC with 40 I/O pins
  - — 28 DIP/SO with 24 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Fourteen multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Three Timers (Each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — USART (2)
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.7V–5.5V
- Temperature ranges: –40˚C to +85˚C

Development Support

- Emulation device for COP888FH
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

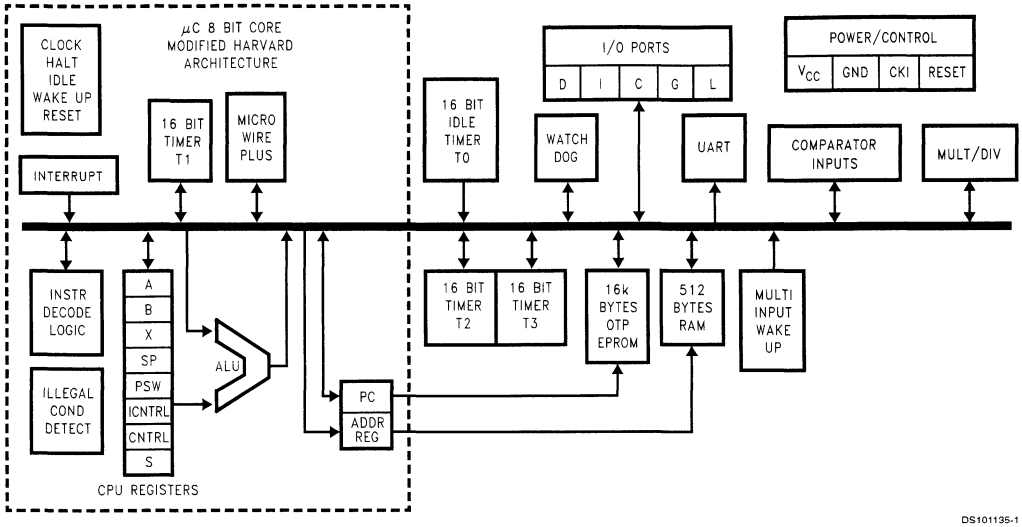
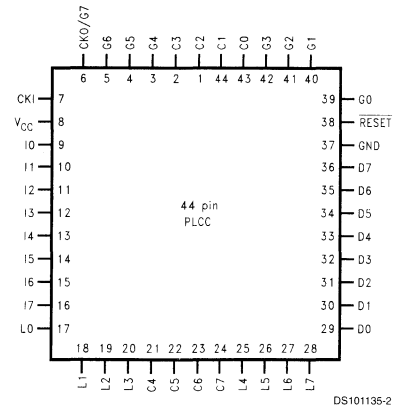


FIGURE 1. COP87L88FH Block Diagram

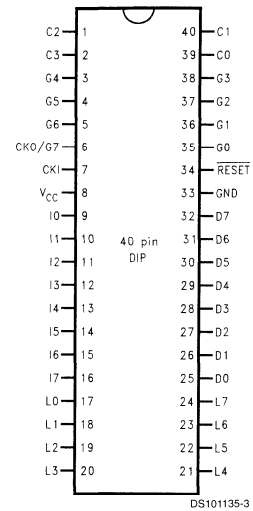
Connection Diagrams

Plastic Chip Carrier



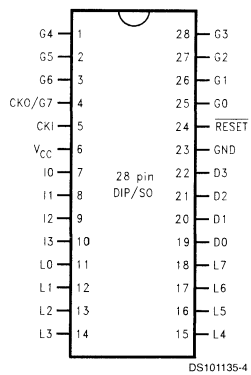
Top View
Order Number COP87L88FHV-XE/TE
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View Order
Number COP87L88FHN-XE/TE
See NS Molded Package Number N40A

Dual-In-Line Package



Order Number COP87L84FHM-XE/TE, or COP87L84FHN-XE/TE
See NS Molded Package Number M28B or N28B

Note: -X Crystal Oscillator
-T External Clock
-E Halt Mode Enable

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU	CKX	12	18	18
L2	I/O	MIWU	TDX	13	19	19
L3	I/O	MIWU	RDX	14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU	T3A	17	23	27
L7	I/O	MIWU	T3B	18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
I0	I			7	9	9
I1	I	COMP1IN−		8	10	10
I2	I	COMP1IN+		9	11	11
I3	I	COMP1OUT		10	12	12
I4	I	COMP2IN−			13	13
I5	I	COMP2IN+			14	14
I6	I	COMP2OUT			15	15
I7	I				16	16
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

National Semiconductor

COP87L84BC
8-Bit CMOS OTP Microcontrollers with 16k Memory, Comparators, and CAN Interface

General Description

The COP87L84BC OTP (One Time Programmable) microcontrollers are highly integrated COP8™ Feature core devices with 16k OTP EPROM memory and advanced features including a CAN 2.0B (passive) interface and two Analog comparators. These multi-chip CMOS devices are suited for applications requiring a full featured controller with a CAN interface, and 8-bit 39 kHz PWM timer, and as pre-production devices for a masked ROM design. Pin and software compatible 2k ROM versions are available (COP884BC) with a range of COP8 software and hardware development tools.

Features include an 8-bit memory mapped architecture, 10 MHz CKI (-XE = crystal oscillator) with 1µs instruction cycle, one multi-function 16-bit timer/counter, 8-bit 39 kHz PWM timer with 2 outputs, CAN 2.0B (passive) interface, MICROWIRE/PLUS™ serial I/O, two Analog comparators, two power saving HALT/IDLE modes, idle timer, MIWU, software selectable I/O options, low EMI 4.5V to 5.5V operation, and 28 pin packages.

Note: The companion devices with CAN interface, more I/O and memory, A/D, and USART are the COP87L88EB/RB.

Device included in this datasheet is:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L84BC	16k OTP EPROM	64	18	28 SOIC	-40 to +85˚C

Key Features

- CAN 2.0B (passive) Interface
- One 16-bit timer, with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- High speed, constant resolution 8-bit PWM/frequency monitor timer with 2 output pins
- 16 kbytes on-board OTP EPROM with security feature
- 64 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake Up (MIWU) with optional interrupts (7)
- Two analog comparators
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Packages: 28 SO with 18 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Eleven multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Timer T1 (with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — PWM Timer
  - — CAN Interface (with 3 interrupts)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 4.5V–5.5V
- Temperature ranges: –40˚C to +85˚C

Development Support

- Emulation device for COP884BC/COP885BC
- Real time emulation and full program debug offered by MetaLink Development Systems

Block Diagram

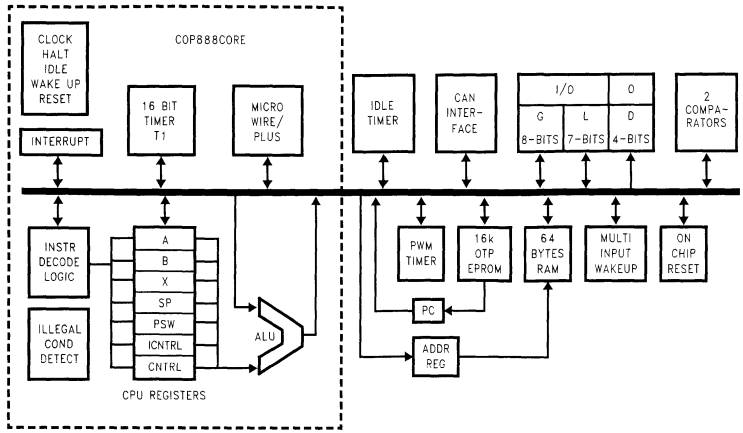
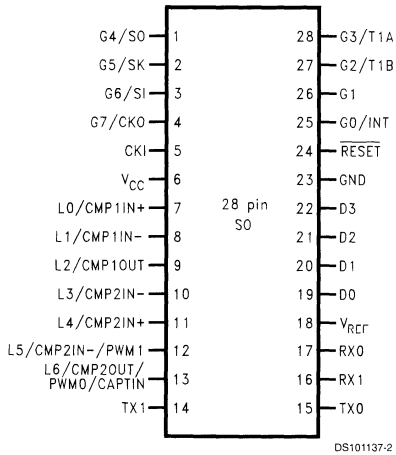


FIGURE 1. Block Diagram

Connection Diagram



Note: X = Crystal Oscillator
E = Halt Mode Enabled

Top View
Order Number COP87L84BCM-XE
See NS Package Number M28B

FIGURE 2. Connection Diagram

Pinouts for 28-Pin SO Package

Port Pin	Type	Alt. Function	28-Pin SO
G0	I/O	INTR	25
G1	I/O		26
G2	I/O	T1B	27
G3	I/O	T1A	28
G4	I/O	SO	1
G5	I/O	SK	2
G6	I	SI	3
G7	I	CKO	4
L0	I/O	CMP1IN+/MIWU	7
L1	I/O	CMP1IN−/MIWU	8
L2	I/O	CMP1OUT/MIWU	9
L3	I/O	CMP2IN−/MIWU	10
L4	I/O	CMP2IN+/MIWU	11
L5	I/O	CMP2IN−/PWM1/MIWU	12
L6	I/O	CMP2OUT/PWM0/ CAPTIN/MIWU	13
D0	O		19
D1	O		20
D2	O		21
D3	O		22
CAN V_{REF}			18
CAN Tx0	O		15
CAN Tx1	O		14
CAN Rx0	I	MIWU	17
CAN Rx1	I	MIWU	16
V_{CC}			6
GND			23
CKI	I		5
$\overline{\text{RESET}}$	I		24

National Semiconductor

COP87L88EB/RB Family
8-Bit CMOS OTP Microcontrollers with 16k or 32k Memory, CAN Interface, 8-Bit A/D, and USART

General Description

The COP87L88EB/RB Family OTP (One Time programmable) microcontrollers are highly integrated COP8™ Feature core devices with 16k or 32k memory and advanced features including a CAN 2.0B (passive) interface, A/D and USART. These multi-chip CMOS devices are suited for applications requiring a full featured controller with a CAN interface, low EMI, and versatile communications interfaces, and as pre-production devices for ROM designs. Pin and software compatible 8k ROM versions (COP888EB) are available as well as a range of COP8 software and hardware development tools.

Features include an 8-bit memory mapped architecture, 10 MHz CKI (-XE = crystal oscillator) with 1μs instruction cycle, two multi-function 16-bit timer/counters, WATCHDOG and clock monitor, idle timer, CAN 2.0B (passive) interface, MICROWIRE/PLUS™ serial I/O, SPI master/slave interface, fully buffered USART, 8 bit A/D with 8 channels, two power saving HALT/IDLE modes, MIWU, software selectable I/O options, low EMI 4.5V to 5.5V operation, program code security, and 44/68 pin packages.

Note: A companion device with CAN interface, less I/O and memory, A/D, and PWM timer is the COP87L84BC.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L88EB	16k OTP EPROM	192	35	44 PLCC	-40 to +85˚C
COP87L89EB	16k OTP EPROM	192	58	68 PLCC	-40 to +85˚C
COP87L88RB	32k OTP EPROM	192	35	44 PLCC	-40 to +85˚C
COP87L89RB	32k OTP EPROM	192	58	68 PLCC	-40 to +85˚C

Key Features

- CAN 2.0B (passive) bus interface, with Software Power save mode
- 8-bit A/D Converter with 8 channels
- Fully buffered USART
- Multi-input wake up (MIWU) on both Port L and M
- SPI Compatible Master/Slave Interface
- 16 or 32 kbytes of on-board OTP EPROM with security feature

  Note: Mask ROMed device with equivalent on-chip features and program memory size of 8k is available.
- 192 bytes of on-board RAM

Additional Peripheral Features

- Idle timer (programmable)
- Two 16-bit timer, with two 16-bit registers supporting
  - — Processor independent PWM mode
  - — External Event counter mode
  - — Input capture mode
- WATCHDOG™ and Clock Monitor
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE® outputs, Push pull outputs, Weak pull up input, High impedance input)
- Schmitt trigger inputs on Port G, L and M
- Packages: 44 PLCC with 35 I/O pins; 68 PLCC with 58 I/O pins

CPU/Instruction Set Features

- 1 μs instruction cycle time
- Fourteen multi-sourced vectored interrupts servicing
  - — External interrupt
  - — Idle Timer T0
  - — Timers (T1 and T2) (4 Interrupts)
  - — MICROWIRE/PLUS and SPI
  - — Multi-input Wake up
  - — Software Trap
  - — CAN interface (3 interrupts)
  - — USART (2 Inputs)
- Versatile easy to use instruction set
- 8-bit stacker pointer (SP) (Stack in RAM)
- Two 8-bit RegisterR Indirect Memory Pointers (B, X)

Fully Static CMOS

- Two power saving modes: HALT, IDLE
- Single supply operation: 4.5V to 5.5V
- Temperature range: –40˚C to +85˚C

Development Support

- Emulation device for COP888EB
- Real time emulation and full program debug offered by MetaLink Development System

Basic Functional Description

- CAN I/F—CAN serial bus interface block as described in the CAN specification part 2.0B (Passive)
  - — Interface rates up to 250k bit/s are supported utilizing standard message identifiers
- Programmable double buffered USART
- A/D—8-bit, 8 channel, 1-LSB Resolution, with improved Source Impedance and improved channel to channel cross talk immunity
- Multi-Input-Wake-Up (MIWU)—edge selectable wake-up and interrupt capability via input port and CAN interface (Port L, Port M and CAN I/F); supports Wake-Up capability on SPI, USART, and T2
- Port C—8-bit bi-directional I/O port
- Port D—8-bit Output port with high current drive capability (10 mA)
- Port F—8-bit bidirectional I/O
- Port G—8-bit bidirectional I/O port, including alternate functions for:
  - — MICROWIRE™ Input and Output
  - — Timer 1 Input or Output (Depending on mode selected)
  - — External Interrupt input
  - — WATCHDOG Output
- Port I—8-bit input port combining either digital input, or up to eight A/D input channels
- Port L—8-bit bidirectional I/O port, including alternate functions for:
  - — USART Transmit/Receive I/O
  - — Multi-input-wake up (MIWU on all pins)
- Port M—8-bit I/O port, with the following alternate function
  - — SPI Interface
  - — MIWU
  - — CAN Interface Wake-up (MSB)
  - — Timer 2 Input or Output (Depending on mode selected)
- Port N—8-bit bidirectional I/O
  - — SPI Slave Select Expander
- Two 16-bit multi-function Timer counters (T1 and T2) plus supporting registers
  - — (I/P Capture, PWM and Event Counting)
- Idle timer—Provides a basic time-base counter, (with interrupt) and automatic wake up from IDLE mode programmable
- MICROWIRE/PLUS—MICROWIRE serial peripheral interface, supporting both Master and Slave operation
- HALT and IDLE—Software programmable low current modes
  - — HALT—Processor stopped, Minimum current
  - — IDLE—Processor semi-active more than 60% power saving
- 16 or 32 kbytes OTP EPROM and 192 bytes of on board static RAM
- SPI Master/Slave interface includes 12 bytes Transmit and 12 bytes Receive FIFO Buffers. Operates up to 1M Bit/S
- On board programmable WATCHDOG and CLOCK Monitor

Applications

- Automobile Body Control and Comfort System
- Integrated Driver Informaiton Systems
- Steering Wheel Control
- Car Radio Control Panel
- Sensor/Actuator Applications in Automotive and Industrial Control

Block Diagram

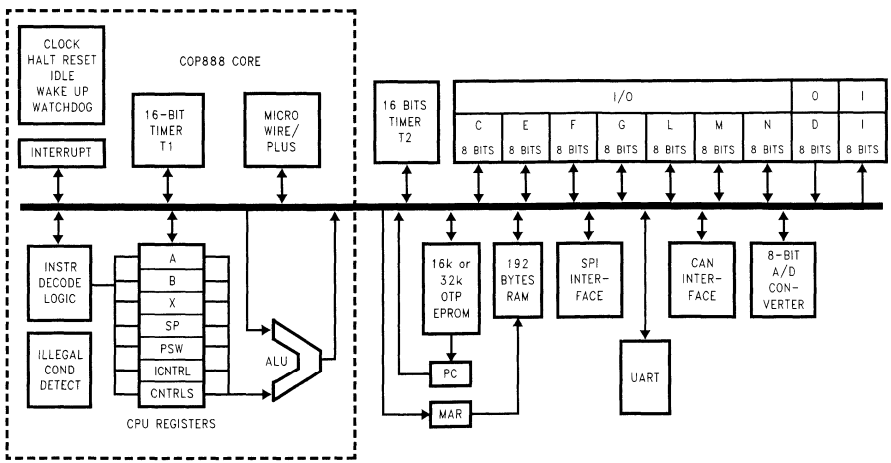
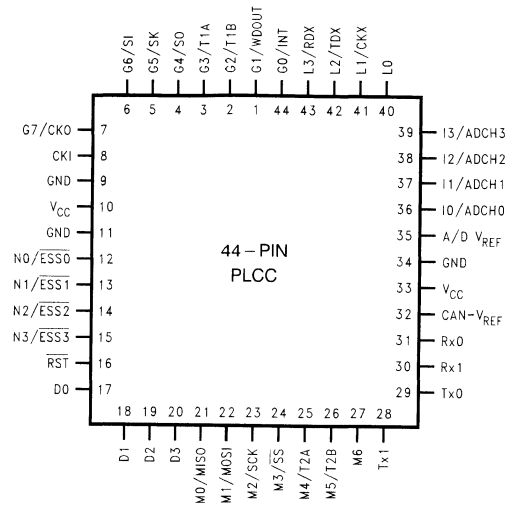


FIGURE 1. Block Diagram

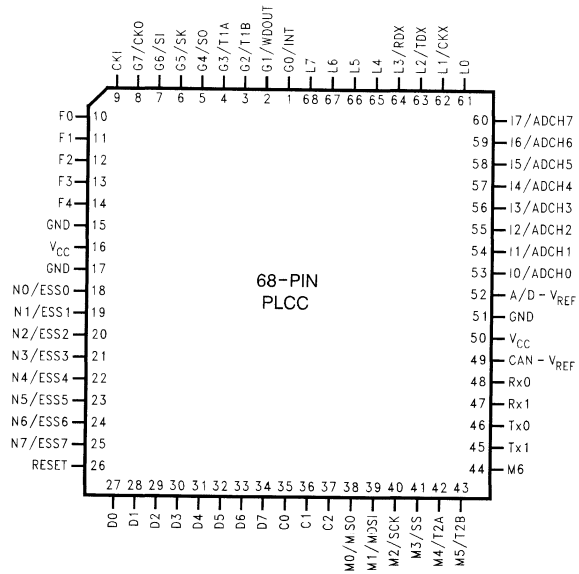
Connection Diagrams

Plastic Chip Carrier



Top View
Order Number COP87L88EBV-XE or COP87L88RBV-XE
See NS Plastic Chip Package Number V44A

Plastic Leaded Chip Carrier



Note:
-X Crystal Oscillator
-E Halt Mode Enabled

Top View
Order Number COP87L89EBV-XE or COP87L89RBV-XE
See NS Plastic Chip Package Number V68A

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 44-Pin and 68-Pin Packages

Port Pin	Type	ALT Function	44-Pin PLCC	68-Pin PLCC
G0	I/O	INT	44	1
G1	I/O	WDOUT	1	2
G2	I/O	T1B	2	3
G3	I/O	T1A	3	4
G4	I/O	SO	4	5
G5	I/O	SK	5	6
G6	I	SI	6	7
G7	I	CKO	7	8
D0	O		17	27
D1	O		18	28
D2	O		19	29
D3	O		20	30
D4	O			31
D5	O			32
D6	O			33
D7	O			34
I0	I	ADCH0	36	53
I1	I	ADCH1	37	54
I2	I	ADCH2	38	55
I3	I	ADCH3	39	56
I4	I	ADCH4		57
I5	I	ADCH5		58
I6	I	ADCH6		59
I7	I	ADCH7		60
L0	I/O	MIWU	40	61
L1	I/O	MIWU;CKX	41	62
L2	I/O	MIWU;TDX	42	63
L3	I/O	MIWU;RDX	43	64
L4	I/O	MIWU		65
L5	I/O	MIWU		66
L6	I/O	MIWU		67
L7	I/O	MIWU		68
M0	I/O	MIWU;MISO	21	38
M1	I/O	MIWU;MOSI	22	39
M2	I/O	MIWU;SCK	23	40
M3	I/O	MIWU;$\overline{SS}$	24	41
M4	I/O	MIWU;T2A	25	42
M5	I/O	MIWU;T2B	26	43
M6	I/O	MIWU	27	44
N0	I/O	ESS0	12	18
N1	I/O	ESS1	13	19
N2	I/O	ESS2	14	20
N3	I/O	ESS3	15	21
N4	I/O	ESS4		22
N5	I/O	ESS5		23
N6	I/O	ESS6		24
N7	I/O	ESS7		25

Port Pin	Type	ALT Function	44-Pin PLCC	68-Pin PLCC
F0	I/O			10
F1	I/O			11
F2	I/O			12
F3	I/O			13
F4	I/O			14
C0	I/O			35
C1	I/O			36
C2	I/O			37
RX0	I		31	48
RX1	I		30	47
TX0	O		29	46
TX1	O		28	45
$CANV_{REF}$			32	49
CKI			8	9
RESET			16	26
DV_{CC}			10, 33	16, 50
GND			9, 11, 34	15, 17, 51
A/D V_{REF}			35	52

National Semiconductor

COP87L88CF
8-Bit CMOS OTP Microcontrollers with 16k Memory and A/D Converter

General Description

The COP87L88CF OTP (One Time Programmable) microcontrollers are highly integrated COP8™ Feature core devices with 16k memory and advanced features including an A/D converter. These multi-chip CMOS devices are suited for applications requiring a full featured controller with an 8-bit A/D converter, and as pre-production devices for a masked ROM design. Lower cost pin and software compatible 16k ROM versions are available (COP888CF) as well as a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI (-XE = crystal oscillator) with 1 µs instruction cycle, two multi-function 16-bit timer/counters, MICROWIRE/PLUS™ serial I/O, one 8-bit/8-channel A/D converter with prescaler and both differential and single ended modes, two power saving HALT/IDLE modes, idle timer, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, 2.7V to 5.5V operation and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L84CF	16k OTP EPROM	128	24	28 DIP/SOIC	-40 to +85˚C
COP87L88CF	16k OTP EPROM	128	36/40	40 DIP, 44 PLCC	-40 to +85˚C

Key Features

- A/D converter (8-bit, 8-channel, with prescaler and both differential and single ended modes)
- Two 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 16 kbytes on-board OTP EPROM with security feature
- 128 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake Up (MIWU) with optional interrupts (8)
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE™Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- High current outputs
- Packages:
  - — 44 PLCC with 38 I/O pins
  - — 40 DIP with 34 I/O pins
  - — 28 DIP/SO with 22 I/O pins
- Schmitt trigger inputs on Port G

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Ten multi-source vectored interrupts servicing
  - — External interrupt with selectable edge
  - — Idle Timer T0
  - — Two Timers (Each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B, X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.7V to 5.5V
- Temperature ranges: -40˚C to +85˚C

Development Support

- Emulation device for the COP888CF/COP884CF
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

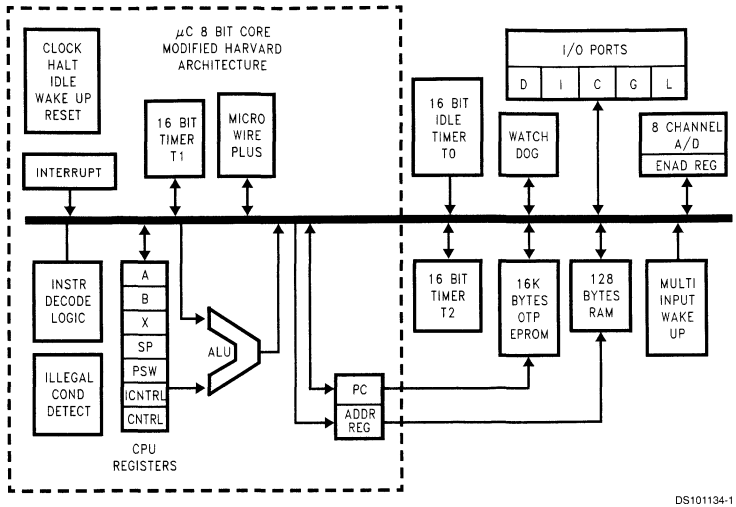
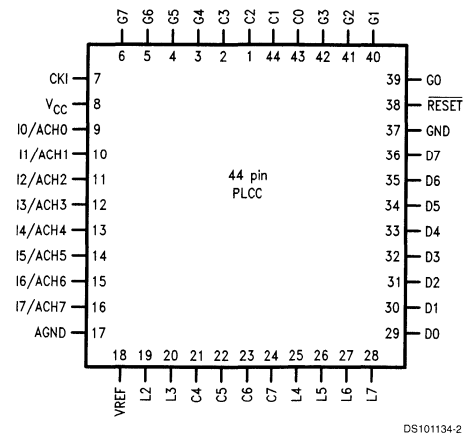


FIGURE 1. Block Diagram

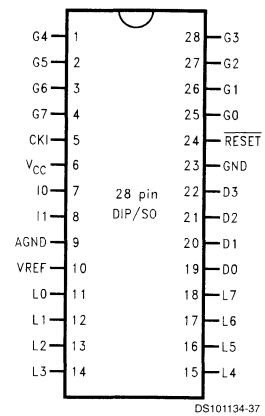
Connection Diagrams

Plastic Chip Carrier



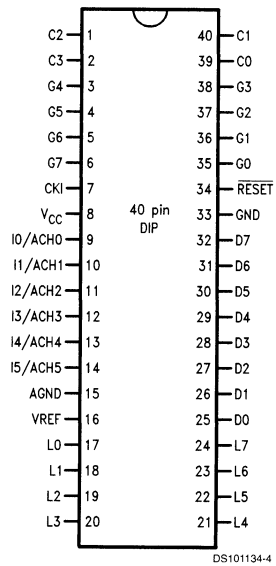
Top View
Order Number COP87L88CFV-XE
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View
Order Number COP87L84CFN-XE or
COP87L84CFM-XE
See NS Package Number N28B or M28B

Dual-In-Line Package



Top View
Order Number COP87L84CFN-XE,
See NS Molded Package Number N40A

Note: -X = Crystal Oscillator
-E = Halt Mode Enable

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40-, and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	—
L1	I/O	MIWU		12	18	—
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU		17	23	27
L7	I/O	MIWU		18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
I0	I	ACH0		7	9	9
I1	I	ACH1		8	10	10
I2	I	ACH2			11	11
I3	I	ACH3			12	12
I4	I	ACH4			13	13
I5	I	ACH5			14	14
I6	I	ACH6				15
I7	I	ACH7				16
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{REF}	$+V_{REF}$			10	16	18
AGND	AGND			9	15	17
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

National Semiconductor

COP87L88GD/RD Family
8-Bit CMOS OTP Microcontrollers with 16k or 32k Memory and 8-Channel A/D with Prescaler

General Description

The COP87L88GD/RD OTP (One Time Programmable) Family microcontrollers are highly integratet COP8™ Feature core devices with 16k or 32k memory and advanced features including an A/D Converter. These multi-chip CMOS devices are suited for applications requiring a full featured controller with an 8-bit A/D converter, and as pre-production devices for a masked ROM design. Pin and software compatible 16k ROM versions are available (COP888GD), as well as a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI (-XE = crystal oscillator) with 1µs instruction cycle, three multi-function 16-bit timer/counters, MICROWIRE/PLUS™ serial I/O, one 8-bit/8-channel A/D converter with prescaler and both differential and single ended modes, two power saving HALT/IDLE modes, MIWU, idle timer, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, 2.7V to 5.5V operation, program code security, and 44 pin package.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L88GD	16k EPROM	256	40	44 PLCC	-40 to +85˚C
COP87L88RD	32k EPROM	256	40	44 PLCC	-40 to +85˚C

Key Features

- 8-channel A/D converter with prescaler and both differential and single ended modes
- Idle Timer with 5 selectable Wake-Up periods
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 16 or 32 kbytes on-board OTP EPROM with security feature
- 256 bytes on-board RAM

Additional Peripheral Features

- Multi-Input Wakeup (MIWU) with optional interrupts (8)
- WATCHDOG and clock monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options (TRI-STATE® Output, Push-Pull Output, Weak Pull Up Input, High Impedance Input)
- Schmitt trigger inputs on ports G and L
- Package:
  - — 44 PLCC with 40 I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Twelve multi-source vectored interrupts servicing
  - — External Interrupt
  - — Idle Timer T0
  - — Three Timers (each with 2 Interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP) – stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B and X)

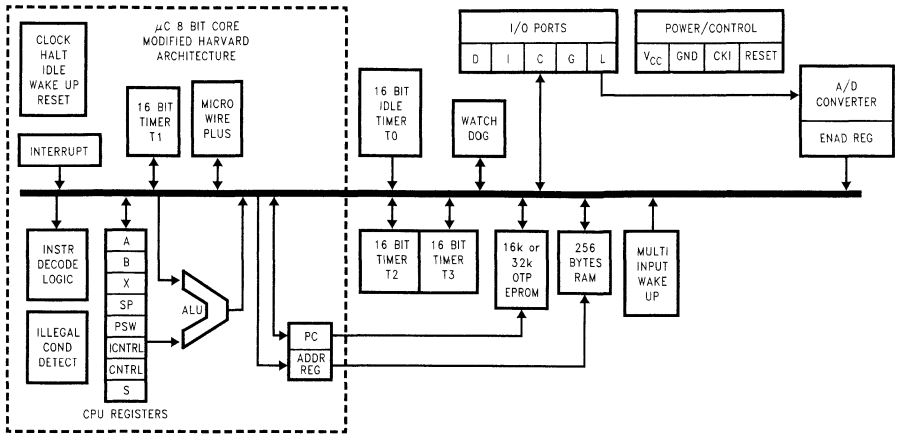
Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.7V to 5.5V
- Temperature range: –40˚C to +85˚C

Development Support

- Emulation device for COP888GD
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

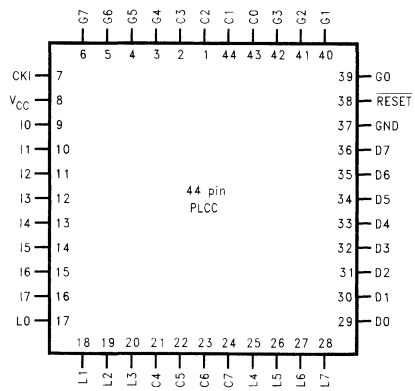


DS012526-1

FIGURE 1. Block Diagram

Connection Diagram

Plastic Chip Carrier



DS012526-2

Note: -X Crystal Oscillator
-E Halt Mode Enabled

Top View
Order Number COP87L88RDV-XE,
or COP87L88GDV-XE
See NS Plastic Chip Package Number V44A

FIGURE 2. Connection Diagram

Connection Diagram (Continued)

Pinouts for 40- and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	44-Pin Package
L0	I/O	MIWU		17
L1	I/O	MIWU		18
L2	I/O	MIWU		19
L3	I/O	MIWU		20
L4	I/O	MIWU	T2A	25
L5	I/O	MIWU	T2B	26
L6	I/O	MIWU	T3A	27
L7	I/O	MIWU	T3B	28
G0	I/O	INT		39
G1	WDOUT			40
G2	I/O	T1B		41
G3	I/O	T1A		42
G4	I/O	SO		3
G5	I/O	SK		4
G6	I	SI		5
G7	I/CKO	HALT Restart		6
D0	O			29
D1	O			30
D2	O			31
D3	O			32
D4	O			33
D5	O			34
D6	O			35
D7	O			36
I0	I	ACH0		9
I1	I	ACH1		10
I2	I	ACH2		11
I3	I	ACH3		12
I4	I	ACH4		13
I5	I	ACH5		14
I6	I	ACH6		15
I7	I	ACH7		16
C0	I/O			43
C1	I/O			44
C2	I/O			1
C3	I/O			2
C4	I/O			21
C5	I/O			22
C6	I/O			23
C7	I/O			24
V_{CC}				8
GND				37
CKI				7
$\overline{\text{RESET}}$				38

National Semiconductor

COP87L88EK/RK Family
8-Bit CMOS OTP Microcontrollers with 8k or 32k Memory, Comparator, and Single-slope A/D Capability

General Description

The COP87L88EK/RK Family OTP (One Time Programmable) microcontrollers are highly integrated COP8™ Feature core devices with 16k or 32k memory and advanced features including a Multi-Input Comparator and Single-slope A/D capability. These multi-chip CMOS devices are suited for applications requiring a full featured, low EMI controller with an analog comparator, current source, and voltage reference, and as pre-production devices for a masked ROM design. Lower cost pin and software compatible 8k ROM versions (COP888EK) are available for use with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10 MHz CKI (-XE = crystal oscillator) with 1 µs instruction cycle, three multi-function 16-bit timer/counters with PWM, MICROWIRE/PLUS™ serial I/O, one analog comparator with seven input multiplexor, an analog current source and $V_{CC}/2$ reference, two power saving HALT/IDLE modes, idle timer, MIWU, high current outputs, software selectable I/O options, WATCHDOG™ timer and Clock Monitor, 2.7V to 5.5V operation and 28/40/44 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L84EK	16k OTP EPROM	256	24	28 DIP/SOIC	-40 to +85˚C
COP87L88EK	16k OTP EPROM	256	36/40	40 DIP, 44 PLCC	-40 to +85˚C
COP87L84RK	32k OTP EPROM	256	24	28 DIP/SOIC	-40 to +85˚C
COP87L88RK	32k OTP EPROM	256	36/40	40 DIP, 44 PLCC	-40 to +85˚C

Key Features

- Analog function block with
  - — Analog comparator with seven input multiplexor
  - — Constant current source and $V_{CC}/2$ reference
- Three 16-bit timers, each with two 16-bit registers supporting:
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- 8 or 32 kbytes on-board EPROM with security feature
- 256 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake Up (MIWU) with optional interrupts (8)
- WATCHDOG and Clock Monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Software selectable I/O options (TRI-STATE™Output, Push-Pull Output, Weak Pull-Up Input, High Impedance Input)
- Packages:
  - — 44 PLCC with 40 I/O pins
  - — 40 DIP with 36 I/O pins
  - — 28 DIP/SO with 24 I/O pins
- Schmitt trigger inputs on Port G and L

CPU/Instruction Set Feature

- 1 µs instruction cycle time
- Twelve multi-source vectored interrupts servicing
  - — External Interrupt with selectable edge
  - — Idle Timer T0
  - — Three Timers (Each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake Up
  - — Software Trap
  - — Default VIS (default interrupt)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit Register Indirect Data Memory Pointers (B, X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.7V to 5.5V
- Temperature ranges: –40˚C to +85˚C

Development Support

- Emulation devices for the COP888EK/COP884EK
- Real time emulation and full program debug offered by MetaLink Development System

Block Diagram

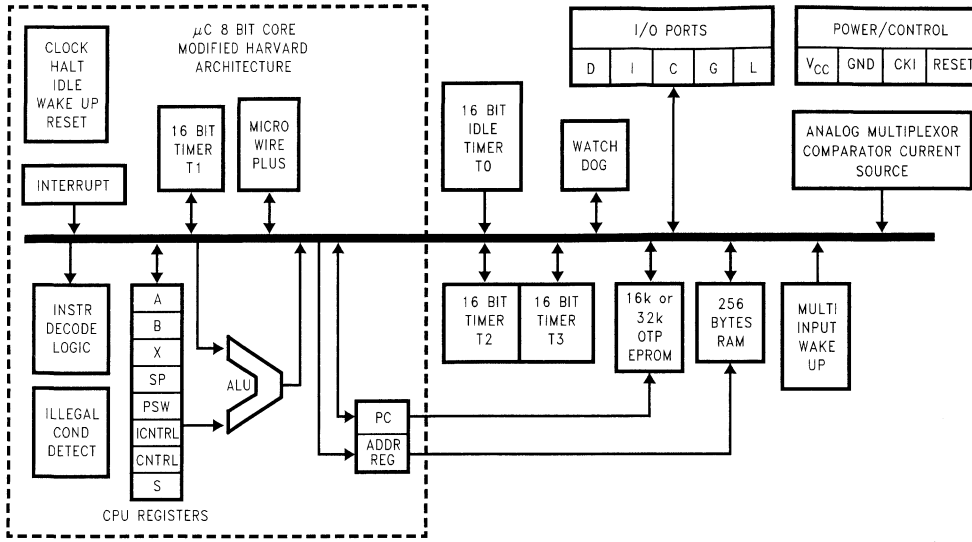
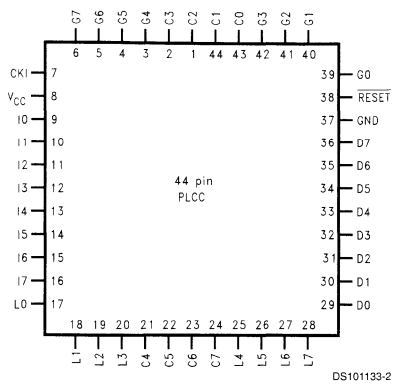


FIGURE 1. Block Diagram

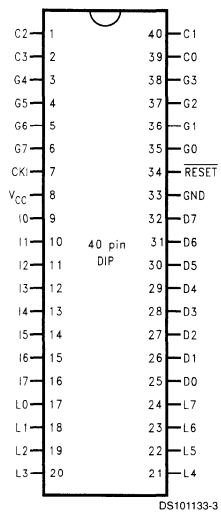
Connection Diagrams

Plastic Chip Carrier



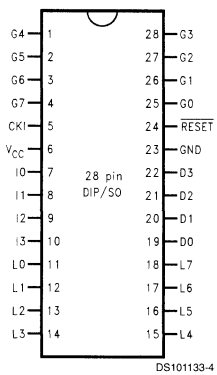
Top View
Order Number COP87L88EKV-XE or COP87L88RKV-XE
See NS Plastic Chip Package Number V44A

Dual-In-Line Package



Top View
Order Number COP87L84EKN-XE or COP87L84RKN-XE
See NS Molded Package Number N40A

Dual-In-Line Package



Top View
Order Number COP87L84EKN-XE or COP87L84RKN-XE
See NS Molded Package Number N28B
Order Number COP87L84EKM-XE or COP87L84RKM-XE
See NS Molded Package Number M28B

Note: -X Crystal Oscillator
-E Halt Mode Enabled

FIGURE 2. Connection Diagrams

Connection Diagrams (Continued)

Pinouts for 28-, 40-, and 44-Pin Packages

Port	Type	Alt. Fun	Alt. Fun	28-Pin Pack.	40-Pin Pack.	44-Pin Pack.
L0	I/O	MIWU		11	17	17
L1	I/O	MIWU		12	18	18
L2	I/O	MIWU		13	19	19
L3	I/O	MIWU		14	20	20
L4	I/O	MIWU	T2A	15	21	25
L5	I/O	MIWU	T2B	16	22	26
L6	I/O	MIWU	T3A	17	23	27
L7	I/O	MIWU	T3B	18	24	28
G0	I/O	INT		25	35	39
G1	WDOUT			26	36	40
G2	I/O	T1B		27	37	41
G3	I/O	T1A		28	38	42
G4	I/O	SO		1	3	3
G5	I/O	SK		2	4	4
G6	I	SI		3	5	5
G7	I/CKO	HALT Restart		4	6	6
D0	O			19	25	29
D1	O			20	26	30
D2	O			21	27	31
D3	O			22	28	32
I0	I	COMPIN1+		7	9	9
I1	I	COMPIN−/Current Source Out		8	10	10
I2	I	COMPIN0+		9	11	11
I3	I	COMPOUT/COMPIN2+		10	12	12
I4	I	COMPIN3+			13	13
I5	I	COMPIN4+			14	14
I6	I	COMPIN5+			15	15
I7	I	COMPOUT			16	16
D4	O				29	33
D5	O				30	34
D6	O				31	35
D7	O				32	36
C0	I/O				39	43
C1	I/O				40	44
C2	I/O				1	1
C3	I/O				2	2
C4	I/O					21
C5	I/O					22
C6	I/O					23
C7	I/O					24
V_{CC}				6	8	8
GND				23	33	37
CKI				5	7	7
$\overline{\text{RESET}}$				24	34	38

National Semiconductor

COP87L88RW
8-Bit One-Time Programmable (OTP) Microcontroller with Pulse Train Generators and Capture Modules

General Description

The COP87L88RW OTP microcontrollers are large memory (32k), highly integrated COP8™ Feature core devices, with advanced features including including Pulse Train Generators, Capture Modules, and hardware multiply/divide. These multi-chip CMOS devices are suited for applications requiring a full featured controller with high I/O pincount, pulse generation and capture, and a full-duplex USART, and for pre-production devices for ROM designs. Pin and software compatible 16k ROM versions are available (COP888GW), along with a range of COP8 software and hardware development tools.

Family features include an 8-bit memory mapped architecture, 10MHz CKI with 1µs instruction cycle, hardware multiply/divide functions, two 100ns capture modules, four pulse train generators with 16 bit prescalers, two multi-function 16-bit timer/counters, idle timer, full-duplex USART, MICROWIRE/PLUS™ serial I/O, two power saving HALT/IDLE modes, MIWU, high current outputs, software selectable I/O options, 2.7v-5.5v operation, program code security, and 68 pin packages.

Devices included in this datasheet are:

Device	Memory (bytes)	RAM (bytes)	I/O Pins	Packages	Temperature
COP87L88RW	32k OTP	512	64	68 PLCC	-40 to +85˚C

Key Features

- Multiply/divide functions
- Full duplex UART
- Four pulse train generators with 16-bit prescalers
- Two 16-bit input capture modules with 8-bit prescalers
- Two 16-bit timers, each with two 16-bit registers supporting
  - — Processor independent PWM mode
  - — External event counter mode
  - — Input capture mode
- 32 kbytes on-board OTP EPROM with security feature

Note: Mask ROMed devices with equivalent on-chip features and program memory sizes of 16k is available.

- 512 bytes on-board RAM

Additional Peripheral Features

- Idle Timer
- Multi-Input Wake-Up (MIWU) with optional interrupts (8)
- WATCHDOG™ and clock monitor logic
- MICROWIRE/PLUS serial I/O

I/O Features

- Memory mapped I/O
- Software selectable I/O options
  - — TRI-STATE® output
  - — Push-pull output
  - — Weak pull-up input
  - — High impedance input
- Schmitt trigger inputs on ports G and L
- Package: 68 PLCC with I/O pins

CPU/Instruction Set Features

- 1 µs instruction cycle time
- Fourteen multi-source vectored interrupts servicing
  - — External interrupt
  - — Idle timer T0
  - — Two timers (each with 2 interrupts)
  - — MICROWIRE/PLUS
  - — Multi-Input Wake-Up
  - — Software trap
  - — UART (2)
  - — Default VIS
  - — Capture timers
  - — Counters (one vector for all four counters)
- Versatile and easy to use instruction set
- 8-bit Stack Pointer (SP)—stack in RAM
- Two 8-bit register indirect data memory pointers (B and X)

Fully Static CMOS

- Two power saving modes: HALT and IDLE
- Single supply operation: 2.7V to 5.5V
- Temperature range: –40˚C to +85˚C

Development Support

- Emulation device for the COP888GW
- Real time emulation and full program debug offered by MetaLink's Development System

Block Diagram

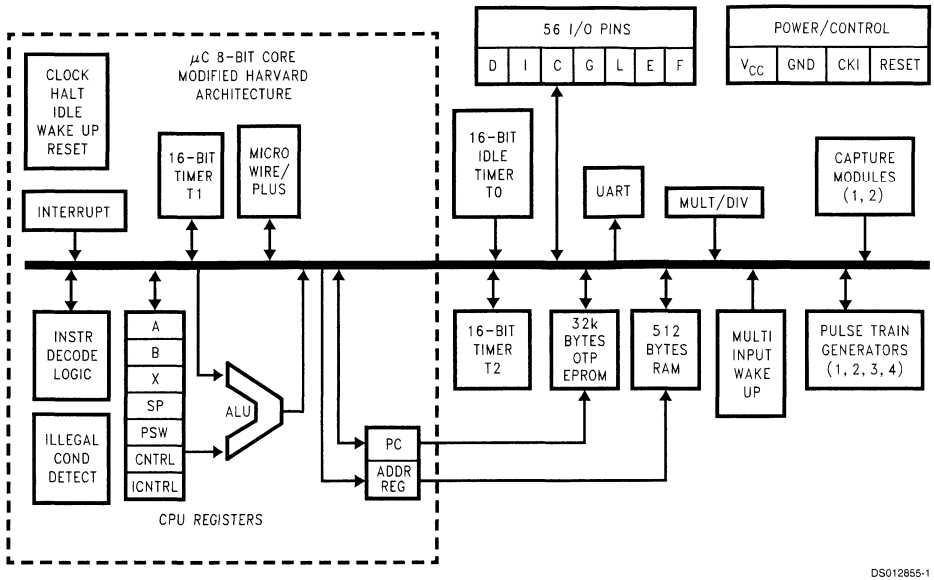
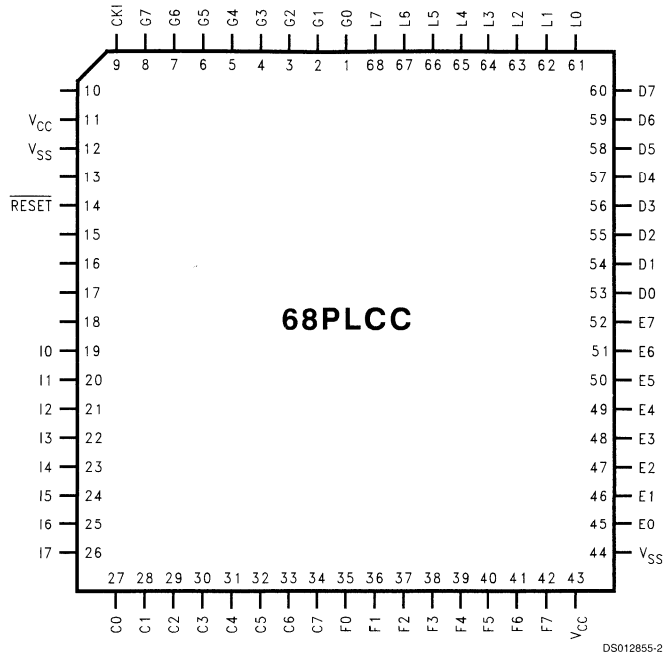


FIGURE 1. COP87L88RW Block Diagram

Connection Diagram



Note: -X Crystal Oscillator
Note: -E Halt Enable

Top View
Order Number COP87L88RWV-XE
See NS Plastic Chip Package Number V68A

FIGURE 2. Connection Diagram

National Semiconductor

Flash Products

National Semiconductor

COP8SBR9/COP8SCR9/COP8SDR9 8-Bit CMOS Flash Based Microcontroller with 32k Memory, Virtual EEPROM and Brownout

General Description

The COP8SBR9/SCR9/SDR9 Flash based microcontrollers are highly integrated COP8™ Feature core devices, with 32k Flash memory and advanced features including Virtual EEPROM, High Speed Timers, USART, and Brownout Reset.

This single-chip CMOS device is suited for applications requiring a full featured, in-system reprogrammable controller with large memory and low EMI. The same device is used for development, pre-production and volume production with a range of COP8 software and hardware development tools.

Devices included in this datasheet:

Device	Flash Program Memory (bytes)	RAM (bytes)	Brownout Voltage	I/O Pins	Packages	Temperature
COP8SBR9	32k	1k	2.7V to 2.9V	37,39,49, 59	44 LLP, 44/68 PLCC, 48/56 TSSOP	−40°C to +85°C
COP8SCR9	32k	1k	4.17V to 4.5V	37,39,49, 59	44 LLP, 44/68 PLCC, 48/56 TSSOP	−40°C to +85°C −40°C to +125°C
COP8SDR9	32k	1k	No Brownout	37,39,49, 59	44 LLP, 44/68 PLCC, 48/56 TSSOP	−40°C to +85°C −40°C to +125°C

Features

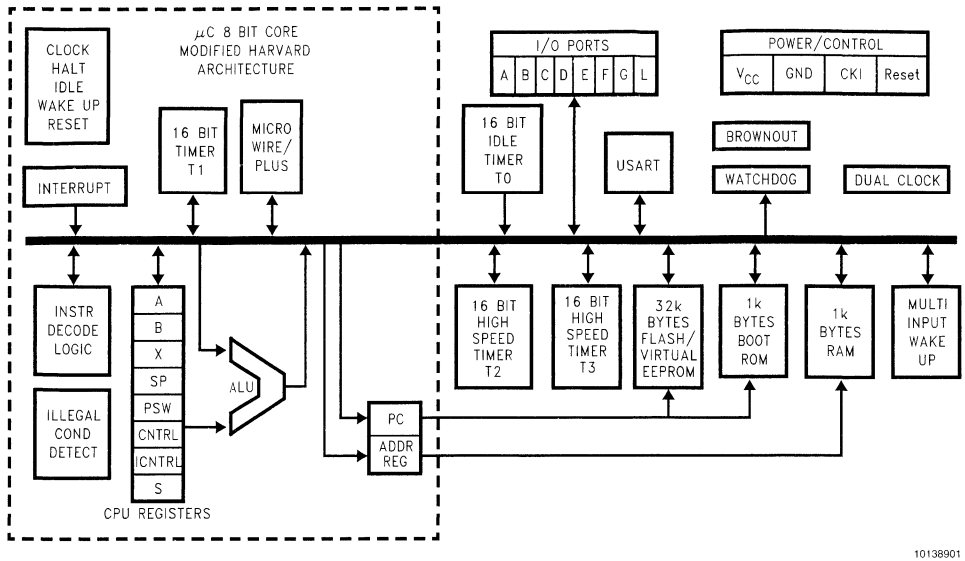
KEY FEATURES

- 32 kbytes Flash Program Memory with Security Feature
- Virtual EEPROM using Flash Program Memory
- 1 kbyte volatile RAM
- USART with on chip baud generator
- 2.7V–5.5V In-System Programmability of Flash
- High endurance - 100k Read/Write Cycles
- Superior data retention - 100 years
- Dual Clock Operation with HALT/IDLE Power Save Modes
- Three 16-bit timers:
  - — Timers T2 and T3 can operate at high speed (50 ns resolution)
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Brown-out Reset (COP8SBR9/SCR9)

OTHER FEATURES

- Single supply operation: 2.7V–5.5V
- Quiet Design (low radiated emissions)
- Multi-Input Wake-up with optional interrupts
- MICROWIRE/PLUS (Serial Peripheral Interface Compatible)
- Clock Doubler for 20 MHz operation from 10 MHz Oscillator, with 0.5 µs Instruction Cycle
- Thirteen multi-source vectored interrupts servicing:
  - — External Interrupt
  - — USART (2)
  - — Idle Timer T0
  - — Three Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS Serial peripheral interface
  - — Multi-Input Wake-Up
  - — Software Trap
- Idle Timer with programmable interrupt interval
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options
  - — TRI-STATE® Output/High Impedance Input
  - — Push-Pull Output
  - — Weak Pull Up Input
- Schmitt trigger inputs on I/O ports
- High Current I/Os
- Temperature range: −40°C to +85°C and −40°C to +125°C (COP8SCR9/SDR9)
- Packaging: 44 and 68 PLCC, 44 LLP, 48 and 56 TSSOP
- True In-System, Real time emulation and debug offered by MetaLink's Development Systemstools available

Block Diagram



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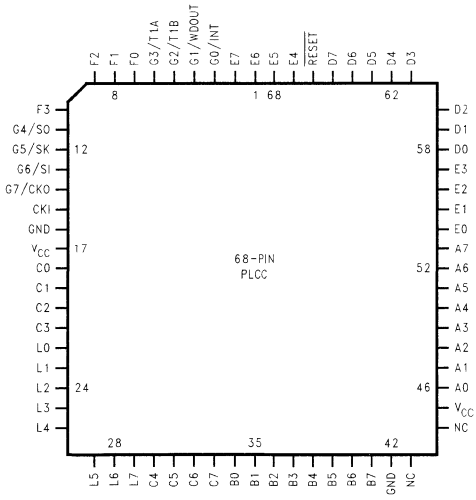
Connection Diagrams



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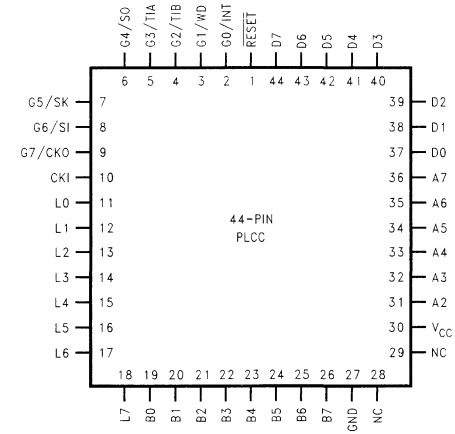
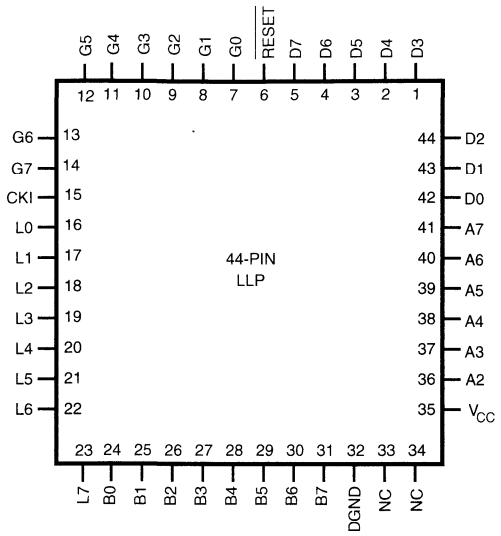
Top View
Plastic Chip Package
See NS Package Number V68A



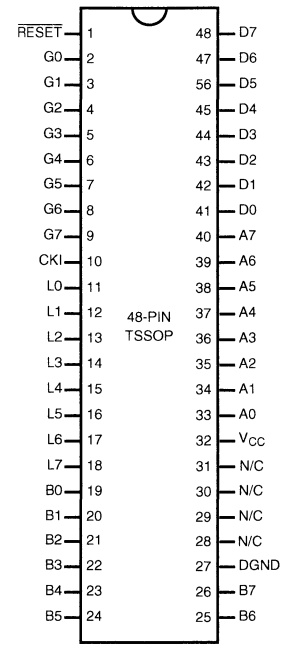
10138903

Top View
Plastic Chip Package
See NS Package Number V44A

Connection Diagrams (Continued)

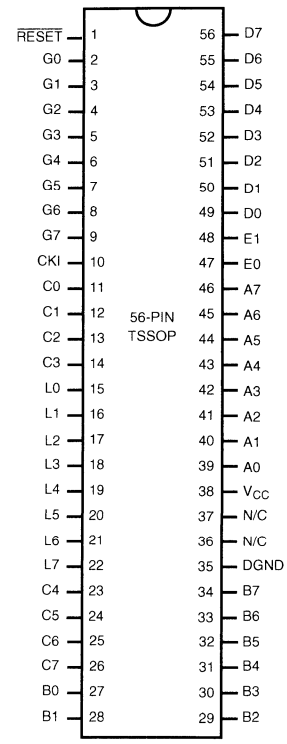


Top View
LLP Package
See NS Package Number LQA44A



Top View
TSSOP Package
See NS Package Number MTD48

Connection Diagrams (Continued)



Top View
TSSOP Package
See NS Package Number MTD56

Pinouts for All Packages

Port	Type	Alt. Fun	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP	56-Pin TSSOP	68-Pin PLCC
L0	I/O	MIWU or Low Speed OSC In		16	11	11	15	22
L1	I/O	MIWU or CKX or Low Speed OSC Out		17	12	12	16	23
L2	I/O	MIWU or TDX		18	13	13	17	24
L3	I/O	MIWU or RDX		19	14	14	18	25
L4	I/O	MIWU or T2A		20	15	15	19	26
L5	I/O	MIWU or T2B		21	16	16	20	27
L6	I/O	MIWU or T3A		22	17	17	21	28
L7	I/O	MIWU or T3B		23	18	18	22	29
G0	I/O	INT	Input	7	2	2	2	3
G1	I/O	WDOUT[a]	POUT	8	3	3	3	4
G2	I/O	T1B	Output	9	4	4	4	5
G3	I/O	T1A	Clock	10	5	5	5	6
G4	I/O	SO		11	6	6	6	11
G5	I/O	SK		12	7	7	7	12
G6	I	SI		13	8	8	8	13
G7	I	CKO		14	9	9	9	14
D0	O			42	37	41	49	58
D1	O			43	38	42	50	59
D2	O			44	39	43	51	60
D3	O			1	40	44	52	61
D4	O			2	41	45	53	62
D5	O			3	42	46	54	63
D6	O			4	43	47	55	64
D7	O			5	44	48	56	65
E0	I/O						47	54
E1	I/O						48	55
E2	I/O							56
E3	I/O							57
E4	I/O							67
E5	I/O							68
E6	I/O							1
E7	I/O							2
C0	I/O						11	18
C1	I/O						12	19
C2	I/O						13	20
C3	I/O						14	21
C4	I/O						23	30
C5	I/O						24	31
C6	I/O						25	32
C7	I/O						26	33
A0	I/O	ADCH0				33	39	46
A1	I/O	ADCH1				34	40	47
A2	I/O	ADCH2		36	31	35	41	48
A3	I/O	ADCH3		37	32	36	42	49
A4	I/O	ADCH4		38	33	37	43	50
A5	I/O	ADCH5		39	34	38	44	51
A6	I/O	ADCH6		40	35	39	45	52

Pinouts for All Packages (Continued)

Port	Type	Alt. Fun	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP	56-Pin TSSOP	68-Pin PLCC
A7	I/O	ADCH7		41	36	40	46	53
B0	I/O	ADCH8		24	19	19	27	34
B1	I/O	ADCH9		25	20	20	28	35
B2	I/O	ADCH10		26	21	21	29	36
B3	I/O	ADCH11		27	22	22	30	37
B4	I/O	ADCH12		28	23	23	31	38
B5	I/O	ADCH13 or A/D MUX OUT		29	24	24	32	39
B6	I/O	ADCH14 or A/D MUX OUT		30	25	25	33	40
B7	I/O	ADCH15 or A/DIN		31	26	26	34	41
F0	I/O							7
F1	I/O							8
F2	I/O							9
F3	I/O							10
DV_{CC}			V_{CC}	35	30	32	38	17, 45
DGND			GND	32	27	27	35	16, 42
CKI	I			15	10	10	10	15
$\overline{RESET}$	I		$\overline{RESET}$	6	1	1	1	66

a. G1 operation as WDOUT is controlled by Option Register bit 2.

Ordering Information

Part Numbering Scheme

COP8	SB	R	9	H	VA	8
	Family and Feature Set Indicator	Program Memory Size	Program Memory Type	No. Of Pins	Package Type	Temperature
	SB = Low Brownout Voltage SC = High Brownout Voltage SD = No Brownout	R = 32k	9 = Flash	H = 44 Pin I = 48 Pin k = 56 Pin L = 68 Pin	LQ = LLP MT = TSSOP VA = PLCC	7 = -40 to +125˚C 8 = -40 to +85˚C

1.0 General Description

1.1 EMI REDUCTION

The COP8SBR9/SCR9/SDR9 devices incorporate circuitry that guards against electromagnetic interference - an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal Icc smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 IN-SYSTEM PROGRAMMING AND VIRTUAL EEPROM

The device includes a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize in system software update capability if MICROWIRE/PLUS is not desired.

Additional functions will copy blocks of data between the RAM and the Flash Memory. These functions provide a virtual EEPROM capability by allowing the user to emulate a variable amount of EEPROM by initializing nonvolatile variables from the Flash Memory and occasionally restoring these variables to the Flash Memory.

The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins. For further information on the FLEX bit, refer to Section 4.5, Option Register.

1.3 DUAL CLOCK AND CLOCK DOUBLER

The device includes a versatile clocking system and two oscillator circuits designed to drive a crystal or ceramic resonator. The primary oscillator operates at high speed up to 10 MHz. The secondary oscillator is optimized for operation at 32.768 kHz.

The user can, through specified transition sequences (please refer to *7.0 Power Saving Features*), switch execution between the high speed and low speed oscillators. The unused oscillator can then be turned off to minimize power dissipation. If the low speed oscillator is not used, the pins are available as general purpose bidirectional ports.

The operation of the CPU will use a clock at twice the frequency of the selected oscillator (up to 20 MHz for high speed operation and 65.536 kHz for low speed operation). This doubled clock will be referred to in this document as 'MCLK'. The frequency of the selected oscillator will be referred to as CKI. Instruction execution occurs at one tenth the selected MCLK rate.

1.4 TRUE IN-SYSTEM EMULATION

On-chip emulation capability has been added which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

1.5 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently constant data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.6 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set - one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM, OTP or Flash). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.6.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

1.6.2 Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.6.3 Many Single-Byte, Multi-Function Instructions

The COP8 instruction set utilizes many single-byte, multi-function instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few

1.0 General Description (Continued)

examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (simplifying "FOR NEXT" or other loop structures in higher level languages).

1.6.4 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.6.5 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-mapped registers allow designers to optimize the precise implementation of certain specific instructions.

1.7 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increase device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins.

National Semiconductor

PRELIMINARY

COP8CBR9/COP8CCR9/COP8CDR9 8-Bit CMOS Flash Microcontroller with 32k Memory, Virtual EEPROM, 10-Bit A/D and Brownout

General Description

The COP8CBR/CCR/CDR9 Flash microcontrollers are highly integrated COP8™ Feature core devices, with 32k Flash memory and advanced features including Virtual EEPROM, A/D, High Speed Timers, USART, and Brownout Reset. This single-chip CMOS device is suited for applications requiring a full featured, in-system reprogrammable controller with large memory and low EMI. The same device is used for development, pre-production and volume production with a range of COP8 software and hardware development tools.

Device included in this datasheet:

Device	Flash Program Memory (bytes)	RAM (bytes)	Brownout Voltage	I/O Pins	Packages	Temperature
COP8CBR9	32k	1k	2.7V to 2.9V	37,39,49, 59	44 LLP, 44/68 PLCC, 48/56 TSSOP	−40°C to +85°C
COP8CCR9	32k	1k	4.17V to 4.5V	37,39,49, 59	44 LLP, 44/68 PLCC, 48/56 TSSOP	−40°C to +85°C −40°C to +125°C
COP8CDR9	32k	1k	No Brownout	37,39,49, 59	44 LLP, 44/68 PLCC, 48/56 TSSOP	−40°C to +85°C −40°C to +125°C

Features

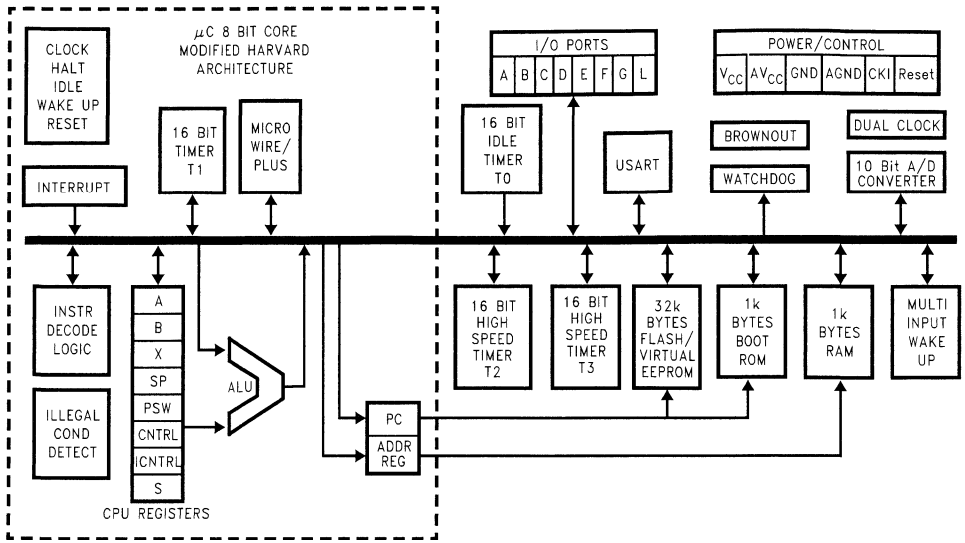
KEY FEATURES

- 32 kbytes Flash Program Memory with Security Feature
- Virtual EEPROM using Flash Program Memory
- 1 kbyte volatile RAM
- 10-bit Successive Approximation Analog to Digital Converter (up to 16 channels)
- 100% Precise Analog Emulation
- USART with onchip baud generator
- 2.7V – 5.5V In-System Programmability of Flash
- High endurance -100k Read/Write Cycles
- Superior Data Retention - 100 years
- Dual Clock Operation with HALT/IDLE Power Save Modes
- Three 16-bit timers:
  - — Timers T2 and T3 can operate at high speed (50 ns resolution)
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Brown-out Reset (COP8CBR9/CCR9)

OTHER FEATURES

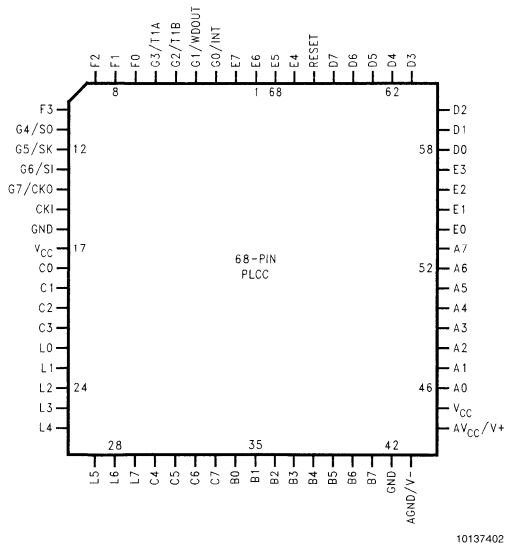
- Single supply operation:
  - — 2.7V–5.5V (−40°C to +85°C)
  - — 4.5V–5.5V (−40°C to +125°C)
- Quiet Design (low radiated emissions)
- Multi-Input Wake-up with optional interrupts
- MICROWIRE/PLUS (Serial Peripheral Interface Compatible)
- Clock Doubler for 20 MHz operation from 10 MHz Oscillator, with 0.5 µs Instruction Cycle
- Thirteen multi-source vectored interrupts servicing:
  - — External Interrupt
  - — USART (2)
  - — Idle Timer T0
  - — Three Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS Serial peripheral interface
  - — Multi-Input Wake-up
  - — Software Trap
- Idle Timer with programmable interrupt interval
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options
  - — TRI-STATE® Output/High Impedance Input
  - — Push-Pull Output
  - — Weak Pull Up Input
- Schmitt trigger inputs on I/O ports
- High Current I/Os
- Temperature range: −40°C to +85°C and −40°C to +125°C (COP8CCR9/CDR9)
- Packaging: 44 and 68 PLCC, 44 LLP, 48 and 56 TSSOP
- True In-System, real time emulation and debug tools available

Block Diagram



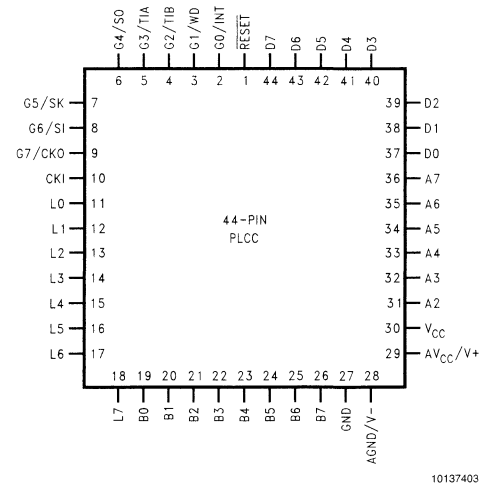
10137401

Connection Diagrams



10137402

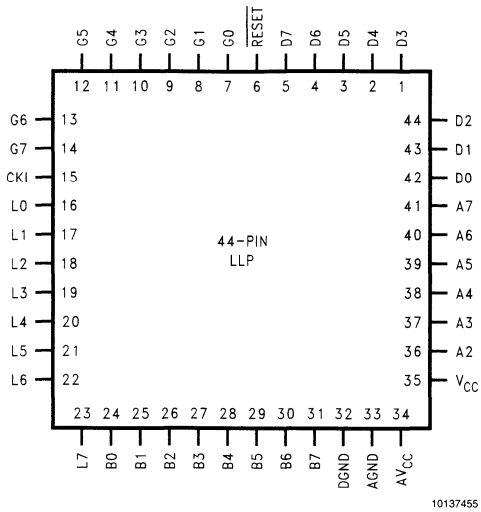
Top View
Plastic Chip Package
See NS Package Number V68A



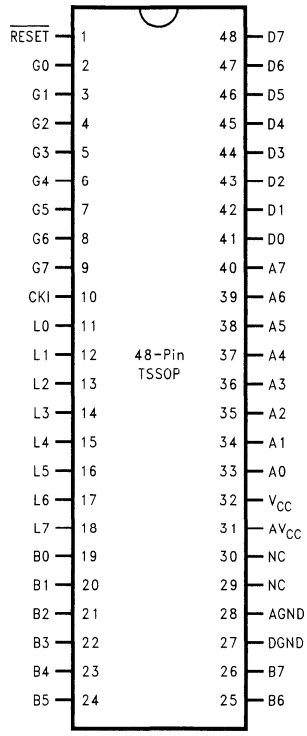
10137403

Top View
Plastic Chip Package
See NS Package Number V44A

Connection Diagrams (Continued)

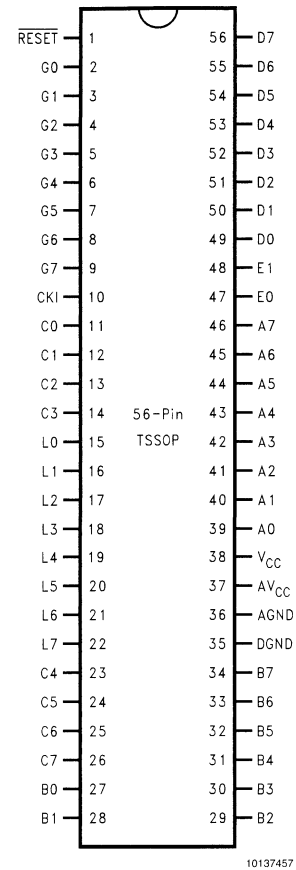


Top View
LLP Package
See NS Package Number LQA44A



Top View
TSSOP Package
See NS Package Number MTD48

Connection Diagrams (Continued)



Top View
TSSOP Package
See NS Package Number MTD56

Pinouts for All Packages

Port	Type	Alt. Fun	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP	56-Pin TSSOP	68-Pin PLCC
L0	I/O	MIWU or Low Speed OSC In		16	11	11	15	22
L1	I/O	MIWU or CKX or Low Speed OSC Out		17	12	12	16	23
L2	I/O	MIWU or TDX		18	13	13	17	24
L3	I/O	MIWU or RDX		19	14	14	18	25
L4	I/O	MIWU or T2A		20	15	15	19	26
L5	I/O	MIWU or T2B		21	16	16	20	27
L6	I/O	MIWU or T3A		22	17	17	21	28
L7	I/O	MIWU or T3B		23	18	18	22	29
G0	I/O	INT	Input	7	2	2	2	3
G1	I/O	WDOUT[a]	POUT	8	3	3	3	4
G2	I/O	T1B	Output	9	4	4	4	5
G3	I/O	T1A	Clock	10	5	5	5	6
G4	I/O	SO		11	6	6	6	11
G5	I/O	SK		12	7	7	7	12
G6	I	SI		13	8	8	8	13
G7	I	CKO		14	9	9	9	14
D0	O			42	37	41	49	58
D1	O			43	38	42	50	59
D2	O			44	39	43	51	60
D3	O			1	40	44	52	61
D4	O			2	41	45	53	62
D5	O			3	42	46	54	63
D6	O			4	43	47	55	64
D7	O			5	44	48	56	65
E0	I/O						47	54
E1	I/O						48	55
E2	I/O							56
E3	I/O							57
E4	I/O							67
E5	I/O							68
E6	I/O							1
E7	I/O							2
C0	I/O						11	18
C1	I/O						12	19
C2	I/O						13	20
C3	I/O						14	21
C4	I/O						23	30
C5	I/O						24	31
C6	I/O						25	32
C7	I/O						26	33
A0	I/O	ADCH0				33	39	46
A1	I/O	ADCH1				34	40	47
A2	I/O	ADCH2		36	31	35	41	48
A3	I/O	ADCH3		37	32	36	42	49
A4	I/O	ADCH4		38	33	37	43	50
A5	I/O	ADCH5		39	34	38	44	51
A6	I/O	ADCH6		40	35	39	45	52

Pinouts for All Packages (Continued)

Port	Type	Alt. Fun	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP	56-Pin TSSOP	68-Pin PLCC
A7	I/O	ADCH7		41	36	40	46	53
B0	I/O	ADCH8		24	19	19	27	34
B1	I/O	ADCH9		25	20	20	28	35
B2	I/O	ADCH10		26	21	21	29	36
B3	I/O	ADCH11		27	22	22	30	37
B4	I/O	ADCH12		28	23	23	31	38
B5	I/O	ADCH13 or A/D MUX OUT		29	24	24	32	39
B6	I/O	ADCH14 or A/D MUX OUT		30	25	25	33	40
B7	I/O	ADCH15 or A/DIN		31	26	26	34	41
F0	I/O							7
F1	I/O							8
F2	I/O							9
F3	I/O							10
DV_{CC}			V_{CC}	35	30	32	38	17, 45
DGND			GND	32	27	27	35	16, 42
AV_{CC}				34	29	31	37	44
AGND				33	28	28	36	43
CKI	I			15	10	10	10	15
$\overline{\text{RESET}}$	I		$\overline{\text{RESET}}$	6	1	1	1	66

a. G1 operation as WDOUT is controlled by Option Register bit 2.

Ordering Information

Part Numbering Scheme

COP8	CB	R	9	H	VA	8
	Family and Feature Set Indicator	Program Memory Size	Program Memory Type	No. Of Pins	Package Type	Temperature
	CB = Low Brownout Voltage CC = High Brownout Voltage CD = No Brownout	R = 32k	9 = Flash	H = 44 Pin I = 48 Pin k = 56 Pin L = 68 Pin	LQ = LLP MT = TSSOP VA = PLCC	7 = -40 to +125°C 8 = -40 to +85°C

1.0 General Description

1.1 EMI REDUCTION

The COP8CBR/CCR/CDR devices incorporate circuitry that guards against electromagnetic interference - an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal Icc smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 IN-SYSTEM PROGRAMMING AND VIRTUAL EEPROM

The device includes a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize in system software update capability if MICROWIRE/PLUS is not desired.

Additional functions will copy blocks of data between the RAM and the Flash Memory. These functions provide a virtual EEPROM capability by allowing the user to emulate a variable amount of EEPROM by initializing nonvolatile variables from the Flash Memory and occasionally restoring these variables to the Flash Memory.

The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins. For further information on the FLEX bit, refer to Section 4.5, Option Register.

1.3 DUAL CLOCK AND CLOCK DOUBLER

The device includes a versatile clocking system and two oscillator circuits designed to drive a crystal or ceramic resonator. The primary oscillator operates at high speed up to 10 MHz. The secondary oscillator is optimized for operation at 32.768 kHz.

The user can, through specified transition sequences (please refer to *7.0 Power Saving Features*), switch execution between the high speed and low speed oscillators. The unused oscillator can then be turned off to minimize power dissipation. If the low speed oscillator is not used, the pins are available as general purpose bidirectional ports.

The operation of the CPU will use a clock at twice the frequency of the selected oscillator (up to 20 MHz for high speed operation and 65.536 kHz for low speed operation). This doubled clock will be referred to in this document as 'MCLK'. The frequency of the selected oscillator will be referred to as CKI. Instruction execution occurs at one tenth the selected MCLK rate.

1.4 TRUE IN-SYSTEM EMULATION

On-chip emulation capability has been added which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

1.5 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently constant data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.6 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set - one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM, OTP or Flash). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.6.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

1.6.2 Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.6.3 Many Single-Byte, Multi-Function Instructions

The COP8 instruction set utilizes many single-byte, multi-function instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few

1.0 General Description (Continued)

examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (simplifying "FOR NEXT" or other loop structures in higher level languages).

1.6.4 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.6.5 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-mapped registers allow designers to optimize the precise implementation of certain specific instructions.

1.7 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increase device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins.

National Semiconductor

PRELIMINARY

COP8CBE9/CCE9/CDE9
8-Bit CMOS Flash Microcontroller with 8k Memory, Virtual EEPROM, 10-Bit A/D and Brownout Reset

General Description

The COP8CBE9/CCE9/CDE9 Flash microcontrollers are highly integrated COP8™ Feature core devices, with 8k Flash memory and advanced features including Virtual EEPROM, A/D, High Speed Timers, USART, and Brownout Reset. This single-chip CMOS device is suited for applications requiring a full featured, in-system reprogrammable controller with large memory and low EMI. The same device is used for development, pre-production and volume production with a range of COP8 software and hardware development tools.

Devices included in this datasheet:

Device	Flash Program Memory (bytes)	RAM (bytes)	Brownout Voltage	I/O Pins	Packages	Temperature
COP8CBE9	8k	256	2.7V to 2.9V	37,39	44 LLP, 44PLCC, 48 TSSOP	0°C to +70°C
COP8CCE9	8k	256	4.17V to 4.5V	37,39	44 LLP, 44PLCC, 48 TSSOP	0°C to +70°C −40°C to +125°C
COP8CDE9	8k	256	No Brownout	37,39	44 LLP, 44 PLCC, 48 TSSOP	0°C to +70°C −40°C to +125°C

Features

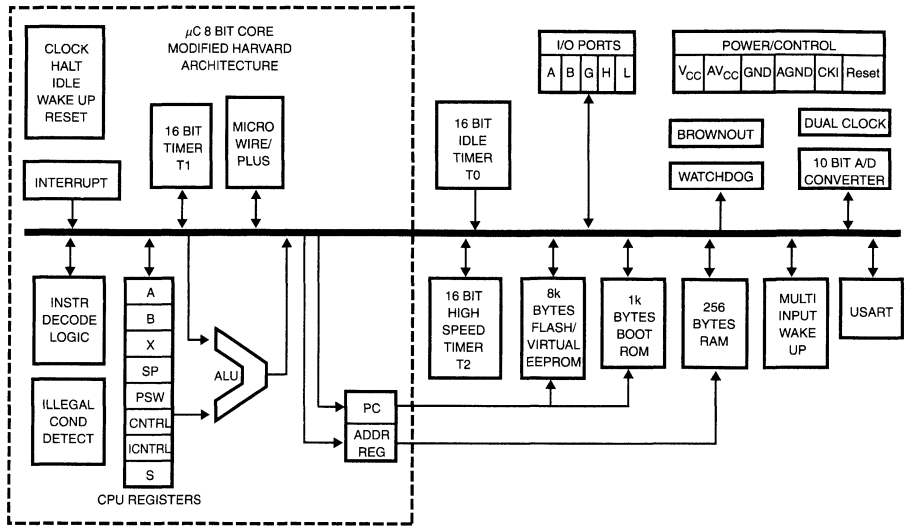
KEY FEATURES

- 8k bytes Flash Program Memory with Security Feature
- Virtual EEPROM using Flash Program Memory
- 256byte volatile RAM
- 10-bit Successive Approximation Analog to Digital Converter (up to 16 channels)
- 100% Precise Analog Emulation
- USART with onchip baud generator
- 2.7V – 5.5V In-System Programmability of Flash
- High endurance -100k Read/Write Cycles
- Superior Data Retention - 100 years
- Dual Clock Operation with HALT/IDLE Power Save Modes
- Two 16-bit timers:
  - — Timer T2 can operate at high speed (50 ns resolution)
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Brown-out Reset (COP8CBE9/CCE9)
- High Current I/Os
  - — B0– B3: 10 mA @ 0.3V
  - — All others: 10 mA @ 1.0V

OTHER FEATURES

- Single supply operation:
  - — 2.7V–5.5V (0°C to +70°C)
  - — 4.5V–5.5V (−40°C to +125°C)
- Quiet Design (low radiated emissions)
- Multi-Input Wake-up with optional interrupts
- MICROWIRE/PLUS (Serial Peripheral Interface Compatible)
- Clock Doubler for 20 MHz operation from 10 MHz Oscillator, with 0.5 µs Instruction Cycle
- Eleven multi-source vectored interrupts servicing:
  - — External Interrupt
  - — USART (2)
  - — Idle Timer T0
  - — Two Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS Serial peripheral interface
  - — Multi-Input Wake-up
  - — Software Trap
- Idle Timer with programmable interrupt interval
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options
  - — TRI-STATE Output/High Impedance Input
  - — Push-Pull Output
  - — Weak Pull Up Input
- Schmitt trigger inputs on I/O ports
- Temperature range: 0°C to +70°C and −40°C to +125°C (COP8CCE9/CDE9)
- Packaging: 44 PLCC, 44 LLP and 48 TSSOP

Block Diagram



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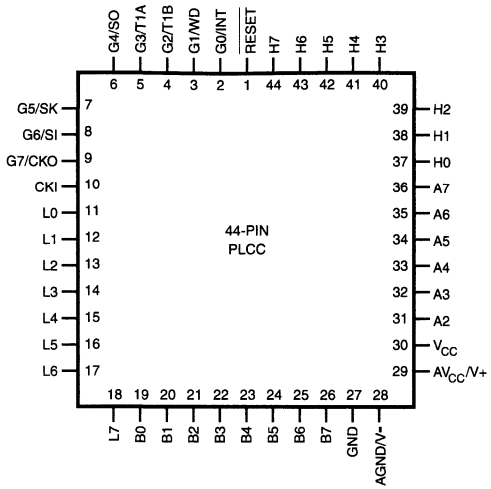
Ordering Information

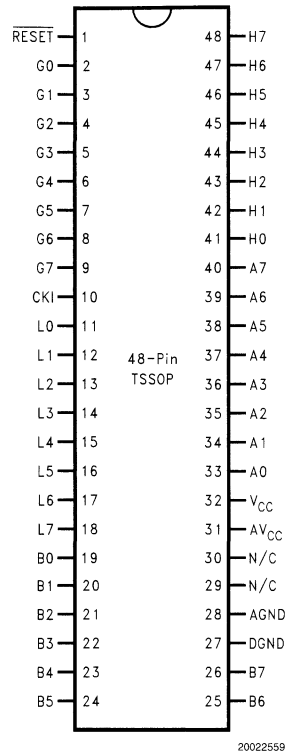
Part Numbering Scheme

COP8	CB	E	9	H	VA	8
	Family and Feature Set Indicator	Program Memory Size	Program Memory Type	No. Of Pins	Package Type	Temperature
	CB = Low Brownout Voltage CC = High Brownout Voltage CD = No Brownout	E = 8k	9 = Flash	H = 44 Pin I = 48 Pin	LQ = LLP MT = TSSOP VA = PLCC	7 = -40 to +125°C 9 = 0 to +70°C

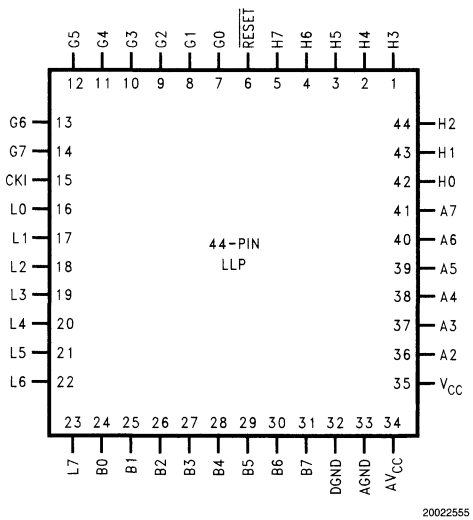
Connection Diagrams



Top View
Plastic Chip Package
See NS Package Number V44A



Top View
TSSOP Package
See NS Package Number MTD48



Top View
LLP Package
See NS Package Number LQA44A

Pinouts for 44- and 48-Pin Packages

Port	Type	Alt. Function	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP
L0	I/O	MIWU or Low Speed OSC In		16	11	11
L1	I/O	MIWU or CKX or Low Speed OSC Out		17	12	12
L2	I/O	MIWU or TDX		18	13	13
L3	I/O	MIWU or RDX		19	14	14
L4	I/O	MIWU or T2A		20	15	15
L5	I/O	MIWU or T2B		21	16	16
L6	I/O	MIWU		22	17	17
L7	I/O	MIWU		23	18	18
G0	I/O	INT	Input	7	2	2
G1	I/O	WDOUT[a]	POUT	8	3	3
G2	I/O	T1B	Output	9	4	4
G3	I/O	T1A	Clock	10	5	5
G4	I/O	SO		11	6	6
G5	I/O	SK		12	7	7
G6	I	SI		13	8	8
G7	I	CKO		14	9	9
H0	I/O			42	37	41
H1	I/O			43	38	42
H2	I/O			44	39	43
H3	I/O			1	40	44
H4	I/O			2	41	45
H5	I/O			3	42	46
H6	I/O			4	43	47
H7	I/O			5	44	48
A0	I/O	ADCH0				33
A1	I/O	ADCH1				34
A2	I/O	ADCH2		36	31	35
A3	I/O	ADCH3		37	32	36
A4	I/O	ADCH4		38	33	37
A5	I/O	ADCH5		39	34	38
A6	I/O	ADCH6		40	35	39
A7	I/O	ADCH7		41	36	40
B0	I/O	ADCH8		24	19	19
B1	I/O	ADCH9		25	20	20
B2	I/O	ADCH10		26	21	21
B3	I/O	ADCH11		27	22	22
B4	I/O	ADCH12		28	23	23
B5	I/O	ADCH13 or A/D MUX OUT		29	24	24
B6	I/O	ADCH14 or A/D MUX OUT		30	25	25
B7	I/O	ADCH15 or A/DIN		31	26	26
DV_{CC}			V_{CC}	35	30	32
DGND			GND	32	27	27
AV_{CC}				34	29	31
AGND				33	28	28
CKI	I			15	10	10
$\overline{\text{RESET}}$	I		$\overline{\text{RESET}}$	6	1	1

a. G1 operation as WDOUT is controlled by Option Register bit 2.

1.0 General Description

1.1 EMI REDUCTION

The COP8CBE9/CCE9/CDE9 devices incorporate circuitry that guards against electromagnetic interference - an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal Icc smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 IN-SYSTEM PROGRAMMING AND VIRTUAL EEPROM

The device includes a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize in system software update capability if MICROWIRE/PLUS is not desired.

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The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins. For further information on the FLEX bit, refer to Section 4.5, Option Register.

1.3 DUAL CLOCK AND CLOCK DOUBLER

The device includes a versatile clocking system and two oscillator circuits designed to drive a crystal or ceramic resonator. The primary oscillator operates at high speed up to 10 MHz. The secondary oscillator is optimized for operation at 32.768 kHz.

The user can, through specified transition sequences (please refer to *7.0 Power Saving Features*), switch execution between the high speed and low speed oscillators. The unused oscillator can then be turned off to minimize power dissipation. If the low speed oscillator is not used, the pins are available as general purpose bidirectional ports.

The operation of the CPU will use a clock at twice the frequency of the selected oscillator (up to 20 MHz for high speed operation and 65.536 kHz for low speed operation). This doubled clock will be referred to in this document as 'MCLK'. The frequency of the selected oscillator will be referred to as CKI. Instruction execution occurs at one tenth the selected MCLK rate.

1.4 TRUE IN-SYSTEM EMULATION

On-chip emulation capability has been added which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

1.5 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently constant data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

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1.6 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set - one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM, OTP or Flash). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.6.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

1.6.2 Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.6.3 Many Single-Byte, Multi-Function Instructions

The COP8 instruction set utilizes many single-byte, multi-function instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few

1.0 General Description (Continued)

examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (simplifying "FOR NEXT" or other loop structures in higher level languages).

1.6.4 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.6.5 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-mapped registers allow designers to optimize the precise implementation of certain specific instructions.

1.7 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increase device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins.

National Semiconductor

PRELIMINARY

COP8SBE9/SCE9/SDE9
8-Bit CMOS Flash Microcontroller with 8k Memory, Virtual EEPROM and Brownout Reset

General Description

The COP8SBE9/SCE9/SDE9 Flash microcontrollers are highly integrated COP8™ Feature core devices, with 8k Flash memory and advanced features including Virtual EEPROM, High Speed Timers, USART, and Brownout Reset.

This single-chip CMOS device is suited for applications requiring a full featured, in-system reprogrammable controller with large memory and low EMI. The same device is used for development, pre-production and volume production with a range of COP8 software and hardware development tools.

Devices included in this datasheet:

Device	Flash Program Memory (bytes)	RAM (bytes)	Brownout Voltage	I/O Pins	Packages	Temperature
COP8SBE9	8k	256	2.7V to 2.9V	37,39	44 LLP, 44PLCC, 48 TSSOP	−40˚C to +85˚
COP8SCE9	8k	256	4.17V to 4.5V	37,39	44 LLP, 44PLCC, 48 TSSOP	−40˚C to +85˚C −40˚C to +125˚C
COP8SDE9	8k	256	No Brownout	37,39	44 LLP, 44 PLCC, 48 TSSOP	−40˚C to +85˚C −40˚C to +125˚C

Features

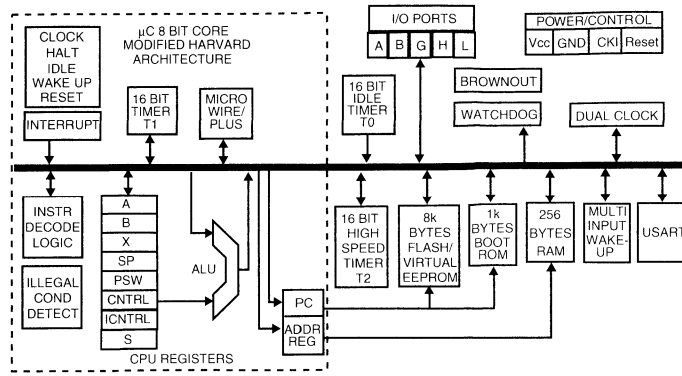
KEY FEATURES

- 8k bytes Flash Program Memory with Security Feature
- Virtual EEPROM using Flash Program Memory
- 256byte volatile RAM
- USART with onchip baud generator
- 2.7V – 5.5V In-System Programmability of Flash
- High endurance -100k Read/Write Cycles
- Superior Data Retention - 100 years
- Dual Clock Operation with HALT/IDLE Power Save Modes
- Two 16-bit timers:
  - — Timer T2 can operate at high speed (50 ns resolution)
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Brown-out Reset (COP8SBE9/SCE9)
- High Current I/Os
  - — Bo – B3: 10 mA @ 0.3V
  - — All others: 10 mA @ 1.0V

OTHER FEATURES

- Single supply operation:
  - — 2.7V–5.5V (−40˚C to +85˚C)
  - — 4.5V–5.5V (−40˚C to +125˚C)
- Quiet Design (low radiated emissions)
- Multi-Input Wake-up with optional interrupts
- MICROWIRE/PLUS (Serial Peripheral Interface Compatible)
- Clock Doubler for 20 MHz operation from 10 MHz Oscillator, with 0.5 µs Instruction Cycle
- Eleven multi-source vectored interrupts servicing:
  - — External Interrupt
  - — USART (2)
  - — Idle Timer T0
  - — Two Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS Serial peripheral interface
  - — Multi-Input Wake-up
  - — Software Trap
- Idle Timer with programmable interrupt interval
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options
  - — TRI-STATE Output/High Impedance Input
  - — Push-Pull Output
  - — Weak Pull Up Input
- Schmitt trigger inputs on I/O ports
- Temperature range: −40˚C to +85˚C and −40˚C to +125˚C (COP8SCE9/SDE9)
- Packaging: 44 PLCC, 44 LLP and 48 TSSOP

Block Diagram



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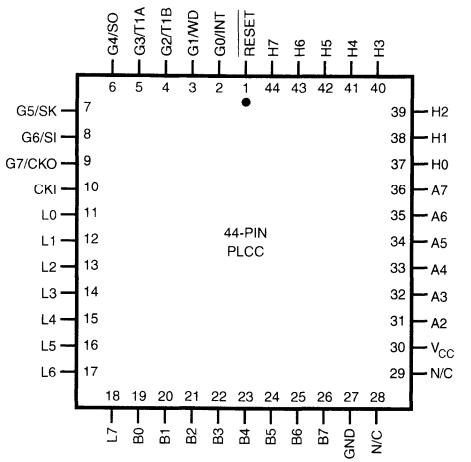
Ordering Information

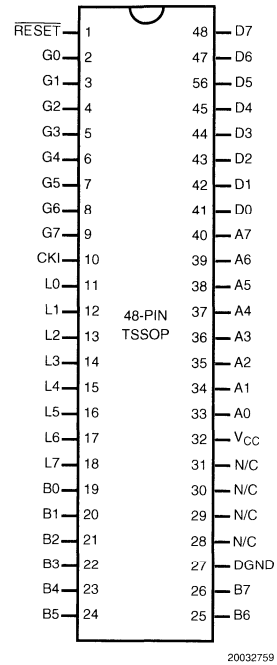
Part Numbering Scheme

COP8	SB	E	9	H	VA	8
	Family and Feature Set Indicator	Program Memory Size	Program Memory Type	No. Of Pins	Package Type	Temperature
	SB = Low Brownout Voltage SC = High Brownout Voltage SD = No Brownout	E = 8k	9 = Flash	H = 44 Pin I = 48 Pin	LQ = LLP MT = TSSOP VA = PLCC	7 = -40 to +125°C 8 = -40 to +85°C

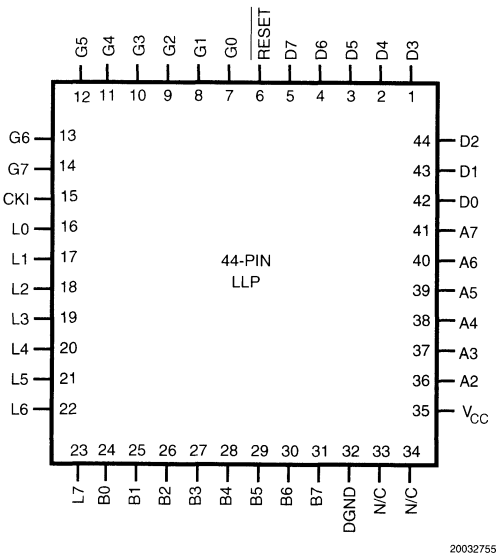
Connection Diagrams



Top View
Plastic Chip Package
See NS Package Number V44A



Top View
TSSOP Package
See NS Package Number MTD48



Top View
LLP Package
See NS Package Number LQA44A

Pinouts for 44- and 48-Pin Packages

Port	Type	Alt. Function	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP
L0	I/O	MIWU or Low Speed OSC In		16	11	11
L1	I/O	MIWU or CKX or Low Speed OSC Out		17	12	12
L2	I/O	MIWU or TDX		18	13	13
L3	I/O	MIWU or RDX		19	14	14
L4	I/O	MIWU or T2A		20	15	15
L5	I/O	MIWU or T2B		21	16	16
L6	I/O	MIWU		22	17	17
L7	I/O	MIWU		23	18	18
G0	I/O	INT	Input	7	2	2
G1	I/O	WDOUT[a]	POUT	8	3	3
G2	I/O	T1B	Output	9	4	4
G3	I/O	T1A	Clock	10	5	5
G4	I/O	SO		11	6	6
G5	I/O	SK		12	7	7
G6	I	SI		13	8	8
G7	I	CKO		14	9	9
H0	I/O			42	37	41
H1	I/O			43	38	42
H2	I/O			44	39	43
H3	I/O			1	40	44
H4	I/O			2	41	45
H5	I/O			3	42	46
H6	I/O			4	43	47
H7	I/O			5	44	48
A0	I/O					33
A1	I/O					34
A2	I/O			36	31	35
A3	I/O			37	32	36
A4	I/O			38	33	37
A5	I/O			39	34	38
A6	I/O			40	35	39
A7	I/O			41	36	40
B0	I/O			24	19	19
B1	I/O			25	20	20
B2	I/O			26	21	21
B3	I/O			27	22	22
B4	I/O			28	23	23
B5	I/O			29	24	24
B6	I/O			30	25	25
B7	I/O			31	26	26
DV_{CC}			V_{CC}	35	30	32
DGND			GND	32	27	27
CKI	I			15	10	10
$\overline{\text{RESET}}$	I		$\overline{\text{RESET}}$	6	1	1

a. G1 operation as WDOUT is controlled by Option Register bit 2.

1.0 General Description

1.1 EMI REDUCTION

The COP8SBE9/SCE9/SDE9 devices incorporate circuitry that guards against electromagnetic interference - an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal Icc smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 IN-SYSTEM PROGRAMMING AND VIRTUAL EEPROM

The device includes a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize in system software update capability if MICROWIRE/PLUS is not desired.

Additional functions will copy blocks of data between the RAM and the Flash Memory. These functions provide a virtual EEPROM capability by allowing the user to emulate a variable amount of EEPROM by initializing nonvolatile variables from the Flash Memory and occasionally restoring these variables to the Flash Memory.

The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins. For further information on the FLEX bit, refer to Section 4.5, Option Register.

1.3 DUAL CLOCK AND CLOCK DOUBLER

The device includes a versatile clocking system and two oscillator circuits designed to drive a crystal or ceramic resonator. The primary oscillator operates at high speed up to 10 MHz. The secondary oscillator is optimized for operation at 32.768 kHz.

The user can, through specified transition sequences (please refer to *7.0 Power Saving Features*), switch execution between the high speed and low speed oscillators. The unused oscillator can then be turned off to minimize power dissipation. If the low speed oscillator is not used, the pins are available as general purpose bidirectional ports.

The operation of the CPU will use a clock at twice the frequency of the selected oscillator (up to 20 MHz for high speed operation and 65.536 kHz for low speed operation). This doubled clock will be referred to in this document as 'MCLK'. The frequency of the selected oscillator will be referred to as CKI. Instruction execution occurs at one tenth the selected MCLK rate.

1.4 TRUE IN-SYSTEM EMULATION

On-chip emulation capability has been added which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

1.5 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently constant data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.6 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set - one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM, OTP or Flash). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.6.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

1.6.2 Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.6.3 Many Single-Byte, Multi-Function Instructions

The COP8 instruction set utilizes many single-byte, multi-function instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few

1.0 General Description (Continued)

examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (simplifying "FOR NEXT" or other loop structures in higher level languages).

1.6.4 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.6.5 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-mapped registers allow designers to optimize the precise implementation of certain specific instructions.

1.7 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increase device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins.

National Semiconductor

PRELIMINARY

COP8CFE9
8-Bit CMOS Flash Microcontroller with 8k Memory, Virtual EEPROM, and 10-Bit A/D

General Description

The COP8CFE9 Flash microcontroller is a highly integrated COP8™ Feature core device, with 8k Flash memory and advanced features including Virtual EEPROM, A/D, and High Speed Timers. This single-chip CMOS device is suited for applications requiring a full featured, in-system reprogrammable controller with large memory and low EMI. The same device is used for development, pre-production and volume production with a range of COP8 software and hardware development tools.

Device included in this datasheet:

Device	Flash Program Memory (bytes)	RAM (bytes)	Brownout Voltage	I/O Pins	Packages	Temperature
COP8CFE9	8k	256	No Brownout	37, 39	44 LLP, 44 PLCC, 48 TSSOP	−40°C to +85°C −40°C to +125°C

Features

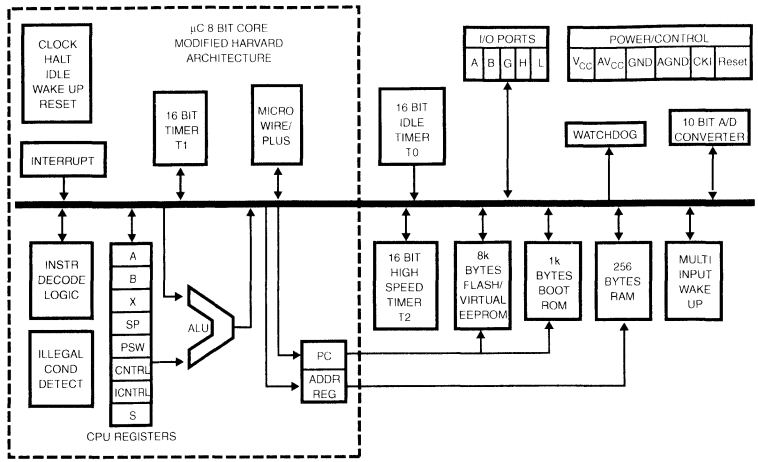
KEY FEATURES

- 8k bytes Flash Program Memory with Security Feature
- Virtual EEPROM using Flash Program Memory
- 256byte volatile RAM
- 10-bit Successive Approximation Analog to Digital Converter (up to 16 channels)
- 100% Precise Analog Emulation
- 2.7V – 5.5V In-System Programmability of Flash
- High endurance -100k Read/Write Cycles
- Superior Data Retention - 100 years
- HALT/IDLE Power Save Modes
- Two 16-bit timers:
  - — Timer T2 can operate at high speed (50 ns resolution)
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- High Current I/Os
  - — B0 – B3: 10 mA @ 0.3V
  - — All others: 10 mA @ 1.0V

OTHER FEATURES

- Single supply operation:
  - — 2.7V–5.5V (−40°C to +85°C)
  - — 4.5V–5.5V (−40°C to +125°C)
- Quiet Design (low radiated emissions)
- Multi-Input Wake-up with optional interrupts
- MICROWIRE/PLUS (Serial Peripheral Interface Compatible)
- Nine multi-source vectored interrupts servicing:
  - — External Interrupt
  - — Idle Timer T0
  - — Two Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS Serial peripheral interface
  - — Multi-Input Wake-up
  - — Software Trap
- Idle Timer with programmable interrupt interval
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options
  - — TRI-STATE Output/High Impedance Input
  - — Push-Pull Output
  - — Weak Pull Up Input
- Schmitt trigger inputs on I/O ports
- Temperature range: −40°C to +85°C and −40°C to +125°C
- Packaging: 44 PLCC, 44 LLP and 48 TSSOP

Block Diagram



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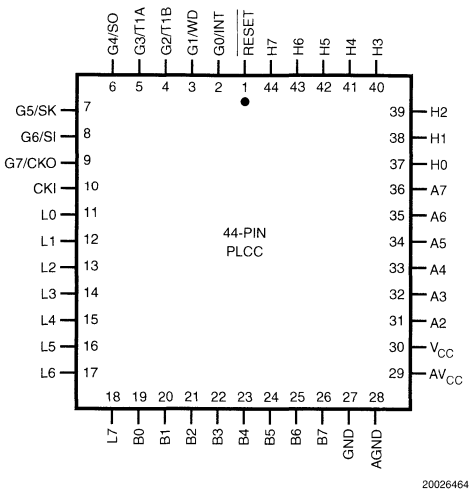
Ordering Information

Part Numbering Scheme

COP8	CF	E	9	H	VA	8
	Family and Feature Set Indicator	Program Memory Size	Program Memory Type	No. Of Pins	Package Type	Temperature
		E = 8k	9 = Flash	H = 44 Pin I = 48 Pin	LQ = LLP MT = TSSOP VA = PLCC	7 = -40 to +125˚C 8 = -40 to +85˚C

Connection Diagrams



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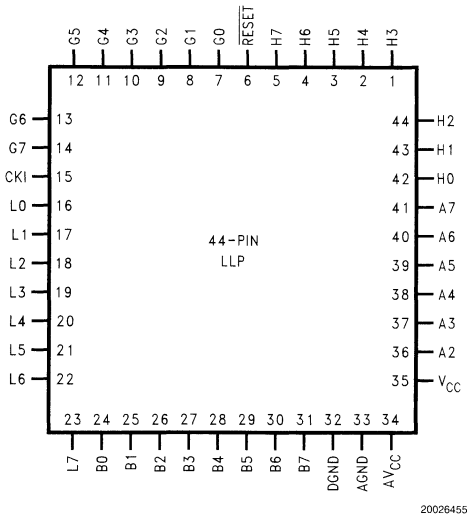
Top View
Plastic Chip Package
See NS Package Number V44A



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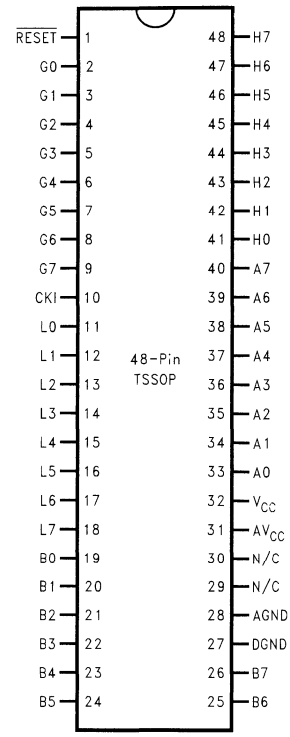
Top View
LLP Package
See NS Package Number LQA44A



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Top View
TSSOP Package
See NS Package Number MTD48

Pinouts for 44- and 48-Pin Packages

Port	Type	Alt. Function	In System Emulation Mode	44-Pin LLP	44-Pin PLCC	48-Pin TSSOP
L0	I/O	MIWU		16	11	11
L1	I/O	MIWU		17	12	12
L2	I/O	MIWU		18	13	13
L3	I/O	MIWU		19	14	14
L4	I/O	MIWU or T2A		20	15	15
L5	I/O	MIWU or T2B		21	16	16
L6	I/O	MIWU		22	17	17
L7	I/O	MIWU		23	18	18
G0	I/O	INT	Input	7	2	2
G1	I/O	WDOUT[a]	POUT	8	3	3
G2	I/O	T1B	Output	9	4	4
G3	I/O	T1A	Clock	10	5	5
G4	I/O	SO		11	6	6
G5	I/O	SK		12	7	7
G6	I	SI		13	8	8
G7	I	CKO		14	9	9
H0	I/O			42	37	41
H1	I/O			43	38	42
H2	I/O			44	39	43
H3	I/O			1	40	44
H4	I/O			2	41	45
H5	I/O			3	42	46
H6	I/O			4	43	47
H7	I/O			5	44	48
A0	I/O	ADCH0				33
A1	I/O	ADCH1				34
A2	I/O	ADCH2		36	31	35
A3	I/O	ADCH3		37	32	36
A4	I/O	ADCH4		38	33	37
A5	I/O	ADCH5		39	34	38
A6	I/O	ADCH6		40	35	39
A7	I/O	ADCH7		41	36	40
B0	I/O	ADCH8		24	19	19
B1	I/O	ADCH9		25	20	20
B2	I/O	ADCH10		26	21	21
B3	I/O	ADCH11		27	22	22
B4	I/O	ADCH12		28	23	23
B5	I/O	ADCH13 or A/D MUX OUT		29	24	24
B6	I/O	ADCH14 or A/D MUX OUT		30	25	25
B7	I/O	ADCH15 or A/DIN		31	26	26
DV_{CC}			V_{CC}	35	30	32
DGND			GND	32	27	27
AV_{CC}				34	29	31
AGND				33	28	28
CKI	I			15	10	10
$\overline{\text{RESET}}$	I		$\overline{\text{RESET}}$	6	1	1

a. G1 operation as WDOUT is controlled by Option Register bit 2.

1.0 General Description

1.1 EMI REDUCTION

The COP8CFE9 device incorporates circuitry that guards against electromagnetic interference - an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal Icc smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 IN-SYSTEM PROGRAMMING AND VIRTUAL EEPROM

The device includes a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize in system software update capability if MICROWIRE/PLUS is not desired.

Additional functions will copy blocks of data between the RAM and the Flash Memory. These functions provide a virtual EEPROM capability by allowing the user to emulate a variable amount of EEPROM by initializing nonvolatile variables from the Flash Memory and occasionally restoring these variables to the Flash Memory.

The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins. For further information on the FLEX bit, refer to Section 4.5, Option Register.

1.3 TRUE IN-SYSTEM EMULATION

On-chip emulation capability has been added which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

1.4 ARCHITECTURE

The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM or EPROM, while data memory is usually RAM. Consequently constant data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.5 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set - one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM, OTP or Flash). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.5.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

1.5.2 Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

1.6.3 Many Single-Byte, Multi-Function Instructions

The COP8 instruction set utilizes many single-byte, multi-function instructions. This enables a single instruction to accomplish multiple functions, such as DRSZ, DCOR, JID, LD (Load) and X (Exchange) instructions with post-incrementing and post-decrementing, to name just a few examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (simplifying "FOR NEXT" or other loop structures in higher level languages).

1.0 General Description (Continued)

1.5.4 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.5.5 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-mapped registers allow designers to optimize the precise implementation of certain specific instructions.

1.6 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increase device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins.

National Semiconductor

PRELIMINARY

COP8AME9/COP8ANE9
8-Bit CMOS Flash Microcontroller with 8k Memory, Dual Op Amps, Virtual EEPROM, Temperature Sensor, 10-Bit A/D and Brownout Reset

General Description

The COP8AME9/ANE9 Flash microcontrollers are highly integrated COP8™ Feature core devices, with 8k Flash memory and advanced features including Virtual EEPROM, dual Op Amps (one programmable gain), temperature sensor, A/D, High Speed Timers, USART, and Brownout Reset. The COP8AME9/ANE9 have True In-System Programmable Flash memory with high-endurance (100k erase/write cycles), and are well suited for applications requiring real-time data collection and processing, multiple sensory interface, and remote monitoring. The same device is used for development, pre-production and volume production with a range of COP8 software and hardware development tools.

Device included in this datasheet:

Device	Flash Program Memory (bytes)	RAM (bytes)	Brownout Voltage	I/O Pins	Packages	Temperature
COP8AME9	8k	512	4.17 to 4.5V	21	28 DIP/SOIC	−40°C to +85°C −40°C to +125°C
COP8ANE9	8k	512	No Brownout	21	28 DIP/SOIC	−40°C to +85°C −40°C to +125°C

Features

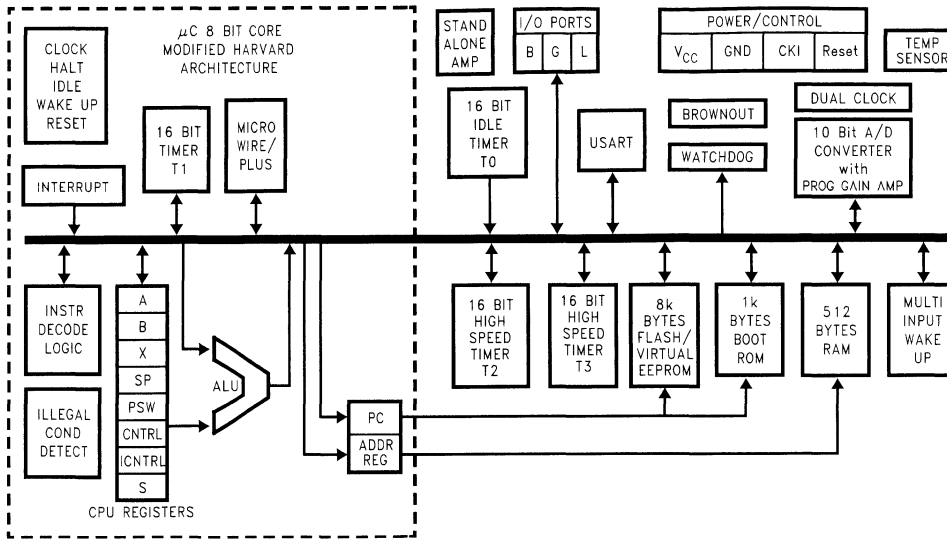
KEY FEATURES

- 8 kbytes Flash Program Memory with High Security
- 512 bytes SRAM
- 10-bit Successive Approximation Analog to Digital Converter (up to 6 external channels)
- Op Amps Specification:
  - — One programmable gain (1, 2, 5, 10, 20, 49, 98) with adjustable offset voltage nulling
  - — One general purpose with all I/O terminals accessible
  - — 1 MHz GBW
  - — Low offset voltage
  - — High input impedance
  - — Rail-to-rail input/output
- Temperature Sensing Diode
- True In-System Programmability of Flash Memory with 100k erase/write cycles
- Dual Clock Operation providing Enhanced Power Save Modes – HALT/IDLE
- 100% Precise Analog Emulation
- Single supply operation: 4.5V–5.5V
- Three 16-bit timers:
  - — Timers T2 and T3 can operate at 50 ns resolution
  - — Processor Independent PWM mode
  - — External Event counter mode
  - — Input Capture mode
- Brownout Reset (COP8AME9)
- 20 high-sink current I/Os
- USART
- Virtual EEPROM using Flash Program Memory
- 7 input analog MUX with selectable output destination

OTHER FEATURES

- Quiet Design (low radiated emissions)
- Multi-Input Wake-up with optional interrupts
- MICROWIRE/PLUS (Serial Peripheral Interface Compatible)
- Clock Doubler for 20 MHz operation from 10 MHz Oscillator
- Thirteen multi-source vectored interrupts servicing:
  - — External Interrupt
  - — USART (2)
  - — Idle Timer T0
  - — Three Timers (each with 2 interrupts)
  - — MICROWIRE/PLUS Serial peripheral interface
  - — Multi-Input Wake-Up
  - — Software Trap
- Idle Timer with programmable interrupt interval
- 8-bit Stack Pointer SP (stack in RAM)
- Two 8-bit Register Indirect Data Memory Pointers
- True bit manipulation
- WATCHDOG and Clock Monitor logic
- Software selectable I/O options
  - — TRI-STATE Output/High Impedance Input
  - — Push-Pull Output
  - — Weak Pull Up Input
- Schmitt trigger inputs on I/O ports
- Temperature range: −40°C to +85°C, −40°C to +125°C
- Packaging: 28 DIP, and 28 SOIC

Block Diagram



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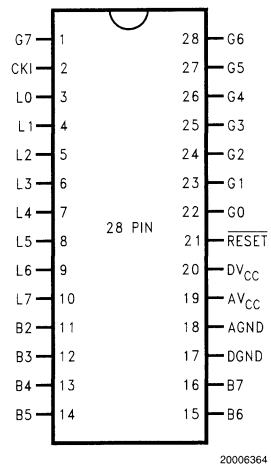
Connection Diagram



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Top View
See NS Package Number M28B or N28B

Pinouts for 28-Pin Packages

Port	Type	Alt. Fun	In System Emulation Mode	28-Pin DIP/SOIC
L0	I/O	MIWU or Low Speed OSC In		3
L1	I/O	MIWU or CKX or Low Speed OSC Out		4
L2	I/O	MIWU or TDX		5
L3	I/O	MIWU or RDX		6
L4	I/O	MIWU or T2A		7
L5	I/O	MIWU or T2B		8
L6	I/O	MIWU or T3A		9
L7	I/O	MIWU or T3B		10
G0	I/O	INT	Input	22
G1	I/O	WDOUT[a]	POUT	23
G2	I/O	T1B	Output	24
G3	I/O	T1A	Clock	25
G4	I/O	SO		26
G5	I/O	SK		27
G6	I	SI		28
G7	I	CKO		1
B2	I/O	ADCH10		11
B3	I/O	ADCH11 or AMP1 Output		12
B4	I/O	ADCH12 or AMP1 – Input		13
B5	I/O	ADCH13 or AMP1 + Input		14
B6	I/O	ADCH14 or A/D MUX OUT		15
B7	I/O	ADCH15 or A/D IN		16
DV_{CC}			V_{CC}	20
DGND			GND	17
AV_{CC}				19
AGND				18
CKI	I			2
$\overline{RESET}$	I		$\overline{RESET}$	21

a. G1 operation as WDOUT is controlled by Option Register bit 2.

Ordering Information

Part Numbering Scheme

COP8	AM	E	9	E	NA	8
	Family and Feature Set Indicator	Program Memory Size	Program Memory Type	No. Of Pins	Package Type	Temperature
	AM = 4.17V - 4.5V Brownout AN = No Brownout	E = 8k	9 = Flash	E = 28 Pin	NA = DIP MW = SOIC	7 = -40 to +125˚C 8 = -40 to +85˚C

1.0 General Description

1.1 EMI REDUCTION

The COP8AME9/ANE9 devices incorporate circuitry that guards against electromagnetic interference - an increasing problem in today's microcontroller board designs. National's patented EMI reduction technology offers low EMI clock circuitry, gradual turn-on output drivers (GTOs) and internal Icc smoothing filters, to help circumvent many of the EMI issues influencing embedded control designs. National has achieved 15 dB–20 dB reduction in EMI transmissions when designs have incorporated its patented EMI reducing circuitry.

1.2 IN-SYSTEM PROGRAMMING AND VIRTUAL EEPROM

The device includes a program in a boot ROM that provides the capability, through the MICROWIRE/PLUS serial interface, to erase, program and read the contents of the Flash memory.

Additional routines are included in the boot ROM, which can be called by the user program, to enable the user to customize in system software update capability if MICROWIRE/PLUS is not desired.

Additional functions will copy blocks of data between the RAM and the Flash Memory. These functions provide a virtual EEPROM capability by allowing the user to emulate a variable amount of EEPROM by initializing nonvolatile variables from the Flash Memory and occasionally restoring these variables to the Flash Memory.

The contents of the boot ROM have been defined by National. Execution of code from the boot ROM is dependent on the state of the FLEX bit in the Option Register on exit from RESET. If the FLEX bit is a zero, the Flash Memory is assumed to be empty and execution from the boot ROM begins. For further information on the FLEX bit, refer to Section 4.5, Option Register.

1.3 DUAL CLOCK AND CLOCK DOUBLER

The device includes a versatile clocking system and two oscillator circuits designed to drive a crystal or ceramic resonator. The primary oscillator operates at high speed up to 10 MHz. The secondary oscillator is optimized for operation at 32.768 kHz.

The user can, through specified transition sequences (please refer to *7.0 Power Saving Features*), switch execution between the high speed and low speed oscillators. The unused oscillator can then be turned off to minimize power dissipation. If the low speed oscillator is not used, the pins are available as general purpose bidirectional ports.

The operation of the CPU will use a clock at twice the frequency of the selected oscillator (up to 20 MHz for high speed operation and 65.536 kHz for low speed operation). This doubled clock will be referred to in this document as 'MCLK'. The frequency of the selected oscillator will be referred to as CKI. Instruction execution occurs at one tenth the selected MCLK rate.

1.4 TRUE IN-SYSTEM EMULATION

On-chip emulation capability has been added which allows the user to perform true in-system emulation using final production boards and devices. This simplifies testing and evaluation of software in real environmental conditions. The user, merely by providing for a standard connector which can be bypassed by jumpers on the final application board, can provide for software and hardware debugging using actual production units.

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The COP8 family is based on a modified Harvard architecture, which allows data tables to be accessed directly from program memory. This is very important with modern microcontroller-based applications, since program memory is usually ROM, EPROM or Flash, while data memory is usually RAM. Consequently constant data tables need to be contained in non-volatile memory, so they are not lost when the microcontroller is powered down. In a modified Harvard architecture, instruction fetch and memory data transfers can be overlapped with a two stage pipeline, which allows the next instruction to be fetched from program memory while the current instruction is being executed using data memory. This is not possible with a Von Neumann single-address bus architecture.

The COP8 family supports a software stack scheme that allows the user to incorporate many subroutine calls. This capability is important when using High Level Languages. With a hardware stack, the user is limited to a small fixed number of stack levels.

1.6 INSTRUCTION SET

In today's 8-bit microcontroller application arena cost/performance, flexibility and time to market are several of the key issues that system designers face in attempting to build well-engineered products that compete in the marketplace. Many of these issues can be addressed through the manner in which a microcontroller's instruction set handles processing tasks. And that's why the COP8 family offers a unique and code-efficient instruction set - one that provides the flexibility, functionality, reduced costs and faster time to market that today's microcontroller based products require.

Code efficiency is important because it enables designers to pack more on-chip functionality into less program memory space (ROM, OTP or Flash). Selecting a microcontroller with less program memory size translates into lower system costs, and the added security of knowing that more code can be packed into the available program memory space.

1.6.1 Key Instruction Set Features

The COP8 family incorporates a unique combination of instruction set features, which provide designers with optimum code efficiency and program memory utilization.

1.6.2 Single Byte/Single Cycle Code Execution

The efficiency is due to the fact that the majority of instructions are of the single byte variety, resulting in minimum program space. Because compact code does not occupy a substantial amount of program memory space, designers can integrate additional features and functionality into the microcontroller program memory space. Also, the majority instructions executed by the device are single cycle, resulting in minimum program execution time. In fact, 77% of the instructions are single byte single cycle, providing greater code and I/O efficiency, and faster code execution.

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1.0 General Description (Continued)

examples. In many cases, the instruction set can simultaneously execute as many as three functions with the same single-byte instruction.

JID: (Jump Indirect); Single byte instruction decodes external events and jumps to corresponding service routines (analogous to "DO CASE" statements in higher level languages).

LAID: (Load Accumulator-Indirect); Single byte look up table instruction provides efficient data path from the program memory to the CPU. This instruction can be used for table lookup and to read the entire program memory for checksum calculations.

RETSK: (Return Skip); Single byte instruction allows return from subroutine and skips next instruction. Decision to branch can be made in the subroutine itself, saving code.

AUTOINC/DEC: (Auto-Increment/Auto-Decrement); These instructions use the two memory pointers B and X to efficiently process a block of data (simplifying "FOR NEXT" or other loop structures in higher level languages).

1.6.4 Bit-Level Control

Bit-level control over many of the microcontroller's I/O ports provides a flexible means to ease layout concerns and save board space. All members of the COP8 family provide the ability to set, reset and test any individual bit in the data memory address space, including memory-mapped I/O ports and associated registers.

1.6.5 Register Set

Three memory-mapped pointers handle register indirect addressing and software stack pointer functions. The memory data pointers allow the option of post-incrementing or post-decrementing with the data movement instructions (LOAD/EXCHANGE). And 15 memory-mapped registers allow designers to optimize the precise implementation of certain specific instructions.

1.7 PACKAGING/PIN EFFICIENCY

Real estate and board configuration considerations demand maximum space and pin efficiency, particularly given today's high integration and small product form factors. Microcontroller users try to avoid using large packages to get the I/O needed. Large packages take valuable board space and increases device cost, two trade-offs that microcontroller designs can ill afford.

The COP8 family offers a wide range of packages and does not waste pins: up to 85.7% are devoted to useful I/O.

National Semiconductor

16-Bit Microcontrollers

National Semiconductor

The 16-bit CR16 Family

Key Features

CPU Features

- Fully static core, capable of operating at any rate from 0 to 25 MHz (4 MHz minimum in active mode)
- 50 ns instruction cycle time with a 25 MHz external clock frequency
- Full CAN class, CAN serial interface for low/high speed applications with 15 orthogonal message buffers, each supporting standard, as well as extended message identifiers
- Multi-source vectored interrupts (internal, external, and on-chip peripheral)
- Dual clock modes
- On-chip power-on reset

On-Chip Memory

- Up to 64k bytes flash program memory; can be programmed, erased, and reprogrammed by software
- 3K bytes of SRAM
- 1.5k bytes flash memory to store boot loader code
- Up to 2k bytes of flash based data memory with low endurance (25K cycles) and 128 bytes with high endurance (100K cycles)

On-Chip Peripherals

- Two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) devices
- Programmable Idle Timer and real-time timer (T0)
- Two dual 16-bit multi-function timers (MFT1 and MFT2)
- 8/16-bit SPI/MICROWIRE-PLUS serial interface
- 12-channel, 8-bit Analog-to-Digital (A/D) converter with external voltage reference, programmable sample-and-hold delay, and programmable conversion frequency
- ACCESS. Bus synchronous serial bus
- Full CAN interface with 15 message buffers complaint to CAN specification 2.0B active
- Versatile Timer Unit with four subsystems (VTU)
- Two analog comparators
- Integrated WATCHDOG logic
- Multi input Wakeup feature
- Integrated Power management function

I/O Features

- Up to 56 general-purpose I/O pins (shared with on-chip peripheral I/O pins)
- Programmable I/O pin characteristics: TRI-STATE output, push-pull output, weak pull-up input, high-impedance input
- Schmitt triggers on inputs
- 4.5V to 5.5V single-supply operation

Temperature Range

- -40˚C to +85˚C
- -40˚C to +125˚C

Package Types

- 80 Lead PQFP Package (14mm*14mm*2mm)
- 44 Lead PLCC Package

Security Features

Program Memory Security Features

The program memory has security features to prevent unauthorized access to the program code and unintentional programming. These features are invoked by programming a non-volatile control register, the Flash EEPROM Security (FLSEC) register. This register contains a read-access control bit and a write-access control bit.

Protection Features

The last byte of the ISP memory is reserved for special functions and provide memory protection and security for the flash EEPROM program memory. Read and write protection is provided.

Memory Protection Features

The 48 kbytes of flash program memory used to store the application program has security features to prevent unintentional programming and to prevent unauthorized access to the program code.

WATCHDOG

The Watchdog is designed to detect program execution errors such as an infinite loop or a 'runaway' program.

ESD Protection

A patented ESD (Electro Static Discharge) protection circuit makes the CR16 family robust to greater than 2000 V (Human body model).

Low EMI

National's EMI (Electromagnetic Interference) reduction technology, covered by three patents, minimizes the EMI of the CR16 family of microcontrollers.

Introduction to the CR16 16-bit Microcontroller Family

The CR16 (CompactRISC) microcontroller is a complete microcomputer with all system timing, interrupt logic, program memory, data memory, and I/O ports included on-chip, making it well-suited to a wide range of embedded controller applications. The family is divided into two groups of products; CAN Interface products and Multi-purpose products. The key differentiators are:

Feature (Max Option)	CAN Interface Series	Multi-Purpose Series
Clock Speed	25 MHz	20 MHz
Flash / ROM	64K	48K
SRAM	3K	2K
EEPROM Data Memory	2176 bytes	640 bytes
8 bit ADC Channels	12	8

Architecture

CompactRISC processor cores are designed specifically for embedded applications. The CompactRISC architecture is available in a wide range of implementations, supported by a common set of software development tools from multiple vendors. The CompactRISC architecture is scalable over a range of 8-, 16-, 32- and 64- bit processors, with common: variable-length instruction set, registers, addressing modes, interrupt and trap handling, debug support, and non-aligned data accesses, and efficient HLL execution.

Modular Extensions

The CompactRISC architecture was designed to be easily extensible. This means that specialized functions needed by specific applications can be easily added to a single-chip design. A modular internal bus provides predefined processor and I/O interfaces to the core bus and the peripheral bus. These buses are designed for maximum flexibility. The core bus is a high-speed bus and can be used to connect performance-demanding functions to the CPU such as fast on-chip memory, DMA channels, and additional coprocessor units such as DSP. The peripheral bus is a simple, lower-speed bus for less demanding peripherals such as counters, timers, PWM lines and Microwire™ serial interfaces. Using a 'template' approach, it is easy to create small, cost-effective custom systems. It is also easy to expand the functionality of CompactRISC core-based systems to include any number of application-specific features.

- Available in Synethesizeable Verilog HDL
- Less than 1mm 2 @ 0.35µ
- 2Mbytes of linear address space
- Less than 0.3mA per MHZ @ 3 Volts, 0.35µ
- Static 0 to 50 Megahertz
- Atomic Memory Direct Bit Manipulation of single bits
- Save and Restore of Multiple Registers
- Push and Pop of Multiple Registers
- Hardware Multiplier Unit for fast 16-bit multiplication

National Semiconductor

CR16HCS5/CR16HCS9/CR16MAR5/CR16MAS5/ CR16MAS9/CR16MBR5/CR16MCS5/CR16MCS9 Family of 16-bit CAN-enabled CompactRISC Microcontrollers

General Description

The family of 16-bit CompactRISC™ microcontroller is based on a Reduced Instruction Set Computer (RISC) architecture. The device operates as a complete microcomputer with all system timing, interrupt logic, flash program memory or ROM memory, RAM, EEPROM data memory, and I/O ports included on-chip. It is ideally suited to a wide range of embedded controller applications because of its high performance, on-chip integrated features and low power consumption resulting in decreased system cost.

The device offers the high performance of a RISC architecture while retaining the advantages of a traditional Complex Instruction Set Computer (CISC): compact code, on-chip memory and I/O, and reduced cost. The CPU uses a three-stage instruction pipeline that allows execution of up to one instruction per clock cycle, or up to 25 million instructions per second (MIPS) at a clock rate of 24 MHz.

The device contains a FullCAN class, CAN serial interface for low/high speed applications with 15 orthogonal message buffers, each supporting standard as well as extended message identifiers.

The device has up to 64K bytes of reprogrammable flash EEPROM program memory or ROM memory, 1.5K bytes of flash EEPROM In-System-Programming memory, 3K bytes of static RAM, 2K bytes of non-volatile EEPROM data memory and 128 bytes with high endurance, two USARTs, two 16-bit multi-function timers, one SPI/MICROWIRE-PLUS™ serial interface, a 12-channel A/D converter, two analog comparators, WATCHDOG™ protection mechanism, and up to 56 general-purpose I/O pins.

The device operates with a high-frequency crystal as the main clock source and either the prescaled main clock source or with a low frequency (32.768 kHz) oscillator in Power Save mode. The device supports several Power Save modes which are combined with multi-source interrupt and wake-up capabilities. This device also has a Versatile Timer Unit (VTU) with four timer sub-systems, a CAN interface, and ACCESS.bus synchronous serial bus interface.

Powerful cross-development tools are available from National Semiconductor and third party suppliers to support the development and debugging of application software for the device. These tools let you program the application software in C and are designed to take full advantage of the CompactRISC architecture.

In the following text, device is always referred to the family of 16-bit CAN-enabled CompactRISC Microcontroller.

Please check the web for the latest update to this datasheet.

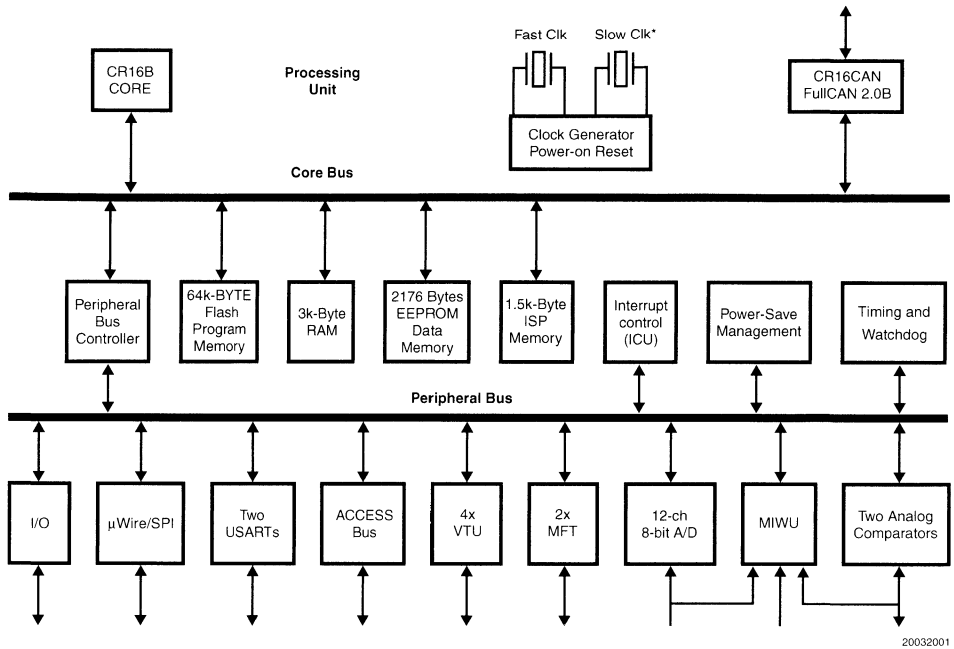
Features

- CPU Features
  - Fully static core, capable of operating at any rate from 0 to 24 MHz (4 MHz minimum in active mode)
  - Multi-source vectored interrupts (internal, external, and on-chip peripheral)
  - Dual clock and reset
- On-chip power-on reset
- On-Chip Memory
  - Up to 64 kbytes flash EEPROM program memory; can be programmed, erased, and reprogrammed by software (100 kcycles)
  - 3 kbytes of static RAM data memory
  - For flash program memory devices, 1.5 kbytes flash EEPROM memory is available to store boot loader code (100 kcycles)
  - 2 kbytes of non-volatile EEPROM data memory with low endurance (25 kcycles) and 128 bytes with high endurance (100 kcycles)
- On-Chip Peripherals
  - Two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) devices
  - Programmable Idle Timer and real-time clock (T0)
  - Two dual 16-bit multi-function timers (MFT1 and MFT2)
  - 8/16-bit SPI/MICROWIRE-PLUS serial interface
  - 12-channel, 8-bit Analog-to-Digital (A/D) converter with external voltage reference, programmable sample-and-hold delay, and programmable conversion frequency
  - ACCESS.bus synchronous serial bus
  - FullCAN interface with 15 message buffers complaint to CAN specification 2.0B active
  - Versatile Timer Unit with four subsystems (VTU)
  - Two analog comparators
  - Integrated WATCHDOG logic
- I/O Features
  - Up to 56 general-purpose I/O pins (shared with on-chip peripheral I/O pins)
  - Programmable I/O pin characteristics: TRI-STATE output, push-pull output, weak pull-up input, high-impedance input
  - Schmitt triggers on general purpose inputs
- Power Supply
  - 4.5V to 5.5V single-supply operation
- Temperature Range
  - −40°C to +85°C
  - −40°C to +125°C

Features (Continued)

- Development Support
  - — Real-time emulation and full program debug capabilities available
  - — CompactRISC tools provide C programming and debugging support

Block Diagram



National Semiconductor

CR16MES5/CR16MES9/CR16MFS5/CR16MFS9/ CR16MHS5/CR16MHS9/CR16MNS5/CR16MNS9/ CR16MPS5/CR16MUS5/CR16MUS9 CompactRISC 16-Bit Microcontrollers

General Description

The family of CompactRISC™ microcontrollers are general-purpose 16-bit microcontrollers based on a Reduced Instruction Set Computer (RISC) architecture. The device operates as a complete microcomputer with all system timing, interrupt logic, flash program memory or ROM memory, RAM, EEPROM data memory, and I/O ports included on-chip. It is ideally suited to a wide range of embedded controller applications because of its high performance, on-chip integrated features and low power consumption, resulting in decreased system cost.

The family of CompactRISC 16-bit microcontrollers offer the high performance of a RISC architecture while retaining the advantages of a traditional Complex Instruction Set Computer (CISC): compact code, on-chip memory and I/O, and reduced cost. The CPU uses a three-stage instruction pipeline that allows execution of up to one instruction per clock cycle, or up to 20 million instructions per second (MIPS) at a clock rate of 24MHz.

In the following text, device is alsays refered to the family of CompactRISC 16-bit microcontrollers. For the exact feature set, check individual datasheets.

The device is available in a variety of package sizes and types. All devices have 48 kbytes of reprogrammable flash program memory, 1.5 kbytes of ISP memory, 2 kbytes of static RAM, and 640 bytes of non-volatile EEPROM data memory. The 80-pin device has two USARTs, two 16-bit multi-function timers, one SPI/MICROWIRE-PLUS™ serial interface, an 8-channel A/D converter, two analog comparators, WATCHDOG™ protection mechanism, and up to 48 general-purpose I/O pins. The 44-pin devices offer the same basic features as the 80-pin device, but with fewer I/O ports and peripheral modules due to the smaller number of available pins.

All devices operate with a high-frequency crystal as the main clock source. Some packages allow the device to operate with either the main clock source or with a slow (32.768 KHz) oscillator in Power Save mode. The device supports several Power Save modes which are combined with multi-source interrupt and wake-up capabilities.

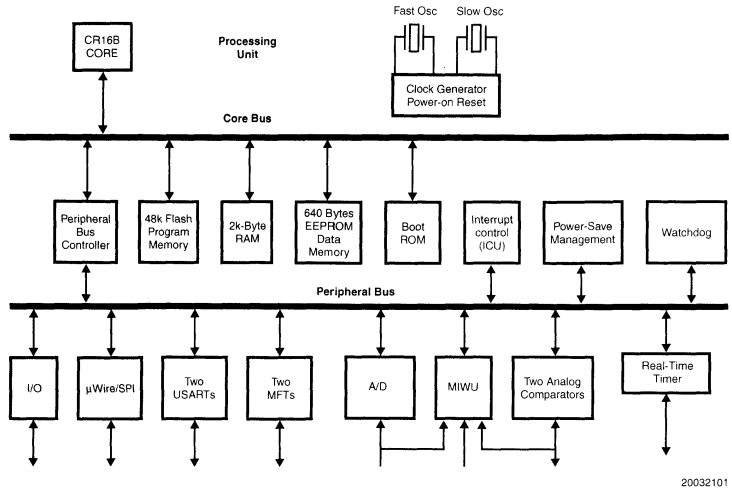
Powerful cross-development tools are available from National Semiconductor and third party suppliers to support the development and debugging of application software for the device. These tools let you program the application software in C and are designed to take full advantage of the CompactRISC architecture.

Please check the web for the latest update to this datasheet.

Features

- CPU Features
  - — Fully static core, capable of operating at any rate from 0 to 24MHz (4 MHz minimum in active mode)
  - — Multi-source vectored interrupts (internal, external, and on-chip peripheral)
  - — On-chip power-on reset
- On-Chip Memory
  - — 48 kbytes of flash program memory or ROM memory (100K cycle)
  - — 1.5 kbytes of ISP memory (100K cycle)
  - — 2 kbytes of static RAM data memory
  - — 640 bytes of non-volatile EEPROM data memory, word-programmable (100K cycle)
- On-Chip Peripherals
  - — Up to two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) devices
  - — Programmable Idle Timer and real-time clock (T0)
  - — Up to two dual 16-bit multi-function timers (MFT1 and MFT2)
  - — SPI/MICROWIRE-PLUS serial interface
  - — 8-channel, 8-bit Analog-to-Digital (A/D) converter with external voltage reference, programmable sample-and-hold delay, and programmable conversion frequency
  - — Up to two analog comparators
  - — Integrated WATCHDOG logic
- I/O Features
  - — Up to 48 general-purpose I/O pins (shared with on-chip peripheral I/O pins)
  - — Programmable I/O pin characteristics: TRI-STATE output, push-pull output, weak pull-up input, high-impedance input
  - — Software-configurable Schmitt triggers on inputs
- Power Supply
  - — 4.5V to 5.5V single-supply operation
- Temperature Range
  - — 0°C to +70°C
  - — −40°C to +85°C
  - — −40°C to +125°C
- Development Support
  - — Real-time emulation and full program debug capabilities available
  - — CompactRISC tools provide C programming and debugging support

Block Diagram



Section 4
Audio

Section 4 Contents

National Semiconductor

Audio Power Amplifiers

National Semiconductor

LM1875
20W Audio Power Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on ±25V supplies. Using an 8Ω load and ±30V supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

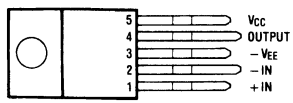
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion: 0.015%, 1 kHz, 20 W
- Wide power bandwidth: 70 kHz
- Protection for AC and DC short circuits to ground
- Thermal protection with parole circuit
- High current capability: 4A
- Wide supply range 16V-60V
- Internal output protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Connection Diagram

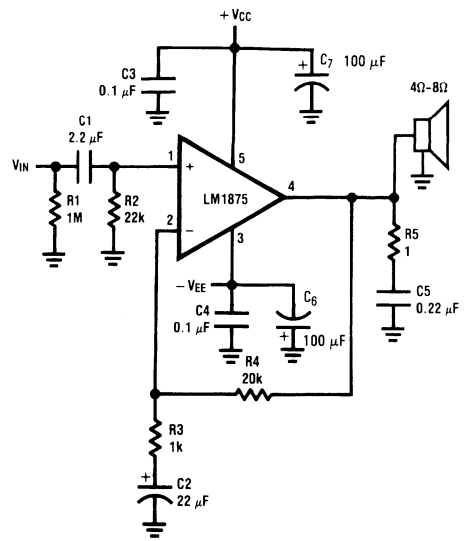


DS005030-1

Front View

Package	Ordering Info	NSC Package Number
For Straight Leads	LM1875T SL108949	T05A
For Stagger Bend	LM1875T LB03	T05D
For 90° Stagger Bend	LM1875T LB05	T05E
For 90° Stagger Bend	LM1875T LB02	TA05B

Typical Applications



DS005030-2

National Semiconductor

LM1876 *Overture*™ Audio Power Amplifier Series Dual 20W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM1876 is a stereo audio amplifier capable of delivering typically 20W per channel of continuous average output power into a 4Ω or 8Ω load with less than 0.1% THD+N.

Each amplifier has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM1876, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- THD+N at 1kHz at 2 x 15W continuous average output power into 4Ω or 8Ω: 0.1% (max)
- THD+N at 1kHz at continuous average output power of 2 x 20W into 8Ω: 0.009% (typ)
- Standby current: 4.2mA (typ)

Features

- SPiKe protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute mode
- Standby-mode
- Isolated 15-lead TO-220 package
- Non-Isolated 15-lead TO-220 package
- Wide supply range 20V - 64V

Applications

- High-end stereo TVs
- Component stereo
- Compact stereo

Typical Application

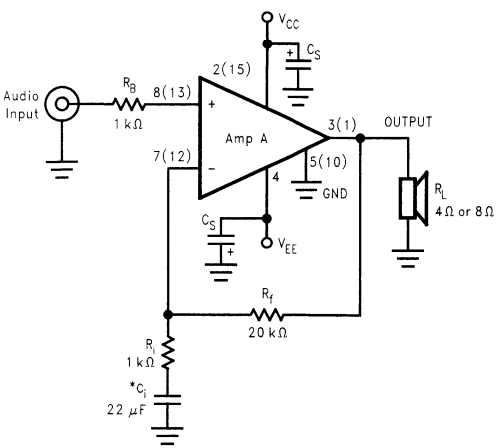


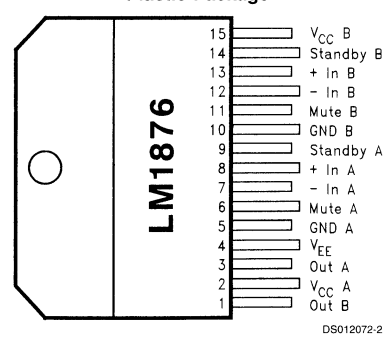
FIGURE 1. Typical Audio Amplifier Application Circuit

Note: Numbers in parentheses represent pinout for amplifier B.

*Optional component dependent upon specific design requirements.

Connection Diagram

Plastic Package



Top View
Isolated Package
Order Number LM1876TF
See NS Package Number TF15B
Non-Isolated Package
Order Number LM1876T
See NS Package Number TA15A

National Semiconductor

LM1877
Dual Audio Power Amplifier

General Description

The LM1877 is a monolithic dual power amplifier designed to deliver 2W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

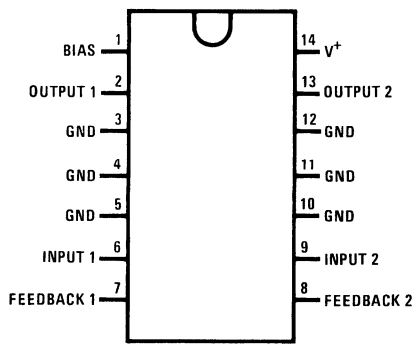
- 2W/channel
- −65 dB ripple rejection, output referred
- −65 dB channel separation, output referred
- Wide supply range, 6V–24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

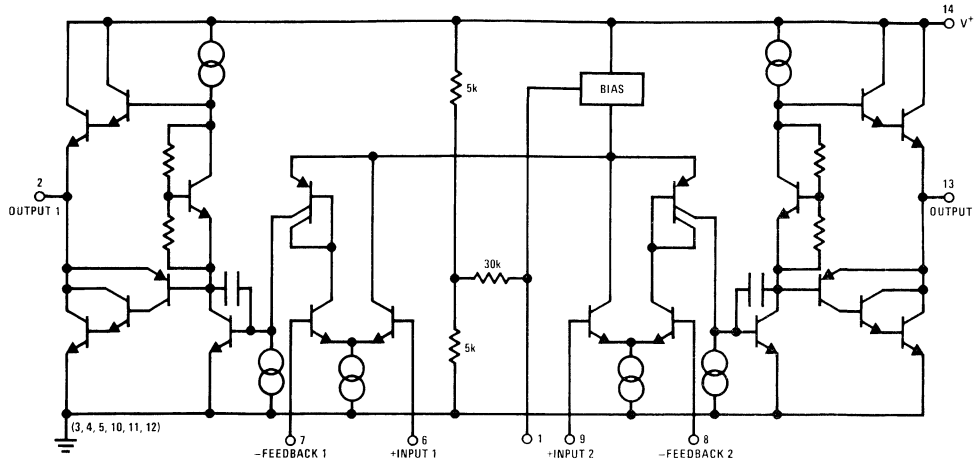
Connection Diagram

Dual-In-Line Package
or Surface Mount Package



Top View
Order Number LM1877M-9 or LM1877N-9
See NS Package Number M14B or N14A

Equivalent Schematic Diagram



DS007913-2

National Semiconductor

LM2876

Overture™ Audio Power Amplifier Series

High-Performance 40W Audio Power Amplifier w/Mute

General Description

The LM2876 is a high-performance audio power amplifier capable of delivering 40W of continuous average power to an 8Ω load with 0.1% THD+N from 20Hz–20kHz.

The performance of the LM2876, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM2876 maintains an excellent signal-to-noise ratio of greater than 95dB (min) with a typical low noise floor of 2.0μV. It exhibits extremely low THD+N values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

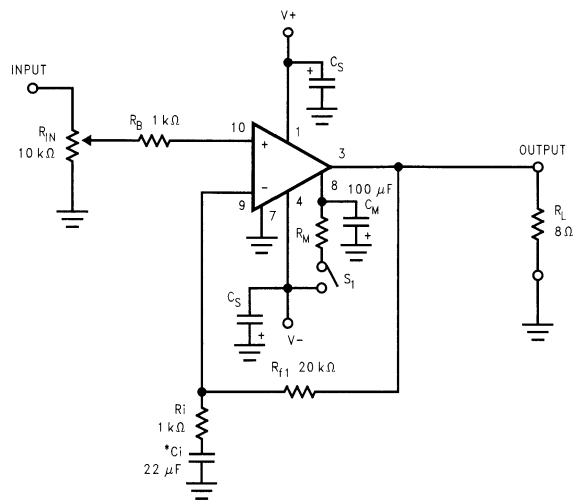
Features

- 40W continuous average output power into 8Ω
- 75W instantaneous peak output power capability
- Signal-to-Noise Ratio ≥ 95 dB(min)
- An input mute function
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11-lead TO-220 package
- Wide supply range 20V - 72V

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

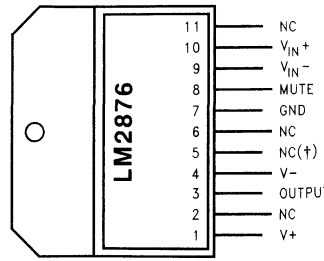
Typical Application



* Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram



DS011775-2

†Connect Pin 5 to V^+ for Compatibility with LM3886.
*Preliminary: Call your local National sales rep. or distributor for availability.

Top View
Order Number LM2876T
or LM2876TF
See NS Package Number TA11B for
Staggered Lead Non-Isolated
Package or TF11B* for
Staggered Lead Isolated Package

National Semiconductor

LM380
2.5W Audio Power Amplifier

General Description

The LM380 is a power audio amplifier for consumer applications. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows ground referenced input signals. The output automatically self-centers to one-half the supply voltage.

The output is short circuit proof with internal thermal limiting. The package outline is standard dual-in-line. The LM380N uses a copper lead frame. The center three pins on either side comprise a heat sink. This makes the device easy to use in standard PC layouts.

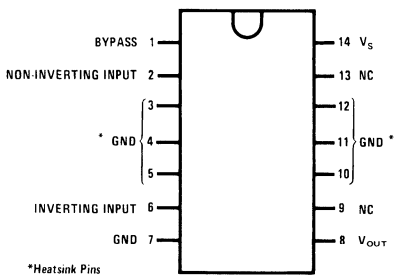
Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, small servo drivers, power converters, etc.

A selected part for more power on higher supply voltages is available as the LM384. For more information see AN-69.

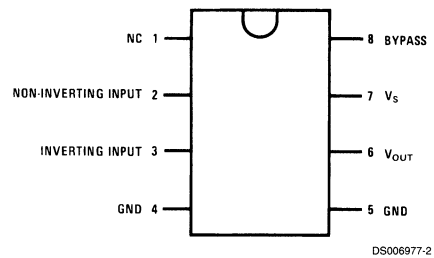
Features

- Wide supply voltage range: 10V-22V
- Low quiescent power drain: 0.13W (V_S= 18V)
- Voltage gain fixed at 50
- High peak current capability: 1.3A
- Input referenced to GND
- High input impedance: 150kΩ
- Low distortion
- Quiescent output voltage is at one-half of the supply voltage
- Standard dual-in-line package

Connection Diagrams (Dual-In-Line Packages, Top View)



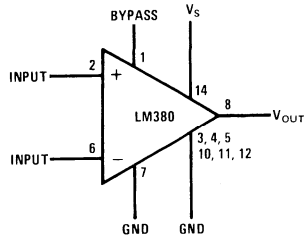
Order Number LM380N
See NS Package Number N14A



Order Number LM380N-8
See NS Package Number N08E

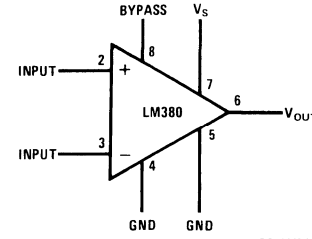
Block and Schematic Diagrams

LM380N

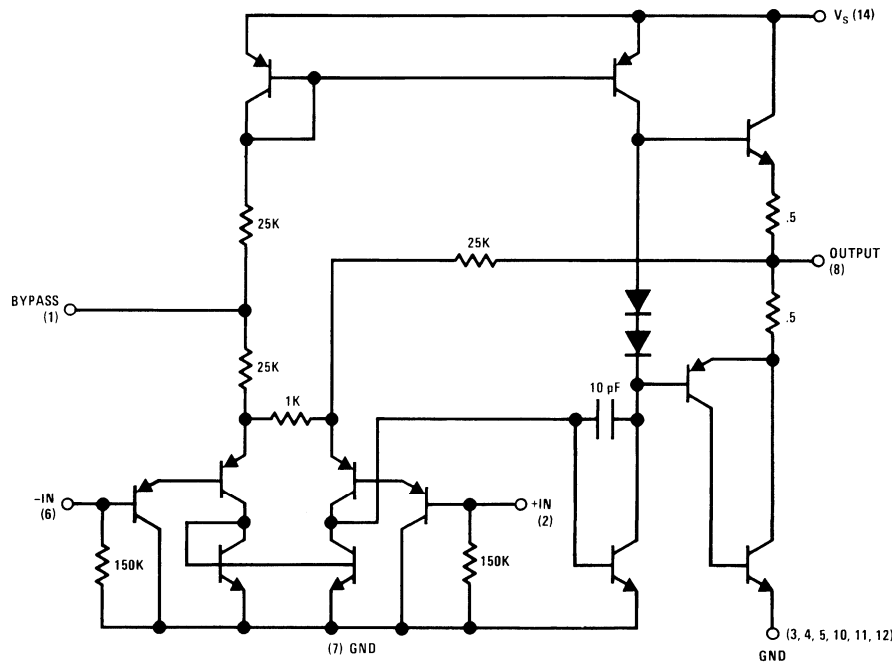


DS006977-3

LM380N-8



DS006977-4



DS006977-5

National Semiconductor

LM384
5W Audio Power Amplifier

General Description

The LM384 is a power audio amplifier for consumer applications. In order to hold system cost to a minimum, gain is internally fixed at 34 dB. A unique input stage allows ground referenced input signals. The output automatically self-centers to one-half the supply voltage.

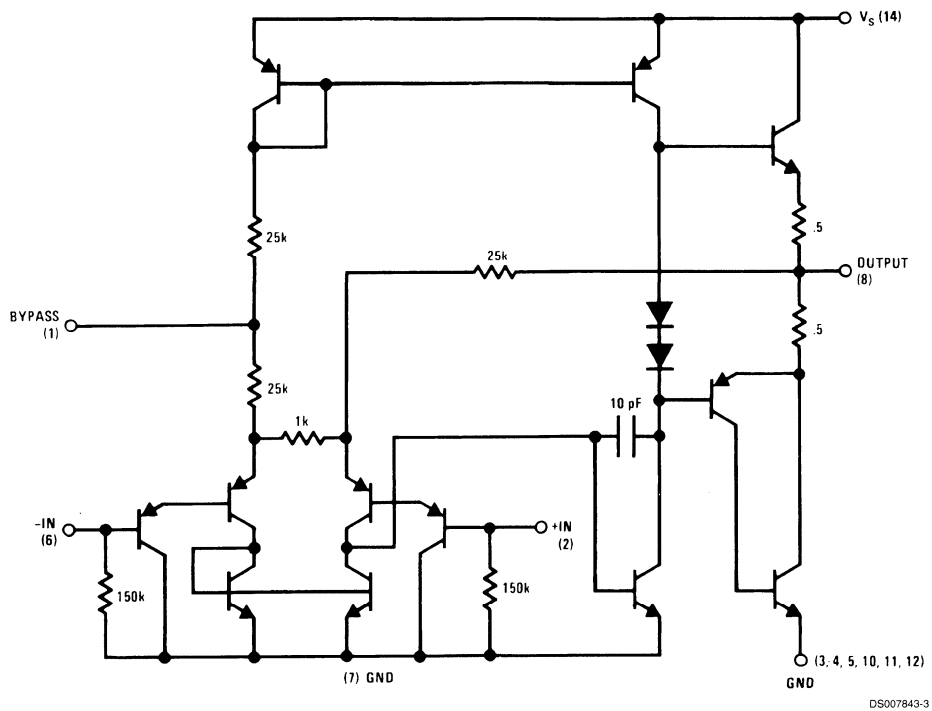
The output is short-circuit proof with internal thermal limiting. The package outline is standard dual-in-line. A copper lead frame is used with the center three pins on either side comprising a heat sink. This makes the device easy to use in standard p-c layout.

Uses include simple phonograph amplifiers, intercoms, line drivers, teaching machine outputs, alarms, ultrasonic drivers, TV sound systems, AM-FM radio, sound projector systems, etc. See AN-69 for circuit details.

Features

- Wide supply voltage range: 12V to 26V
- Low quiescent power drain
- Voltage gain fixed at 50
- High peak current capability: 1.3A
- Input referenced to GND
- High input impedance: 150kΩ
- Low distortion: 0.25% (P_O=4W, R_L=8Ω)
- Quiescent output voltage is at one half of the supply voltage
- Standard dual-in-line package

Schematic Diagram



National Semiconductor

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value from 20 to 200.

The inputs are ground referenced while the output automatically biases to one-half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

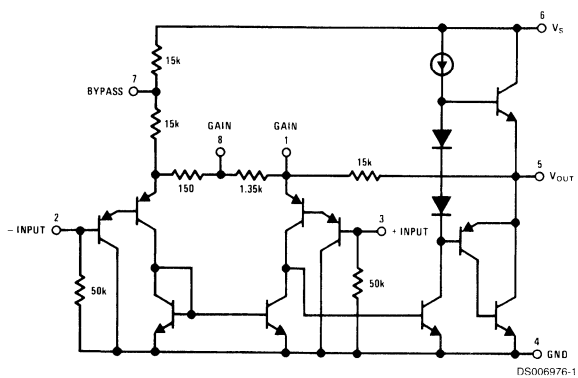
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

Applications

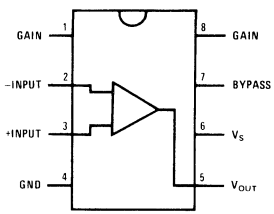
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



DS006976-2

Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

National Semiconductor

LM3875 *Overture*™ Audio Power Amplifier Series High-Performance 56W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% THD+N from 20Hz to 20kHz.

The performance of the LM3875, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, caused by shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3875 maintains an excellent signal-to-noise ratio of greater than 95dB(min) with a typical low noise floor of 2.0μV. It exhibits extremely low THD+N values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

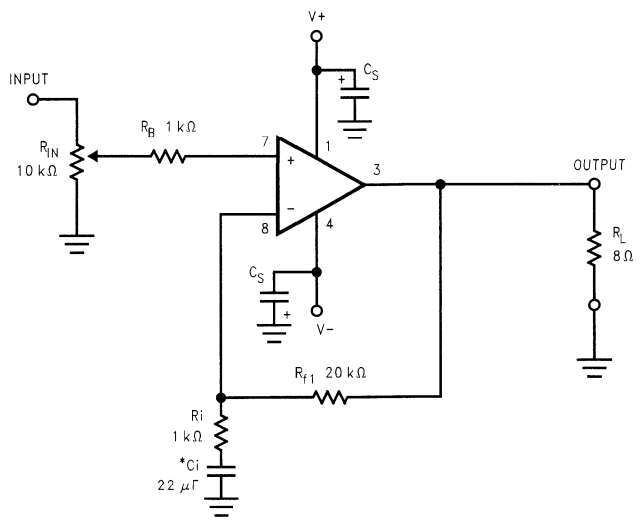
Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio >95dB (min)
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when |V+| + |V−| ≤ 12V, thus eliminating turn-on and turn-off transients
- 11 lead TO-220 package
- Wide supply voltage range: |V+| + |V−| = 20V to 84V

Applications

- Component or compact stereos
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

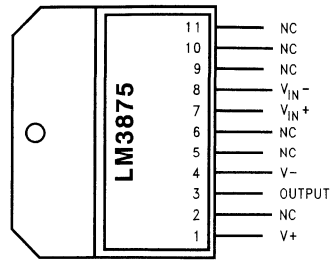


*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

FIGURE 1. Typical Audio Amplifier Application Circuit

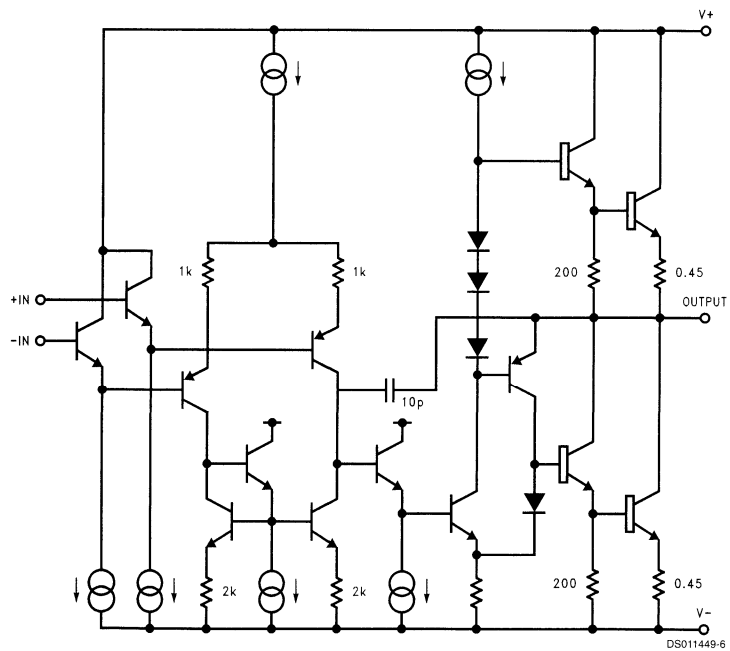
Connection Diagram

Plastic Package (Note 8)



Top View
Order Number LM3875T or LM3875TF
See NS Package Number TA11B for
Staggered Lead Non-Isolated Package
or TF11B for Staggered Lead Isolated Package

Equivalent Schematic (Excluding active protection circuitry)



National Semiconductor

LM3876 *Overture*™ Audio Power Amplifier Series High-Performance 56W Audio Power Amplifier w/Mute

General Description

The LM3876 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% THD+N from 20Hz–20kHz.

The performance of the LM3876, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3876 maintains an excellent signal-to-noise ratio of greater than 95dB (min) with a typical low noise floor of 2.0μV. It exhibits extremely low THD+N values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

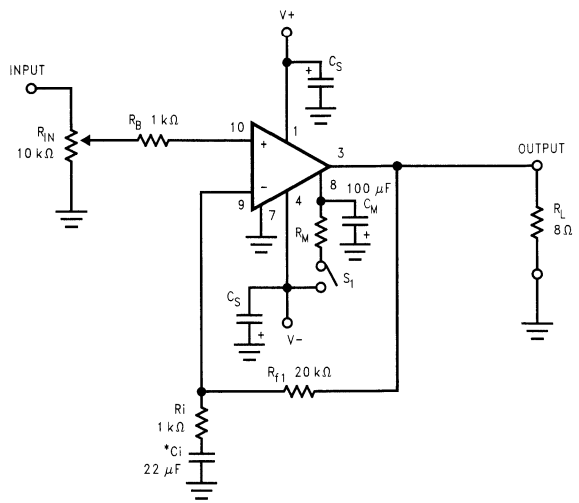
Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio ≥ 95 dB(min)
- An input mute function
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11-lead TO-220 package
- Wide supply range 20V - 94V

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

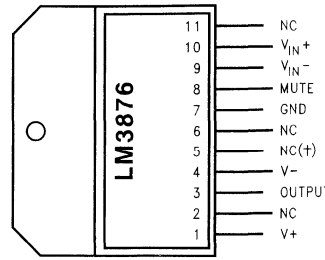


*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Plastic Package (Note 11)



DS011832-2

†Connect Pin 5 to V^+ for Compatibility with LM3886.

Top View
Order Number LM3876T
or LM3876TF
See NS Package Number TA11B for
Staggered Lead Non-Isolated
Package or TF11B for
Staggered Lead Isolated Package

National Semiconductor

LM3886 *Overture*™ Audio Power Amplifier Series High-Performance 68W Audio Power Amplifier w/Mute

General Description

The LM3886 is a high-performance audio power amplifier capable of delivering 68W of continuous average power to a 4Ω load and 38W into 8Ω with 0.1% THD+N from 20Hz–20kHz.

The performance of the LM3886, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3886 maintains an excellent signal-to-noise ratio of greater than 92dB with a typical low noise floor of 2.0μV. It exhibits extremely low THD+N values of 0.03% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

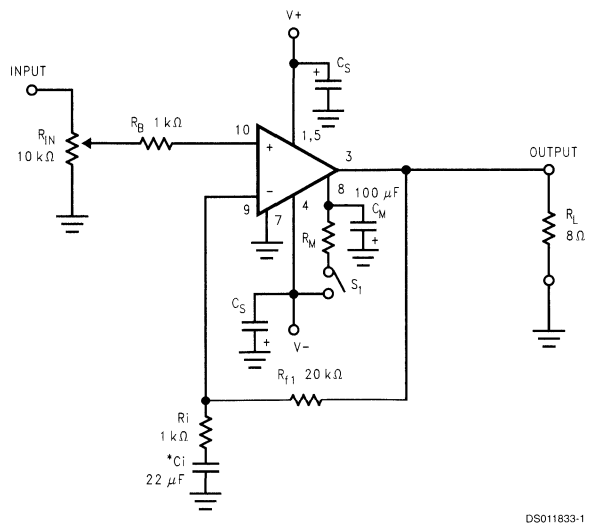
Features

- 68W cont. avg. output power into 4Ω at V_{CC} = ±28V
- 38W cont. avg. output power into 8Ω at V_{CC} = ±28V
- 50W cont. avg. output power into 8Ω at V_{CC} = ±35V
- 135W instantaneous peak output power capability
- Signal-to-Noise Ratio ≥ 92dB
- An input mute function
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11-lead TO-220 package
- Wide supply range 20V - 94V

Applications

- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application

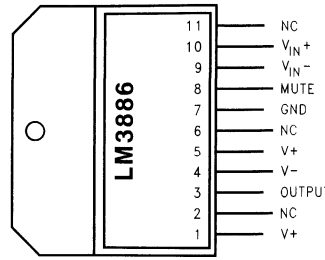


*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Plastic Package (Note 12)



DS011833-2

Note 1: Preliminary: call you local National Sales Rep. or distributor for availability

Top View
Order Number LM3886T
or LM3886TF
See NS Package Number TA11B for Staggered Lead Non-Isolated Package or TF11B (Note 1) **for Staggered Lead Isolated Package**

National Semiconductor

LM4651 & LM4652 *Overture*™ Audio Power Amplifier 170W Class D Audio Power Amplifier Solution

General Description

The IC combination of the LM4651 driver and the LM4652 power MOSFET provides a high efficiency, Class D subwoofer amplifier solution.

The LM4651 is a fully integrated conventional pulse width modulator driver IC. The IC contains short circuit, under voltage, over modulation, and thermal shut down protection circuitry. It contains a standby function, which shuts down the pulse width modulation and minimizes supply current. The LM4652 is a fully integrated H-bridge power MOSFET IC in a TO-220 power package. Together, these two IC's form a simple, compact high power audio amplifier solution complete with protection normally seen only in Class AB amplifiers. Few external components and minimal traces between the IC's keep the PCB area small and aids in EMI control.

The near rail-to-rail switching amplifier substantially increases the efficiency compared to Class AB amplifiers. This high efficiency solution significantly reduces the heat sink size compared to a Class AB IC of the same power level. This two-chip solution is optimum for powered subwoofers and self powered speakers.

Key Specifications

- Output power into 4Ω with < 10% THD. 170W (Typ)
- THD at 10W, 4Ω, 10 – 500Hz. < 0.3% THD (Typ)
- Maximum efficiency at 125W 85% (Typ)
- Standby attenuation. >100dB (Min)

Features

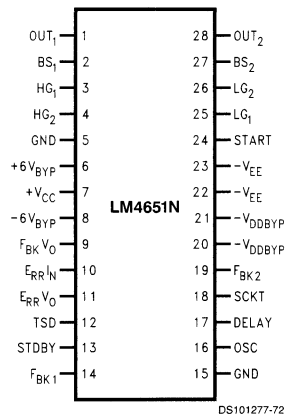
- Conventional pulse width modulation.
- Externally controllable switching frequency.
- 50kHZ to 200kHz switching frequency range.
- Integrated error amp and feedback amp.
- Turn–on soft start and under voltage lockout.
- Over modulation protection (soft clipping).
- Short circuit current limiting and thermal shutdown protection.
- 15 Lead TO–220 isolated package.
- Self checking protection diagnostic.

Applications

- Powered subwoofers for home theater and PC's
- Car booster amplifier
- Self-powered speakers

Connection Diagrams

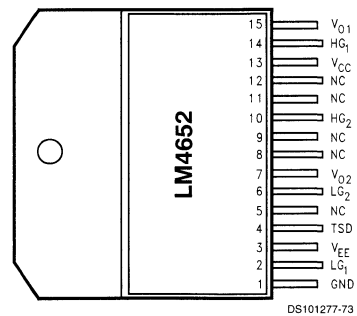
LM4651 Plastic Package



DS101277-72

Top View
Order Number LM4651N
See NS Package Number N28B

LM4652 Plastic Package (Note 8)



DS101277-73

Isolated TO-220 Package
Order Number LM4652TF
See NS Package Number TF15B
or
Non-Isolated TO-220 Package
Order Number LM4652TA
See NS Package Number TA15A

National Semiconductor

LM4663 Boomer® Audio Power Amplifier Series

2 Watt Stereo Class D Audio Power Amplifier with Stereo Headphone Amplifier

General Description

The LM4663 is a fully integrated single supply, high efficiency Class D audio power amplifier solution. The LM4663 utilizes a continuous time delta-sigma modulation technique that lowers output noise and THD when compared to conventional pulse width modulators.

The LM4663 also features a stereo headphone amplifier that delivers 80mW into a 32Ω headset with less than 0.5% THD. The LM4663 has two stereo inputs that can be selected to drive either the headphone amplifier or the Class D amplifier. All amplifiers are protected with thermal shutdown.

In standby mode, the LM4663 draws an extremely low 2µA supply current. With a 4Ω load, the IC's efficiency for a 250mW power level is 69%, reaching 83% at a power level of 2W. The IC features click and pop reduction circuitry that minimizes audible popping during device turn-on and turn-off. The LM4663 is available in a 24-lead TSSOP package, ideal for portable and desktop computer applications.

Key Specifications

- P_O at THD+N=1% 2.1W (typ)
- THD+N at 1kHz at 1 Watt into 4Ω (Power Amp) 0.2% (typ)
- Efficiency at 2 Watt into 4Ω 83% (typ)
- Efficiency at 250mW into 4Ω 69% (typ)
- Total quiescent power supply current 22mA (typ)
- Total shutdown power supply current 2µA (typ)
- THD+N 1kHz, 20mW, 32Ω (Headphone) 0.15% (typ)
- Single supply range 4.5V to 5.5V

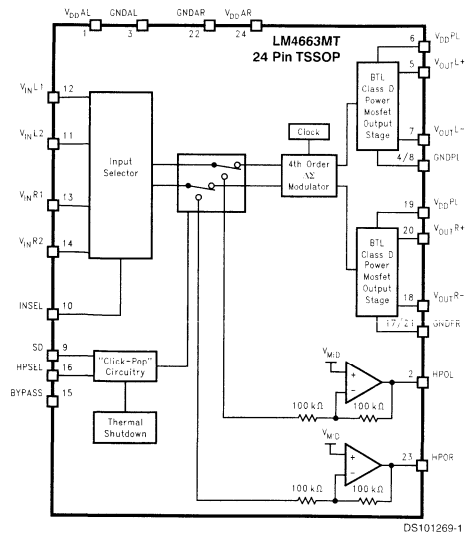
Features

- Delta-sigma modulator.
- Two stereo input selector.
- "Click and pop" suppression circuitry.
- Micropower shutdown mode.
- 24 lead TSSOP package (No heatsink required).
- Stereo headphone amplifier.

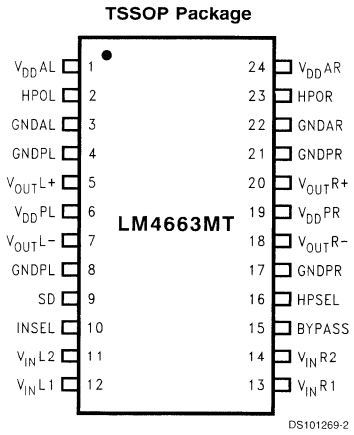
Applications

- Portable computers
- Desktop computers
- Multimedia Monitors

Block Diagram



Connection Diagram



Top View
Order Number LM4663MT
See NS Package Number MTC24
(TSSOP Package)

National Semiconductor

LM4700
Overture™ Audio Power Amplifier Series
30W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM4700 is an audio power amplifier capable of delivering typically 30W of continuous average output power into an 8Ω load with less than 0.1% THD+N.

The LM4700 has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM4700, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- THD+N at 1kHz at continuous average output power of 25W into 8Ω: 0.1% (max)
- THD+N from 20Hz to 20kHz at 30W of continuous average output power into 8Ω: 0.08% (typ)
- Standby current: 2.1mA (typ)

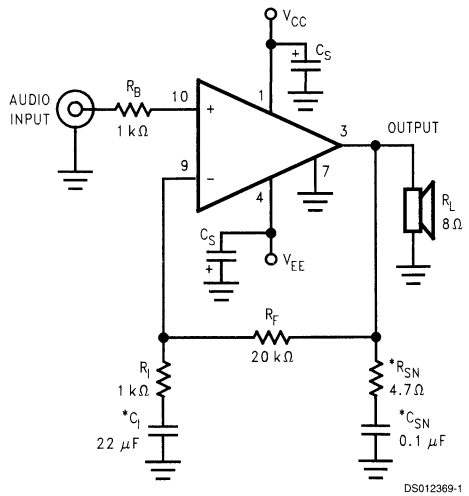
Features

- **SPiKe** Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute function
- Power conserving standby-mode
- Isolated 11-lead TO-220 package
- Wide supply range 20V - 66V

Applications

- Component stereo
- Compact stereo

Typical Application

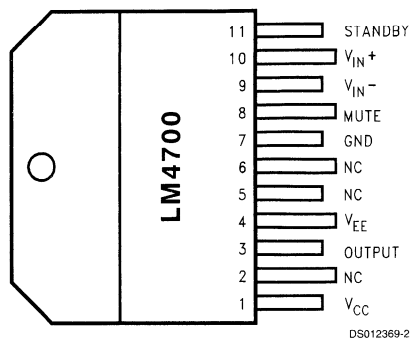


*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Isolated Plastic Package



Top View
Order Number LM4700TF or LM4700T
See NS Package Number TF11B for Staggered Lead Isolated Package
See TA11B for Staggered Lead Non-Isolated Package

National Semiconductor

LM4701 *Overture*™ Audio Power Amplifier Series 30W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM4701 is an audio power amplifier capable of delivering typically 30W of continuous average output power into an 8Ω load with less than 0.1% THD+N.

The LM4701 has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM4701, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- THD+N at 1kHz at continuous average output power of 25W into 8Ω: 0.1% (max)
- THD+N from 20Hz to 20kHz at 30W of continuous average output power into 8Ω: 0.08% (typ)
- Standby current: 2.1mA (typ)

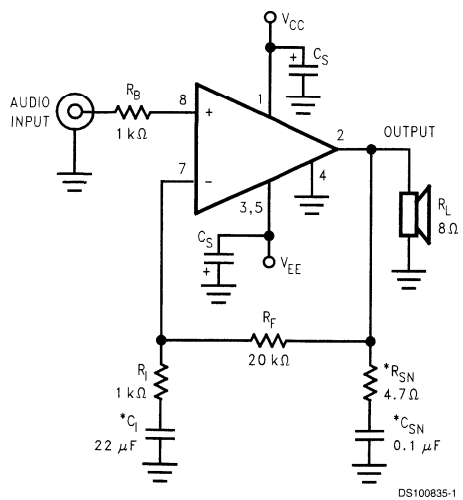
Features

- **SPiKe** Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute function
- Power conserving standby-mode
- Non-Isolated 9-lead TO-220 package
- Wide supply range 20V - 66V

Applications

- TVs
- Component stereo
- Compact stereo

Typical Application

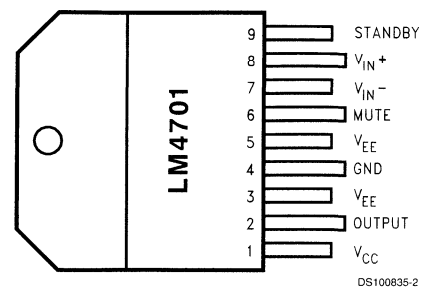


*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component functional description.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Plastic Package



Top View
Order Number LM4701T
See NS Package Number TA9A
For Staggered Lead Non-Isolated Package
Only a 9-Pin Package

National Semiconductor

LM4752
Stereo 11W Audio Power Amplifier

General Description

The LM4752 is a stereo audio amplifier capable of delivering 11W per channel of continuous average output power to a 4Ω load, or 7W per channel into 8Ω using a single 24V supply at 10% THD+N.

The LM4752 is specifically designed for single supply operation and a low external component count. The gain and bias resistors are integrated on chip, resulting in a 11W stereo amplifier in a compact 7 pin TO220 package. High output power levels at both 20V and 24V supplies and low external component count offer high value for compact stereo and TV applications. A simple mute function can be implemented with the addition of a few external components.

Key Specifications

- Output power at 10% THD+N with 1kHz into 4Ω at V_{CC} = 24V: 11W (typ)
- Output power at 10% THD+N with 1kHz into 8Ω at V_{CC} = 24V: 7W (typ)
- Closed loop gain: 34dB (typ)
- P_O at 10% THD+N @ 1 kHz into 4Ω single-ended TO-263 package at V_{CC} = 12V: 2.5W (typ)
- P_O at 10% THD+N @ 1kHz into 8Ω bridged TO-263 package at V_{CC} = 12V: 5W (typ)

Features

- Drives 4Ω and 8Ω loads
- Internal gain resistors (A_V = 34 dB)
- Minimum external component requirement
- Single supply operation
- Internal current limiting
- Internal thermal protection
- Compact 7-lead TO-220 package
- Low cost-per-watt
- Wide supply range 9V - 40V

Applications

- Compact stereos
- Stereo TVs
- Mini component stereos
- Multimedia speakers

Typical Application

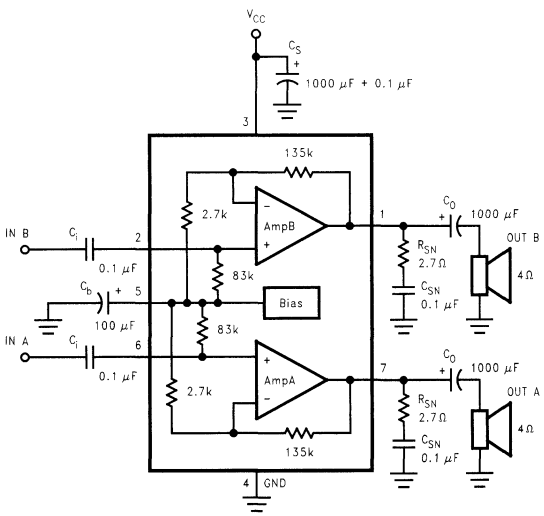
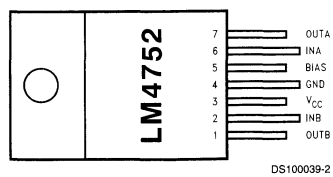


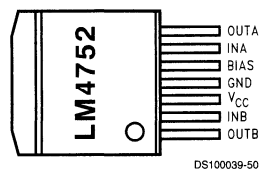
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

Plastic Package



Package Description
Top View
Order Number LM4752T
Package Number TA07B



Package Description
Top View
Order Number LM4752TS
Package Number TS07B

National Semiconductor

LM4753
Dual 10W Audio Power Amplifier w/Mute, Standby and Volume Control

General Description

The LM4753 is a stereo audio amplifier capable of delivering 10W/channel at 10% distortion into a 8Ω load. The power amp has an internally set gain of 30 dB. A 0V–5V DC controlled volume block provides 80 dB of attenuation from input to line-out. Line outputs are available after the volume control for signal routing.

The amplifier has a smooth transition fade-in/out mute and a power conserving standby function which are controlled through TTL or CMOS logic. Both functions provide over 75 dB of attenuation.

The LM4753 maintains an excellent Signal-to-Noise ratio of greater than 70 dB with a low noise floor less than 2 mV. The IC also maintains above 50 dB of channel separation.

The LM4753 is available in a 15-lead non-isolated plastic package and is designed for use in TV applications requiring single supply operation.

Key Specifications

- Output power into 8Ω at 10% THD 10W
- Maximum operating voltage 28V
- Power output stage Noise floor 2 mV
- Line output Noise floor 55 µV
- 0V–5V DC controlled volume attenuation 80 dB
- Mute attenuation 75 dB
- Standby-mode supply current 7 mA

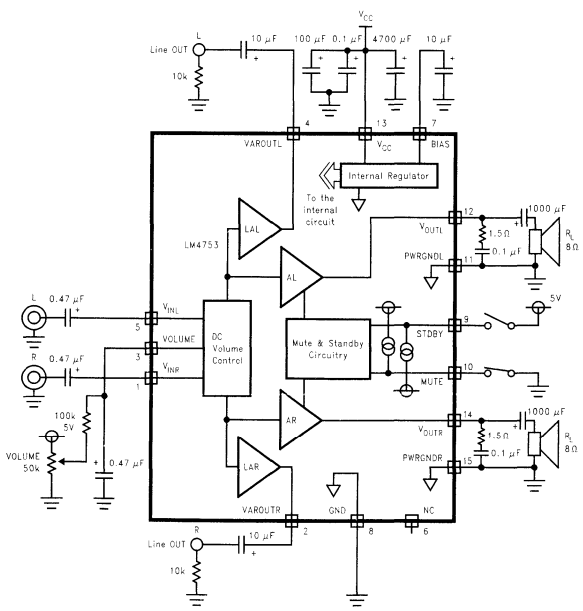
Features

- Quiet fade-in/out mute function
- Stereo variable line-out pins
- AC output short circuit protection
- Thermal shutdown protection

Applications

- Stereo TVs
- Component stereo
- Compact stereo

Typical Application

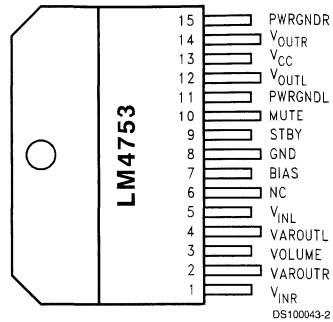


DS100043-1

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Plastic Package



Top View
Order Number
See NS Package Number TA15A for
Staggered Lead Non-Isolated Package

National Semiconductor

LM4755
Stereo 11W Audio Power Amplifier with Mute

General Description

The LM4755 is a stereo audio amplifier capable of delivering 11W per channel of continuous average output power to a 4Ω load or 7W per channel into 8Ω using a single 24V supply at 10% THD+N. The internal mute circuit and pre-set gain resistors provide for a very economical design solution.

Output power specifications at both 20V and 24V supplies and low external component count offer high value to consumer electronic manufacturers for stereo TV and compact stereo applications. The LM4755 is specifically designed for single supply operation.

Key Specifications

- Output power at 10% THD with 1kHz into 4Ω at V_{CC} = 24V: 11W (typ)
- Output power at 10% THD with 1kHz into 8Ω at V_{CC} = 24V: 7W (typ)
- Closed loop gain: 34dB (typ)
- P_O at 10% THD+N @ 1kHz into 4Ω single-ended TO-263 package at V_{CC}=12V: 2.5W (typ)
- P_O at 10% THD+N @ 1kHz into 8Ω bridged TO-263 package at V_{CC}=12V: 5W (typ)

Features

- Drives 4Ω and 8Ω loads
- Integrated mute function
- Internal Gain Resistors
- Minimal external components needed
- Single supply operation
- Internal current limiting and thermal protection
- Compact 9-lead TO-220 package
- Wide supply range 9V - 40V

Applications

- Stereos TVs
- Compact stereos
- Mini component stereos

Typical Application

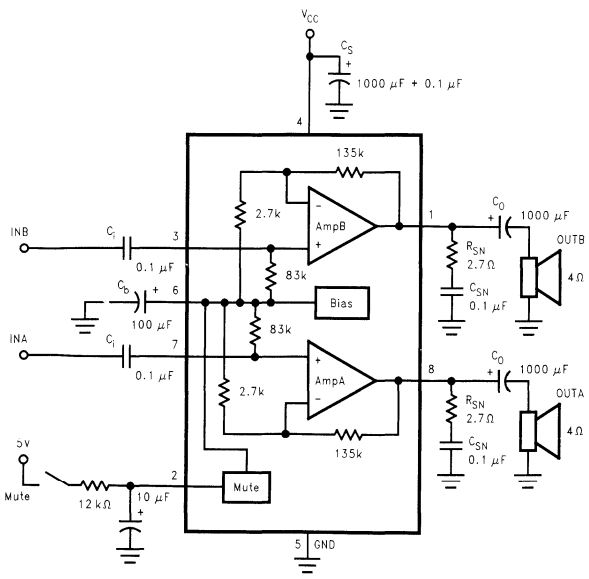
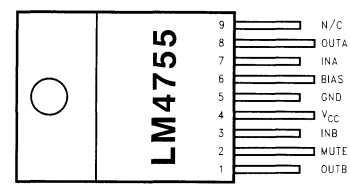


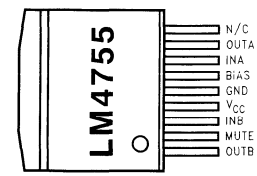
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

Plastic Package



Package Description
Top View
Order Number LM4755T
Package Number TA09A



Top View
Order Number LM4755TS
Package Number TS9A

National Semiconductor

LM4765 *Overture*™ Audio Power Amplifier Series Dual 30W Audio Power Amplifier with Mute and Standby Modes

General Description

The LM4765 is a stereo audio amplifier capable of delivering typically 30W per channel of continuous average output power into an 8Ω load with less than 0.1% THD+N.

Each amplifier has an independent smooth transition fade-in/out mute and a power conserving standby mode which can be controlled by external logic.

The performance of the LM4765, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) protection circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** protection means that these parts are safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Key Specifications

- THD+N at 1kHz at 2 x 25W continuous average output power into 8Ω: 0.1% (max)
- THD+N at 1kHz at continuous average output power of 2 x 30W into 8Ω: 0.009% (typ)
- Standby current: 6.5mA (typ)

Features

- SPiKe Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute mode
- Standby-mode
- Non-Isolated 15-lead TO-220 package
- Wide supply range 20V - 66V

Applications

- High-end stereo TVs
- Component stereo
- Compact stereo

Typical Application

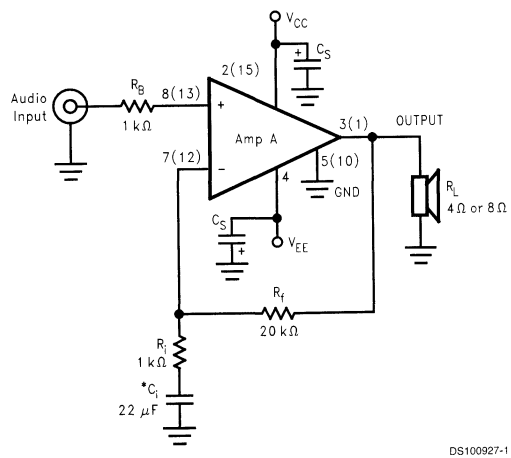


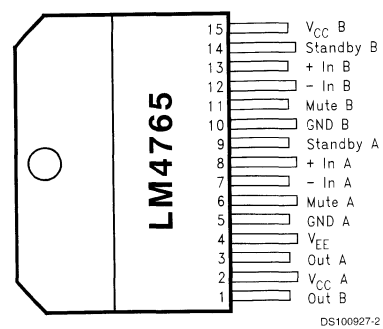
FIGURE 1. Typical Audio Amplifier Application Circuit

Note: Numbers in parentheses represent pinout for amplifier B.

*Optional component dependent upon specific design requirements.

Connection Diagram

Plastic Package



Top View
Non-Isolated Package
Order Number LM4765T
See NS Package Number TA15A

National Semiconductor

PRELIMINARY

LM4766 *Overture*™ Audio Power Amplifier Series Dual 40W Audio Power Amplifier with Mute

General Description

The LM4766 is a stereo audio amplifier capable of delivering typically 40W per channel with the non-isolated 'T' package and 30W per channel with the isolated 'TF' package of continuous average output power into an 8Ω load with less than 0.1% (THD+N).

The performance of the LM4766, utilizing its Self Peak Instantaneous Temperature (°Ke) (**SPiKe**™) Protection Circuitry, places it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). **SPiKe** Protection means that these parts are safeguarded at the output against overvoltage, undervoltage, overloads, including thermal runaway and instantaneous temperature peaks.

Each amplifier within the LM4766 has an independent smooth transition fade-in/out mute that minimizes output pops. The IC's extremely low noise floor at 2μV and its extremely low THD+N value of 0.06% at the rated power make the LM4766 optimum for high-end stereo TVs or mini-component systems.

Key Specifications

- THD+N at 1kHz at 2 x 30W continuous average output power into 8Ω: 0.1% (max)
- THD+N at 1kHz at continuous average output power of 2 x 30W into 8Ω: 0.009% (typ)

Features

- SPiKe Protection
- Minimal amount of external components necessary
- Quiet fade-in/out mute mode
- Non-Isolated 15-lead TO-220 package
- Wide Supply Range 20V - 78V

Applications

- High-end stereo TVs
- Component stereo
- Compact stereo

Typical Application

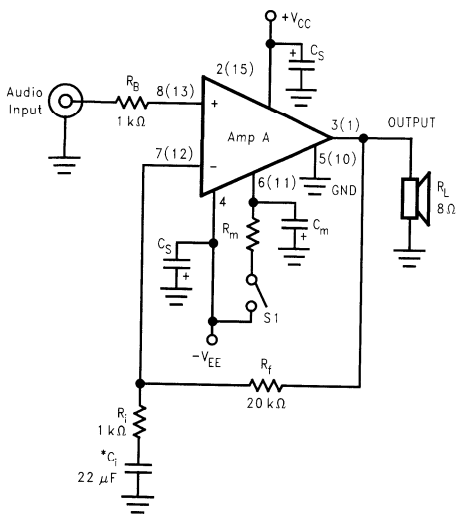


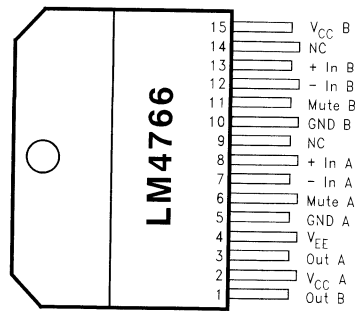
FIGURE 1. Typical Audio Amplifier Application Circuit

Note: Numbers in parentheses represent pinout for amplifier B.

*Optional component dependent upon specific design requirements.

Connection Diagram

Plastic Package



Top View
Non-Isolated TO-220 Package
Order Number LM4766T
See NS Package Number TA15A
Isolated TO-220 Package
Order Number LM4766TF
See NS Package Number TF15B

National Semiconductor

LM4808 Boomer® Audio Power Amplifier Series
Dual 105mW Headphone Amplifier

General Description

The LM4808 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4808 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The unity-gain stable LM4808 can be configured by external gain-setting resistors.

Key Specifications

- THD+N at 1kHz at 105mW continuous average output power into 16Ω 0.1% (typ)
- THD+N at 1kHz at 70mW continuous average output power into 32Ω 0.1% (typ)
- Output power at 0.1% THD+N at 1kHz into 32Ω 70mW (typ)

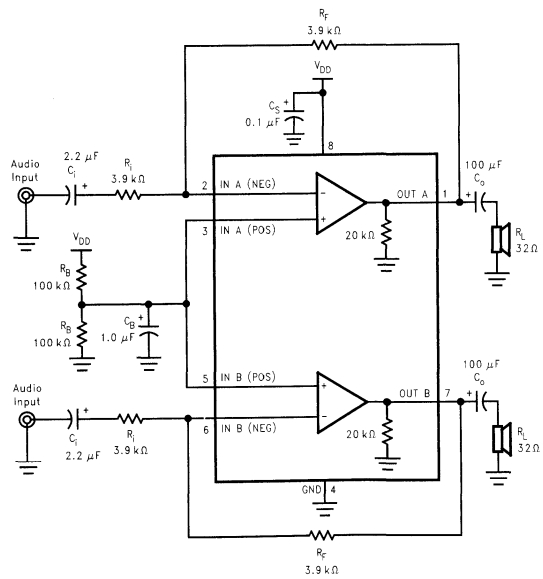
Features

- LLP, MSOP, and SOP surface mount packaging
- Switch on/off click suppression
- Excellent power supply ripple rejection
- Unity-gain stable
- Minimum external components

Applications

- Headphone Amplifier
- Personal Computers
- Portable electronic devices

Typical Application

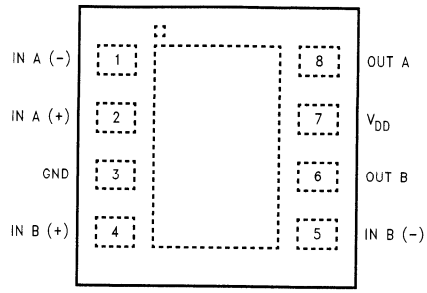


*Refer to the **Application Information** Section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

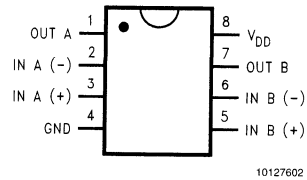
Connection Diagrams

LLP Package



Top View
Order Number LM4808LD
See NS Package Number LDA08B

SOP & MSOP Package



Top View
Order Number LM4808M, LM4808MM
See NS Package Number M08A, MUA08A

National Semiconductor

LM4809 Boomer® Audio Power Amplifier Series
Dual 105mW Headphone Amplifier with Active-Low Shutdown Mode

General Description

The LM4809 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4809 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The unity-gain stable LM4809 can be configured by external gain-setting resistors.

The LM4809 features an externally controlled, active-low, micropower consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

Key Specifications

- THD+N at 1kHz at 105mW continuous average power into 16Ω 0.1% (typ)
- THD+N at 1kHz at 70mW continuous average power into 32Ω 0.1% (typ)
- Shutdown Current 0.4µA (typ)

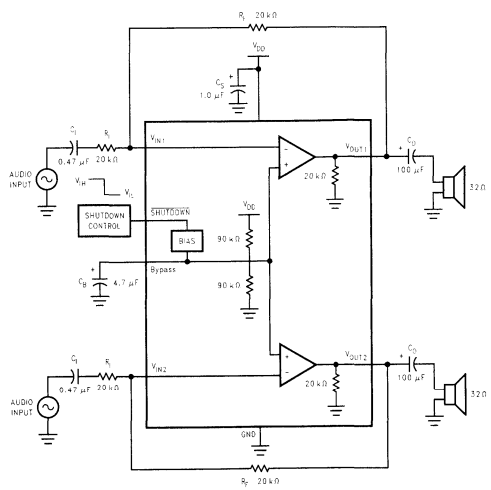
Features

- Active-low shutdown mode
- 'Click and Pop' reduction circuitry
- Low shutdown current
- LLP and MSOP surface mount packaging
- No bootstrap capacitors required
- Unity-gain stable

Applications

- Headphone Amplifier
- Personal Computers
- Microphone Preamplifier
- PDA's

Typical Application



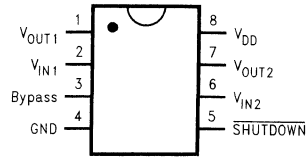
20009001

*Refer to the **Application Information** Section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

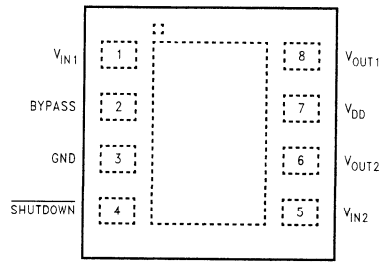
MSOP Package



20009002

Top View
Order Number LM4809MM
See NS Package Number MUA08A

LLP Package



20009061

Top View
Order Number LM4809LD
See NS Package Number LDA08B

National Semiconductor

LM4810 Boomer® Audio Power Amplifier Series
Dual 105mW Headphone Amplifier with Active-High Shutdown Mode

General Description

The LM4810 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4810 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The unity-gain stable LM4810 can be configured by external gain-setting resistors.

The LM4810 features an externally controlled, active-high, micropower consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

Key Specifications

- THD+N at 1kHz, 105mW continuous average power into 16Ω 0.1% (typ)
- THD+N at 1kHz, 70mW continuous average power into 32Ω 0.1% (typ)
- Shutdown Current 0.4µA (typ)

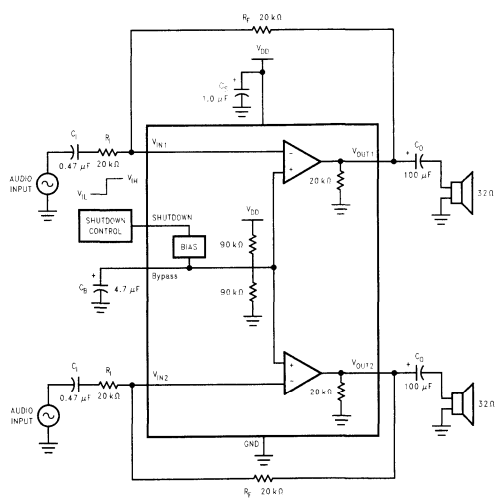
Features

- Active-high shutdown mode
- LLP and MSOP surface mount packaging
- 'Click and Pop' suppression circuitry
- Low shutdown current
- No bootstrap capacitors required
- Unity-gain stable

Applications

- Cellular Phones
- Personal Computers
- Microphone Preamplifier
- PDA's

Typical Application



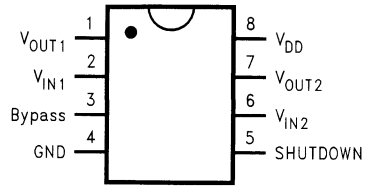
DS200089-1

*Refer to the **Application Information** Section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

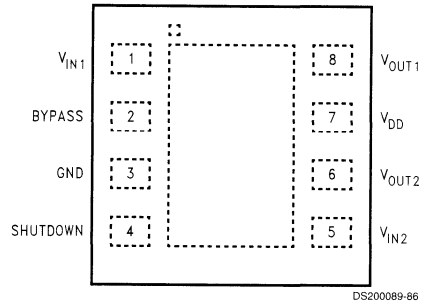
Connection Diagrams

MSOP Package



Top View
Order NumberLM4810MM
See NS Package Number MUA08A

LLP Package



Top View
Order NumberLM4810LD
See NS Package Number LDA08B

National Semiconductor

LM4811 Boomer® Audio Power Amplifier Series
Dual 105mW Headphone Amplifier with Digital Volume Control and Shutdown Mode

General Description

The LM4811 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4811 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4811 features a digital volume control that sets the amplifier's gain from +12dB to −33dB in 16 discrete steps using a two−wire interface.

The unity-gain stable LM4811 also features an externally controlled, active-high, micropower consumption shutdown mode. It also has an internal thermal shutdown protection mechanism.

Key Specifications

- THD+N at 1kHz, 105mW continuous average output power into 16Ω 0.1% (typ)
- THD+N at 1kHz, 70mW continuous average power into 32Ω 0.1% (typ)
- Shutdown Current 0.3µA (typ)

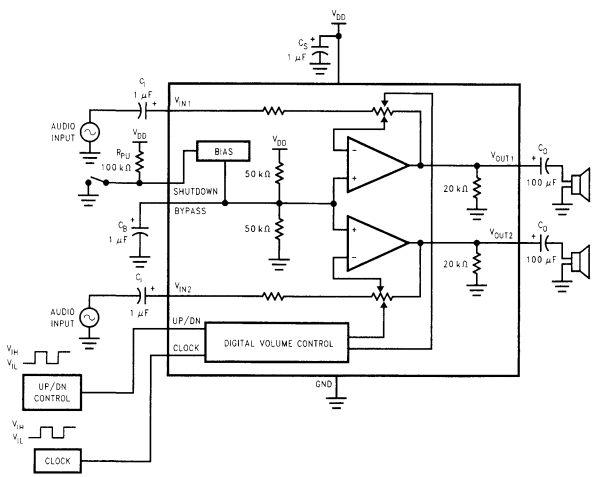
Features

- Digital volume control range from +12dB to −33dB
- LD and MSOP surface mount packaging
- 'Click and Pop' suppression circuitry
- No bootstrap capacitors required
- Low shutdown current

Applications

- Cellular Phones
- MP3, CD, DVD players
- PDA's
- Portable electronics

Typical Application



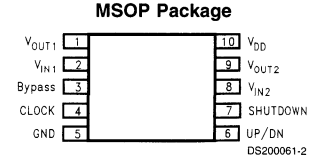
DS200061-1

*Refer to the **Application Information** Section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

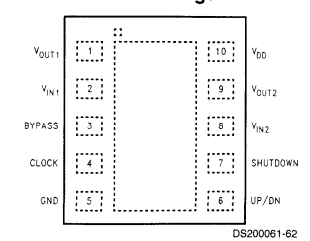
MSOP Package



DS200061-2

Top View
Order Number LM4811MM
See NS Package Number MUB10A

LD Package



DS200061-62

Top View
Order Number LM4811LD
See NS Package Number LDA10A

National Semiconductor

LM4819 Boomer® Audio Power Amplifier Series
350mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4819 is a mono bridged power amplifier that is capable of delivering 350mW$_{RMS}$ output power into a 16Ω load or 300mW$_{RMS}$ output power into an 8Ω load with 10% THD+N from a 5V power supply.

The LM4819 Boomer audio power amplifier is designed specifically to provide high quality output power and minimize PCB area with surface mount packaging and a minimal amount of external components. Since the LM4819 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable applications.

The closed loop response of the unity-gain stable LM4819 can be configured using external gain-setting resistors. The device is available in LLP, MSOP, and SO package types to suit various applications.

Key Specifications

- THD+N at 1kHz, 350mW continuous average output power into 16Ω 10% (max)
- THD+N at 1kHz, 300mW continuous average output power into 8Ω 10% (max)
- Shutdown Current 0.7µA (typ)

Features

- LLP, SOP, and MSOP surface mount packaging.
- Switch on/off click suppression.
- Unity-gain stable.
- Minimum external components.

Applications

- General purpose audio
- Portable electronic devices
- Information Appliances (IA)

Typical Application

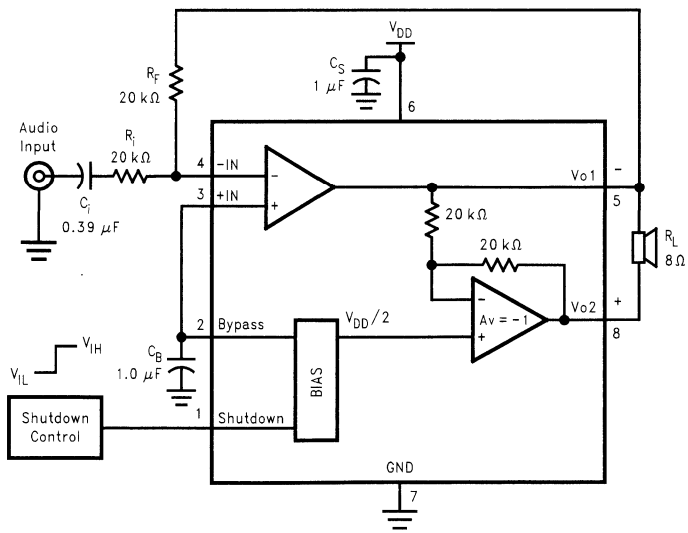
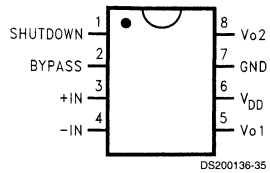


FIGURE 1. Typical Audio Amplifier Application Circuit

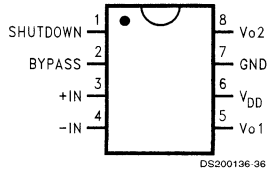
Connection Diagrams

Small Outline (SO) Package



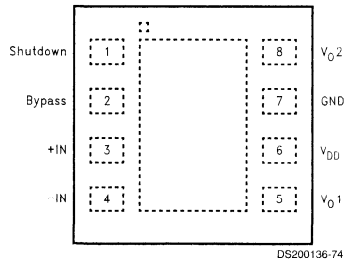
Top View
Order Number LM4819M
See NS Package Number M08A

Mini Small Outline (MSOP) Package



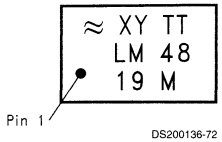
Top View
Order Number LM4819MM
See NS Package Number MUA08A

LLP Package



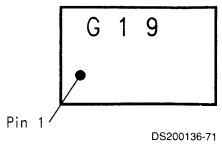
Top View
Order Number LM4819LD
See NS Package Number LDA08B

SO Marking



Top View
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number

MSOP Marking



Top View
G - Boomer Family
19 - LM4819MM

National Semiconductor

LM4820-6 Boomer® Audio Power Amplifier Series
Fixed Gain 1 Watt Audio Power Amplifier

General Description

The LM4820-6 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) at 6dB of BTL gain from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4820-6 does not require input and gain resistors, output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal parts count and low power consumption is a primary requirement.

The LM4820-6 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4820-6 features an internal thermal shutdown protection mechanism.

The LM4820-6 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Key Specifications

- Improved PSRR at 217Hz 62dB
- Power Output at 5.0V & 1% THD 1.0W(typ.)
- Power Output at 3.3V & 1% THD 400mW(typ.)
- Shutdown Current 0.1μA(typ.)

Features

- Fixed 6dB BTL voltage gain
- Available in space-saving packages micro SMD, MSOP and SOIC
- Ultra low current shutdown mode
- Can drive capacitive loads up to 500 pF
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.0 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- External gain configuration still possible

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

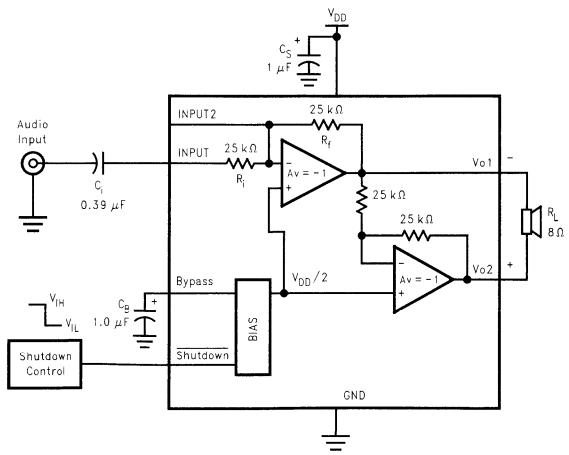
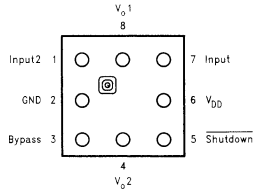


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

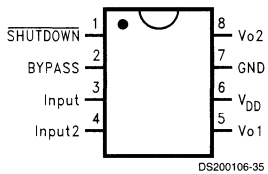
8 Bump micro SMD



DS200106-23

Top View
Order Number LM4820IBP-6, LM4820IBPX-6
See NS Package Number BPA08FFB

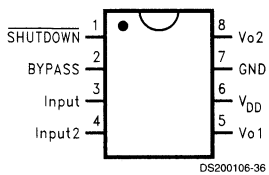
Small Outline (SO) Package



DS200106-35

Top View
Order Number LM4820M-6
See NS Package Number M08A

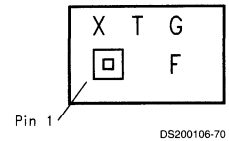
Mini Small Outline (MSOP) Package



DS200106-36

Top View
Order Number LM4820MM-6
See NS Package Number MUA08A

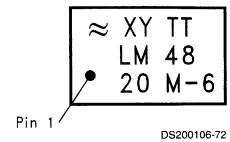
micro SMD Marking



DS200106-70

Top View
X - Date Code
T - Die Traceability
G - Boomer Family
F - LM4820IBP-6

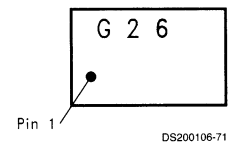
SO Marking



DS200106-72

Top View
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number (LM4820M-6)

MSOP Marking



DS200106-71

Top View
G- Boomer Family
26 - LM4820MM-6

National Semiconductor

LM4830
Two-Way Audio Amplification System with Volume Control

General Description

The LM4830 is an integrated solution for two-way audio amplification. It contains a bridge-connected audio power amplifier capable of delivering 1W of continuous average power to an 8Ω load with less than 1% THD from a 5V power supply. It also has the capability of driving 100 mW into a single-ended 32Ω impedance for headset operation. There is a 30 dB attenuator in front of a bridged power amplifier with 6 dB of gain. The attenuation is controlled through 4 bits of parallel digital control; 15 steps of 2 dB each.

The device also contains a microphone preamp with two selectable inputs. Mic2 is selected when HS is high and A1 is in single-ended mode. Mic1 is selected when HS is low and A1 is in bridged mode. This configuration is optimum for switching between an internal system speaker and external headset with microphone. The device also incorporates a buffer used for driving capacitive loads.

The LM4830 also provides a low-current consumption shutdown mode making it optimally suited for low-power portable systems. In addition, the device has an internal thermal shutdown protection mechanism.

Key Specifications

- THD at 1W cont. avg P_O into 8Ω: 1% (max)
- Instantaneous peak output power: 1.4W
- Shutdown current: 0.5 µA (typ)
- Supply voltage range: $2.7V \leq V_{DD} \leq 5.5V$

Features

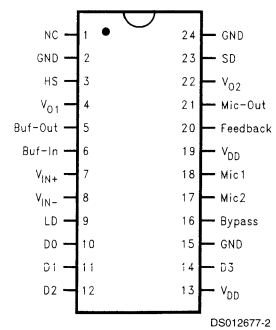
- 4-bit digital control for 30 dB of volume attenuation
- Two selectable microphone inputs
- High performance microphone preamp
- Extra buffer for driving long cables
- No bootstrap capacitors or snubber circuits are necessary
- Small Outline (SO) packaging
- Thermal shutdown protection circuitry

Applications

- Hands-free phone systems
- Mobile phone accessories
- Desktop conference phones
- Portable computers
- Teleconference computer applications

Connection Diagram

Dual-In-Line and Small Outline Packages



DS012677-2

Top View
Order Number LM4830M
See NS Package Number M24B for SO
Order Number LM4830N
See NS Package Number N24A for DIP

Typical Application

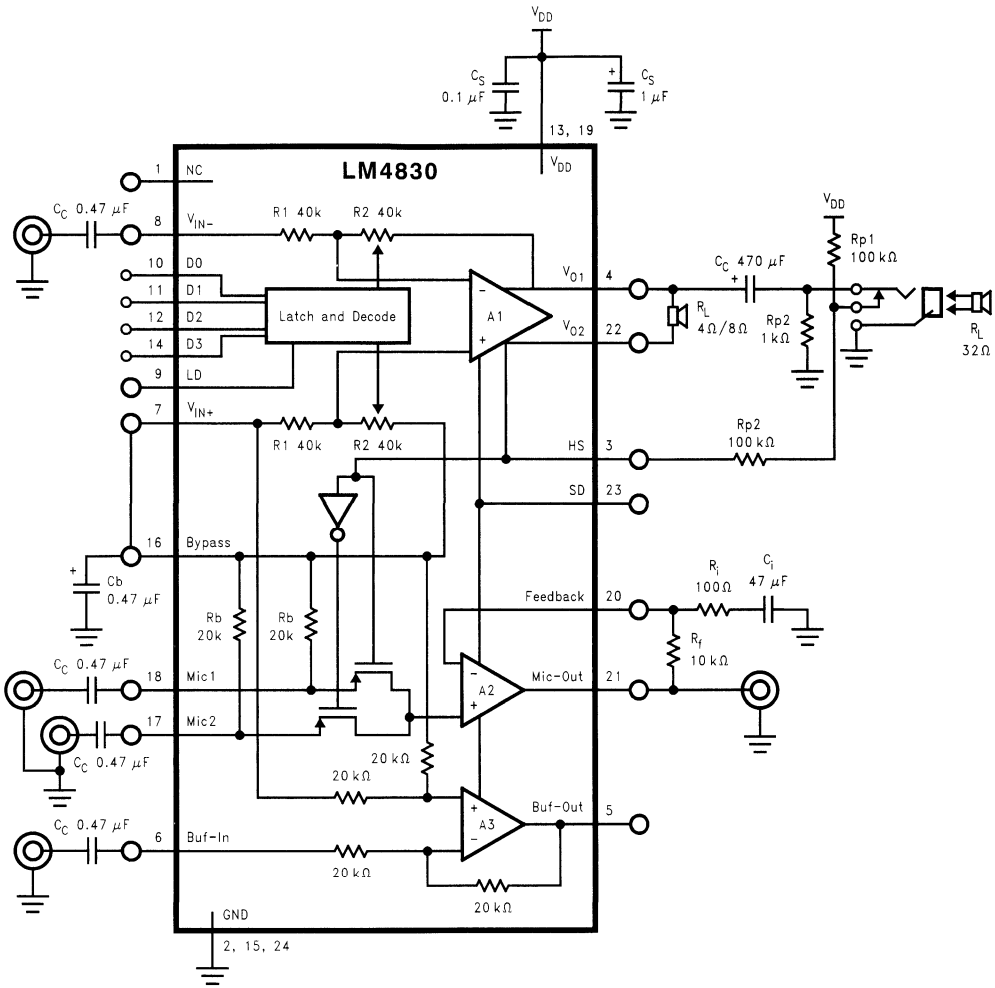


FIGURE 1. Typical Application Circuit

National Semiconductor

LM4831 Boomer® Audio Power Amplifier Series
Multimedia Computer Audio Chip

General Description

The LM4831 is a monolithic integrated circuit that provides a stereo three input mixer, two stereo input analog multiplexer, a stereo line out and a dual 1W bridged audio power amplifier. In addition, a low noise microphone preamp is included on-chip.

The LM4831 is ideal for multimedia computers since it incorporates an input mixer, analog multiplexer, and configurable stereo audio power amplifier, as well as a microphone preamp stage. This combination allows for all of the analog audio processing to be enclosed in a 44-pin TQFP package.

The LM4831 features an externally controlled, low-power consumption shutdown mode, as well as both headphone and docking station modes. To temporarily override the shutdown mode and allow audio signals to be amplified, the LM4831 provides four "beep" pins.

Key Specifications

- THD+N at 1W into 8Ω — 0.6% (typ)
- Microphone Input Referred Noise — 10μV (typ)
- Supply Current - Bridged Mode — 16mA (typ)
- Shutdown Current — 2μA (typ)

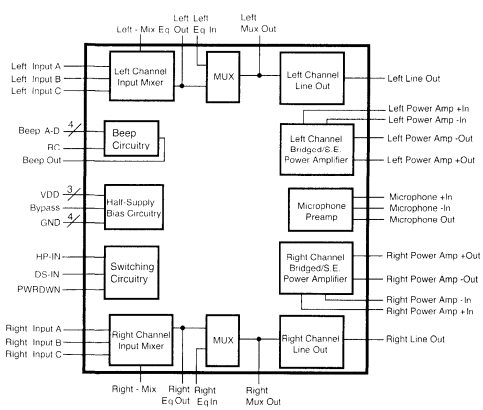
Features

- Stereo 1W audio power amplifier
- "Click and pop" suppression circuitry
- Stereo three input mixer
- Shutdown mode
- Multiple operating modes—bridged, single-ended and docking station modes
- Internal mux for switching in/out external filter
- Beep circuitry for "wake-up" while in shutdown
- 44 Pin TQFP Packaging

Applications

- Portable and Desktop Computers

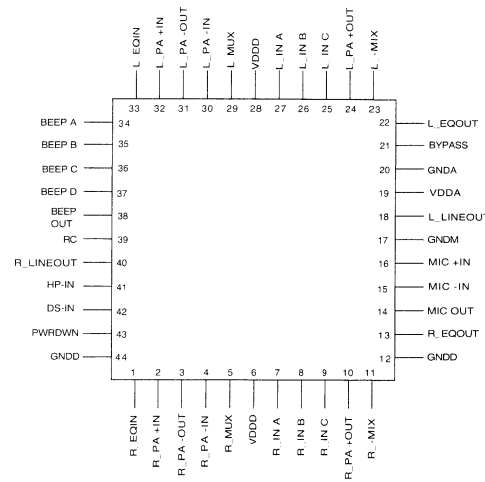
Block Diagram



DS100057-1

FIGURE 1. LM4831 Block Diagram

Connection Diagram



DS100057-3

Top View
Order Number LM4831VF
See NS Package Number VEJ44A

National Semiconductor

LM4832 Boomer® Audio Power Amplifier Series
Digitally Controlled Tone and Volume Circuit with Stereo Audio Power Amplifier, Microphone Preamp Stage and National 3D Sound

General Description

The LM4832 is a monolithic integrated circuit that provides volume and tone (bass and treble) controls as well as a stereo audio power amplifier capable of producing 250 mW (typ) into 8Ω or 90 mW (typ) into 32Ω with less than 1.0% THD. In addition, a two input microphone preamp stage, with volume control, capable of driving a 1 kΩ load is implemented on chip.

The LM4832 also features National's 3D Sound circuitry which can be externally adjusted via a simple RC network. For maximum system flexibility, the LM4832 has an externally controlled, low-power consumption shutdown mode, and an independent mute for power and microphone amplifiers .

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring few external components. Since the LM4832 incorporates tone and volume controls, a stereo audio power amplifier and a microphone preamp stage, it is optimally suited to multimedia monitors and desktop computer applications.

Key Specifications

- Output Power at 10% into 8Ω — 350mW (typ)
- Output Power at 10% into 32Ω — 100mW (typ)
- THD+N at 75mW into 32Ω at 1kHz — 0.5% (max)
- Microphone Input Referred Noise — 7μV (typ)
- Supply Current — 13mA (typ)
- Shutdown Current — 4μA (typ)

Features

- Independent Left and Right Output Volume Controls
- Treble and Bass Control
- National 3D Sound
- I^2C Compatible Interface
- Two Microphone Inputs with Selector
- Software Controlled Shutdown Function

Applications

- Multimedia Monitors
- Portable and Desktop Computers

Block Diagram

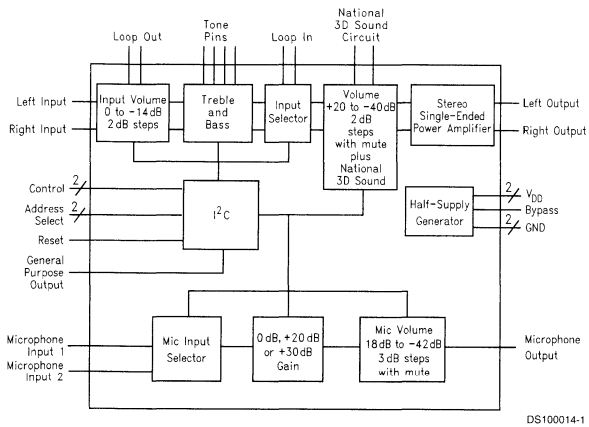
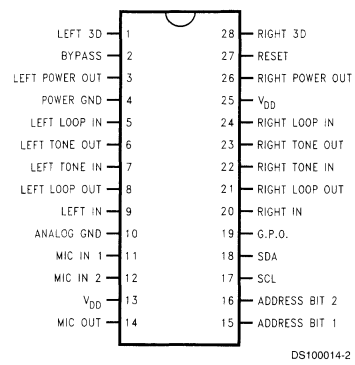


FIGURE 1. LM4832 Block Diagram

Connection Diagram



Top View
Order Number LM4832N, LM4832M
See NS Package Number N28B for DIP
See NS Package Number M28B for SOIC

National Semiconductor

LM4834 Boomer® Audio Power Amplifier Series
1.75W Audio Power Amplifier with DC Volume Control and Microphone Preamp

General Description

The LM4834 is a monolithic integrated circuit that provides DC volume control, and a bridged audio power amplifier capable of producing 1.75W into 4Ω with less than 1.0% (THD). In addition, the headphone/lineout amplifier is capable of driving 70 mW into 32Ω with less than 0.1%(THD). The LM4834 incorporates a volume control and an input microphone preamp stage capable of driving a 1 kΩ load impedance.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components in surface mount packaging. The LM4834 incorporates a DC volume control, a bridged audio power amplifier and a microphone preamp stage, making it optimally suited for multimedia monitors and desktop computer applications.

The LM4834 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Key Specifications

- THD at 1.1W continuous average output power into 8Ω at 1kHz 0.5% (max)
- Output Power into 4Ω at 1.0% THD+N 1.75W (typ)
- THD at 70mW continuous average output power into 32Ω at 1kHz 0.1% (typ)
- Shutdown Current 1.0µA (max)
- Supply Current 17.5mA (typ)

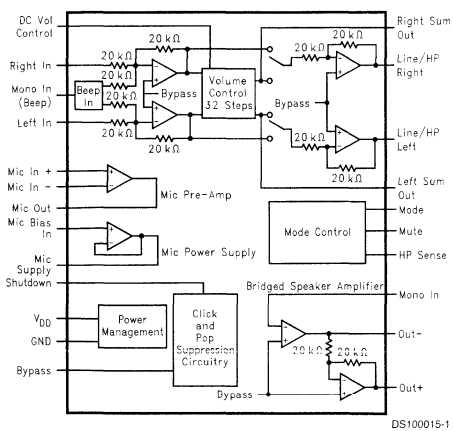
Features

- PC98 Compliant
- "Click and Pop" suppression circuitry
- Stereo line level outputs with mono input capability for system beeps
- Microphone preamp with buffered power supply
- DC Volume Control Interface
- Thermal shutdown protection circuitry

Applications

- Multimedia Monitors
- Desktop and Portable Computers

Block Diagram

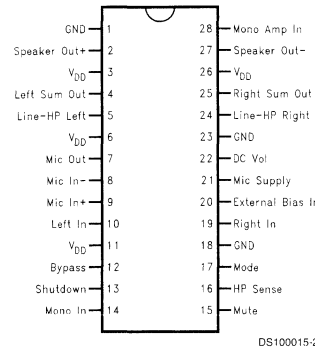


DS100015-1

FIGURE 1. LM4834 Block Diagram

Connection Diagram

SSOP Package



DS100015-2

Top View
Order Number LM4834MS
See NS Package Number MSA028CB for SSOP

National Semiconductor

LM4835 Boomer® Audio Power Amplifier Series

Stereo 2W Audio Power Amplifiers with DC Volume Control and Selectable Gain

General Description

The LM4835 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD or 2.2W into 3Ω (Note 2) with less than 1.0% THD.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4835 incorporates a DC volume control, stereo bridged audio power amplifiers and a selectable gain or bass boost, making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4835 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4835LQ and LM4835MTE will deliver 2W into 4Ω. The LM4835MT will deliver 1.1W into 8Ω. See the Application Information section LM4835LQ and for LM4835MTE usage information.

Note 2: An LM4835LQ and LM4835MTE that have been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- into 3Ω (LM4835LQ, LM4835MTE) 2.2W (typ)
- into 4Ω (LM4835LQ, LM4835MTE) 2.0W (typ)
- into 8Ω (LM4835) 1.1W (typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0% (typ)
- Shutdown current 0.7µA (typ)

Features

- PC98 Compliant
- DC Volume Control Interface
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain and bass boost configurable
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry

Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

Block Diagram

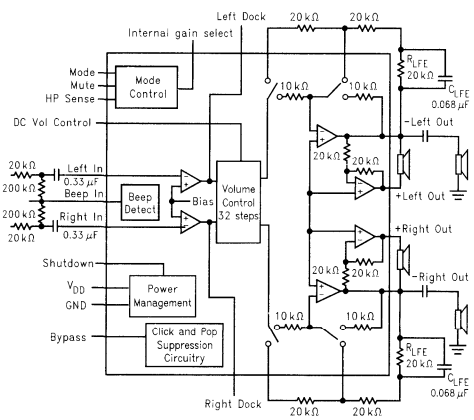
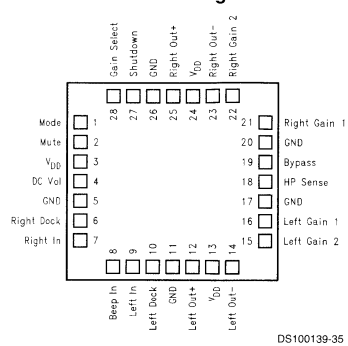


FIGURE 1. LM4835 Block Diagram

Connection Diagram

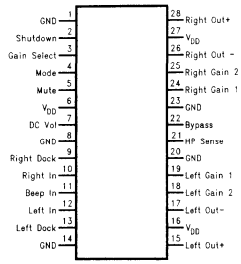
LLP Package



Top View
Order Number LM4835LQ
See NS Package Number LQA028AA for Exposed-DAP LLP

Connection Diagram (Continued)

TSSOP Package



DS100139-2

Top View
Order Number LM4835MT
See NS Package Number MTC28 for TSSOP
Order Number LM4835MTE
See NS Package Number MXA28A for Exposed-DAP TSSOP

National Semiconductor

LM4836 Boomer® Audio Power Amplifier Series
Stereo 2W Audio Power Amplifiers with DC Volume Control, Bass Boost, and Input Mux

General Description

The LM4836 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD+N, or 2.2W into 3Ω (Note 2) with less than 1.0% THD+N.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4836 incorporates a DC volume control, stereo bridged audio power amplifiers, selectable gain or bass boost, and an input mux making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4836 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4836LQ and LM4836MTE will deliver 2W into 4Ω. The LM4836MT will deliver 1.1W into 8Ω. See the Application Information section for LM4836LQ and LM4836MTE usage information.

Note 2: An LM4836LQ and LM4836MTE that have been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- into 3Ω (LM4836LQ, LM4836MTE) 2.2W(typ)
- into 4Ω (LM4836LQ, LM4836MTE) 2.0W(typ)
- into 8Ω (LM4836) 1.1W(typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0%(typ)
- Shutdown current 0.2μA(typ)

Features

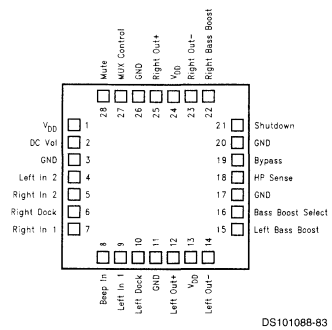
- PC98 and PC99 Compliant
- DC Volume Control Interface
- Input mux
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain and bass boost configurable
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry

Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

Connection Diagrams

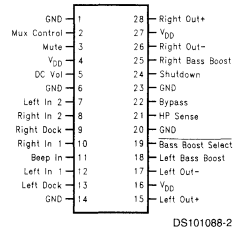
LLP Package



DS101088-83

Top View
Order Number LM4836LQ
See NS Package Number LQA028AA for Exposed-DAP LLP

TSSOP Package



DS101088-2

Top View
Order Number LM4836MT
See NS Package Number MTC28 for TSSOP
Order Number LM4836MTE
See NS Package Number MXA28A for Exposed-DAP TSSOP

National Semiconductor

LM4838 Boomer® Audio Power Amplifier Series
Stereo 2W Audio Power Amplifiers with DC Volume Control and Selectable Gain

General Description

The LM4838 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD or 2.2W into 3Ω (Note 2) with less than 1.0% THD.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4838 incorporates a DC volume control, stereo bridged audio power amplifiers and a selectable gain or bass boost, making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4838 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4838LQ and LM4838MTE will deliver 2W into 4Ω. The LM4838MT will deliver 1.1W into 8Ω. See the Application Information section LM4838LQ and for LM4838MTE usage information.

Note 2: An LM4838LQ and LM4838MTE that have been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- into 3Ω (LQ & MTE) 2.2W (typ)
- into 4Ω (LQ & MTE) 2.0W (typ)
- into 8Ω (MT, MTE, & LQ) 1.1W (typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0%(typ)
- Shutdown current 0.7μA (typ)

Features

- DC Volume Control Interface
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain and bass boost
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry

Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

Block Diagram

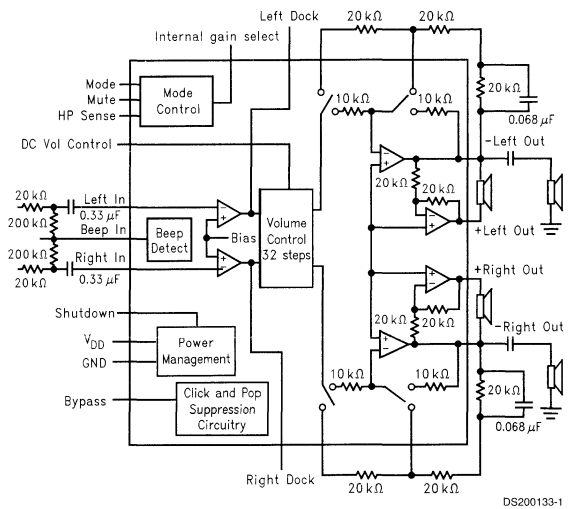
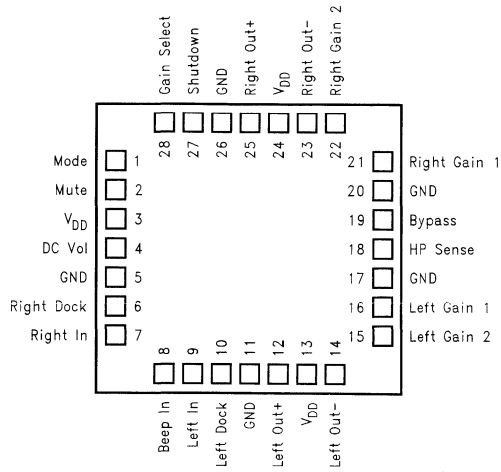


FIGURE 1. LM4838 Block Diagram

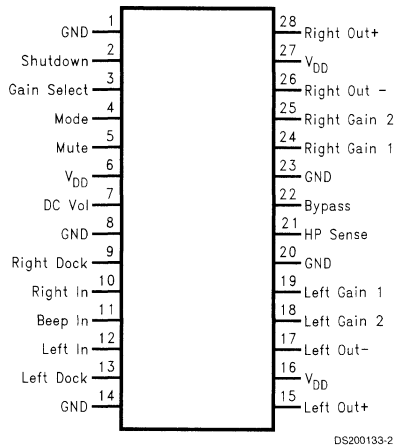
Connection Diagrams

LLP Package



Top View
Order Number LM4838LQ
See NS Package Number LQA028AA for Exposed-DAP LLP

TSSOP Package



Top View
Order Number LM4838MT
See NS Package Number MTC28 for TSSOP
Order Number LM4838MTE
See NS Package Number MXA28A for Exposed-DAP TSSOP

National Semiconductor

LM4839 Boomer® Audio Power Amplifier Series
Stereo 2W Audio Power Amplifiers with DC Volume Control, Bass Boost, and Input Mux

General Description

The LM4839 is a monolithic integrated circuit that provides DC volume control, and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD+N, or 2.2W into 3Ω (Note 2) with less than 1.0% THD+N.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4839 incorporates a DC volume control, stereo bridged audio power amplifiers, selectable gain or bass boost, and an input mux making it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4839 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4839LQ and LM4839MTE will deliver 2W into 4Ω. The LM4839MT will deliver 1.1W into 8Ω. See the Application Information section for LM4839LQ and LM4839MTE usage information.

Note 2: An LM4839LQ and LM4839MTE that have been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- into 3Ω (LQ & MTE) 2.2W(typ)
- into 4Ω (LQ & MTE) 2.0W(typ)
- into 8Ω (LM4839) (MT, MTE, & LQ) 1.1W(typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0%(typ)
- Shutdown current 0.2μA(typ)

Features

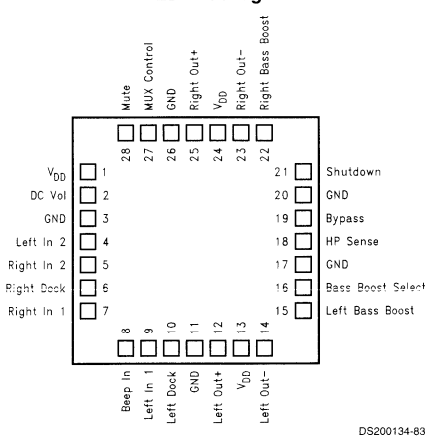
- DC Volume Control Interface
- Input mux
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- Selectable internal/external gain and bass boost
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry

Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

Connection Diagrams

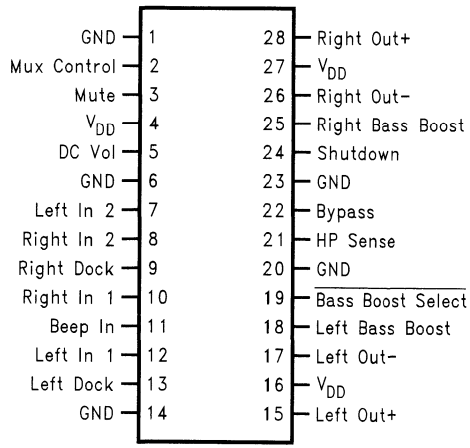
LLP Package



Top View
Order Number LM4839LQ
See NS Package Number LQA028AA for Exposed-DAP LLP

Connection Diagrams (Continued)

TSSOP Package



DS200134-2

Top View
Order Number LM4839MT
See NS Package Number MTC28 for TSSOP
Order Number LM4839MTE
See NS Package Number MXA28A for Exposed-DAP TSSOP

National Semiconductor

LM4840 Boomer® Audio Power Amplifier Series
Stereo 2W Audio Power Amplifiers with Digital Volume Control and Input Mux

General Description

The LM4840 is a monolithic integrated circuit that provides digital volume control and stereo bridged audio power amplifiers capable of producing 2W into 4Ω (Note 1) with less than 1.0% THD or 2.2W into 3Ω (Note 2) with less than 1.0% THD.

Boomer® audio integrated circuits were designed specifically to provide high quality audio while requiring a minimum amount of external components. The LM4840 incorporates a digital volume control, stereo bridged audio power amplifiers, an input mux, and a last volume level memory function to save the volume setting during shutdown. These features make it optimally suited for multimedia monitors, portable radios, desktop, and portable computer applications.

The LM4840 features an externally controlled, low-power consumption shutdown mode, and both a power amplifier and headphone mute for maximum system flexibility and performance.

Note 1: When properly mounted to the circuit board, the LM4840LQ and LM4840MH will deliver 2W into 4Ω. The LM4840MT will deliver 1.1W into 8Ω. See the Application Information section LM4840LQ and for LM4840MH usage information.

Note 2: An LM4840LQ and LM4840MH that have been properly mounted to the circuit board and forced-air cooled will deliver 2.2W into 3Ω.

Key Specifications

- P_O at 1% THD+N
  - into 3Ω (LM4840LQ, LM4840MH) 2.2W (typ)
  - into 4Ω (LM4840LQ, LM4840MH) 2.0W (typ)
  - into 8Ω (LM4840) 1.1W (typ)
- Single-ended mode - THD+N at 85mW into 32Ω 1.0% (typ)
- Shutdown current 0.2μA (typ)

Features

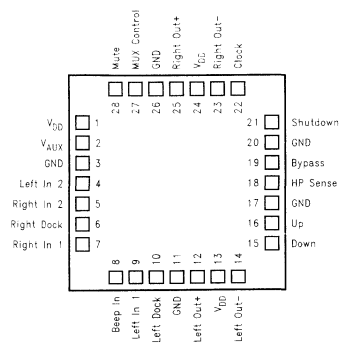
- PC98 and PC99 Compliant
- Digital Volume Control Interface
- System Beep Detect
- Stereo switchable bridged/single-ended power amplifiers
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry
- Input Mux
- Capless headphone drivers
- Last volume memory from shutdown

Applications

- Portable and Desktop Computers
- Multimedia Monitors
- Portable Radios, PDAs, and Portable TVs

Connection Diagram

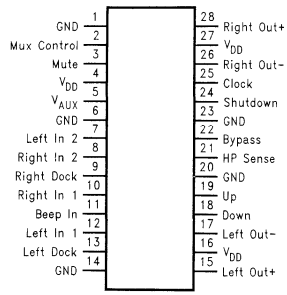
LLP Package



Top View
Order Number LM4840LQ
See NS Package Number LQA028A for Exposed-DAP LLP

Connection Diagram (Continued)

TSSOP Package



Top View
Order Number LM4840MT
See NS Package Number MTC28 for TSSOP
Order Number LM4840MH
See NS Package Number MXA28A for Exposed-DAP TSSOP

Block Diagram

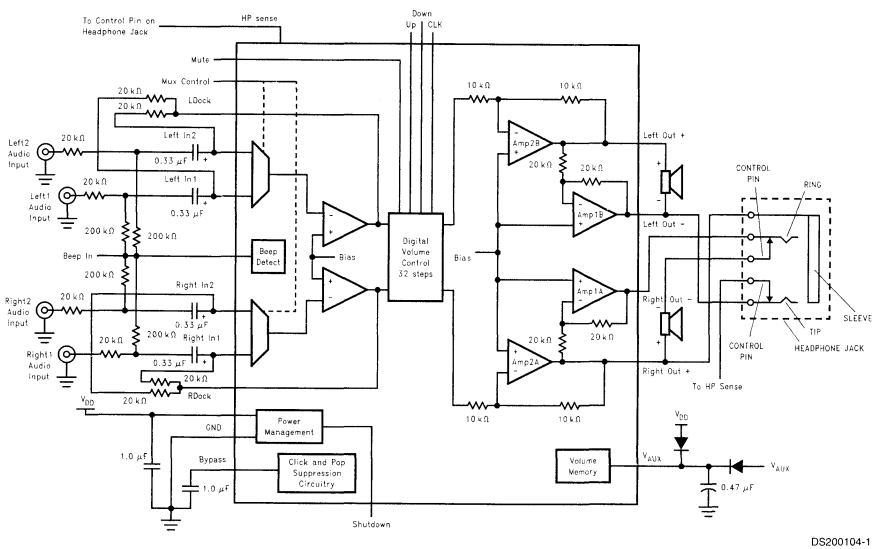


FIGURE 1. LM4840 Block Diagram

National Semiconductor

LM4850 Boomer® Audio Power Amplifier Series
Mono 1.5 W / Stereo 300 mW Power Amplifier

General Description

The LM4850 is an audio power amplifier capable of delivering 1.5W (typ) of continuous average power into a mono 4Ω bridged-tied load (BTL) with 1% THD+N or 95mW per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, using a 5V power supply.

The LM4850 can automatically switch between mono BTL and stereo SE modes utilizing a headphone sense pin. It is ideal for any system that provides both a monaural speaker output and a stereo line or headphone output

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4850 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4850 features an externally controlled, micropower consumption shutdown mode and thermal shutdown protection. The unity-gain stable LM4850's gain is set by external gain-setting resistors

Note 1: An LM4850LD that has been properly mounted to a circuit board will deliver 1.9W into 3Ω (at 1% THD+N). The other package options for the LM4850 will deliver 1.1W into 8Ω (at 1% THD+N). See **Application Information** sections for further information concerning the LM4850LD, LM4850MM, and LM4850MT.

Key Specifications

- Output Power at 1% THD+N, 1kHz:
  - LM4850LD 3Ω BTL 1.9W (typ)
  - LM4850LD 4Ω BTL 1.7W (typ)
  - LM4850MM, MT 4Ω BTL 1.5W (typ)
  - LM4850LD, MM, MT 8Ω BTL 1.1W (typ)
  - LM4850LD, MM, MT 4Ω SE 300mW (typ)
  - LM4850LD, MM, MT 32Ω SE 95mW (typ)
- THD+N at 1kHz, 95mW into 32Ω SE 1% (typ)
- Single Supply Operation 2.4 to 5.5V
- Shutdown Current 44µA (typ)

Features

- Mono 1.5W BTL or stereo 300mW output
- Headphone sense
- "Click and pop" suppression circuitry
- No bootstrap capacitors required
- Thermal shutdown protection
- Unity-gain stable
- LLP, TSSOP, and MSOP packaging

Applications

- Portable computers
- Desktop computers
- PDA's
- Handheld games

Typical Application

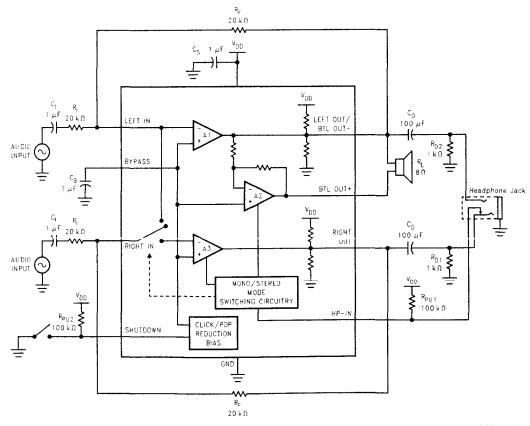
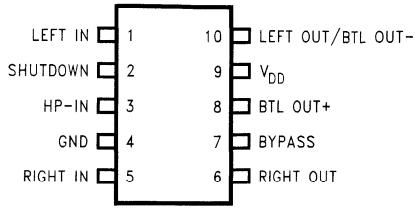
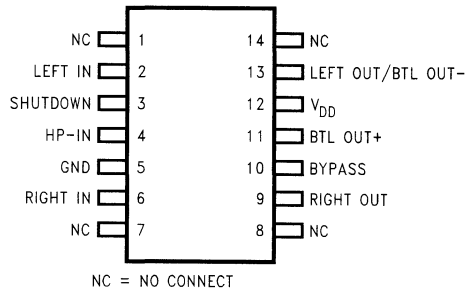


FIGURE 1. Typical Audio Amplifier Application Circuit

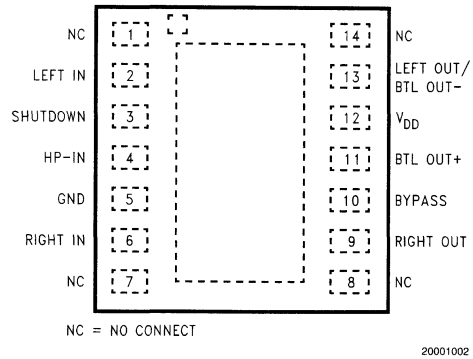
Connection Diagrams



Top View
10 Lead MSOP
Order Number LM4850MM
See NS Package Number MUB10A



Top View
14 Lead TSSOP
Order Number LM4850MT
See NS Package Number MTC14



Top View
14 Lead LLP
Order Number LM4850LD
See NS Package Number LDA14A

National Semiconductor

LM4860 Boomer® Audio Power Amplifier Series
1W Audio Power Amplifier with Shutdown Mode

General Description

The LM4860 is a bridge-connected audio power amplifier capable of delivering 1W of continuous average power to an 8Ω load with less than 1% THD+N over the audio spectrum from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4860 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4860 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism. It also includes two headphone control inputs and a headphone sense output for external monitoring.

The unity-gain stable LM4860 can be configured by external gain setting resistors for differential gains of up to 10 without the use of external compensation components. Higher gains may be achieved with suitable compensation.

Key Specifications

- THD+N at 1W continuous average output power into 8Ω: 1% (max)
- Instantaneous peak output power: >2W
- Shutdown current: 0.6µA (typ)

Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) packaging
- Compatible with PC power supplies
- Thermal shutdown protection circuitry
- Unity-gain stable
- External gain configuration capability
- Two headphone control inputs and headphone sensing output

Applications

- Personal computers
- Portable consumer products
- Cellular phones
- Self-powered speakers
- Toys and games

Typical Application

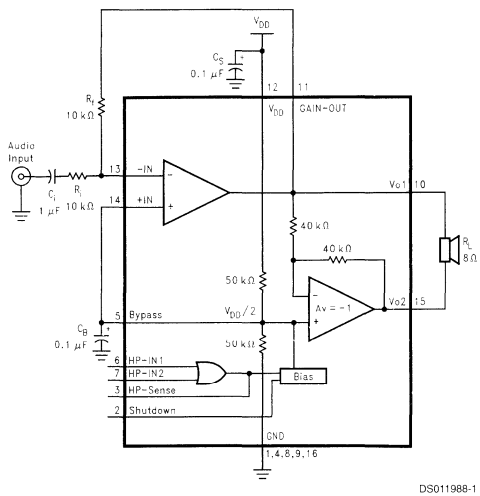
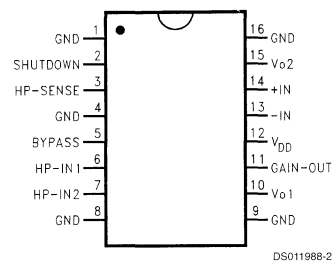


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



Top View
Order Number LM4860M
See NS Package Number M16A

National Semiconductor

LM4861 Boomer® Audio Power Amplifier Series
1.1W Audio Power Amplifier with Shutdown Mode

General Description

The LM4861 is a bridge-connected audio power amplifier capable of delivering 1.1W of continuous average power to an 8Ω load with 1% THD+N using a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4861 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is optimally suited for low-power portable systems.

The LM4861 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4861 can be configured by external gain-setting resistors for differential gains of up to 10 without the use of external compensation components. Higher gains may be achieved with suitable compensation.

Key Specifications

- THD+N for 1kHz at 1W continuous average output power into 8Ω — 1.0% (max)
- Output power at 10% THD+N at 1kHz into 8Ω — 1.5W (typ)
- Shutdown Current — 0.6µA (typ)

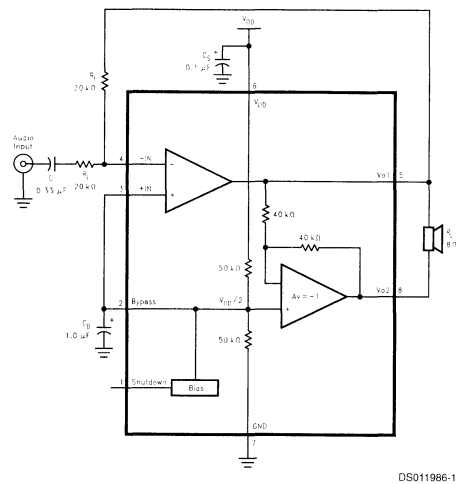
Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SO) packaging
- Compatible with PC power supplies
- Thermal shutdown protection circuitry
- Unity-gain stable
- External gain configuration capability

Applications

- Personal computers
- Portable consumer products
- Self-powered speakers
- Toys and games

Typical Application

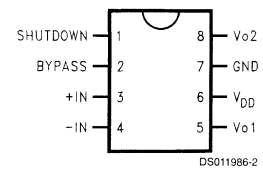


DS011986-1

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



DS011986-2

Top View
Order Number LM4861M
See NS Package Number M08A

National Semiconductor

LM4862 Boomer® Audio Power Amplifier Series
675 mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4862 is a bridge-connected audio power amplifier capable of delivering typically 675mW of continuous average power to an 8Ω load with 1% THD+N from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4862 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is optimally suited for low-power portable systems.

The LM4862 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4862 can be configured by external gain-setting resistors.

Key Specifications

- THD+N for 500mW continuous average output power at 1kHz into 8Ω — 1% (max)
- Output power at 10% THD+N at 1kHz into 8Ω — 825mW (typ)
- Shutdown Current — 0.7μA (typ)

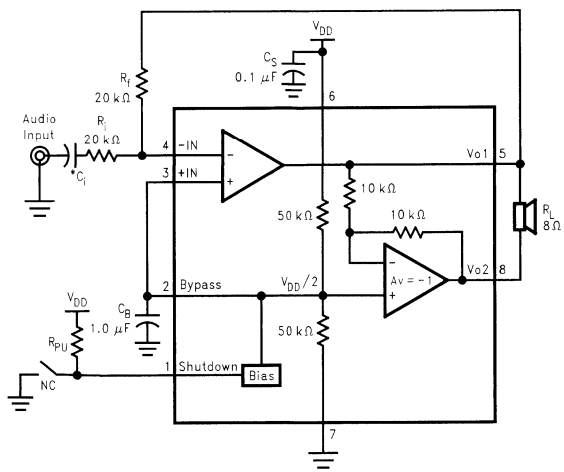
Features

- No output coupling capacitors, bootstrap capacitors or snubber circuits are necessary
- Small Outline or DIP packaging
- Unity-gain stable
- External gain configuration capability
- Pin compatible with LM4861

Applications

- Portable computers
- Cellular phones
- Toys and games

Typical Application

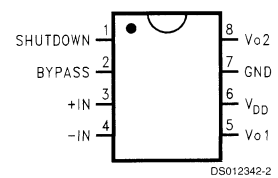


*Refer to the **Application Information** section for information concerning proper selection of the input coupling capacitor.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline and DIP Package



Top View
Order Number LM4862M, LM4862N
See NS Package Number M08A or N08E

National Semiconductor

LM4863 Boomer® Audio Power Amplifier Series
Dual 2.2W Audio Amplifier Plus Stereo Headphone Function

General Description

The LM4863 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.2W to a 4Ω load (Note 1) or 2.5W to a 3Ω load (Note 2) with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

Boomer audio power amplifiers were designed specifically to provide high quality output power from a surface mount package while requiring few external components. To simplify audio system design, the LM4863 combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The LM4863 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

Note 1: An LM4863MTE or LM4863LQ that has been properly mounted to a circuit board will deliver 2.2W into 4Ω. The other package options for the LM4863 will deliver 1.1W into 8Ω. See the Application Information sections for further information concerning the LM4863MTE and LM4863LQ.

Note 2: An LM4863MTE or LM4863LQ that has been properly mounted to a circuit board and forced-air cooled will deliver 2.5W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- LM4863LQ, 3Ω, 4Ω loads 2.5W(typ), 2.2W(typ)
- LM4863MTE, 3Ω, 4Ω loads 2.5W(typ), 2.2W(typ)
- LM4863MTE, 8Ω load 1.1W(typ)
- LM4863, 8Ω 1.1W(typ)
- Single-ended mode THD+N at 75mW into 32Ω 0.5%(max)
- Shutdown current 0.7μA(typ)
- Supply voltage range 2.0V to 5.5V

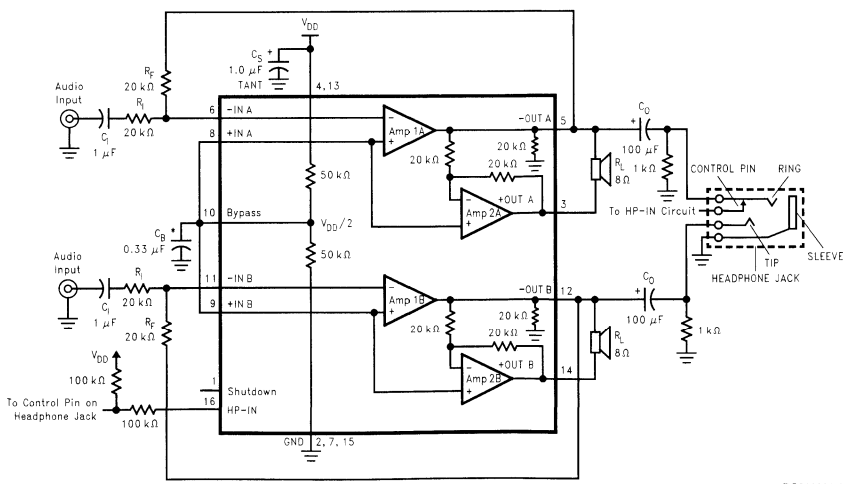
Features

- Stereo headphone amplifier mode
- "Click and pop" suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- SOIC, DIP, TSSOP and exposed-DAP TSSOP and LLP packages

Applications

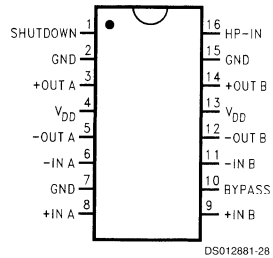
- Multimedia monitors
- Portable and desktop computers
- Portable televisions

Typical Application

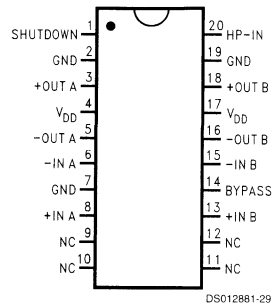


Note: Pin out shown for DIP and SO packages. Refer to the Connection Diagrams for the pinout of the TSSOP, Exposed-DAP TSSOP, and Exposed-DAP LLP packages.

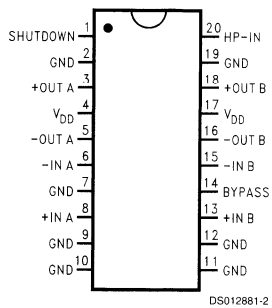
Connection Diagrams



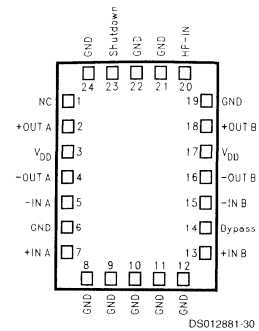
Top View
Order Number LM4863M, LM4863N
See NS Package Number M16B for SO
See NS Package Number N16E for DIP



Top View
Order Number LM4863MT
See NS Package Number MTC20 for TSSOP



Top View
Order Number LM4863MTE
See NS Package Number MXA20A for Exposed-DAP TSSOP



Top View
Order Number LM4863LQ
See NS Package Number LQA24A for Exposed-DAP LLP

National Semiconductor

LM4864 Boomer® Audio Power Amplifier Series
725mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4864 is a bridged audio power amplifier capable of delivering 725mW of continuous average power into an 8Ω load with 1% THD+N from a 5V power supply.

Boomer® audio power amplifiers were designed specifically to provide high quality output power from a low supply voltage while requiring a minimal amount of external components. Since the LM4864 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable applications.

The LM4864 features an externally controlled, low power consumption shutdown mode, and thermal shutdown protection.

The closed loop response of the unity-gain stable LM4864 can be configured by external gain-setting resistors. The device is available in multiple package types to suit various applications.

Key Specifications

- P_O at 1% THD+N with V_{DD} = 5V, 1kHz

LM4864LD, 4Ω load	625mW (typ)
LM4864LD, 8Ω load	725mW (typ)
LM4864M & LM4864N, 8Ω load	675mW (typ)
LM4864MM, 8Ω load (Note 10)	300mW (typ)
LM4864, 16Ω load	550mW (typ)

- Shutdown current 0.7µA (typ)

Features

- MSOP, SOP, DIP, and LD packaging
- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Thermal shutdown protection circuitry
- Unity-gain stable
- External gain configuration capability

Applications

- Cellular phones
- Personal computers
- General purpose audio

Typical Application

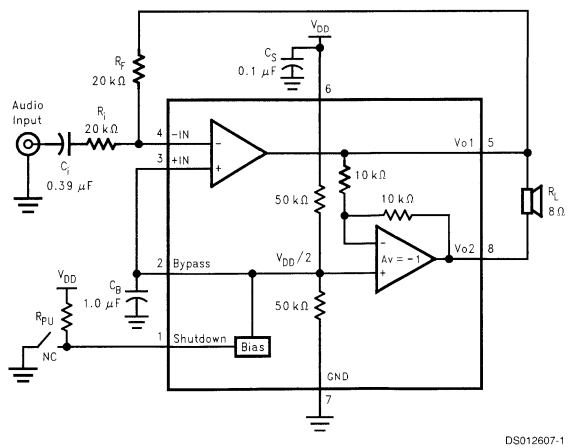
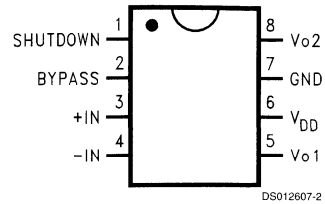


FIGURE 1. Typical Audio Amplifier Application Circuit

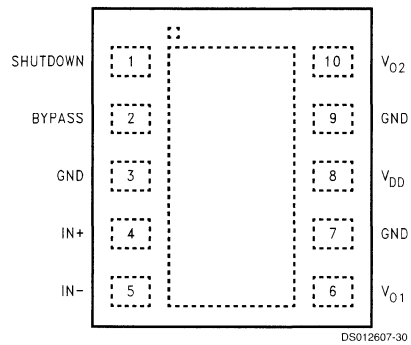
Connection Diagrams

MSOP, SOP, and DIP Package



Top View
Order Number LM4864MM,
LM4864M or LM4864N
See NS Package Number MUA08A,
M08A or N08E

LD Package



Top View
Order Number LM4864LD,
See NS Package Number LDA10A

National Semiconductor

LM4865 Boomer® Audio Power Amplifier Series

750 mW Audio Power Amplifier with DC Volume Control and Headphone Switch

General Description

The LM4865 is a mono bridged audio power amplifier with DC voltage volume control. The LM4865 is capable of delivering 750mW of continuous average power into an 8Ω load with less than 1% THD when powered by a 5V power supply. Switching between bridged speaker mode and headphone (single ended) mode is accomplished using the headphone sense pin. To conserve power in portable applications, the LM4865's micropower shutdown mode (I_Q = 0.7µA, typ) is activated when less than 300mV is applied to the DC Vol/$\overline{SD}$ pin.

Boomer audio power amplifiers are designed specifically to provide high power audio output while maintaining high fidelity. They require few external components and operate on low supply voltages.

Applications

- GSM phones and accessories, DECT, office phones
- Hand held radio
- Other portable audio devices

Key Specifications

■ P_O at 1.0% THD+N into 8Ω SO, micro SMD	750mW (typ)
■ P_O at 10% THD+N into 8Ω SO, micro SMD	1W (typ)
■ Shutdown current	0.7µA(typ)
■ Supply voltage range	2.7V to 5.5V

Features

- DC voltage volume control
- Headphone amplifier mode
- "Click and pop" suppression
- Shutdown control when volume control pin is low
- Thermal shutdown protection

Typical Application

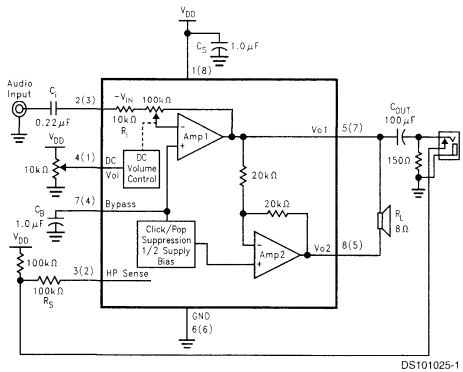
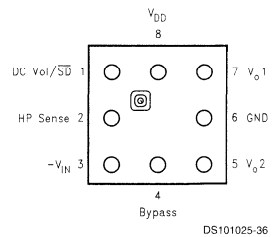


FIGURE 1. Typical Audio Amplifier Application Circuit
(Numbers in ( ) are specific to the micro SMD package)

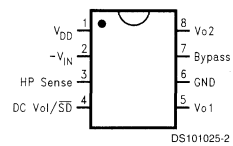
Connection Diagrams

micro SMD Package



Top View
Order Number LM4865IBP
See NS Package Number BPA08CFB

Small Outline Package (SO)
Mini Small Outline Package (MSOP)



Top View
Order Number LM4865M, LM4865MM
See NS Package Number M08A, MUA08A

National Semiconductor

LM4866 Boomer® Audio Power Amplifier Series
2.2W Stereo Audio Amplifier

General Description

The LM4866 is a bridge-connected (BTL) stereo audio power amplifier which, when connected to a 5V supply, delivers 2.2W to a 4Ω load (Note 1) or 2.5W to a 3Ω load (Note 2) with less than 1.0% THD+N.

With the LM4866 packaged in the LLP, the customer benefits include low thermal impedance, low profile, and small size. This package minimizes PCB area and maximizes output power.

The LM4866 features an externally controlled, low-power consumption shutdown mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

Note 1: An LM4866MTE or LM4866LQ that has been properly mounted to a circuit board will deliver 2.2W into 4Ω. The other package options for the LM4866 will deliver 1.1W into 8Ω. See the Application Information sections for further information concerning the LM4866MTE and LM4866LQ.

Note 2: An LM4866MTE or LM4866LQ that has been properly mounted to a circuit board will deliver 2.5W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- LM4866LQ, 3Ω, 4Ω loads — 2.5W(typ), 2.2W(typ)
- LM4866MTE, 3Ω, 4Ω loads — 2.5W(typ), 2.2W(typ)
- LM4866MTE, 8Ω load — 1.1W(typ)
- LM4866MT, 8Ω load — 1.1W(typ)
- Shutdown current — 0.7μA(typ)
- Supply voltage range — 2.0V to 5.5V

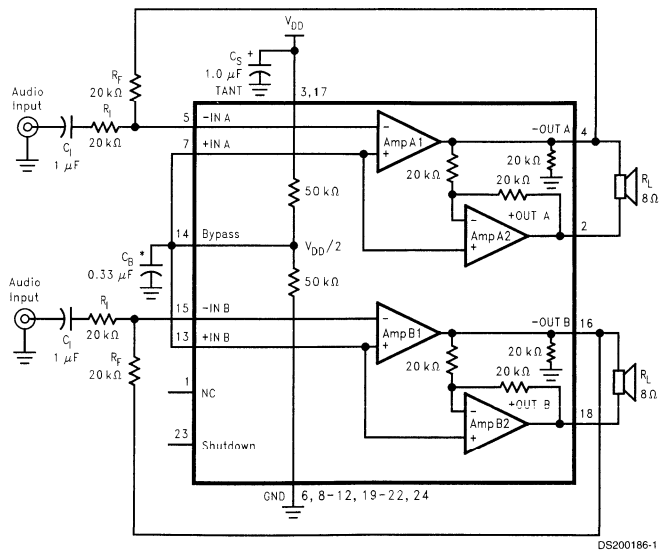
Features

- Stereo BTL amplifier mode
- "Click and pop" suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- TSSOP and Exposed-DAP LLP packages

Applications

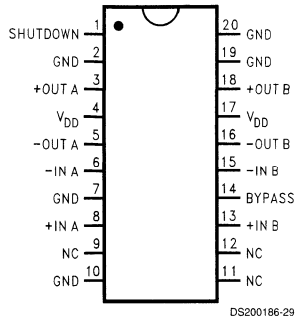
- Multimedia monitors
- Portable and desktop computers
- Portable televisions

Typical Application

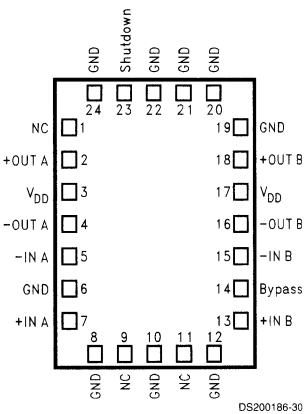


Note: Pin out shown for LLP package. Refer to the Connection Diagrams for the pinout of the TSSOP package.

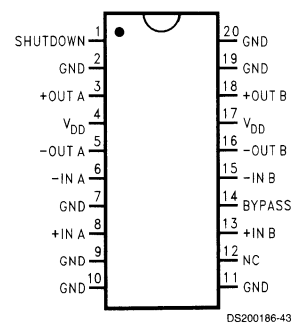
Connection Diagrams



Top View
Order Number LM4866MT
See NS Package Number MTC20 for TSSOP



Top View
Order Number LM4866LQ
See NS Package Number LQA24A for Exposed-DAP LLP



Top View
Order Number LM4866MTE
See NS Package Number MXA20A for Exposed-DAP TSSOP

National Semiconductor

LM4867 Boomer® Audio Power Amplifier Series
Output-Transient-Free Dual 2.1W Audio Amplifier Plus No Coupling Capacitor Stereo Headphone Function

General Description

The LM4867 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.1W to a 4Ω load (Note 1) or 2.4W to a 3Ω load (Note 2) with less than 1.0% THD+N. The LM4867 uses advanced, latest generation circuitry to eliminate all traces of clicks and pops when the supply voltage is first applied. The amplifier has a headphone-amplifier-select input pin. It is used to switch the amplifiers from bridge to single-ended mode for driving headphones. A new circuit topology eliminates headphone output coupling capacitors. A MUX control pin allows selection between the two sets of stereo input signals. The MUX control can also be used to select between two different customer-specified closed-loop responses.

Boomer audio power amplifiers are designed specifically to provide high quality output power from a surface mount package and require few external components. To simplify audio system design, the LM4867 combines dual bridge speaker amplifiers and stereo headphone amplifiers in one package.

The LM4867 features an externally controlled power-saving micropower shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection.

Note 1: An LM4867LQ or LM4867MTE that has been properly mounted to a circuit board will deliver 2.1W into 4Ω. The Mux control can also be used to select two different closed-loop responses. LM4867MT will deliver 1.1W into 8Ω. See the Application Information sections for further information concerning the LM4867LQ and the LM4867MT.

Note 2: An LM4867LQ or LM4867MTE that has been properly mounted to a circuit board and forced-air cooled will deliver 2.4W into 3Ω.

Key Specifications

- P_O at 1% THD+N
  - LM4867LQ, 3Ω load 2.4W (typ)
  - LM4867LQ, 4Ω load 2.1W (typ)
  - LM4867MTE, 4Ω 1.9W (typ)
  - LM4867MT, 8Ω 1.1W (typ)
- Single-ended mode - THD+N at 75mW into 32Ω 0.5% (max)
- Shutdown current 0.7µA (typ)

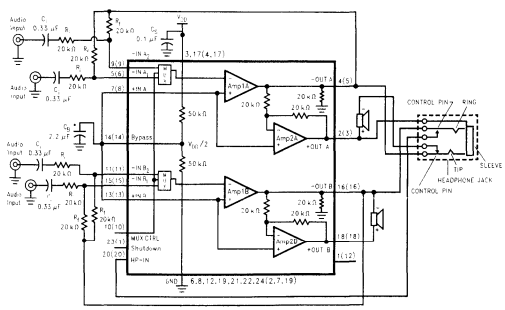
Features

- Advanced "click and pop" suppression circuitry
- Eliminates headphone amplifier output coupling capacitors
- Stereo headphone amplifier mode
- Input mux control and two separate inputs per channel
- Thermal shutdown protection circuitry
- LLP, TSSOP, and exposed-DAP TSSOP packaging available

Applications

- Multimedia monitors
- Portable and desktop computers
- Portable audio systems

Typical Application



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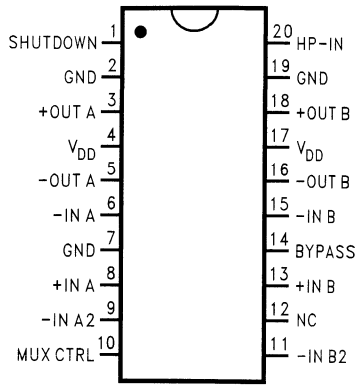
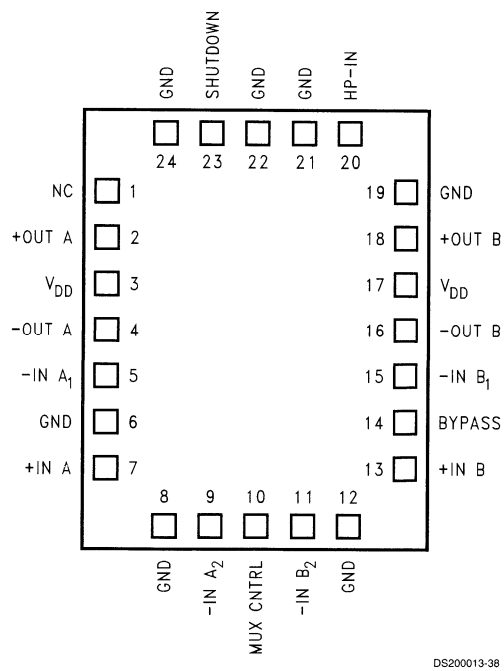
* Refer to the Application Information section titled PROPER SELECTION OF EXTERNAL COMPONENTS for details concerning the value of C_B.

FIGURE 1. Typical Audio Amplifier Application Circuit (Pin out shown for the 24-pin Exposed-DAP LLP package. Numbers in ( ) are for the 20-pin MTE and MT packages.)

Connection Diagrams



Top View
Order Number LM4867MT, LM4867MTE
See NS Package Number MTC20 for TSSOP
See NS Package Number MXA20A for Exposed-DAP TSSOP



Top View
Order Number LM4867LQ
See NS Package Number LQA24A for Exposed-DAP LLP

National Semiconductor

LM4868 Boomer® Audio Power Amplifier Series
Output-Transient-Free Dual 2.1W Audio Amplifier Plus No Coupling Capacitor Stereo Headphone Function

General Description

The LM4868 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.1W to a 4Ω load (Note 1) or 2.4W to a 3Ω load (Note 2) with less than 1.0% THD+N. The LM4868 uses advanced, latest generation circuitry to eliminate all traces of clicks and pops when the supply voltage is first applied. The amplifier has a headphone-amplifier-select input pin. It is used to switch the amplifiers from bridge to single-ended mode for driving headphones. A new circuit topology eliminates headphone output coupling capacitors. A MUX control pin allows selection between the two sets of stereo input signals. The MUX control can also be used to select between two different customer-specified closed-loop responses.

Boomer audio power amplifiers are designed specifically to provide high quality output power from a surface mount package and require few external components. To simplify audio system design, the LM4868 combines dual bridge speaker amplifiers and stereo headphone amplifiers in one package.

The LM4868 features an externally controlled power-saving micropower shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection.

Note 1: An LM4868LQ or LM4868MTE that has been properly mounted to a circuit board will deliver 2.1W into 4Ω. The Mux control can also be used to select two different closed-loop responses. LM4868MT will deliver 1.1W into 8Ω. See the Application Information sections for further information concerning the LM4868LQ and the LM4868MT.

Note 2: An LM4868LQ or LM4868MTE that has been properly mounted to a circuit board and forced-air cooled will deliver 2.4W into 3Ω.

Key Specifications

- P_O at 1% THD+N
- LM4868LQ, 3Ω load 2.4W (typ)
- LM4868LQ, 4Ω load 2.1W (typ)
- LM4868MTE, 4Ω 1.9W (typ)
- LM4868MT, 8Ω 1.1W (typ)
- Single-ended mode - THD+N at 75mW into 32Ω 0.5% (max)
- Shutdown current 0.7µA (typ)

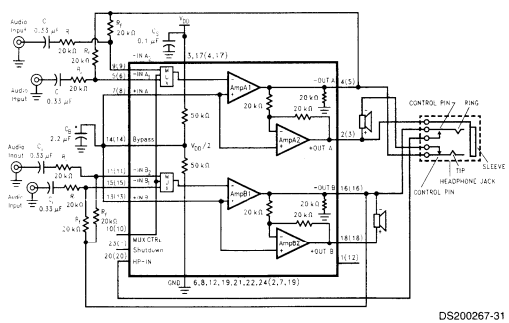
Features

- Advanced "click and pop" suppression circuitry
- Eliminates headphone amplifier output coupling capacitors
- Stereo headphone amplifier mode
- Input mux control and two separate inputs per channel
- Thermal shutdown protection circuitry
- LLP, TSSOP, and exposed-DAP TSSOP packaging available

Applications

- Multimedia monitors
- Portable and desktop computers
- Portable audio systems

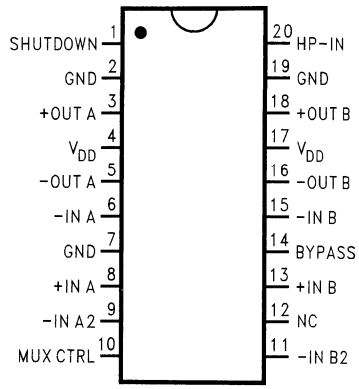
Typical Application



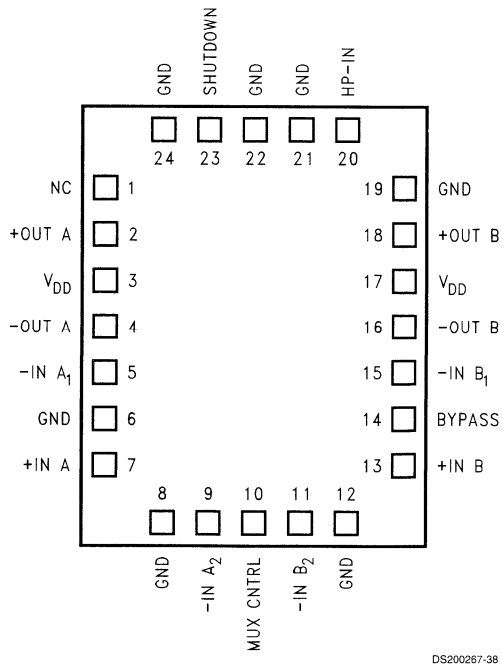
[1] Refer to the Application Information section titled PROPER SELECTION OF EXTERNAL COMPONENTS for details concerning the value of C_B.

FIGURE 1. Typical Audio Amplifier Application Circuit
(Pin out shown for the 24-pin Exposed-DAP LLP package. Numbers in ( ) are for the 20-pin MTE and MT packages.)

Connection Diagrams



Top View
Order Number LM4868MT, LM4868MTE
See NS Package Number MTC20 for TSSOP
See NS Package Number MXA20A for Exposed-DAP TSSOP



Top View
Order Number LM4868LQ
See NS Package Number LQA24A for Exposed-DAP LLP

National Semiconductor

LM4870 Boomer® Audio Power Amplifier Series
1.1W Audio Power Amplifier with Shutdown Mode

General Description

The LM4870 is a bridge-connected audio power amplifier capable of delivering 1.1W of continuous average power to an 8Ω load with less than 0.5% THD+N over the audio spectrum from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal number of external components. Since the LM4870 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4870 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism. It also includes two headphone control inputs and a headphone sense output for external monitoring. The LM4870 is unity-gain stable and the gain is set using external resistors.

Key Specifications

- THD+N at 1W into 8Ω 0.5% (max)
- Output power into 8Ω at 1kHz at 10% THD+N 1.5W (typ)
- Shutdown Current 0.6µA (typ)

Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Small Outline (SOIC) power packaging
- Unity-gain stable
- External gain configuration capability

Applications

- Personal computers
- Desktop computers
- Low voltage audio system

Typical Application

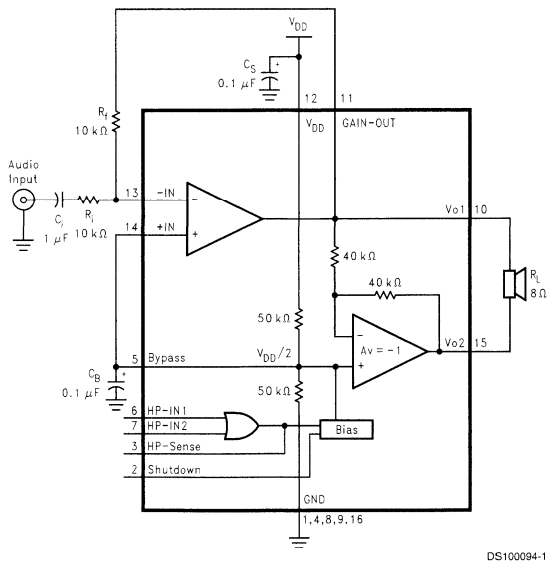
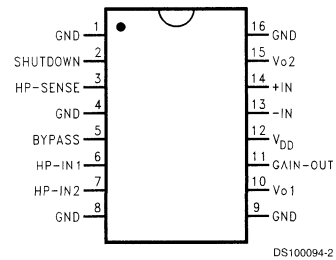


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline Package



Top View
Order Number LM4870M
See NS Package Number M16A

National Semiconductor

LM4871 Boomer® Audio Power Amplifier Series
3W Audio Power Amplifier with Shutdown Mode

General Description

The LM4871 is a mono bridged audio power amplifier capable of delivering 3W of continuous average power into a 3Ω load with less than 10% THD when powered by a 5V power supply (Note 1). To conserve power in portable applications, the LM4871's micropower shutdown mode (I_Q = 0.6μA, typ) is activated when V_{DD} is applied to the SHUTDOWN pin.

Boomer audio power amplifiers are designed specifically to provide high power, high fidelity audio output. They require few external components and operate on low supply voltages from 2.0V to 5.5V. Since the LM4871 does not require output coupling capacitors, bootstrap capacitors, or snubber networks, it is ideally suited for low-power portable systems that require minimum volume and weight.

Additional LM4871 features include thermal shutdown protection, unity-gain stability, and external gain set.

Note 1: An LM4871LD that has been properly mounted to a circuit board will deliver 3W into 3Ω (at 10% THD). The other package options for the LM4871 will deliver 1.5W into 8Ω (at 10% THD). See the **Application Information** sections for further information concerning the LM4871LD, LM4871MM, LM4871M, and the LM4871N.

Key Specifications

- PO at 10% THD+N, 1kHz
  - LM4871LD: 3Ω , 4Ω loads — 3W (typ), 2.5W (typ)
  - All other LM4871 packages: 8Ω load — 1.5W (typ)
- Shutdown current — 0.6μA (typ)
- Supply voltage range — 2.0V to 5.5V
- THD at 1kHz at 1W continuous average output power into 8Ω — 0.5% (max)

Features

- No output coupling capacitors, bootstrap capacitors, or snubber circuits required
- Unity-gain stable
- LLP, MSOP, SO, or DIP packaging
- External gain configuration capability
- Pin compatible with the LM4861

Applications

- Portable computers
- Desktop computers
- Low voltage audio systems

Typical Application

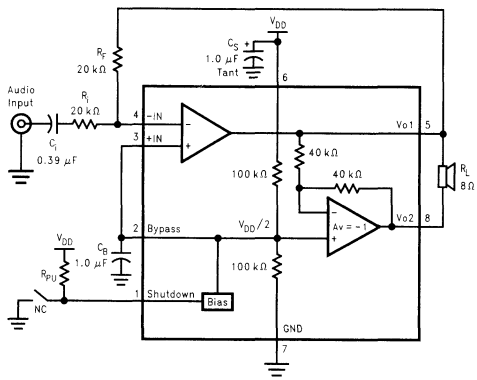
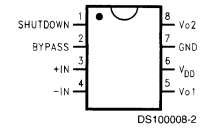


FIGURE 1. Typical Audio Amplifier Application Circuit

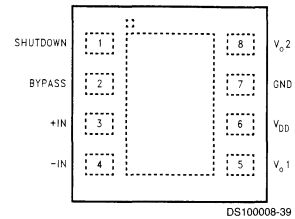
Connection Diagrams

MSOP, Small Outline, and DIP Package



Top View
Order Number LM4871MM, LM4871M, or LM4871N
See NS Package Number MUA08A, M08A, or N08E

LLP Package



Top View
Order Number LM4871LD
See NS Package Number LDC08A

National Semiconductor

LM4872 Boomer® Audio Power Amplifier Series
1 Watt Audio Power Amplifier in micro SMD package

General Description

The LM4872 is a bridge-connected audio power amplifier capable of delivering 1 W of continuous average power to an 8Ω load with less than .2% (THD) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4872 does not require output coupling capacitors or bootstrap capacitors. It is optimally suited for low-power portable applications.

The LM4872 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4872 can be configured by external gain-setting resistors.

Key Specifications

- Power Output at 0.2% THD 1W (typ)
- Shutdown Current 0.01µA (typ)

Features

- micro SMD package (see App. note AN-1112)
- 5V - 2V operation
- No output coupling capacitors or bootstrap capacitors.
- Unity-gain stable
- External gain configuration capability

Applications

- Cellular Phones
- Portable Computers
- Low Voltage Audio Systems

Typical Application

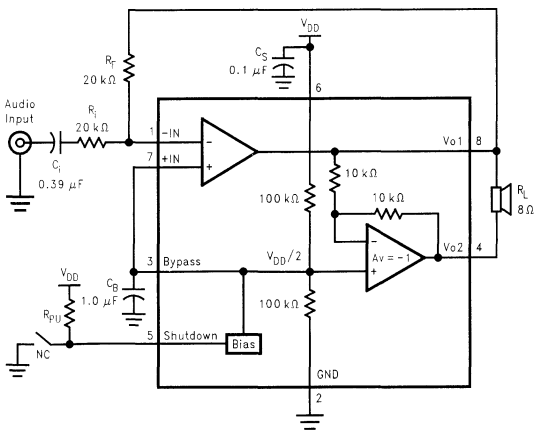
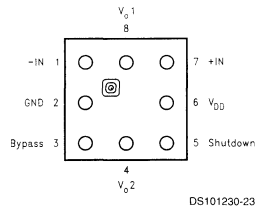


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

8 Bump micro SMD



Top View
Order Number LM4872IBP, LM4872IBPX
See NS Package Number BPA08B6B

National Semiconductor

LM4873 Boomer® Audio Power Amplifier Series
Dual 2.1W Audio Amplifier Plus Stereo Headphone Function

General Description

The LM4873 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.1W to a 4Ω load (Note 1) or 2.4W to a 3Ω load (Note 2) with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones. A MUX control pin allows selection between the two stereo sets of amplifier inputs. The MUX control can also be used to select two different closed-loop responses.

Boomer audio power amplifiers were designed specifically to provide high quality output power from a surface mount package while requiring few external components. To simplify audio system design, the LM4873 combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The LM4873 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce "clicks and pops" during device turn-on.

Note 1: An LM4873MTE-1, LM4873MTE, or LM4873LQ that has been properly mounted to a circuit board will deliver 2.1W into 4Ω. The other package options for the LM4873 will deliver 1.1W into 8Ω. See the Application Information sections for further information concerning the LM4873MTE-1, LM4873MTE, and the LM4873LQ.

Note 2: An LM4873MTE-1, LM4873MTE, or LM4873LQ that has been properly mounted to a circuit board and forced-air cooled will deliver 2.4W into 3Ω.

Key Specifications

- P_O at 1% THD+N
  - LM4873LQ, 3Ω, 4Ω loads 2.4W(typ), 2.1W(typ)
  - LM4873MTE-1, 3Ω, 4Ω loads 2.4W(typ), 2.1W(typ)
  - LM4873IBL, 8Ω load 1.1W(typ)
  - LM4873MTE, 4Ω 1.9W(typ)
  - LM4873, 8Ω 1.1W(typ)
- Single-ended mode THD+N at 75mW into 32Ω 0.5%(max)
- Shutdown current 0.7μA(typ)
- Supply voltage range 2V to 5.5V

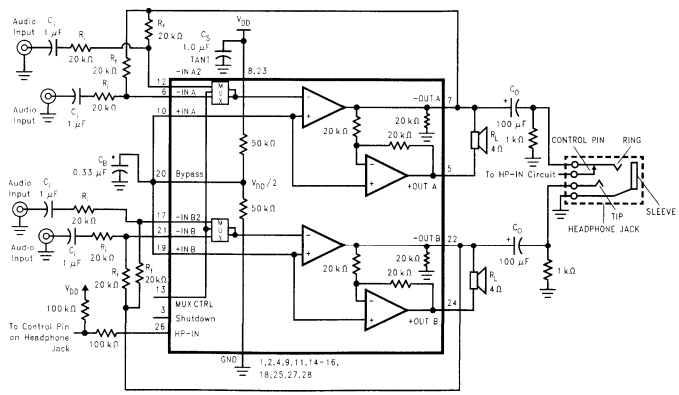
Features

- Input mux control and two separate inputs per channel
- Stereo headphone amplifier mode
- "Click and pop" suppression circuitry
- Thermal shutdown protection circuitry
- PCB area-saving micro SMD package
- TSSOP and exposed-DAP TSSOP and LLP packages

Applications

- Multimedia monitors
- Portable and desktop computers
- Portable audio systems

Typical Application



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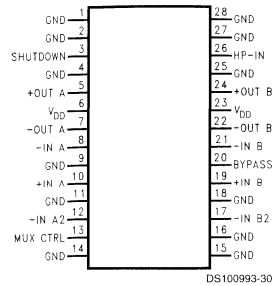
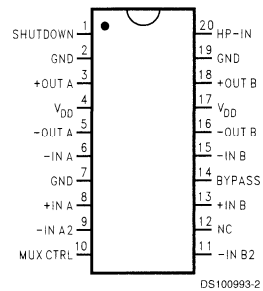
Note: Pin out shown for the 28-pin Exposed-DAP TSSOP package. Refer to the Connection Diagrams for the pin out of the 20-pin Exposed-DAP TSSOP, Exposed-DAP LLP, and micro SMD packages.

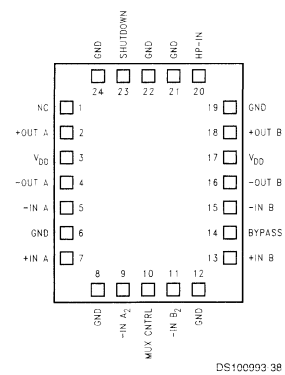
Connection Diagrams



Top View
Order Number LM4873MTE-1
See NS Package Number MXA28A for Exposed-DAP TSSOP

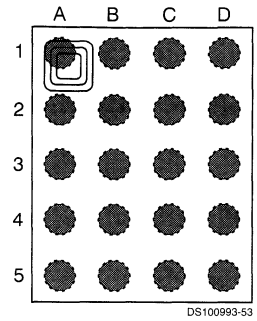


Top View
Order Number LM4873MT, LM4873MTE
See NS Package Number MTC20 for TSSOP
See NS Package Number MXA20A for Exposed-DAP TSSOP



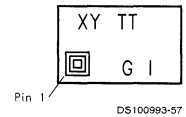
Top View
Order Number LM4873LQ
See NS Package Number LQA24A for Exposed-DAP LLP

Connection Diagrams (Continued)



Top View (Bump-side down)
Order Number LM4873IBL
See NS Package Number BPA20AAB for micro SMD

micro SMD Marking



Top View
XY - Date Code
TT - Die Traceability
G - Boomer Family
I - LM4873IBL

LM4873IBP Pin Designation

Pin (Bump) Number	Pin (Bump) Function	Pin (Bump) Number	Pin (Bump) Function
1A	-IN A_1	3C	V_{DD}
1B	-IN A_2	3D	+IN B
1C	-IN B_2	4A	+OUT A
1D	-IN B_1	4B	GND
2A	-OUT A	4C	GND
2B	GND	4D	+OUT B
2C	GND	5A	MUX CTRL
2D	-OUT B	5B	SHUTDOWN
3A	+IN A	5C	HP-IN
3B	V_{DD}	5D	BYPASS

National Semiconductor

LM4876 Boomer® Audio Power Amplifier Series
1.1W Audio Power Amplifier with Logic Low Shutdown

General Description

The LM4876 is a single 5V supply bridge-connected audio power amplifier capable of delivering 1.1W (typ) of continuous average power to an 8Ω load with 0.5% THD+N.

Like other audio amplifiers in the Boomer series, the LM4876 is designed specifically to provide high quality output power with a minimal amount of external components. The LM4876 does not require output coupling capacitors, bootstrap capacitors, or snubber networks. It is perfectly suited for low-power portable systems.

The LM4876 features an active low externally controlled, micro-power shutdown mode. Additionally, the LM4876 features an internal thermal shutdown protection mechanism. For PCB space efficiency, the LM4876 is available in MSOP and SO surface mount packages.

The unity-gain stable LM4876's closed loop gain is set using external resistors.

Key Specifications

- THD+N at 1kHz for 1W continuous average output power into 8Ω — 0.5% (max)
- Output power at 1kHz into 8Ω with 10% THD+N — 1.5W (typ)
- Shutdown current — 0.01μA (typ)
- Supply voltage range — 2.0V to 5.5V

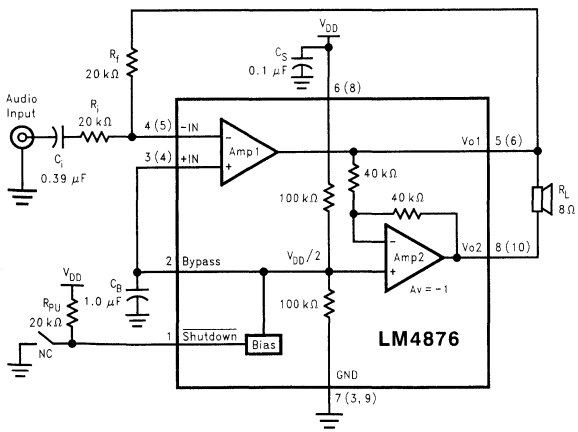
Features

- Does not require output coupling capacitors, bootstrap capacitors, or snubber circuits
- 10-pin MSOP and 8-pin SO packages
- Unity-gain stable
- External gain set

Applications

- Mobile Phones
- Portable Computers
- Desktop Computers
- Low-Voltage Audio Systems

Typical Application

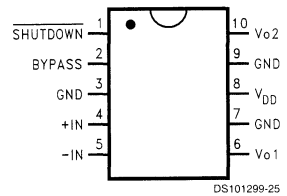


DS101299-1

FIGURE 1. Typical LM4876 Audio Amplifier Application Circuit. Numbers in ( ) are specific to the 10-pin MSOP package

Connection Diagrams

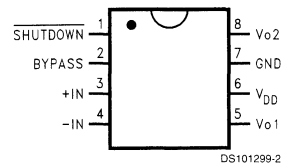
Mini Small Outline MSOP Package



DS101299-25

Top View
Order Number LM4876MM
See NS Package Number MUB10A

Small Outline SO Package



DS101299-2

Top View
Order Number LM4876M
See NS Package Number M08A

National Semiconductor

LM4877 Boomer® Audio Power Amplifier Series

1 Watt Audio Power Amplifier in micro SMD package with Shutdown Logic Low

General Description

The LM4877 is a bridge-connected audio power amplifier capable of delivering 1 W of continuous average power to an 8Ω load with less than .2% (THD) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4877 does not require output coupling capacitors or bootstrap capacitors. It is optimally suited for low-power portable applications.

The LM4877 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4877 can be configured by external gain-setting resistors.

Key Specifications

- Power Output at 0.2% THD 1W (typ)
- Shutdown Current 0.01μA (typ)

Features

- micro SMD package (see App. note AN-1112)
- 5V - 2V operation
- No output coupling capacitors or bootstrap capacitors.
- Unity-gain stable
- External gain configuration capability

Applications

- Cellular Phones
- Portable Computers
- Low Voltage Audio Systems

Typical Application

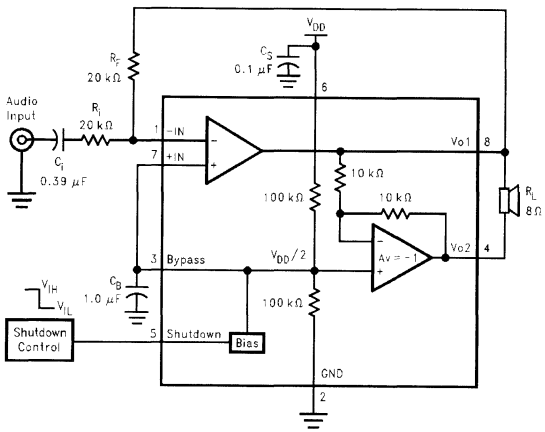
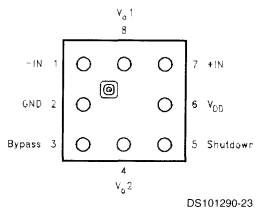


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

8 Bump micro SMD



Top View
Order Number LM4877IBP, LM4877IBPX
See NS Package Number BPA08B6B

National Semiconductor

LM4878 Boomer® Audio Power Amplifier Series
1 Watt Audio Power Amplifier in micro SMD package with Shutdown Logic Low

General Description

The LM4878 is a bridge-connected audio power amplifier capable of delivering 1 W of continuous average power to an 8Ω load with less than .2% (THD) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. Since the LM4878 does not require output coupling capacitors or bootstrap capacitors. It is optimally suited for low-power portable applications.

The LM4878 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4878 can be configured by external gain-setting resistors.

Key Specifications

- Power Output at 0.2% THD 1 W (typ)
- Shutdown Current 0.01 µA (typ)

Features

- Internal pulldown resistor on shutdown.
- micro SMD package (see App. note AN-1112)
- 5V - 2V operation
- No output coupling capacitors or bootstrap capacitors.
- Unity-gain stable
- External gain configuration capability

Applications

- Cellular Phones
- Portable Computers
- Low Voltage Audio Systems

Typical Application

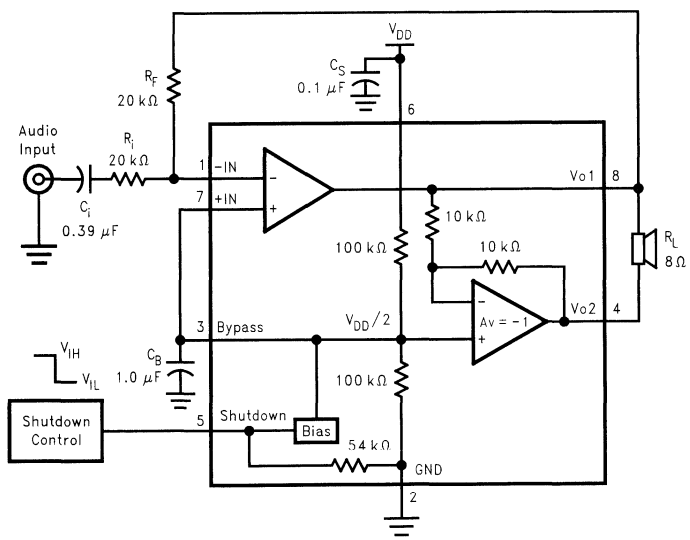
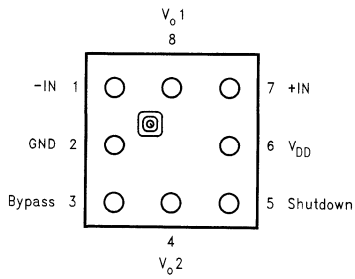


FIGURE 1. Typical Audio Amplifier Application Circuit

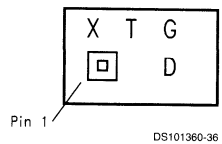
Connection Diagrams

8 Bump micro SMD



Top View
Order Number LM4878IBP, LM4878IBPX
See NS Package Number BPA08B6B

micro SMD Marking



Top View
X - Date Code
T - Die Traceability
G - Boomer Family
D - LM4878IBP

National Semiconductor

LM4879 Boomer® Audio Power Amplifier Series
1.1 Watt Audio Power Amplifier

General Description

The LM4879 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1.1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4879 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for lower-power portable applications where minimal space and power consumption are primary requirements.

The LM4879 features a low-power consumption global shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4879 features an internal thermal shutdown protection mechanism.

The LM4879 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4879 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- PSRR at 5V, 3V, & 217Hz — 62dB (typ)
- Power Output at 5V & 1% THD — 1.1W (typ)
- Power Output at 3V & 1% THD — 350mW (typ)
- Shutdown Current — 0.1μA (typ)

Features

- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity gain stable
- Ultra low current shutdown mode
- Fast turn on: 80mS (typ), 110mS (max) with 1.0μF capacitor
- BTL output can drive capacitive loads up to 100pF
- Advanced pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2V - 5.0V operation
- Available in space-saving μSMD and MSOP packages

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

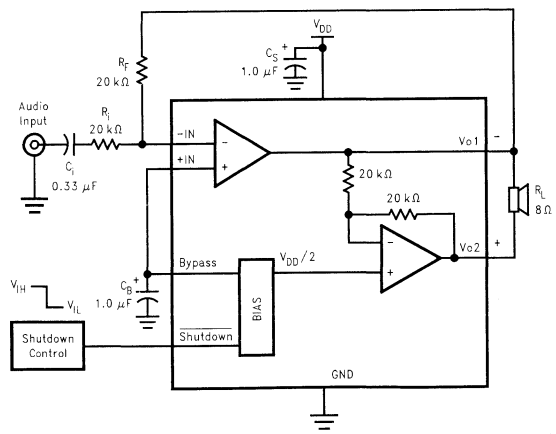
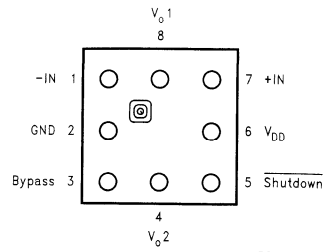


FIGURE 1. Typical Audio Amplifier Application Circuit

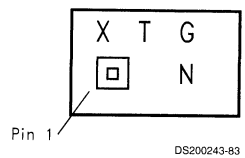
Connection Diagrams

8 Bump micro SMD



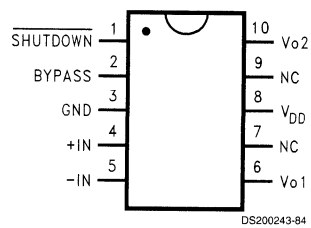
Top View
Order Number LM4879IBP, LM4879IBPX
See NS Package Number BPA08DDB

8 Bump micro SMD Marking



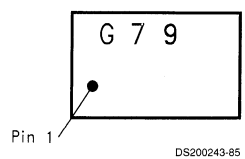
Top View
X - Date Code
T - Die Traceability
G - Boomer Family
N- LM4879IBP

Mini Small Outline (MSOP) Package



Top View
NC = No Connect
Order Number LM4879MM
See NS Package Number MUB10A

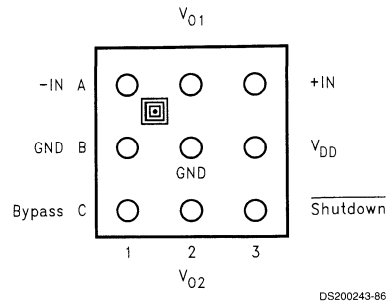
MSOP Marking



Top View
G - Boomer Family
79-LM4879MM

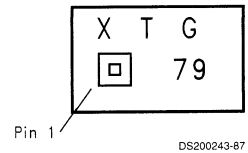
Connection Diagrams (Continued)

9 Bump micro SMD



Top View
Order Number LM4879IBL, LM4879IBLX
See NS package Number BLA09AAB

9 Bump micro SMD Marking



Top View
X - Date Code
T - Die Traceability
G - Boomer Family
79 - LM4879IBL

National Semiconductor

LM4880 Boomer® Audio Power Amplifier Series
Dual 250 mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4880 is a dual audio power amplifier capable of delivering typically 250mW per channel of continuous average power to an 8Ω load with 0.1% THD+N using a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging.

Since the LM4880 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4880 features an externally controlled, low-power consumption shutdown mode, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4880 can be configured by external gain-setting resistors.

Key Specifications

- THD+N at 1kHz at 200mW continuous average output power into 8Ω: 0.1% (max)
- THD+N at 1kHz at 85mW continuous average output power into 32Ω: 0.1% (typ)
- Output power at 10% THD+N at 1kHz into 8Ω: 325mW (typ)
- Shutdown current: 0.7μA (typ)
- 2.7V to 5.5V supply voltage range

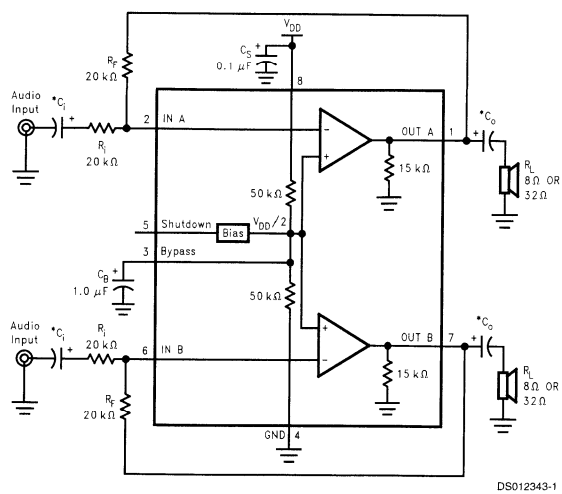
Features

- No bootstrap capacitors or snubber circuits are necessary
- Small Outline (SO) and DIP packaging
- Unity-gain stable
- External gain configuration capability

Applications

- Headphone Amplifier
- Personal Computers
- CD-ROM Players

Typical Application

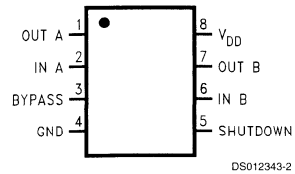


*Refer to the **Application Information** section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

Small Outline and DIP Packages



Top View
Order Number LM4880M or LM4880N
See NS Package Number M08A for SO
or NS Package Number N08E for DIP

National Semiconductor

LM4881 Boomer® Audio Power Amplifier Series

Dual 200 mW Headphone Amplifier with Shutdown Mode

General Description

The LM4881 is a dual audio power amplifier capable of delivering 200mW of continuous average power into an 8Ω load with 0.1% THD+N from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4881 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4881 features an externally controlled, low power consumption shutdown mode which is virtually clickless and popless, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4881 can be configured by external gain-setting resistors.

Key Specifications

- THD+N at 1kHz at 125mW continuous average output power into 8Ω — 0.1% (max)
- THD+N at 1kHz at 75mW continuous average output power into 32Ω — 0.02% (typ)
- Output power at 10% THD+N at 1kHz into 8Ω — 300mW (typ)
- Shutdown Current — 0.7µA (typ)
- Supply voltage range — 2.7V to 5.5V

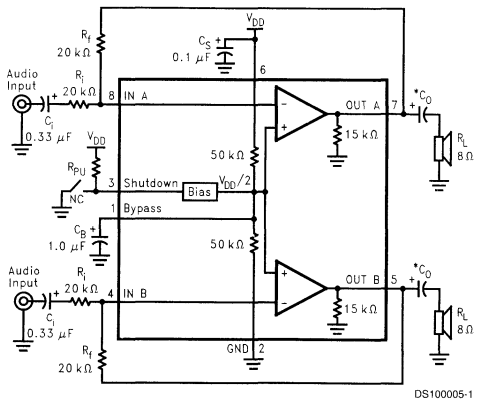
Features

- MSOP surface mount packaging
- Unity-gain stable
- External gain configuration capability
- Thermal shutdown protection circuitry
- No bootstrap capacitors, or snubber circuits are necessary

Applications

- Headphone Amplifier
- Personal Computers
- Microphone Preamplifier

Typical Application

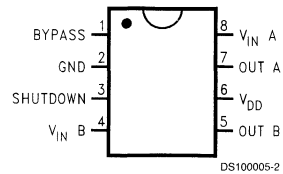


*Refer to the **Application Information** Section for information concerning proper selection of the input and output coupling capacitors.

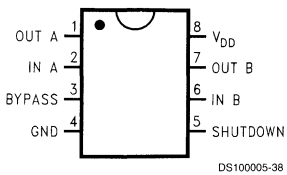
FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

MSOP Package



SOP and DIP Package



Top View
Order Number LM4881MM, LM4881M, or LM4881N
See NS Package Number MUA08A, M08A, or N08E

National Semiconductor

LM4882 Boomer® Audio Power Amplifier Series
250mW Audio Power Amplifier with Shutdown Mode

General Description

The LM4882 is a single-ended audio power amplifier capable of delivering 250mW of continuous average power into an 8Ω load with 1% THD+N from a 5V power supply.

Boomer® audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4882 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

The LM4882 features an externally controlled, low power consumption shutdown mode which is virtually clickless and popless, as well as an internal thermal shutdown protection mechanism.

The unity-gain stable LM4882 can be configured by external gain-setting resistors.

Key Specifications

- THD+N at 1kHz at 250mW continuous average output power into 8Ω — 1.0% (max)
- Output Power at 1% THD+N at 1kHz into 4Ω — 380mW (typ)
- THD+N at 1kHz at 85mW continuous average output power into 32Ω — 0.1% (typ)
- Shutdown Current — 0.7µA (typ)

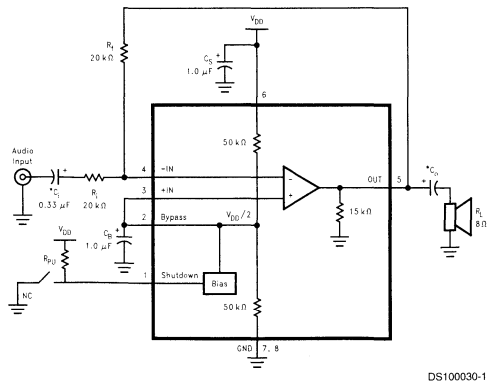
Features

- MSOP surface mount packaging
- "Click and Pop" Suppression Circuitry
- Supply voltages from 2.4V–5.5V
- Operating Temperature −40°C to 85°C
- Unity-gain stable
- External gain configuration capability
- No bootstrap capacitors, or snubber circuits are necessary

Applications

- Personal Computers
- Cellular Phones
- General Purpose Audio

Typical Application

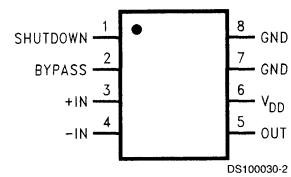


*Refer to the **Application Information** Section for information concerning proper selection of the input and output coupling capacitors.

FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagram

MSOP and SOIC Package



Top View
Order Number LM4882MM or LM4882M
See NS Package Number MUA08A or M08A

National Semiconductor

LM4890 Boomer® Audio Power Amplifier Series
1 Watt Audio Power Amplifier

General Description

The LM4890 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4890 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4890 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4890 features an internal thermal shutdown protection mechanism.

The LM4890 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4890 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- PSRR at 217Hz, V_{DD} = 5V (Fig. 1) 62dB(typ.)
- Power Output at 5.0V & 1% THD 1W(typ.)
- Power Output at 3.3V & 1% THD 400mW(typ.)
- Shutdown Current 0.1μA(typ.)

Features

- Available in space-saving packages: micro SMD, MSOP, SOIC, and LLP
- Ultra low current shutdown mode
- BTL output can drive capacitive loads
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

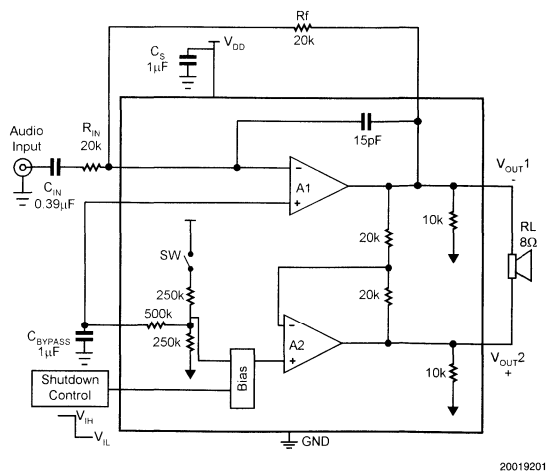
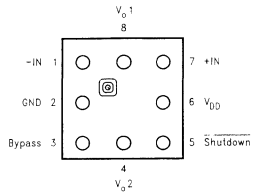


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

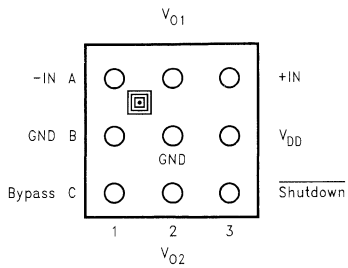
8 Bump micro SMD



20019223

Top View
Order Number LM4890IBP, LM4890IBPX
See NS Package Number BPA08DDB

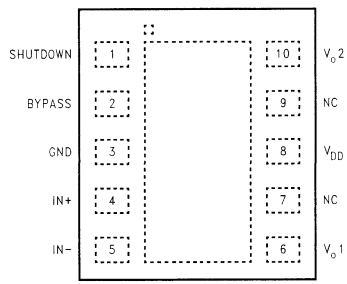
9 Bump micro SMD



200192C1

Top View
Order Number LM4890IBL, LM4890IBLX
See NS Package Number BLA09AAB

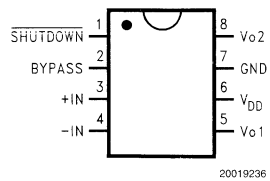
LLP Package



200192C7

Top View
Order Number LM4890LD
See NS Package Number LDA10B

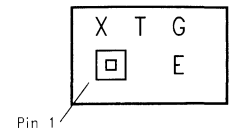
Mini Small Outline (MSOP) Package



20019236

Top View
Order Number LM4890MM
See NS Package Number MUA08A

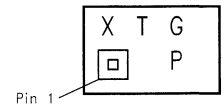
8 bump micro SMD Marking



20019270

Top View
X - Date Code
T - Die Traceability
G - Boomer Family
E - LM4890IBP

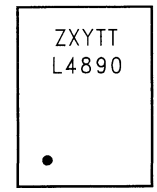
9 Bump micro Marking



200192C2

Top View
X - Date Code
T - Die Traceability
G - Boomer Family
P - LM4890IBL

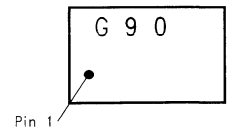
10 Pin LLP Marking



200192C6

Top View
Z - Assembly Plant Date Code (M for Malacca)
XY - Digit Date Code
TT - Die Traceability
L4890 - LM4890LD

MSOP Marking

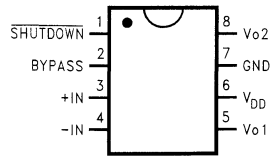


20019271

Top View
G - Boomer Family
90 - LM4890MM

Connection Diagrams (Continued)

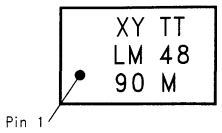
Small Outline (SO) Package



20019235

Top View
Order Number LM4890M
See NS Package Number M08A

SO Marking



20019272

Top View
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number

National Semiconductor

LM4891 Boomer® Audio Power Amplifier Series
1 Watt Audio Power Amplifier

General Description

The LM4891 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4891 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4891 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic high. Additionally, the LM4891 features an internal thermal shutdown protection mechanism.

The LM4891 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4891 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- PSRR at 217Hz, V_{DD} = 5V, 8Ω Load — 62dB (typ)
- Power Output at 5.0V & 1% THD — 1.0W (typ)
- Power Output at 3.3V & 1% THD — 400mW (typ)
- Shutdown Current — 0.1μA (typ)

Features

- Available in space-saving packages: micro SMD, MSOP, SOIC, and LLP
- Ultra low current shutdown mode
- BTL output can drive capacitive loads
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2 to 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

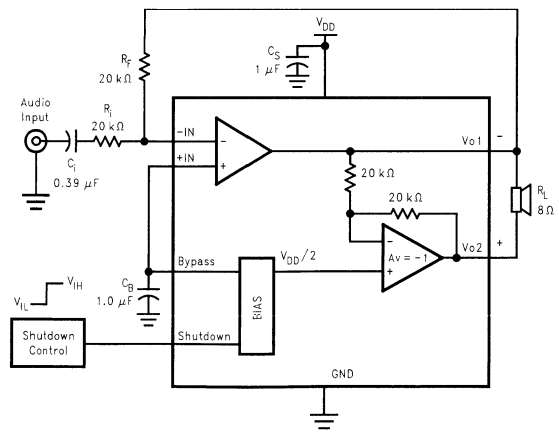
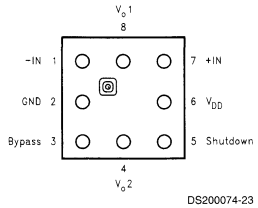


FIGURE 1. Typical Audio Amplifier Application Circuit

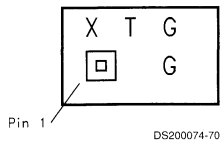
Connection Diagrams

8 Bump micro SMD



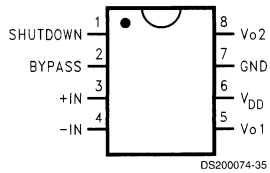
Top View
Order Number LM4891IBP, LM4891IBPX
See NS Package Number BPA08DDB

8 Bump micro SMD Marking



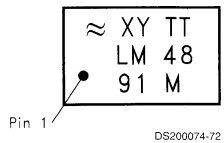
Top View
X - Date Code
T - Die Traceability
G - Boomer Family
G - LM4891IBP

Small Outline (SO) Package



Top View
Order Number LM4891M
See NS Package Number M08A

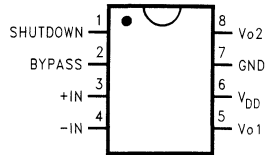
SO Marking



Top View
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number

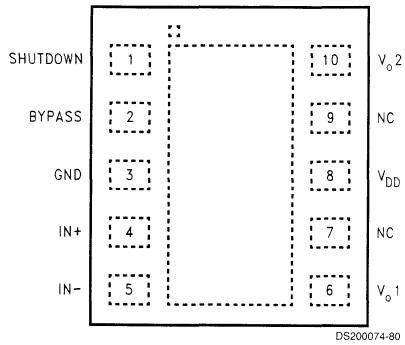
Connection Diagrams (Continued)

Mini Small Outline (MSOP) Package



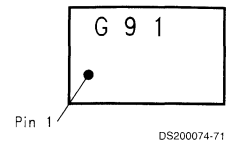
Top View
Order Number LM4891MM
See NS Package Number MUA08A

LLP Package



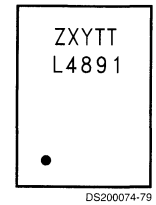
Top View
Order Number LM4891LD
See NS Package Number LDA10B

MSOP Marking



Top View
G - Boomer Family
91 - LM4891MM

10 Pin LLP Marking



Top View
Z - Assembly Plant Code (M for Malacca)
XY - 2 Digit Datecode
TT - 2 Letter Code for Traceability
L4891 - LM4891LD

National Semiconductor

LM4892 Boomer® Audio Power Amplifier Series
1 Watt Audio Power Amplifier with Headphone Sense

General Description

The LM4892 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply. Switching between bridged speaker mode and headphone (single-ended) mode is accomplished using the headphone sense pin.

Boomer audio power amplifiers are designed specifically to provide high quality output power with a minimal amount of external components. The LM4892 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4892 features a low-power consumption shutdown mode, which is achieved by driving the shutdown pin with logic low. Additionally, the LM4892 features an internal thermal shutdown protection mechanism.

The LM4892 contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions.

The LM4892 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- PSRR at 217Hz, V_{DD} = 5V, 8Ω Load — 62dB (typ)
- Power Output at 5.0V & 1% THD — 1.0W (typ)
- Power Output at 3.3V & 1% THD — 400mW (typ)
- Shutdown Current — 0.1µA (typ)

Features

- Available in space-saving packages micro SMD, MSOP and SOIC
- Ultra low current shutdown mode
- BTL output can drive capacitive loads up to 500 pF
- Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- Headphone amplifier mode

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

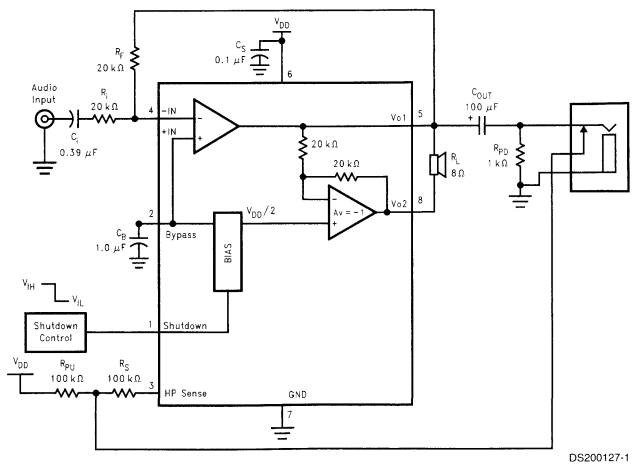
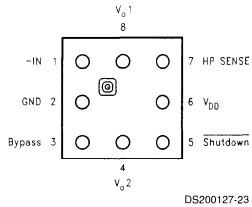


FIGURE 1. Typical Audio Amplifier Application Circuit (Pin #'s apply to M & MM packages)

Connection Diagrams

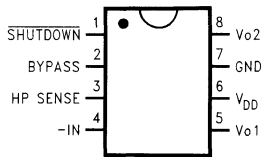
8 Bump micro SMD



DS200127-23

Top View
Order Number LM4892IBP, LM4892IBPX
See NS Package Number BPA08FFB

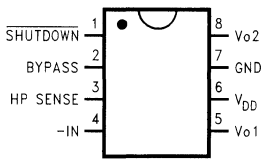
Small Outline (SO) Package



DS200127-35

Top View
Order Number LM4892M
See NS Package Number M08A

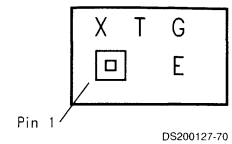
Mini Small Outline (MSOP) Package



DS200127-36

Top View
Order Number LM4892MM
See NS Package Number MUA08A

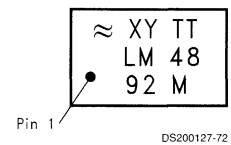
micro SMD Marking



DS200127-70

Top View
X - Date Code
T - Die Traceability
G - Boomer Family
E - LM4892IBP

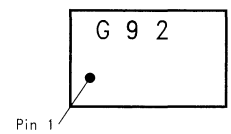
SO Marking



DS200127-72

Top View
XY - Date Code
TT - Die Traceability
Bottom 2 lines - Part Number

MSOP Marking



DS200127-71

Top View
G - Boomer Family
92 - LM4892MM

National Semiconductor

LM4894 Boomer® Audio Power Amplifier Series
1 Watt Fully Differential Audio Power Amplifier With Shutdown Select

General Description

The LM4894 is a fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4894 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4894 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown select pin to be driven in a likewise manner to enable Shutdown. Additionally, the LM4894 features an internal thermal shutdown protection mechanism.

The LM4894 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4894 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Improved PSRR at 217Hz — 80dB(typ)
- Power Output at 5.0V & 1% THD — 1.0W(typ)
- Power Output at 3.3V & 1% THD — 400mW(typ)
- Shutdown Current — 0.1µA(typ)

Features

- Fully differential amplification
- Available in space-saving packages micro SMD, MSOP, and LLP
- Ultra low current shutdown mode
- Can drive capacitive loads up to 500 pF
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- Shutdown high or low selectivity
- High CMRR

Applications

- Mobile phones
- PDAs
- Portable electronic devices

Typical Application

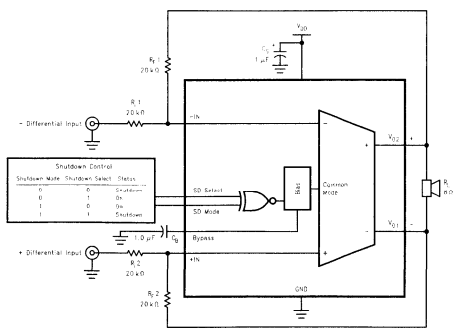
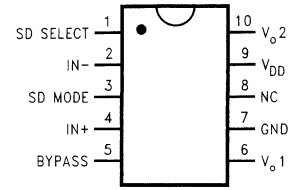


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

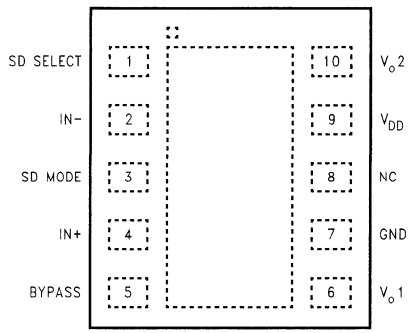
Mini Small Outline (MSOP) Package



20013723

Top View
Order Number LM4894MM
See NS Package Number MUB10A

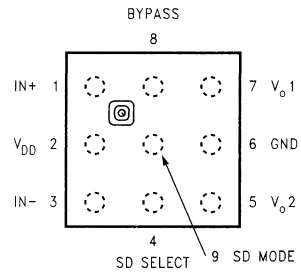
LLP Package



20013735

Top View
Order Number LM4894LD
See NS Package Number LDA10B

9 Bump micro SMD Package



20013736

Top View
Order Number LM4894IBP
See NS Package Number BPA09CDB

National Semiconductor

LM4895 Boomer® Audio Power Amplifier Series
1 Watt Fully Differential Audio Power Amplifier With Shutdown Select and Fixed 6dB Gain

General Description

The LM4895 is a fully differential audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4895 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4895 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown select pin to be driven in a likewise manner to enable Shutdown. Additionally, the LM4895 features an internal thermal shutdown protection mechanism.

The LM4895 contains advanced pop & click circuitry which eliminates noises which would otherwise occur during turn-on and turn-off transitions.

The LM4895 has an internally fixed gain of 6dB.

Key Specifications

- Improved PSRR at 217Hz 80dB
- Power Output at 5.0V & 1% THD 1.0W(typ.)
- Power Output at 3.3V & 1% THD 400mW(typ.)
- Shutdown Current 0.1μA(typ.)

Features

- Fully differential amplification
- Internal-gain-setting resistors
- Available in space-saving packages micro SMD, MSOP and LLP
- Ultra low current shutdown mode
- Can drive capacitive loads up to 500 pF
- Improved pop & click circuitry eliminates noises during turn-on and turn-off transitions
- 2.2 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Shutdown high or low selectivity

Applications

- Mobile phones
- PDAs
- Portable electronic devices

Typical Application

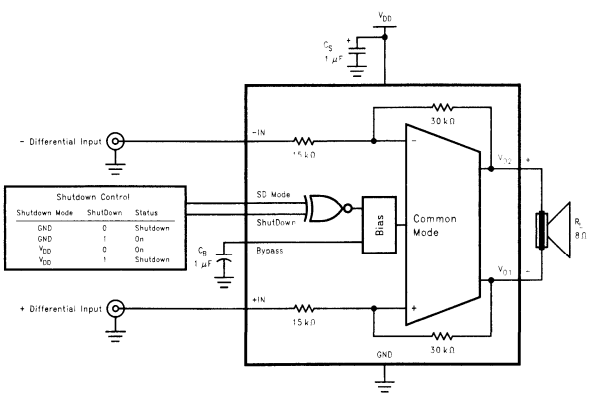
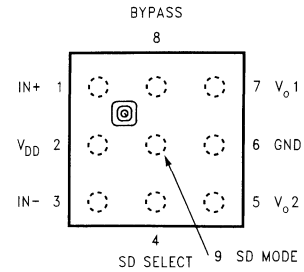


FIGURE 1. Typical Audio Amplifier Application Circuit

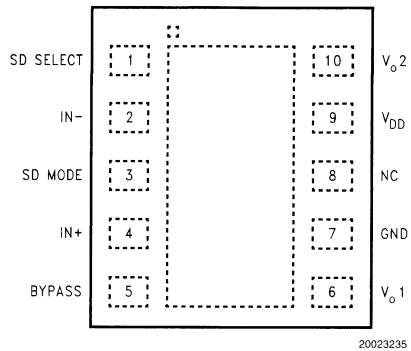
Connection Diagrams

9 Bump micro SMD Package



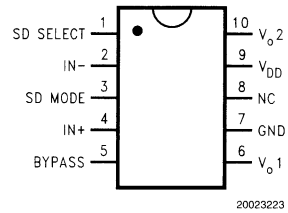
Top View
Order Number LM4895IBP
See NS Package Number BPA09CDB

LLP Package



Top View
Order Number LM4895LD
See NS Package Number LDA10B

Mini Small Outline (MSOP) Package



Top View
Order Number LM4895MM
See NS Package Number MUB10A

National Semiconductor

LM4900 Boomer® Audio Power Amplifier Series
265mW at 3.3V Supply Audio Power Amplifier with Shutdown Mode

General Description

The LM4900 is a bridged audio power amplifier capable of delivering 265mW of continuous average power into an 8Ω load with 1% THD+N from a 3.3V power supply.

Boomer® audio power amplifiers were designed specifically to provide high quality output power from a low supply voltage while requiring a minimal amount of external components. Since the LM4900 does not require output coupling capacitors, bootstrap capacitors or snubber networks, it is optimally suited for low-power portable applications.

The LM4900 features an externally controlled, low power consumption shutdown mode, and thermal shutdown protection.

The closed loop response of the unity-gain stable LM4900 can be configured by external gain-setting resistors.

Features

- MSOP, LLP, and SOP packaging
- No output coupling capacitors, bootstrap capacitors, or snubber circuits are necessary
- Thermal shutdown protection circuitry
- Unity-gain stable
- External gain configuration capability
- Latest generation 'click and pop' suppression circuitry

Applications

- Cellular phones
- PDA's
- Any portable audio application

Key Specifications

- THD+N at 1kHz for 265mW continuous average output power into 8Ω, V_{DD} = 3.3V — 1.0% (max)
- THD+N at 1kHz for 675mW continuous average output power into 8Ω, V_{DD} = 5V — 1.0% (max)
- Shutdown current — 0.1μA (typ)

Typical Application

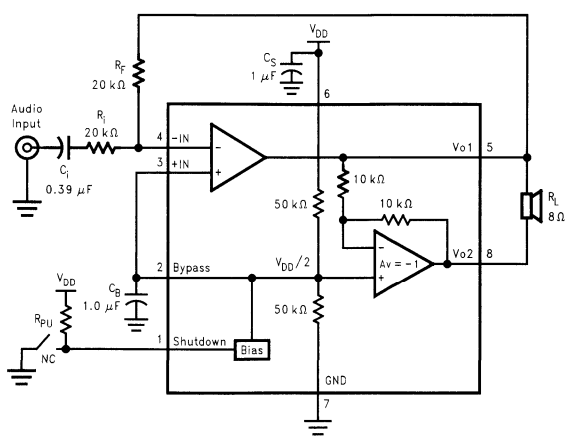
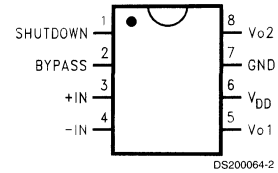


FIGURE 1. Typical Audio Amplifier Application Circuit

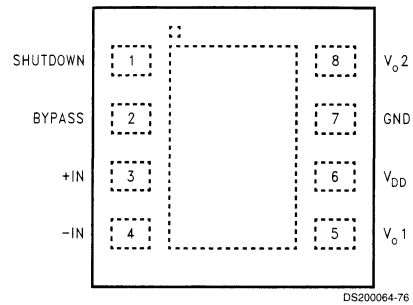
Connection Diagrams

MSOP and SOP Package



Top View
Order Number LM4900MM, LM4900M
See NS Package Number MUA08A, M08A

LLP Package



Top View
Order Number LM4900LD
See NS Package Number LDA08B

National Semiconductor

LM4901 Boomer® Audio Power Amplifier Series
1 Watt Audio Power Amplifier with Selectable Shutdown Logic Level

General Description

The LM4901 is an audio power amplifier primarily designed for demanding applications in mobile phones and other portable communication device applications. It is capable of delivering 1 watt of continuous average power to an 8Ω BTL load with less than 1% distortion (THD+N) from a $5V_{DC}$ power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM4901 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM4901 features a low-power consumption shutdown mode. To facilitate this, Shutdown may be enabled by either logic high or low depending on mode selection. Driving the shutdown mode pin either high or low enables the shutdown pin to be driven in a likewise manner to enable shutdown.

The LM4901 contains advanced pop & click circuitry which eliminates noise which would otherwise occur during turn-on and turn-off transitions.

The LM4901 is unity-gain stable and can be configured by external gain-setting resistors.

Key Specifications

- Improved PSRR at 217Hz & 1KHz 62dB
- Power Output at 5.0V & 1% THD 1.0W(typ.)
- Power Output at 3.0V & 1% THD 375mW(typ.)
- Shutdown Current 0.1μA(typ.)

Features

- Available in space-saving packages: micro SMD and MSOP
- Ultra low current shutdown mode
- BTL output can drive capacitive loads
- Improved pop & click circuitry eliminates noise during turn-on and turn-off transitions
- 2.0 - 5.5V operation
- No output coupling capacitors, snubber networks or bootstrap capacitors required
- Unity-gain stable
- External gain configuration capability
- User select shutdown High or Low

Applications

- Mobile Phones
- PDAs
- Portable electronic devices

Typical Application

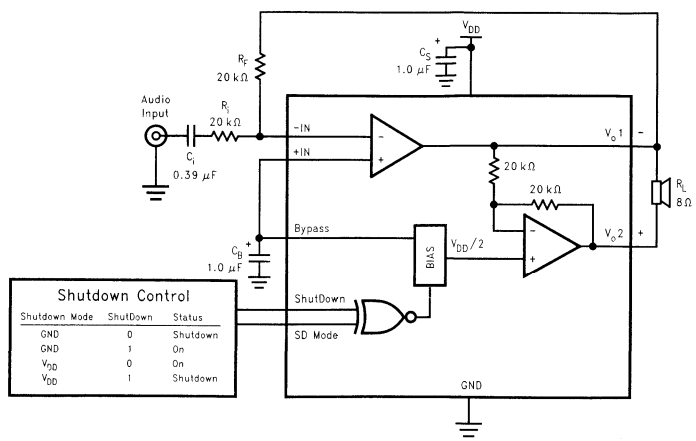
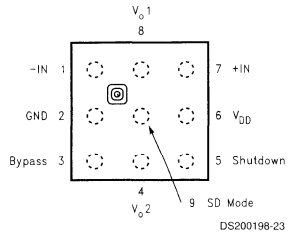


FIGURE 1. Typical Audio Amplifier Application Circuit

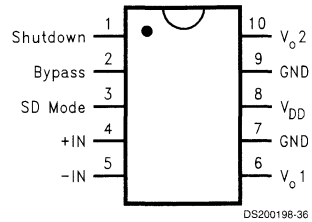
Connection Diagrams

9 Bump micro SMD



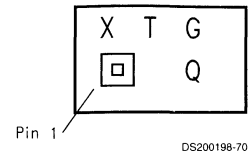
Top View
Order Number LM4901IBP, LM4901IBPX
See NS Package Number BPA09CDB

Mini Small Outline (MSOP) Package



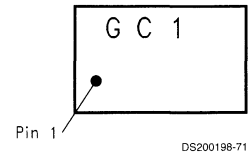
Top View
Order Number LM4901MM
See NS Package Number MUB10A

micro SMD Marking



Top View
X - Date Code
T - Die Traceability
G - Boomer Family
Q - LM4901IBP

MSOP Marking



Top View
G - Boomer Family
C1 - LM4901MM

National Semiconductor

LM675
Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

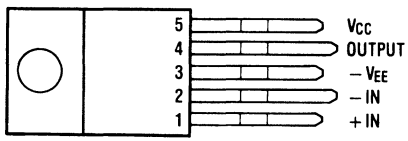
- 3A current capability
- A_{VO} typically 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/μs slew rate
- Wide power bandwidth 70 kHz
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parole circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)



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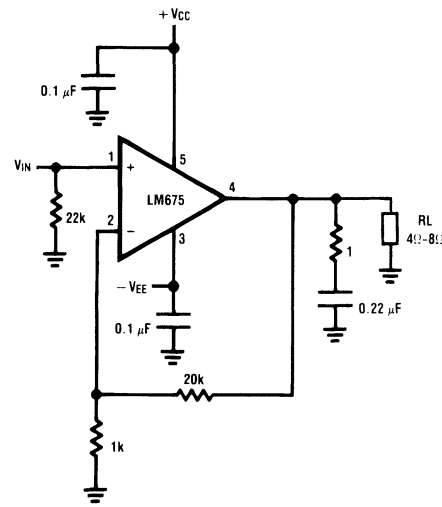
*The tab is internally connected to pin 3 ($-V_{EE}$)

Front View
Order Number LM675T
See NS Package T05D

Typical Applications

Non-Inverting Amplifier



DS006739-2

National Semiconductor

Audio Controls and Signal Processing

National Semiconductor

LM1036
Dual DC Operated Tone/Volume/Balance Circuit

General Description

The LM1036 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

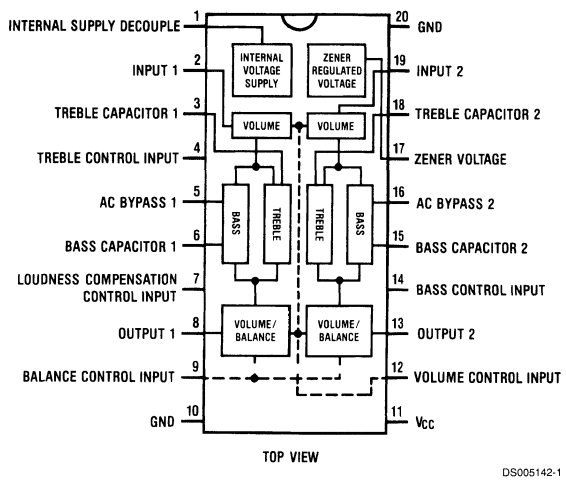
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



DS005142-1

Order Number LM1036N
See NS Package Number N20A

National Semiconductor

LM1971 *Overture*™ Audio Attenuator Series
Digitally Controlled 62 dB Audio Attenuator with/Mute

General Description

The LM1971 is a digitally controlled single channel audio attenuator fabricated on a CMOS process. Attenuation is variable in 1 dB steps from 0 dB to −62 dB. A mute function disconnects the input from the output, providing over 100 dB of attenuation.

The performance of the device is exhibited by its ability to change attenuation levels without audible clicks or pops. In addition, the LM1971 features a low Total Harmonic Distortion (THD) of 0.0008%, and a Dynamic Range of 115 dB, making it suitable for digital audio needs. The LM1971 is available in both 8-pin plastic DIP or SO packages.

The LM1971 is controlled by a TTL/CMOS compatible 3-wire serial digital interface. The active low LOAD line enables the data input registers while the CLOCK line provides system timing. Its DATA pin receives serial data on the rising edge of each CLOCK pulse, allowing the desired attenuation setting to be selected.

Key Specifications

- Total harmonic distortion 0.0008% (typ)
- Frequency response > 200 kHz (−3 dB) (typ)
- Attenuation range (excluding mute) 62 dB (typ)
- Dynamic range 115 dB (typ)
- Mute attenuation 102 dB (typ)

Features

- 3-wire serial interface
- Mute function
- Click and pop free attenuation changes
- 8-pin plastic DIP and SO packages available

Applications

- Communication systems
- Cellular Phones and Pagers
- Personal computer audio control
- Electronic music (MIDI)
- Sound reinforcement systems
- Audio mixing automation

Typical Application

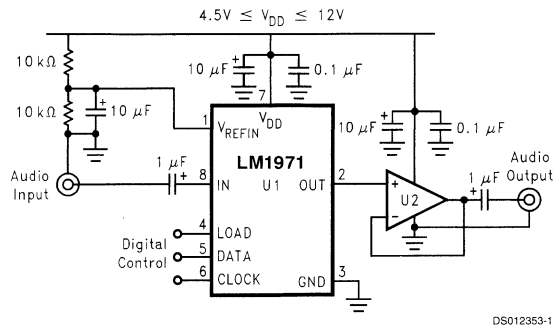
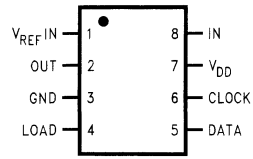


FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Dual-In-Line Plastic or Surface Mount Package



DS012353-2

Top View
Order Number LM1971M or LM1971N
See NS Package Number M08A or N08E

National Semiconductor

LM1972
µPot™ 2-Channel 78dB Audio Attenuator with Mute

General Description

The LM1972 is a digitally controlled 2-channel 78dB audio attenuator fabricated on a CMOS process. Each channel has attenuation steps of 0.5dB from 0dB–47.5dB, 1.0dB steps from 48dB–78dB, with a mute function attenuating 104dB. Its logarithmic attenuation curve can be customized through software to fit the desired application.

The performance of a µPot is demonstrated through its excellent Signal-to-Noise Ratio, extremely low (THD+N), and high channel separation. Each µPot contains a mute function that disconnects the input signal from the output, providing a minimum attenuation of 96dB. Transitions between any attenuation settings are pop free.

The LM1972's 3-wire serial digital interface is TTL and CMOS compatible; receiving data that selects a channel and the desired attenuation level. The Data-Out pin of the LM1972 allows multiple µPots to be daisy-chained together, reducing the number of enable and data lines to be routed for a given application.

Key Specifications

- Total Harmonic Distortion + Noise: 0.003% (max)
- Frequency response: 100 kHz (–3dB) (min)
- Attenuation range (excluding mute): 78dB (typ)
- Differential attenuation: ±0.25dB (max)
- Signal-to-noise ratio (ref. 4 Vrms): 110dB (min)
- Channel separation: 100dB (min)

Features

- 3-wire serial interface
- Daisy-chain capability
- 104dB mute attenuation
- Pop and click free attenuation changes

Applications

- Automated studio mixing consoles
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Typical Application

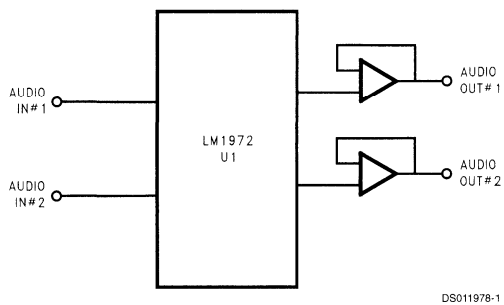
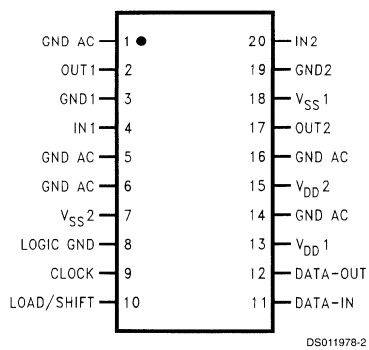


FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Dual-In-Line Plastic or Surface Mount Package



Top View
Order Number LM1972M or LM1972N
See NS Package Number M20B or N20A

National Semiconductor

LM1973
µPot 3-Channel 76dB Audio Attenuator with Mute

General Description

The LM1973 is a digitally controlled 3-channel 76dB audio attenuator fabricated on a CMOS process. Each channel has attenuation steps of 0.5dB from 0dB–15.5dB, 1.0dB steps from 16dB–47dB, and 2.0dB steps from 48dB– 76dB, with a mute function attenuating 104dB. Its logarithmic attenuation curve can be customized through software to fit the desired application.

The performance of a µPot™ is demonstrated through its excellent Signal-to-Noise Ratio, extremely low (THD+N), and high channel separation. Each µPot contains a mute function that disconnects the input signal from the output, providing a minimum attenuation of 96dB. Transitions between any attenuation settings are pop free.

The LM1973's 3-wire serial digital interface is TTL and CMOS compatible; receiving data that selects a channel and the desired attenuation level. The Data-Out pin of the LM1973 allows multiple µPots to be daisy-chained together, reducing the number of enable and data lines to be routed for a given application.

Key Specifications

- Total Harmonic Distortion + Noise: 0.003% (max)
- Frequency response: 100 kHz (–3dB) (min)
- Attenuation range (excluding mute): 76dB (typ)
- Differential attenuation: ±0.25dB (max)
- Signal-to-noise ratio (ref. 4 Vrms): 110dB (min)
- Channel separation: 110dB (typ)

Features

- 3-wire serial interface
- Daisy-chain capability
- 104dB mute attenuation
- Pop and click free attenuation changes

Applications

- Automated studio mixing consoles
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Typical Application

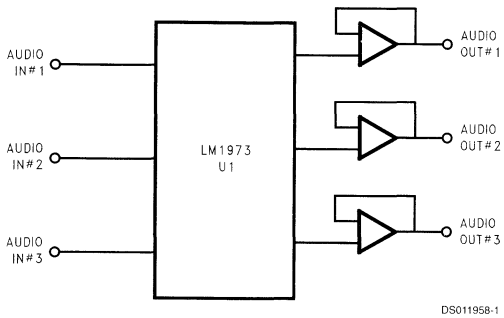
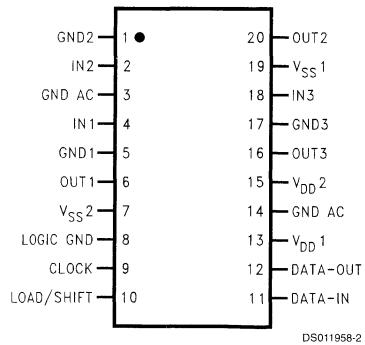


FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Dual-In-Line Plastic or Surface Mount Package



Top View
Order Number LM1973M or LM1973N
See NS Package Number M20B or N20A

National Semiconductor

LM3914
Dot/Bar Display Driver

General Description

The LM3914 is a monolithic integrated circuit that senses analog voltage levels and drives 10 LEDs, providing a linear analog display. A single pin changes the display from a moving dot to a bar graph. Current drive to the LEDs is regulated and programmable, eliminating the need for resistors. This feature is one that allows operation of the whole system from less than 3V.

The circuit contains its own adjustable reference and accurate 10-step voltage divider. The low-bias-current input buffer accepts signals down to ground, or V^-, yet needs no protection against inputs of 35V above or below ground. The buffer drives 10 individual comparators referenced to the precision divider. Indication non-linearity can thus be held typically to ½%, even over a wide temperature range.

Versatility was designed into the LM3914 so that controller, visual alarm, and expanded scale functions are easily added on to the display system. The circuit can drive LEDs of many colors, or low-current incandescent lamps. Many LM3914s can be "chained" to form displays of 20 to over 100 segments. Both ends of the voltage divider are externally available so that 2 drivers can be made into a zero-center meter.

The LM3914 is very easy to apply as an analog meter circuit. A 1.2V full-scale meter requires only 1 resistor and a single 3V to 15V supply in addition to the 10 display LEDs. If the 1 resistor is a pot, it becomes the LED brightness control. The simplified block diagram illustrates this extremely simple external circuitry.

When in the dot mode, there is a small amount of overlap or "fade" (about 1 mV) between segments. This assures that at no time will all LEDs be "OFF", and thus any ambiguous display is avoided. Various novel displays are possible.

Much of the display flexibility derives from the fact that all outputs are individual, DC regulated currents. Various effects can be achieved by modulating these currents. The individual outputs can drive a transistor as well as a LED at the same time, so controller functions including "staging" control can be performed. The LM3914 can also act as a programmer, or sequencer.

The LM3914 is rated for operation from 0°C to +70°C. The LM3914N-1 is available in an 18-lead molded (N) package.

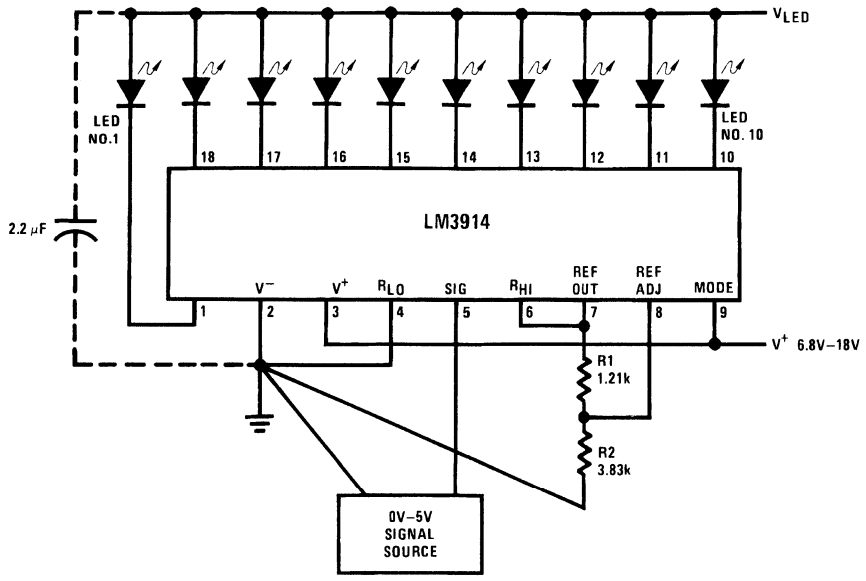
The following typical application illustrates adjusting of the reference to a desired value, and proper grounding for accurate operation, and avoiding oscillations.

Features

- Drives LEDs, LCDs or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 100 steps
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of less than 3V
- Inputs operate down to ground
- Output current programmable from 2 mA to 30 mA
- No multiplex switching or interaction between outputs
- Input withstands ±35V without damage or false outputs
- LED driver outputs are current regulated, open-collectors
- Outputs can interface with TTL or CMOS logic
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

Typical Applications

0V to 5V Bar Graph Meter



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$$\text{Ref Out V} = 1.25\left(1 + \frac{R2}{R1}\right)$$

$$I_{LED} \cong \frac{12.5}{R1}$$

Note: Grounding method is typical of *all* uses. The 2.2 µF tantalum or 10 µF aluminum electrolytic capacitor is needed if leads to the LED supply are 6" or longer.

National Semiconductor

LM3915
Dot/Bar Display Driver

General Description

The LM3915 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing a logarithmic 3 dB/step analog display. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 1 dB.

The LM3915's 3 dB/step display is suited for signals with wide dynamic range, such as audio level, power, light intensity or vibration. Audio applications include average or peak level indicators, power meters and RF signal strength meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3915 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3915 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display with a range of 60 or 90 dB. LM3915s can also be cascaded with LM3914s for a linear/log display or with LM3916s for an extended-range VU meter.

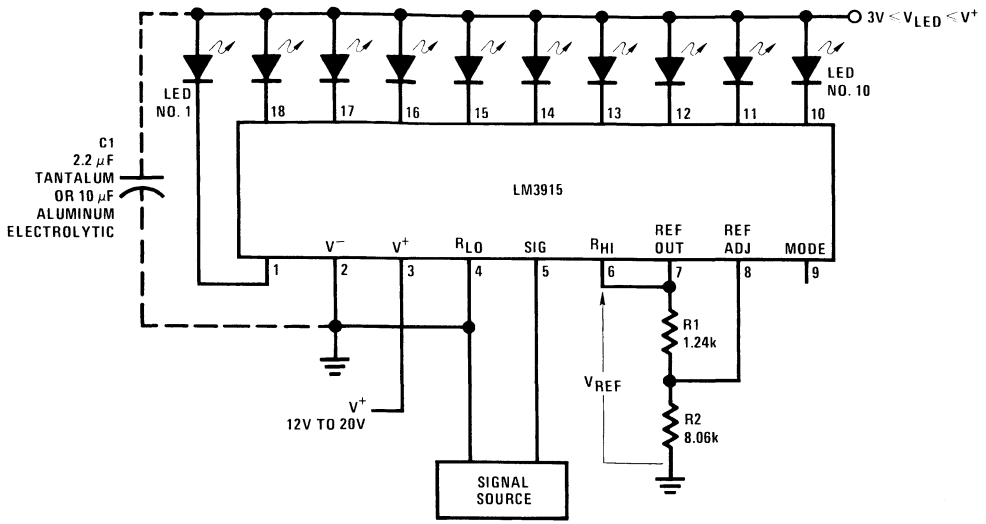
Features

- 3 dB/step, 30 dB range
- Drives LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 90 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3915 is rated for operation from 0°C to +70°C. The LM3915N-1 is available in an 18-lead molded DIP package.

Typical Applications

0V to 10V Log Display



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Notes: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

$$V_{REF} = 1.25V \left(1 + \frac{R2}{R1}\right) + R2 \times 80\,\mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\,k\Omega}$$

National Semiconductor

LM3916
Dot/Bar Display Driver

General Description

The LM3916 is a monolithic integrated circuit that senses analog voltage levels and drives ten LEDs, LCDs or vacuum fluorescent displays, providing an electronic version of the popular VU meter. One pin changes the display from a bar graph to a moving dot display. LED current drive is regulated and programmable, eliminating the need for current limiting resistors. The whole display system can operate from a single supply as low as 3V or as high as 25V.

The IC contains an adjustable voltage reference and an accurate ten-step voltage divider. The high-impedance input buffer accepts signals down to ground and up to within 1.5V of the positive supply. Further, it needs no protection against inputs of ±35V. The input buffer drives 10 individual comparators referenced to the precision divider. Accuracy is typically better than 0.2 dB.

Audio applications include average or peak level indicators, and power meters. Replacing conventional meters with an LED bar graph results in a faster responding, more rugged display with high visibility that retains the ease of interpretation of an analog display.

The LM3916 is extremely easy to apply. A 1.2V full-scale meter requires only one resistor in addition to the ten LEDs. One more resistor programs the full-scale anywhere from 1.2V to 12V independent of supply voltage. LED brightness is easily controlled with a single pot.

The LM3916 is very versatile. The outputs can drive LCDs, vacuum fluorescents and incandescent bulbs as well as LEDs of any color. Multiple devices can be cascaded for a dot or bar mode display for increased range and/or resolution. Useful in other applications are the linear LM3914 and the logarithmic LM3915.

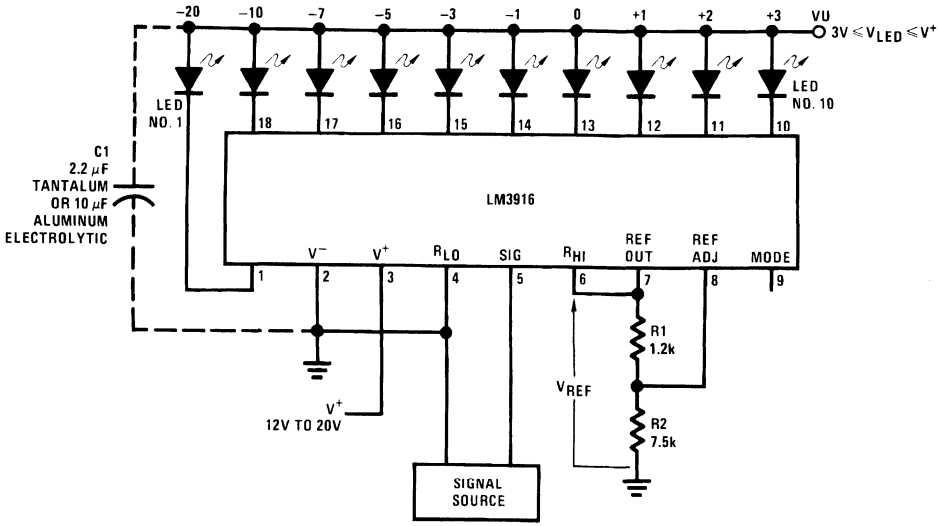
Features

- Fast responding electronic VU meter
- Drivers LEDs, LCDs, or vacuum fluorescents
- Bar or dot display mode externally selectable by user
- Expandable to displays of 70 dB
- Internal voltage reference from 1.2V to 12V
- Operates with single supply of 3V to 25V
- Inputs operate down to ground
- Output current programmable from 1 mA to 30 mA
- Input withstands ±35V without damage or false outputs
- Outputs are current regulated, open collectors
- Directly drives TTL or CMOS
- The internal 10-step divider is floating and can be referenced to a wide range of voltages

The LM3916 is rated for operation from 0°C to +70°C. The LM3916N-1 is available in an 18-lead molded DIP package.

Typical Applications

0V to 10V VU Meter



DS007971-1

$$V_{REF} = 1.25V\left(1 + \frac{R2}{R1}\right) + R2 \times 80\,\mu A$$

$$I_{LED} = \frac{12.5V}{R1} + \frac{V_{REF}}{2.2\,k\Omega}$$

Notes: Capacitor C1 is required if leads to the LED supply are 6" or longer.

Circuit as shown is wired for dot mode. For bar mode, connect pin 9 to pin 3. V_{LED} must be kept below 7V or dropping resistor should be used to limit IC power dissipation.

National Semiconductor

LM4610
Dual DC Operated Tone/Volume/Balance Circuit with National 3-D Sound

General Description

The LM4610 is a DC controlled tone (bass/treble), volume and balance circuit for stereo applications in car radio, TV and audio systems. It also features National's 3D-Sound Circuitry which can be externally adjusted via a simple RC Network. An additional control input allows loudness compensation to be simply effected.

Four control inputs provide control of the bass, treble, balance and volume functions through application of DC voltages from a remote control system or, alternatively, from four potentiometers which may be biased from a zener regulated supply provided on the circuit.

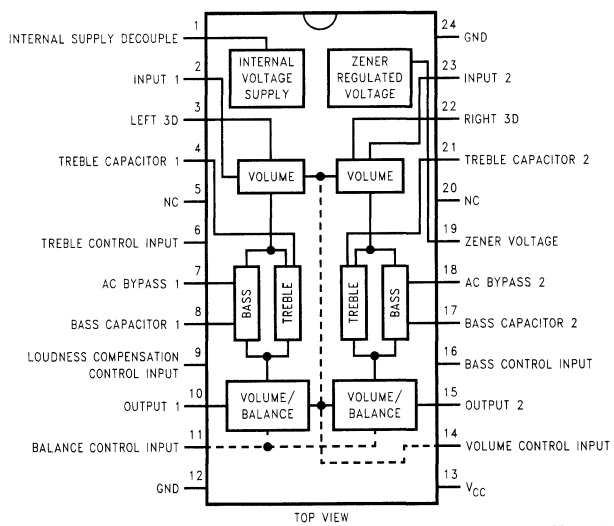
Each tone response is defined by a single capacitor chosen to give the desired characteristic.

Features

- National 3-D Sound
- Wide supply voltage range, 9V to 16V
- Large volume control range, 75 dB typical
- Tone control, ±15 dB typical
- Channel separation, 75 dB typical
- Low distortion, 0.06% typical for an input level of 0.3 Vrms
- High signal to noise, 80 dB typical for an input level of 0.3 Vrms
- Few external components required

Block and Connection Diagram

Dual-In-Line Package



DS101125-1

Order Number LM4610N
See NS Package Number N24A

National Semiconductor

LM565/LM565C
Phase Locked Loop

General Description

The LM565 and LM565C are general purpose phase locked loops containing a stable, highly linear voltage controlled oscillator for low distortion FM demodulation, and a double balanced phase detector with good carrier suppression. The VCO frequency is set with an external resistor and capacitor, and a tuning range of 10:1 can be obtained with the same capacitor. The characteristics of the closed loop system—bandwidth, response speed, capture and pull in range—may be adjusted over a wide range with an external resistor and capacitor. The loop may be broken between the VCO and the phase detector for insertion of a digital frequency divider to obtain frequency multiplication.

The LM565H is specified for operation over the −55°C to +125°C military temperature range. The LM565CN is specified for operation over the 0°C to +70°C temperature range.

Features

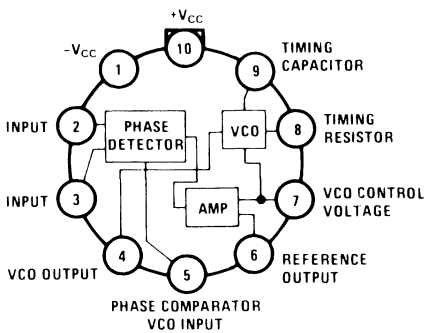
- 200 ppm/°C frequency stability of the VCO
- Power supply range of ±5 to ±12 volts with 100 ppm/% typical
- 0.2% linearity of demodulated output
- Linear triangle wave with in phase zero crossings available
- TTL and DTL compatible phase detector input and square wave output
- Adjustable hold in range from ±1% to > ±60%

Applications

- Data and tape synchronization
- Modems
- FSK demodulation
- FM demodulation
- Frequency synthesizer
- Tone decoding
- Frequency multiplication and division
- SCA demodulators
- Telemetry receivers
- Signal regeneration
- Coherent demodulators

Connection Diagrams

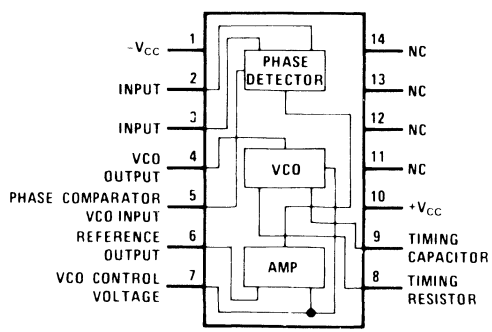
Metal Can Package



DS007853-2

Order Number LM565H
See NS Package Number H10C

Dual-in-Line Package



DS007853-3

Order Number LM565CN
See NS Package Number N14A

National Semiconductor

LM567/LM567C
Tone Decoder

General Description

The LM567 and LM567C are general purpose tone decoders designed to provide a saturated transistor switch to ground when an input signal is present within the passband. The circuit consists of an I and Q detector driven by a voltage controlled oscillator which determines the center frequency of the decoder. External components are used to independently set center frequency, bandwidth and output delay.

Features

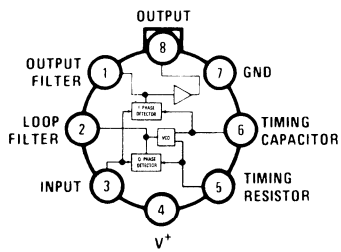
- 20 to 1 frequency range with an external resistor
- Logic compatible output with 100 mA current sinking capability
- Bandwidth adjustable from 0 to 14%
- High rejection of out of band signals and noise
- Immunity to false signals
- Highly stable center frequency
- Center frequency adjustable from 0.01 Hz to 500 kHz

Applications

- Touch tone decoding
- Precision oscillator
- Frequency monitoring and control
- Wide band FSK demodulation
- Ultrasonic controls
- Carrier current remote controls
- Communications paging decoders

Connection Diagrams

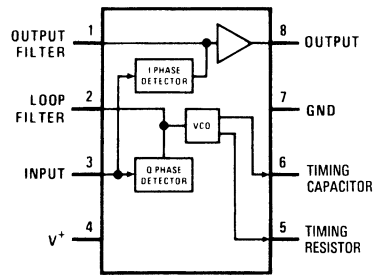
Metal Can Package



DS006975-1

Top View
Order Number LM567H or LM567CH
See NS Package Number H08C

Dual-In-Line and Small Outline Packages



DS006975-2

Top View
Order Number LM567CM
See NS Package Number M08A
Order Number LM567CN
See NS Package Number N08E

National Semiconductor

LMC1982
Digitally-Controlled Stereo Tone and Volume Circuit with Two Selectable Stereo Inputs

General Description

The LMC1982 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), enhanced stereo, and loudness controls and selection between two pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1982 is designed for line level input signals (300 mV–2V) and has a maximum gain of –0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1982's SELECT OUT/SELECT IN external processor loop.

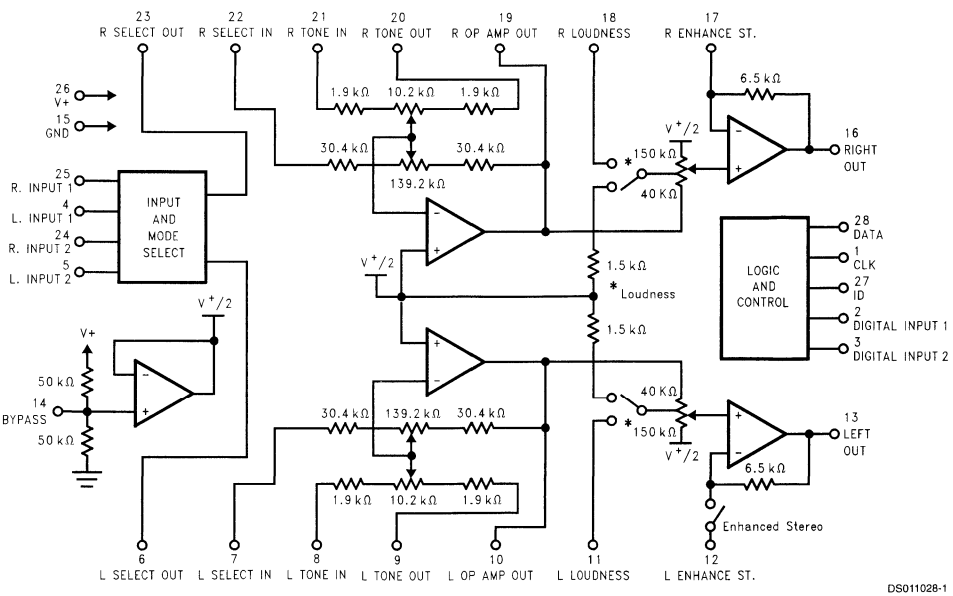
Features

- Low noise and distortion
- Two pairs of stereo inputs
- Enhanced stereo function
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block and Connection Diagrams



DS011028-1

National Semiconductor

LMC1983
Digitally-Controlled Stereo Tone and Volume Circuit with Three Selectable Stereo Inputs

General Description

The LMC1983 is a monolithic integrated circuit that provides volume, balance, tone (bass and treble), loudness controls and selection between three pairs of stereo inputs. These functions are digitally controlled through a three-wire communication interface. There are two digital inputs for easy interface to other audio peripherals such as stereo decoders. The LMC1983 is designed for line level input signals (300 mV–2V) and has a maximum gain of –0.5 dB. Volume is set at minimum and tone controls are flat when supply voltage is first applied.

Low noise and distortion result from using analog switches and poly-silicon resistor networks in the signal path.

Additional tone control can be achieved using the LMC835 stereo 7-band graphic equalizer connected to the LMC1983's SELECT OUT/SELECT IN external processor loop.

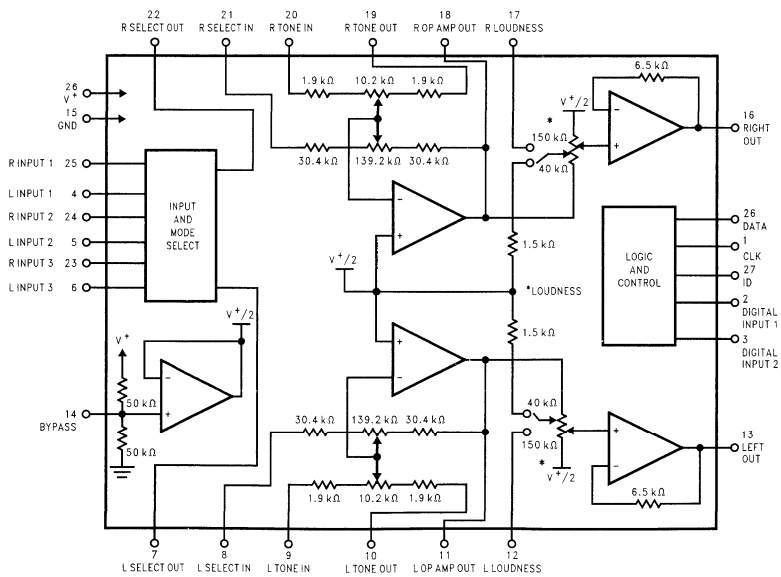
Features

- Low noise and distortion
- Three pairs of stereo inputs
- Loudness compensation
- 40 position 2 dB/step volume attenuator plus mute
- Independent left and right volume controls
- Low noise-suitable for use with DNR® and Dolby® noise reduction
- External processor loop
- Signal handling suitable for compact discs
- Pop-free switching
- Serially programmable: INTERMETAL bus (IM) interface
- 6V to 12V single supply operation
- 28 Pin DIP or PLCC Package

Applications

- Stereo television
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Block Diagram



DS011279-1

National Semiconductor

LMC567
Low Power Tone Decoder

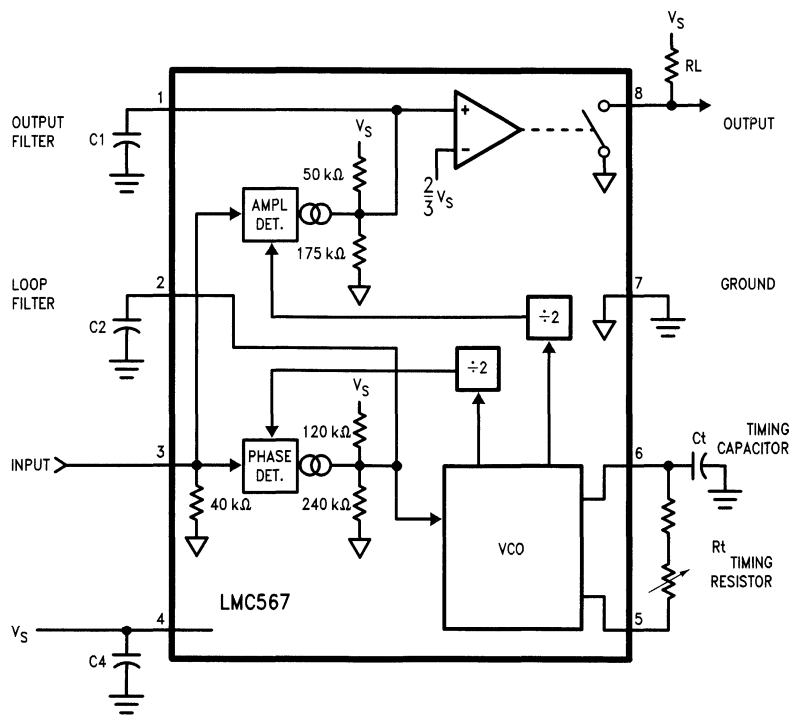
General Description

The LMC567 is a low power general purpose LMCMOS™ tone decoder which is functionally similar to the industry standard LM567. It consists of a twice frequency voltage-controlled oscillator (VCO) and quadrature dividers which establish the reference signals for phase and amplitude detectors. The phase detector and VCO form a phase-locked loop (PLL) which locks to an input signal frequency which is within the control range of the VCO. When the PLL is locked and the input signal amplitude exceeds an internally pre-set threshold, a switch to ground is activated on the output pin. External components set up the oscillator to run at twice the input frequency and determine the phase and amplitude filter time constants.

Features

- Functionally similar to LM567
- 2V to 9V supply voltage range
- Low supply current drain
- No increase in current with output activated
- Operates to 500 kHz input frequency
- High oscillator stability
- Ground-referenced input
- Hysteresis added to amplitude comparator
- Out-of-band signals and noise rejected
- 20 mA output current capability

Block Diagram (with External Components)



Order Number LMC567CM or LMC567CN
See NS Package Number M08A or N08E

National Semiconductor

LMC568
Low Power Phase-Locked Loop

General Description

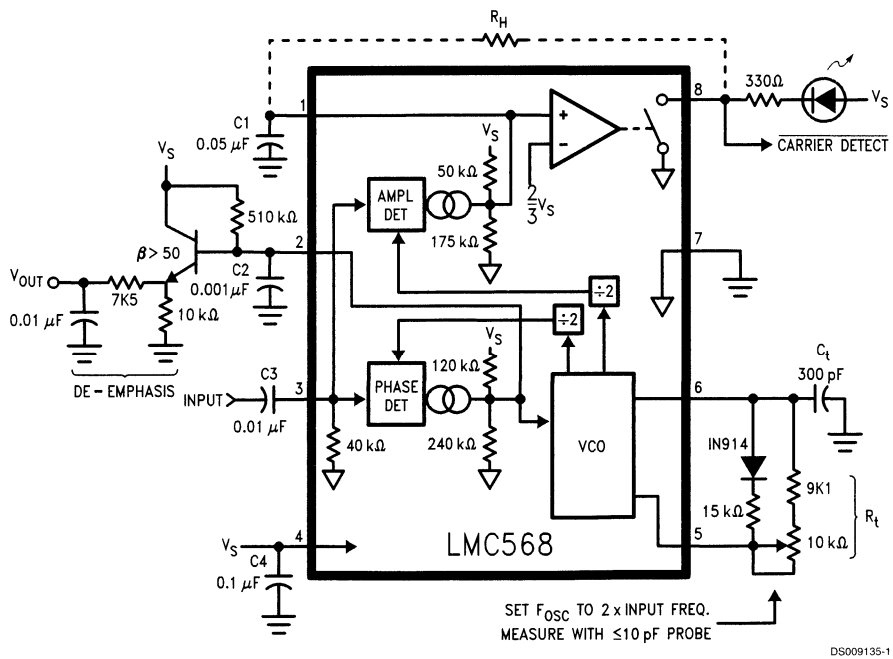
The LMC568 is an amplitude-linear phase-locked loop consisting of a linear VCO, fully balanced phase detectors, and a carrier detect output. LMCMOS™ technology is employed for high performance with low power consumption.

The VCO has a linearized control range of ±30% to allow demodulation of FM and FSK signals. Carrier detect is indicated when the PLL is locked to an input signal greater than 26 mVrms. LMC568 applications include FM SCA and TV second audio program decoders, FSK data demodulators, and voice pagers.

Features

- Demodulates ±15% deviation FM/FSK signals
- Carrier Detect Output with hysteresis
- Operation to 500 kHz input frequency
- Low THD—0.5% typ. for ±10% deviation
- 2V to 9V supply voltage range
- Low supply current drain

Typical Application (100 kHz input frequency, refer to notes pg. 3)



Order Number LMC568CM or LMC568CN
See NS Package Number M08A or N08E

National Semiconductor

LF411
Low Offset, Low Drift JFET Input Operational Amplifier

General Description

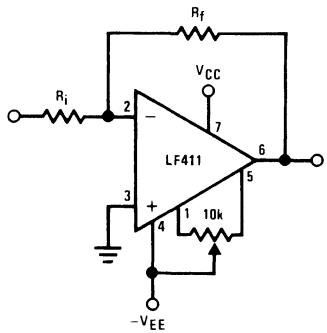
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage: 0.5 mV(max)
- Input offset voltage drift: 10 µV/°C(max)
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/√Hz
- Wide gain bandwidth: 3 MHz(min)
- High slew rate: 10V/µs(min)
- Low supply current: 1.8 mA
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion: ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 µs

Typical Connection



DS005655-1

Ordering Information

LF411XYZ

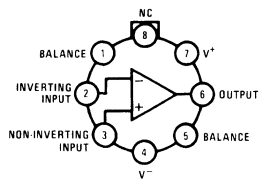
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package

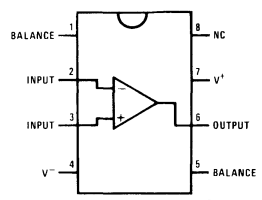


DS005655-5

Note: Pin 4 connected to case.

Top View
Order Number LF411ACH
or LF411MH/883 (Note 11)
See NS Package Number H08A

Dual-In-Line Package



DS005655-7

Top View
Order Number LF411ACN, LF411CN
See NS Package Number N08E

National Semiconductor

LF412
Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

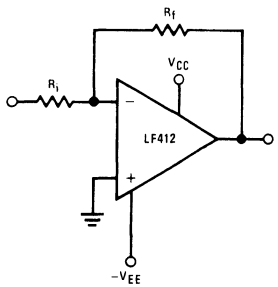
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage: 1 mV (max)
- Input offset voltage drift: 10 μV/°C (max)
- Low input bias current: 50 pA
- Low input noise current: 0.01 pA/$\sqrt{Hz}$
- Wide gain bandwidth: 3 MHz (min)
- High slew rate: 10V/μs (min)
- Low supply current: 1.8 mA/Amplifier
- High input impedance: $10^{12}\Omega$
- Low total harmonic distortion ≤0.02%
- Low 1/f noise corner: 50 Hz
- Fast settling time to 0.01%: 2 μs

Typical Connection



DS005656-41

Ordering Information

LF412XYZ

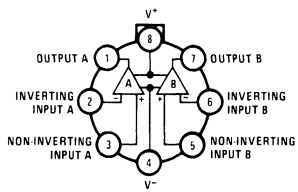
X indicates electrical grade

Y indicates temperature range
"M" for military
"C" for commercial

Z indicates package type
"H" or "N"

Connection Diagrams

Metal Can Package



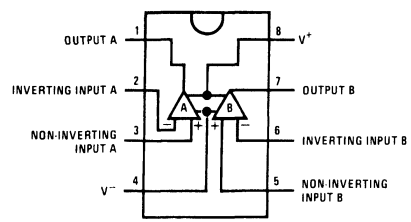
Note. Pin 4 connected to case.

TOP VIEW

DS005656-42

Order Number LF412MH, LF412CH or LF412MH/883 (Note 1)
See NS Package Number H08A

Dual-In-Line Package



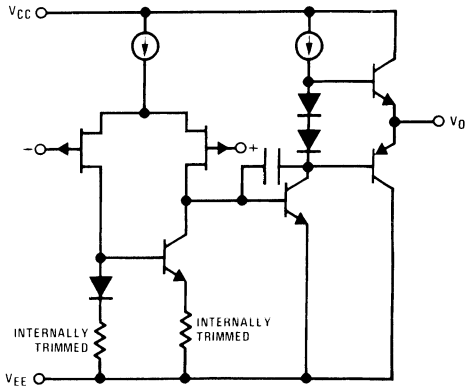
TOP VIEW

DS005656-44

Order Number LF412ACN, LF412CN or LF412MJ/883 (Note 1)
See NS Package Number J08A or N08E

Simplified Schematic

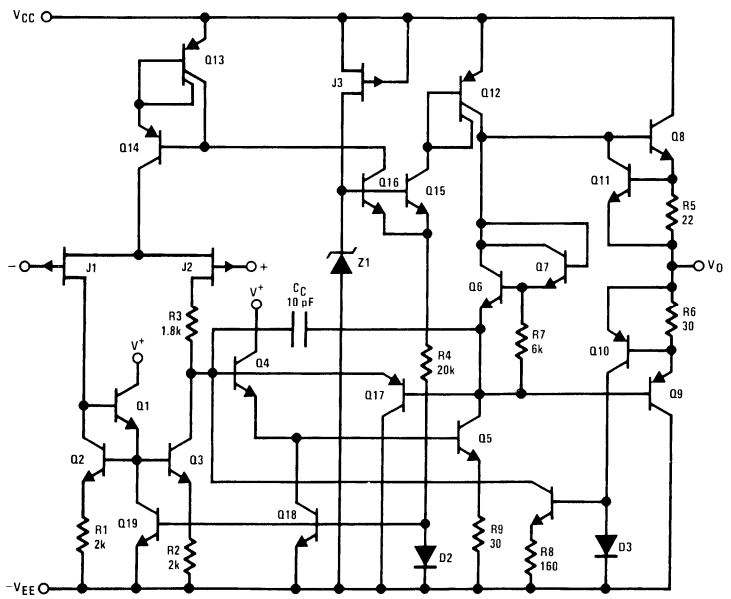
1/2 Dual



DS005656-43

Note 1: Available per JM38510/11905

Detailed Schematic



DS005656-32

National Semiconductor

LM6142 and LM6144
17 MHz Rail-to-Rail Input-Output Operational Amplifiers

General Description

Using patent pending new circuit topologies, the LM6142/44 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/44 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 µA/Amplifier supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

Features

At V_S = 5V. Typ unless noted.

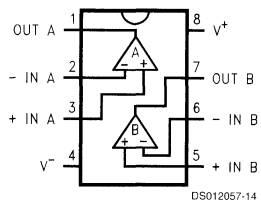
- Rail-to-rail input CMVR −0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17 MHz at 50 kHz (typ)
- Slew rate:
  - Small signal, 5V/µs
  - Large signal, 30V/µs
- Low supply current 650 µA/Amplifier
- Wide supply range 1.8V to 24V
- CMRR 107 dB
- Gain 108 dB with R_L = 10k
- PSRR 87 dB

Applications

- Battery operated instrumentation
- Depth sounders/fish finders
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

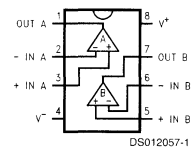
Connection Diagrams

8-Pin CDIP



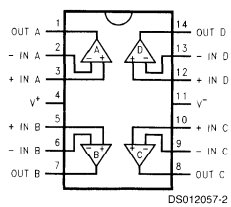
Top View

8-Pin DIP/SO



Top View

14-Pin DIP/SO



Top View

National Semiconductor

LM833
Dual Audio Operational Amplifier

General Description

The LM833 is a dual general purpose operational amplifier designed with particular emphasis on performance in audio systems.

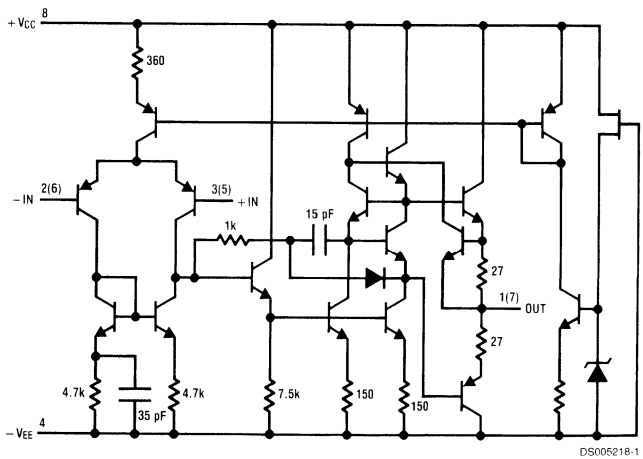
This dual amplifier IC utilizes new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 is internally compensated for all closed loop gains and is therefore optimized for all preamp and high level stages in PCM and HiFi systems.

The LM833 is pin-for-pin compatible with industry standard dual operational amplifiers.

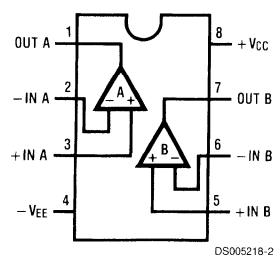
Features

- Wide dynamic range: >140dB
- Low input noise voltage: 4.5nV/√Hz
- High slew rate: 7 V/μs (typ); 5V/μs (min)
- High gain bandwidth: 15MHz (typ); 10MHz (min)
- Wide power bandwidth: 120KHz
- Low distortion: 0.002%
- Low offset voltage: 0.3mV
- Large phase margin: 60°
- Available in 8 pin MSOP package

Schematic Diagram (1/2 LM833)



Connection Diagram



Order Number LM833M, LM833MX, LM833N, LM833MM or LM833MMX
See NS Package Number
M08A, N08E or MUA08A

National Semiconductor

LM837
Low Noise Quad Operational Amplifier

General Description

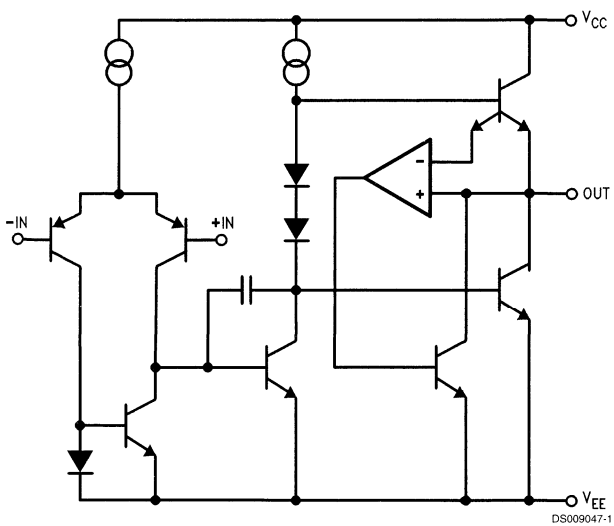
The LM837 is a quad operational amplifier designed for low noise, high speed and wide bandwidth performance. It has a new type of output stage which can drive a 600Ω load, making it ideal for almost all digital audio, graphic equalizer, preamplifiers, and professional audio applications. Its high performance characteristics also make it suitable for instrumentation applications where low noise is the key consideration.

The LM837 is internally compensated for unity gain operation. It is pin compatible with most other standard quad op amps and can therefore be used to upgrade existing systems with little or no change.

Features

- High slew rate — 10 V/μs (typ); 8 V/μs (min)
- Wide gain bandwidth product (min) — 25 MHz (typ); 15 MHz
- Power bandwidth — 200 kHz (typ)
- High output current — ±40 mA
- Excellent output drive performance — >600Ω
- Low input noise voltage — 4.5 nV/$\sqrt{Hz}$
- Low total harmonic distortion — 0.0015%
- Low offset voltage — 0.3 mV

Schematic and Connection Diagrams



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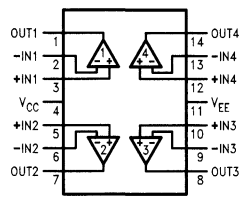
Dual-In-Line Package



DS009047-2

Top View
Order Number LM837M, LM837MX or LM837N
See NS Package Number M14A or N14A

National Semiconductor

LM1894
Dynamic Noise Reduction System DNR®

General Description

The LM1894 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is non-complementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

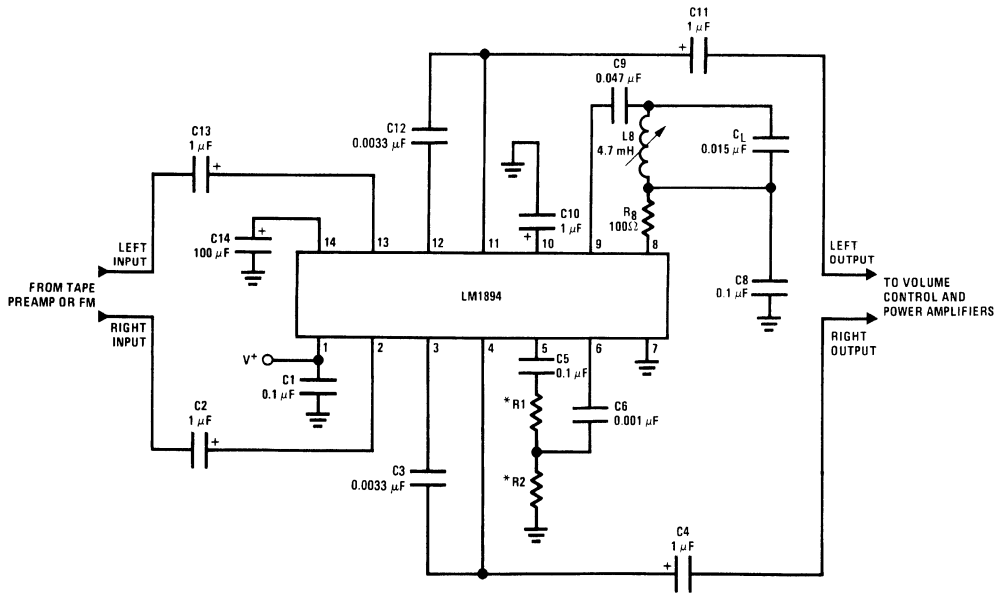
Features

- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 4.5V to 18V
- 1 Vrms input overload

Applications

- Automotive radio/tape players
- Compact portable tape players
- Quality HI-FI tape systems
- VCR playback noise reduction
- Video disc playback noise reduction

Typical Application



DS007918-1

*R1 + R2 = 1 kΩ total.
See Application Hints.

Order Number LM1894M or LM1894N
See NS Package Number M14A or N14A

FIGURE 1. Component Hook-Up for Stereo DNR System

National Semiconductor

Audio Codecs

National Semiconductor

LM4540
AC '97 Codec with National 3D Sound

General Description

The LM4540 is an audio codec for PC systems which performs the analog-intensive function of the Analog Codec '97 Rev 1.03 architecture. Using 18-Bit ΣΔ A/D and D/A converters, the LM4540 provides 90dB of dynamic range.

The LM4540 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 2 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. In addition, the LM4540 provides National's 3D Sound stereo enhancement technology.

The LM4540 features AC-Link, a synchronous, fixed rate serial bus for connection to the digital AC '97 Controller. The separation of the analog and digital functions of the AC '97 architecture allows for system design flexibility and increased overall performance.

Key Specifications

- Analog Mixer Dynamic Range 95dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)

Features

- Audio Codec '97 compliant
- Stereo 18-Bit ΣΔ A/D's and D/A's with 128X oversampling
- National's 3D Sound circuitry
- Power management support
- Digital Interface 3V and 5V compliant

Applications

- PC Audio Systems Requiring Only 2 Stereo Inputs (CD, Line) and 3 Mono Inputs (Mic, Phone, PC Beep)

Block Diagram

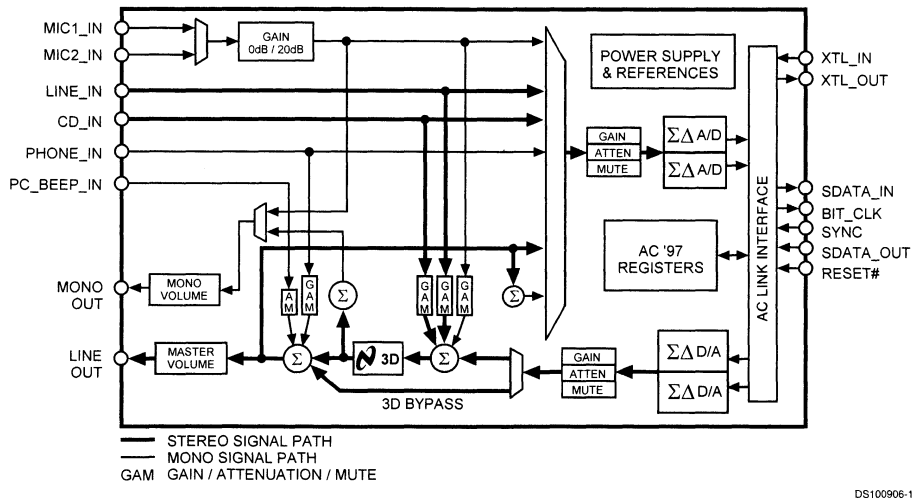


FIGURE 1. LM4540 Block Diagram

National Semiconductor

LM4543
AC '97 Codec with National 3D Sound

General Description

The LM4543 is an audio codec for PC systems which performs the analog-intensive function of the Analog Codec '97 Rev 1.03 architecture. Using 18-Bit ΣΔ A/D and D/A converters, the LM4543 provides 90dB of dynamic range.

The LM4543 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 4 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. In addition, the LM4543 provides National's 3D Sound stereo enhancement technology.

The LM4543 features AC-Link, a synchronous, fixed rate serial bus for connection to the digital AC '97 Controller. The separation of the analog and digital functions of the AC '97 architecture allows for system design flexibility and increased overall performance.

Key Specifications

- Analog Mixer Dynamic Range 95dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)

Features

- Audio Codec '97 compliant
- Stereo 18-Bit ΣΔ A/D's and D/A's with 128X oversampling
- National's 3D Sound circuitry
- Power management support
- Digital Interface 3V and 5V compliant

Applications

- Desktop PC Audio Systems
- Portable PC Audio Systems
- Mobile PC Audio Solutions

Block Diagram

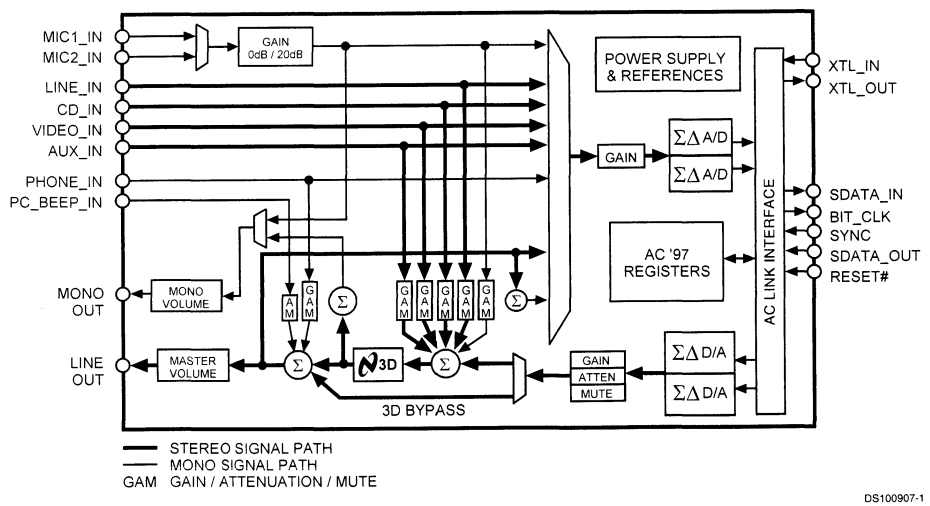


FIGURE 1. LM4543 Block Diagram

National Semiconductor

LM4545
AC '97 Codec with Stereo Headphone Amplifier and National 3D Sound

General Description

The LM4545 is an audio codec for PC systems which performs the analog-intensive function of the Analog Codec '97 Rev 1.03 Architecture. Using 18-Bit ΣΔ A/D and D/A converters, the LM4545 provides 90dB of dynamic range.

The LM4545 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 4 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. In addition, the LM4545 provides a stereo headphone amplifier with an independent gain control and National's 3D Sound stereo enhancement technology.

The LM4545 features AC-Link, a synchronous, fixed rate serial bus for connection to the digital AC '97 Controller. The separation of the analog and digital functions of the AC '97 architecture allows for system design flexibility and increased overall performance.

Key Specifications

- Analog Mixer Dynamic Range 95dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)
- Headphone THD+N at 50mW into 32Ω 0.02% (typ)

Features

- Audio Codec '97 compliant
- Stereo 18-Bit ΣΔ A/D's and D/A's with 128X oversampling
- Stereo headphone amp with separate gain control
- National's 3D Sound circuitry
- Power management support
- Digital Interface 3V and 5V compliant

Applications

- Desktop PC Audio Systems
- Portable PC Audio Systems
- Mobile PC Audio Solutions

Block Diagram

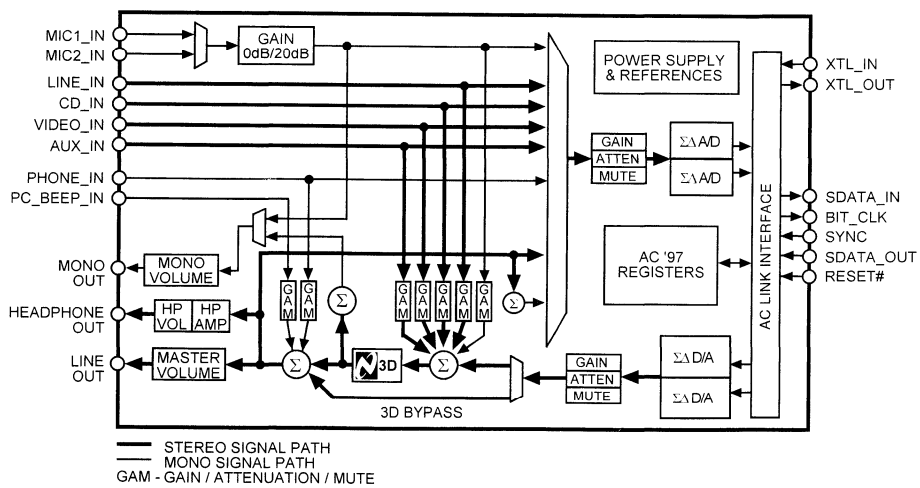


FIGURE 1. LM4545 Block Diagram

National Semiconductor

LM4546
AC '97 Rev 2 Codec with Sample Rate Conversion and National 3D Sound

General Description

The LM4546 is an audio codec for PC systems which is fully PC98 compliant and performs the analog intensive functions of the AC97 Rev 2 architecture. Using 18-bit Sigma-Delta A/D's and D/A's, the LM4546 provides 90dB of Dynamic Range.

The LM4546 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 2 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. The LM4546 also provides National's 3D Sound stereo enhancement.

The LM4546 supports variable sample rate conversion as defined in the AC97 Rev2 specification. The sample rate for the A/D and D/A can be programmed separately to convert any rate between 4kHz - 48kHz with a resolution of 1Hz. The AC97 architecture separates the analog and digital functions of the PC audio system allowing both for system design flexibility and increased performance.

Key Specifications

- Analog Mixer Dynamic Range 97dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)

Features

- AC'97 Rev 2 compliant
- National's 3D Sound circuitry
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz in 1Hz increments
- Multiple Codec support
- Advanced power management support
- Digital 3V and 5V compliant

Applications

- Desktop PC Audio Systems
- Portable PC Systems
- Mobile PC Systems

Block Diagram

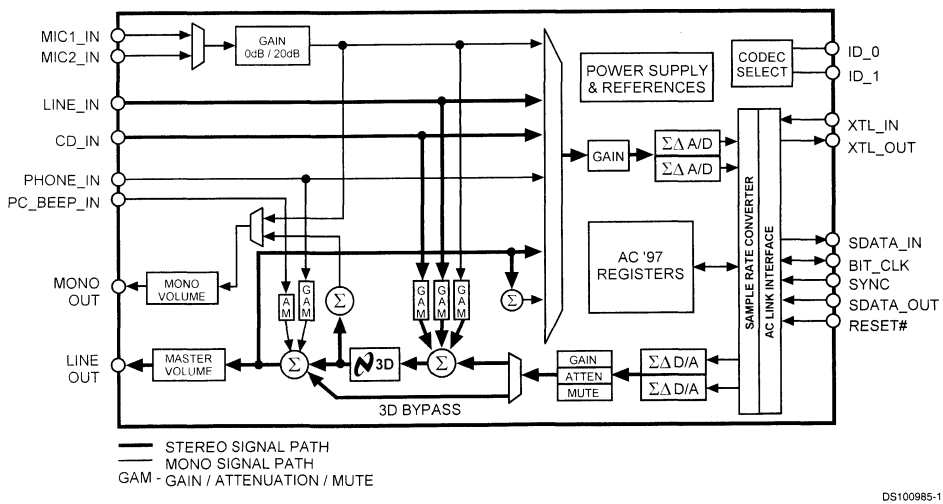


FIGURE 1. LM4546 Block Diagram

National Semiconductor

LM4548
AC '97 Rev 2 Codec with Sample Rate Conversion and National 3D Sound

General Description

The LM4548 is an audio codec for PC systems which is fully PC98 compliant and performs the analog intensive functions of the AC97 Rev2 architecture. Using 18-bit Sigma-Delta A/D's and D/A's, the LM4548 provides 90dB of Dynamic Range.

The LM4548 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 4 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. The LM4548 also provides the additional True Line-Level output and National's 3D Sound stereo enhancement.

The LM4548 supports variable sample rate conversion as defined in the AC97 Rev2 specification. The sample rate for the A/D and D/A can be programmed separately to convert any rate between 4kHz - 48kHz with a resolution of 1Hz. The AC97 architecture separates the analog and digital functions of the PC audio system allowing both for system design flexibility and increased performance.

Key Specifications

- Analog Mixer Dynamic Range 97dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)

Features

- AC'97 Rev2 compliant
- National's 3D Sound circuitry
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz in 1Hz increments.
- Multiple Codec Support
- True Line Level Output with volume control in addition to standard Line Out
- Advanced power management support
- Digital 3V and 5V compliant

Applications

- Desktop PC Audio Systems
- Portable PC Systems
- Mobile PC Systems

Block Diagram

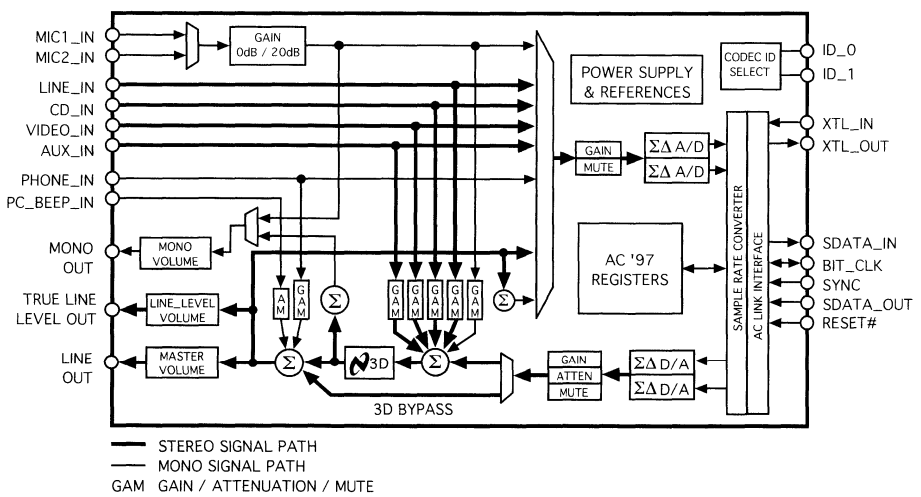


FIGURE 1. LM4548 Block Diagram

National Semiconductor

LM4549
AC '97 Rev 2.1 Codec with Sample Rate Conversion and National 3D Sound

General Description

The LM4549 is an audio codec for PC systems which is fully PC98 compliant and performs the analog intensive functions of the AC97 Rev2.1 architecture. Using 18-bit Sigma-Delta A/D's and D/A's, the LM4549 provides 90dB of Dynamic Range.

The LM4549 was designed specifically to provide a high quality audio path and provide all analog functionality in a PC audio system. It features full duplex stereo A/D's and D/A's and an analog mixer with 4 stereo and 3 mono inputs, each of which has separate gain, attenuation and mute control. The codec features a second Line Output known as True Line Level Out that is identical to Line Out but with independent volume control. The LM4549 also features National's 3D Sound stereo enhancement and variable sample rate conversion. The sample rate for the A/D and D/A can be programmed separately with a resolution of 1Hz to convert any rate between 4kHz-48kHz.

The AC97 architecture separates the analog and digital functions of the PC audio system allowing both for system design flexibility and increased performance.

Key Specifications

- Analog Mixer Dynamic Range 97dB (typ)
- D/A Dynamic Range 89dB (typ)
- A/D Dynamic Range 90dB (typ)

Features

- AC'97 Rev 2.1 compliant
- National's 3D Sound circuitry
- High quality Sample Rate Conversion (SRC) from 4kHz to 48kHz in 1Hz increments.
- Multiple Codec Support
- External Amplifier Power Down (EAPD) control from codec
- PC-Beep passthrough to Line Out while reset is held active low
- True Line Level Output with volume control independent of Line Out
- Digital 3V and 5V compliant

Applications

- Desktop PC Audio Systems on PCI cards, AMR cards, or with motherboard chips sets featuring AC-Link
- Portable PC Systems as on MDC cards, or with a chipset or accelerator featuring AC-Link

Block Diagram

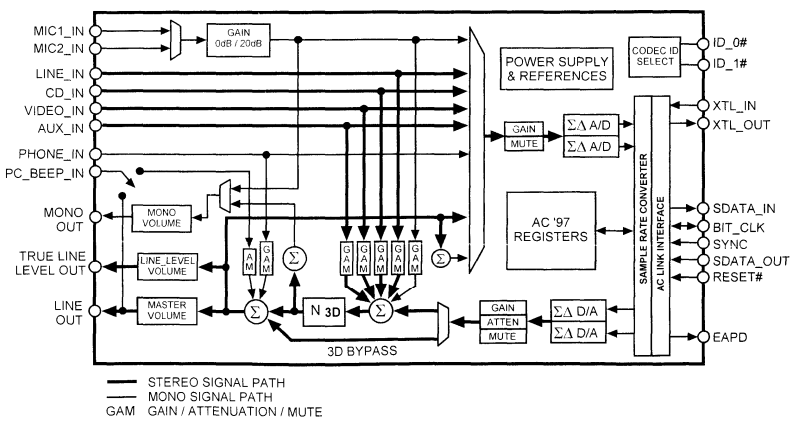


FIGURE 1. LM4549 Block Diagram

Section 5
Comparators

Section 5 Contents

National Semiconductor

Voltage Comparators Selection Guide

Part Number	Number Of Channels	Output Type (Note 1)	Response Time (ns) Typ (Note 2)	V_{OS} (mV) Max (Note 2)	Supply Voltage Range	I_S (mA) Max (Note 2)	I_B (nA) Max (Note 2)	Packages (Note 3)	Operating Temperature Ranges (Note 4)
LM111/211/311	1	OC	200	7.5	5 to 36	7.5	250	W10, J08, H08, M08, N08, E20, WG10	C, I, M
LM119/219/319	1	OC	80	8	5 to 36	12.5	1000	W10, J14, H10, M14, N14, E20, WG10	C, I, M
LM139/239/339	4	OC	1300	5	3 to 36	2.5	250	W14, J14, M14, N14, E20, WG14	C, I, M
LM161	1	OC	14	5	11 to 32	20	30000	H10	C, M
LM193/293/393	2	OC	1300	5	3 to 36	2.5	250	J08, H08, M08, N08	C, I, M
LM360	1	OC	14	5	9 to 16	.32	20000	M08, N08, H10	C
LM392	1	OC	1300	10	3 to 32	1	400	M08, N08	C
LM397	1	OC	250	7	5 to 30	0.7	250	M5	I
LM613	2	OC	1500	5	4 to 36	1	35	J16, M16	C, M
LM2901	4	OC	1300	7	3 to 36	2.5	250	M14, N14	I
LM2903	2	OC	1500	7	3 to 36	2.5	250	M08, N08	I
LM3302	4	OC	1300	20	3 to 28	2.5	500	N14	I
LM6511	1	OC	180	5	2.7 to 36	3.5	130	M08	I
LMC6762	2	PP	4000	3	2.7 to 15	0.02	40fA (typ)	M08	I
LMC6772	2	OC	4000	3	2.7 to 15	0.02	40fA (typ)	M08, N08	I
LMC7211A	1	PP	8000	5	2.7 to 15	0.014	40fA (typ)	M5, M08	I
LMC7211B	1	PP	8000	15	2.7 to 15	0.014	40fA (typ)	M5, M08	I
LMC7215	1	PP	12000	1	2 to 8	0.001	5fA (typ)	M08, M5	I, M
LMC7221A	1	OC	4000	5	2.7 to 15	0.014	40fA (typ)	M08, M5	I
LMC7221B	1	OC	4000	15	2.7 to 15	0.014	40fA (typ)	M08, M5	I
LMC7225	1	OC	12000	1	2 to 8	0.008	5fA (typ)	M5	I, M
LMV331	1	OC	300	7	2.7 to 5.5	0.1	250	M7, M5	I
LMV339	4	OC	300	7	2.7 to 5.5	0.20	250	M14, MT14	I
LMV393	2	OC	300	7	2.7 to 5.5	0.14	250	M08, MM08	I
LMV7219	1	PP	7	6	2.5 to 5.5	1.8	950	M5, M7	I
LMV7235	1	OC	45	6	2.7 to 5.5	.095	400	M5, M7	I
LMV7239	1	PP	45	6	2.7 to 5.5	.095	400	M5, M7	I
LMV7251	1	PP	400	6	1.8 to 5	.02	16	M5, M7	I
LMV7255	1	OC	400	6	1.8 to 5	.02	16	M5, M7	I
LP339	4	OC	8000	5	2 to 36	0.1	25	H14, N14	C

Note 1: OC = Open Collector, PP = Push-Pull

Note 2: Specifications are at T_A = 25˚C & V_S = +5V.

Note 3: Package Code Key (Letter = Package Type, Number = # of Pins)

Code Letter	Package Type
E	LCC
H/G	Metal Can
J/D	Ceramic Dual-in-Line
M	SOIC
MT	TSSOP
MM	MSOP
M5	SOT23-5
M7	SC70-5
N	Plastic Dual-in-Line (PDIP)
W	Flatpak
WG	Ceramic SOIC

Note 4: Temperature Ranges:

C = 0 to 70˚C

I = −40 to 85˚C

M = −55 to 125˚C

National Semiconductor

Voltage Comparator Definition Of Terms

Input Current (I_B or I_{in}): The average of the two input currents.

Input Offset Current (I_{OS}): The difference of currents between the two input terminals.

Input Offset Voltage (V_{OS}): The DC error voltage which exists between the input terminals due to non-ideal balancing of the input stage.

Input Voltage Range (V_{CM}): Typically the range of voltages on the input terminals for which the comparator's performance is specified.

Logic threshold Voltage (V_T): The voltage that exceeds the input offset voltage causing the output to change state.

Offset Voltage Temperature Coefficient (TCV_{OS}): The average rate of change in offset voltage for junction temperature variation over a specified temperature range.

Offset Current Temperature Coefficient (TCI_{OS}): The average rate of change in offset current for junction temperature variation over a specified temperature range.

Output High Voltage (V_{OH}): The high DC output voltage with output driven high with specified output current.

Output Low Voltage (V_{OL}): The low DC output voltage with the output driven low with specified sinking current.

Output Leakage Current ($I_{LEAKAGE}$): The current into the output terminal with the output driven high. Applies to open collector or open drain outputs.

Output Resistance (R_O): The apparent output resistance of a comparator, typically illustrated with an ideal comparator with zero output resistance in series with an output resistor, Rout, measured under DC conditions.

Output Sink Current (I_{SC-}): The maximum negative current that can be sunk by the comparator.

Output Source Current (I_{SC+}): The maximum positive current that can be sourced by the comparator with push/pull output state.

Power Consumption: The power required to operate the comparator with no output load.

Response Time (t_r): The interval between the application of an input step function and the time when the output crosses the logic threshold voltage.

Saturation Voltage (V_{SAT}): The low DC voltage of an open collector output with the output driven low the with specified sinking current.

Strobe Current: The current out of the strobe terminal when it is a zero logic level.

Strobe Output Level: The comparator DC output voltage, independent of input conditions, when the strobe is active.

Strobe "ON" Voltage: The maximum voltage on the strobe terminal required forcing the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to a logic one level and the input is at a level that would drive the output low.

Supply current (I_S). The current required from the positive or negative supply to operate the comparator with no output load.

Voltage Gain (A_V): The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

Voltage Overdrive: The input step voltage that goes beyond the minimum drive required to change the output state from one logic level to the opposite logic level.

NOTE: All parameters are under specific conditions.

National Semiconductor

LM111/LM211/LM311 Voltage Comparator

1.0 General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

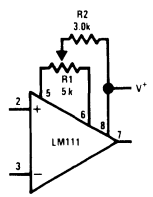
The LM211 is identical to the LM111, except that its performance is specified over a −25°C to +85°C temperature range instead of −55°C to +125°C. The LM311 has a temperature range of 0°C to +70°C.

2.0 Features

- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V

3.0 Typical Applications (Note 3)

Offset Balancing



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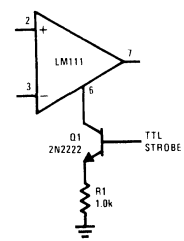
Strobing



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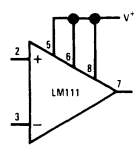
Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

Increasing Input Stage Current (Note 1)



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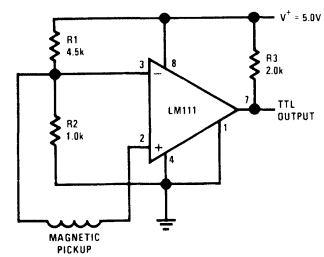
Note 1: Increases typical common mode slew from 7.0V/μs to 18V/μs.

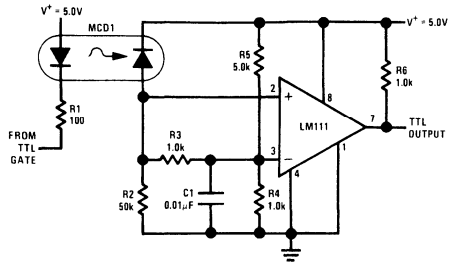
Detector for Magnetic Transducer



DS005704-39

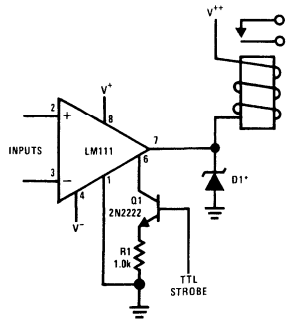
3.0 Typical Applications (Note 3) (Continued)

Digital Transmission Isolator



DS005704-40

Relay Driver with Strobe

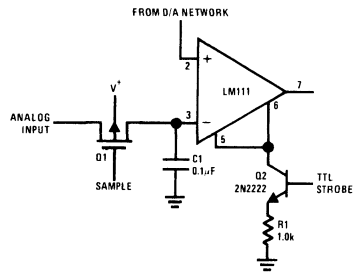


DS005704-41

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input and Output Stages (Note 2)



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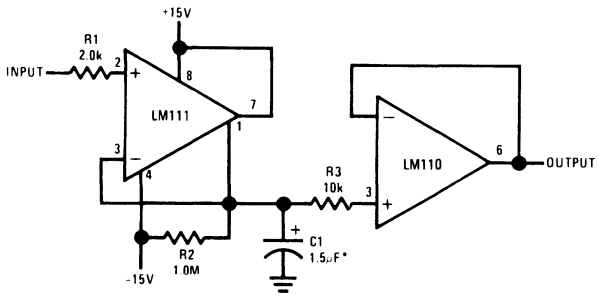
Note: Do Not Ground Strobe Pin.

Note 2: Typical input current is 50 pA with inputs strobed off.

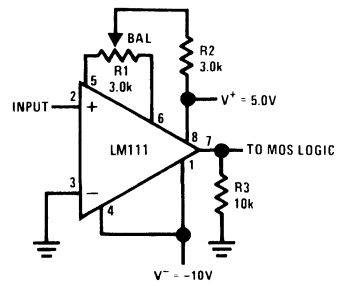
Note 3: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

Positive Peak Detector



DS005704-23

Zero Crossing Detector Driving MOS Logic



DS005704-24

*Solid tantalum

4.0 Absolute Maximum Ratings for the LM111/LM211 (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	50V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 4)	±15V
Output Short Circuit Duration	10 sec
Operating Temperature Range	
LM111	−55°C to 125°C
LM211	−25°C to 85°C
Lead Temperature (Soldering, 10 sec)	260°C
Voltage at Strobe Pin	V^+−5V
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 11)	300V

Electrical Characteristics (Note 6)

for the LM111 and LM211

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 7)	T_A=25°C, R_S≤50k		0.7	3.0	mV
Input Offset Current	T_A=25°C		4.0	10	nA
Input Bias Current	T_A=25°C		60	100	nA
Voltage Gain	T_A=25°C	40	200		V/mV
Response Time (Note 8)	T_A=25°C		200		ns
Saturation Voltage	V_{IN}≤−5 mV, I_{OUT}=50 mA T_A=25°C		0.75	1.5	V
Strobe ON Current (Note 9)	T_A=25°C		2.0	5.0	mA
Output Leakage Current	V_{IN}≥5 mV, V_{OUT}=35V T_A=25°C, I_{STROBE}=3 mA		0.2	10	nA
Input Offset Voltage (Note 7)	R_S≤50 k			4.0	mV
Input Offset Current (Note 7)				20	nA
Input Bias Current				150	nA
Input Voltage Range	V^+=15V, V^-=−15V, Pin 7 Pull-Up May Go To 5V	−14.5	13.8,-14.7	13.0	V
Saturation Voltage	V^+≥4.5V, V^-=0 V_{IN}≤−6 mV, I_{OUT}≤8 mA		0.23	0.4	V
Output Leakage Current	V_{IN}≥5 mV, V_{OUT}=35V		0.1	0.5	μA
Positive Supply Current	T_A=25°C		5.1	6.0	mA
Negative Supply Current	T_A=25°C		4.1	5.0	mA

Note 4: This rating applies for ±15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 5: The maximum junction temperature of the LM111 is 150°C, while that of the LM211 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 110°C/W, junction to ambient.

Note 6: These specifications apply for V_S=±15V and Ground pin at ground, and −55°C≤T_A≤+125°C, unless otherwise stated. With the LM211, however, all temperature specifications are limited to −25°C≤T_A≤+85°C. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 7: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

Note 8: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 9: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 10: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 11: Human body model, 1.5 kΩ in series with 100 pF.

5.0 Absolute Maximum Ratings for the LM311 (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage (V_{84})	36V
Output to Negative Supply Voltage (V_{74})	40V
Ground to Negative Supply Voltage (V_{14})	30V
Differential Input Voltage	±30V
Input Voltage (Note 13)	±15V
Power Dissipation (Note 14)	500 mW
ESD Rating (Note 19)	300V
Output Short Circuit Duration	10 sec
Operating Temperature Range	0° to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (soldering, 10 sec)	260°C
Voltage at Strobe Pin	V^+−5V
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 15)

for the LM311

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage (Note 16)	T_A=25°C, R_S≤50k		2.0	7.5	mV
Input Offset Current(Note 16)	T_A=25°C		6.0	50	nA
Input Bias Current	T_A=25°C		100	250	nA
Voltage Gain	T_A=25°C	40	200		V/mV
Response Time (Note 17)	T_A=25°C		200		ns
Saturation Voltage	V_{IN}≤−10 mV, I_{OUT}=50 mA T_A=25°C		0.75	1.5	V
Strobe ON Current (Note 18)	T_A=25°C		2.0	5.0	mA
Output Leakage Current	V_{IN}≥10 mV, V_{OUT}=35V T_A=25°C, I_{STROBE}=3 mA V^- = Pin 1 = −5V		0.2	50	nA
Input Offset Voltage (Note 16)	R_S≤50K			10	mV
Input Offset Current (Note 16)				70	nA
Input Bias Current				300	nA
Input Voltage Range		−14.5	13.8,−14.7	13.0	V
Saturation Voltage	V^+≥4.5V, V^-=0 V_{IN}≤−10 mV, I_{OUT}≤8 mA		0.23	0.4	V
Positive Supply Current	T_A=25°C		5.1	7.5	mA
Negative Supply Current	T_A=25°C		4.1	5.0	mA

Note 12: "Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits."

Note 13: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 14: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 15: These specifications apply for V_S=±15V and Pin 1 at ground, and 0°C < T_A < +70°C, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

Note 16: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S.

Note 17: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 18: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 19: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM119/LM219/LM319
High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

The LM319A offers improved precision over the standard LM319, with tighter tolerances on offset voltage, offset current, and voltage gain.

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to ±15V. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

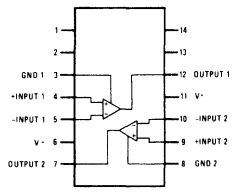
The LM119 is specified from −55°C to +125°C, the LM219 is specified from −25°C to +85°C, and the LM319A and LM319 are specified from 0°C to +70°C.

Features

- Two independent comparators
- Operates from a single 5V supply
- Typically 80 ns response time at ±15V
- Minimum fan-out of 2 each side
- Maximum input current of 1 μA over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Connection Diagram

Dual-In-Line Package



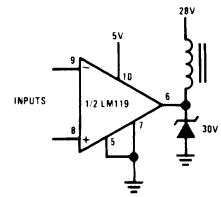
DS005705-4

Top View
Order Number LM119J, LM119J/883 (Note 1), **LM219J, LM319J, LM319AM, LM319M, LM319AN or LM319N**
See NS Package Number J14A, M14A or N14A

Note 1: Also available per SMD# 8601401 or JM38510/10306

Typical Applications (Note 2)

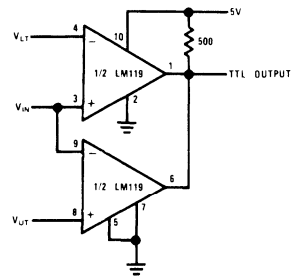
Relay Driver



DS005705-5

Note 2: Pin numbers are for metal can package.

Window Detector



DS005705-6

V_{OUT} = 5V for $V_{LT} \leq V_{IN} \leq V_{UT}$
V_{OUT} = 0 for $V_{IN} \leq V_{LT}$ or $V_{IN} \geq V_{UT}$

Absolute Maximum Ratings (Note 9)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 3)	±15V
ESD rating (1.5 kΩ in series with 100 pF)	800V
Power Dissipation (Note 4)	500 mW
Output Short Circuit Duration	10 sec
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM119	−55°C to 125°C
LM219	−25°C to 85°C

Electrical Characteristics (Note 5)

Parameter	Conditions	LM119/LM219			Units
		Min	Typ	Max	
Input Offset Voltage (Note 6)	$T_A = 25°C$, $R_S \leq 5k$		0.7	4.0	mV
Input Offset Current (Note 6)	$T_A = 25°C$		30	75	nA
Input Bias Current	$T_A = 25°C$		150	500	nA
Voltage Gain	$T_A = 25°C$ (Note 8)	10	40		V/mV
Response Time (Note 7)	$T_A = 25°C$, $V_S = \pm 15V$		80		ns
Saturation Voltage	$V_{IN} \leq -5$ mV, $I_{OUT} = 25$ mA				
	$T_A = 25°C$		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$				
	$T_A = 25°C$		0.2	2	μA
Input Offset Voltage (Note 6)	$R_S \leq 5k$			7	mV
Input Offset Current (Note 6)				100	nA
Input Bias Current				1000	nA
Input Voltage Range	$V_S = \pm 15V$	−12	±13	+12	V
	$V^+ = 5V$, $V^- = 0$	1		3	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$				
	$V_{IN} \leq -6$ mV, $I_{SINK} \leq 3.2$ mA				
	$T_A \geq 0°C$		0.23	0.4	V
	$T_A \leq 0°C$			0.6	V
Output Leakage Current	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$,		1	10	μA
	$V^- = V_{GND} = 0V$				
Differential Input Voltage				±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	11.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	4.5	mA

Note 3: For supply voltages less than ±15V the absolute maximum input voltage is equal to the supply voltage.

Note 4: The maximum junction temperature of the LM119 is 150°C, while that of the LM219 is 110°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the J14 and N14 packages is 100°C/W, junction to ambient.

Note 5: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

Note 6: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 7: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 8: Output is pulled up to 15V through a 1.4 kΩ resistor.

Note 9: Refer to RETS119X for LM119H/883 and LM119J/883 specifications.

Absolute Maximum Ratings

LM319A/319 (Note 9)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Total Supply Voltage	36V
Output to Negative Supply Voltage	36V
Ground to Negative Supply Voltage	25V
Ground to Positive Supply Voltage	18V
Differential Input Voltage	±5V
Input Voltage (Note 10)	±15V
Power Dissipation (Note 11)	500 mW
Output Short Circuit Duration	10 sec
ESD rating (1.5 kΩ in series with 100 pF)	800V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec.)	260°C
Small Outline Package	
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM319A, LM319	0°C to 70°C

Electrical Characteristics (Note 12)

Parameter	Conditions	LM319A			LM319			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (Note 13)	$T_A = 25°C$, $R_S \leq 5k$		0.5	1.0		2.0	8.0	mV
Input Offset Current (Note 13)	$T_A = 25°C$		20	40		80	200	nA
Input Bias Current	$T_A = 25°C$		150	500		250	1000	nA
Voltage Gain	$T_A = 25°C$ (Note 15)	20	40		8	40		V/mV
Response Time (Note 14)	$T_A = 25°C$, $V_S = \pm 15V$		80			80		ns
Saturation Voltage	$V_{IN} \leq -10$ mV, $I_{OUT} = 25$ mA $T_A = 25°C$		0.75	1.5		0.75	1.5	V
Output Leakage Current	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$, $V^- = {}^V GND = 0V$, $T_A = 25°C$		0.2	10		0.2	10	µA
Input Offset Voltage (Note 13)	$R_S \leq 5k$			10			10	mV
Input Offset Current (Note 13)				300			300	nA
Input Bias Current				1000			1200	nA
Input Voltage Range	$V_S = \pm 15V$		±13			±13		V
	$V^+ = 5V$, $V^- = 0$	1		3	1		3	V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10$ mV, $I_{SINK} \leq 3.2$ mA		0.3	0.4		0.3	0.4	V
Differential Input Voltage				±5			±5	V
Positive Supply Current	$T_A = 25°C$, $V^+ = 5V$, $V^- = 0$		4.3			4.3		mA
Positive Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		8	12.5		8	12.5	mA
Negative Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		3	5		3	5	mA

Note 10: For supply voltages less than ±15 the absolute maximum input voltage is equal to the supply voltage.

Note 11: The maximum junction temperature of the LM319A and LM319 is 85°C. For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 19°C/W, junction to case. The thermal resistance of the N14 and J14 package is 100°C/W, junction to ambient. The thermal resistance of the M14 package is 115°C/W, junction to ambient.

Note 12: These specifications apply for $V_S = \pm 15V$, and $0°C < T_A < 70°C$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. Do not operate the device with more than 16V from ground to V_S.

Note 13: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 14: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 15: Output is pulled up to 15V through a 1.4 kΩ resistor.

National Semiconductor

LM139/LM239/LM339/LM2901/LM3302
Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

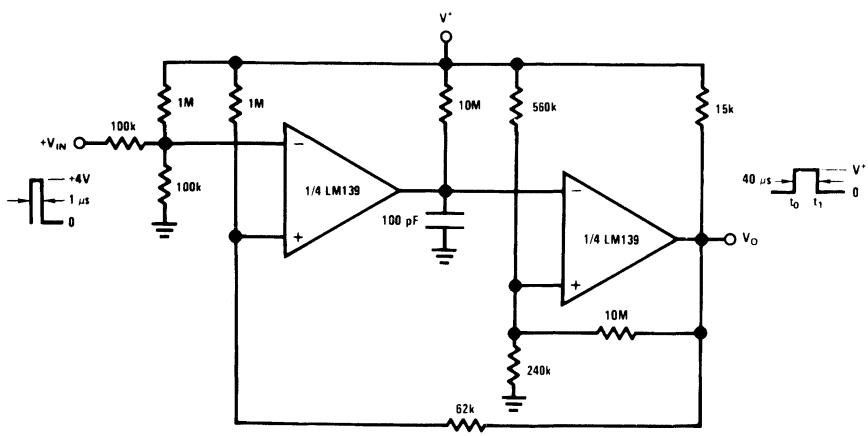
Features

- Wide supply voltage range
- LM139/139A Series 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM2901: 2 to 36 V_{DC} or ±1 to ±18 V_{DC}
- LM3302: 2 to 28 V_{DC} or ±1 to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Offset voltage: ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

One-Shot Multivibrator with Input Lock Out



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Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Input Current (V_{IN}<−0.3 V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD rating (1.5 kΩ in series with 100 pF)	600V	600V

Electrical Characteristics

(V^+=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		1.0	2.0		1.0	2.0		2.0	5.0	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM}=0V		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)}$−$I_{IN(-)}$, V_{CM}=0V		3.0	25		5.0	50		3.0	25	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+−1.5	0		V^+−1.5	0		V^+−1.5	V_{DC}
Supply Current	R_L=∞ on all Comparators,		0.8	2.0		0.8	2.0		0.8	2.0	mA_{DC}
	R_L=∞, V^+=36V,					1.0	2.5		1.0	2.5	mA_{DC}
	(LM3302, V^+=28 V_{DC})										
Voltage Gain	R_L≥15 kΩ, V^+=15 V_{DC} V_o= 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}= 1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ		300			300			300		ns
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, (Note 7)		1.3			1.3			1.3		µs

Electrical Characteristics (Continued)

(V^+=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Sink Current	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, $V_O \leq$1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, $I_{SINK} \leq$4 mA		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=5 V_{DC}		0.1			0.1			0.1		nA_{DC}

Electrical Characteristics

(V^+=5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		2.0	5.0		2.0	7.0		3	20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM}=0V		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)}$–$I_{IN(-)}$, V_{CM}=0V		5.0	50		5	50		3	100	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+–1.5	0		V^+–1.5	0		V^+–1.5	V_{DC}
Supply Current	R_L=∞ on all Comparators, R_L=∞, V^+=36V, (LM3302, V^+=28 V_{DC})		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5		0.8 1.0	2.0 2.5	mA_{DC} mA_{DC}
Voltage Gain	$R_L \geq$15 kΩ, V^+=15 V_{DC} V_o= 1 V_{DC} to 11 V_{DC}	50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}= 1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ,		300			300			300		ns
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, (Note 7)		1.3			1.3			1.3		µs
Output Sink Current	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, $V_O \leq$1.5 V_{DC}	6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, $I_{SINK} \leq$4 mA		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=5 V_{DC}		0.1			0.1			0.1		nA_{DC}

Electrical Characteristics

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0			4.0			9.0	mV_{DC}
Input Offset Current	$I_{IN(+)}$–$I_{IN(-)}$, V_{CM}=0V			100			150			100	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, V_{CM}=0V (Note 5)			300			400			300	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)	0		V^+–2.0	0		V^+–2.0	0		V^+–2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, $I_{SINK} \leq$4 mA			700			700			700	mV_{DC}

Electrical Characteristics (Continued)

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=30 V_{DC}, (LM3302, V_O=28 V_{DC})			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s≥0 V_{DC} (or V^-, if used), (Note 8)			36			36			36	V_{DC}

Electrical Characteristics

(V^+ = 5.0 V_{DC}, (Note 4))

Parameter	Conditions	LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)}$–$I_{IN(-)}$, V_{CM}=0V			150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, V_{CM}=0V (Note 5)			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	V^+=30 V_{DC} (LM3302, V^+=28 V_{DC}) (Note 6)			V^+–2.0	0		V^+–2.0	0		V^+–2.0	V_{DC}
Saturation Voltage	$V_{IN(-)}$=1 V_{DC}, $V_{IN(+)}$=0, I_{SINK}≤4 mA			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)}$=1 V_{DC}, $V_{IN(-)}$=0, V_O=30 V_{DC}, (LM3302, V_O=28 V_{DC})			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s≥0 V_{DC} (or V^-, if used), (Note 8)			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D≤100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°)C.

Note 4: These specifications are limited to −55°C≤T_A≤+125°C, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to −25°C≤T_A≤+85°C, the LM339/LM339A temperature specifications are limited to 0°C≤T_A≤+70°C, and the LM2901, LM3302 temperature range is −40°C≤T_A≤+85°C.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ −1.5V at 25°C, but either or both inputs can go to +30 V_{DC} without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC}below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, V_O≅1.4 V_{DC}, R_S=0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ −1.5 V_{DC}), at 25°C. For LM3302, V^+ from 5 V_{DC} to 28 V_{DC}.

Note 10: Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

National Semiconductor

LM160/LM360
High Speed Differential Comparator

General Description

The LM160/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the μA760/μA760C, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital convertors and zero-crossing detectors in disk file systems.

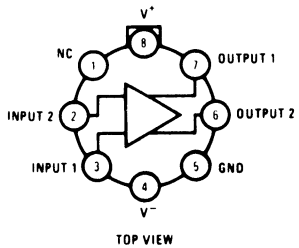
Features

- Guaranteed high speed: 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

5

Connection Diagrams

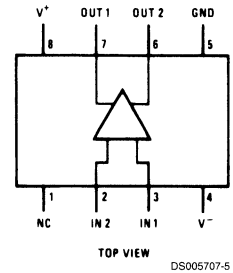
Metal Can Package



DS005707-4

Order Number LM160H/883 (Note 1)
See NS Package Number H08C

Dual-In-Line Package



DS005707-5

Order Number LM360M, LM360MX or LM360N
See NS Package Number M08A or N08E

Note 1: Also available in SMD# 5962-8767401

Absolute Maximum Ratings (Notes 6, 8)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage	+8V
Negative Supply Voltage	−8V
Peak Output Current	20 mA
Differential Input Voltage	±5V
Input Voltage	$V^+ \geq V_{IN} \geq V^-$
ESD Tolerance (Note 9)	1600V
Operating Temperature Range	
LM160	−55°C to +125°C
LM360	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 sec.)	260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

($T_{MIN} \leq T_A \leq T_{MAX}$)

Parameter	Conditions	Min	Typ	Max	Units
Operating Conditions					
Supply Voltage V_{CC}^+		4.5	5	6.5	V
Supply Voltage V_{CC}^-		−4.5	−5	−6.5	V
Input Offset Voltage	$R_S \leq 200\Omega$		2	5	mV
Input Offset Current			0.5	3	μA
Input Bias Current			5	20	μA
Output Resistance (Either Output)	$V_{OUT} = V_{OH}$		100		Ω
Response Time	$T_A = 25°C$, $V_S = \pm5V$ (Notes 2, 7)		13	25	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Notes 3, 7)		12	20	ns
	$T_A = 25°C$, $V_S = \pm5V$ (Notes 4, 7)		14		ns
Response Time Difference between Outputs					
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$ (Notes 2, 7)		2		ns
(t_{pd} of $+V_{IN2}$) − (t_{pd} of $-V_{IN1}$)	$T_A = 25°C$ (Notes 2, 7)		2		ns
(t_{pd} of $+V_{IN1}$) − (t_{pd} of $+V_{IN2}$)	$T_A = 25°C$ (Notes 2, 7)		2		ns
(t_{pd} of $-V_{IN1}$) − (t_{pd} of $-V_{IN2}$)	$T_A = 25°C$ (Notes 2, 7)		2		ns
Input Resistance	f = 1 MHz		17		kΩ
Input Capacitance	f = 1 MHz		3		pF
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$		8		μV/°C
Average Temperature Coefficient of Input Offset Current			7		nA/°C
Common Mode Input Voltage Range	$V_S = \pm6.5V$	±4	±4.5		V
Differential Input Voltage Range		±5			V
Output High Voltage (Either Output)	$I_{OUT} = -320$ μA, $V_S = \pm4.5V$	2.4	3		V
Output Low Voltage (Either Output)	$I_{SINK} = 6.4$ mA		0.25	0.4	V
Positive Supply Current	$V_S = \pm6.5V$		18	32	mA
Negative Supply Current	$V_S = \pm6.5V$		−9	−16	mA

Note 2: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 3: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.

Electrical Characteristics (Continued)

Note 4: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Note 5: Typical thermal impedances are as follows:

Cavity DIP (J):	θ_{jA}	135°C/W	Header (H)	θ_{jA}	165°C/W	(Still Air)
Molded DIP (N):	θ_{jA}	130°C/W			67°C/W	(400 LF/min Air Flow)
				θ_{jC}	25°C/W	

Note 6: The device may be damaged if used beyond the maximum ratings.

Note 7: Measurements are made in AC Test Circuit, Fanout = 1

Note 8: Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.

Note 9: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM161/LM361
High Speed Differential Comparators

General Description

The LM161/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (±15V).

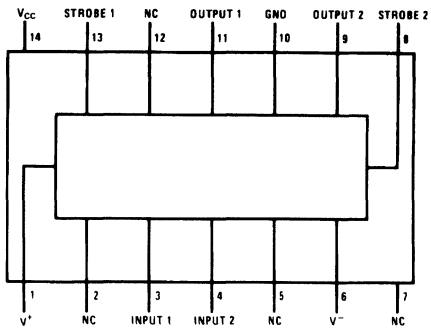
Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

Features

- Independent strobes
- Guaranteed high speed: 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies: ±15V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Connection Diagrams

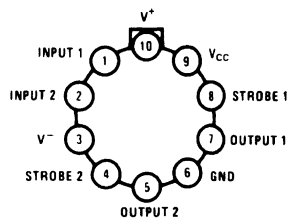
Dual-In-Line Package



DS005708-2

Top View
Order Number LM361M, LM361MX or LM361N
See NS Package Number M14A or N14A

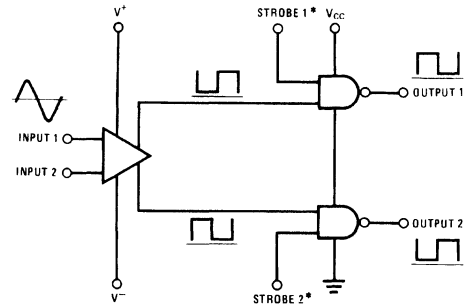
Metal Can Package



DS005708-3

Order Number LM161H/883 or LM361H
See NS Package Number H10C

Logic Diagram



DS005708-4

*Output is low when current is drawn from strobe pin.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Positive Supply Voltage, V^+	+16V
Negative Supply Voltage, V^-	−16V
Gate Supply Voltage, V_{CC}	+7V
Output Voltage	+7V
Differential Input Voltage	±5V
Input Common Mode Voltage	±6V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	T_{MIN} T_{MAX}
LM161	−55°C to +125°C
	−25°C to +85°C
LM361	0°C to +70°C
Lead Temp. (Soldering, 10 seconds)	260°C
For Any Device Lead Below V^-	0.3V

Operating Conditions

	Min	Typ	Max
Supply Voltage V^+			
LM161	5V		15V
LM361	5V		15V
Supply Voltage V^-			
LM161	−6V		−15V
LM361	−6V		−15V
Supply Voltage V_{CC}			
LM161	4.5V	5V	5.5V
LM361	4.75V	5V	5.25V
ESD Tolerance (Note 5)			1600V
Soldering Information			
Dual-In-Line Package			
Soldering (10 seconds)			260°C
Small Outline Package			
Vapor Phase (60 seconds)			215°C
Infrared (15 seconds)			220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

(V^+ = +10V, V_{CC} = +5V, V^- = −10V, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161			LM361			
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage			1	3		1	5	mV
Input Bias Current	T_A=25°C		5			10		µA
				20			30	µA
Input Offset Current	T_A=25°C		2			2		µA
				3			5	µA
Voltage Gain	T_A=25°C		3			3		V/mV
Input Resistance	T_A=25°C, f=1 kHz		20			20		kΩ
Logical "1" Output Voltage	V_{CC}=4.75V, I_{SOURCE}=−0.5 mA	2.4	3.3		2.4	3.3		V
Logical "0" Output Voltage	V_{CC}=4.75V, I_{SINK}=6.4 mA			0.4			0.4	V
Strobe Input "1" Current (Output Enabled)	V_{CC}=5.25V, V_{STROBE}=2.4V			200			200	µA
Strobe Input "0" Current (Output Disabled)	V_{CC}=5.25V, V_{STROBE}=0.4V			−1.6			−1.6	mA
Strobe Input "0" Voltage	V_{CC}=4.75V			0.8			0.8	V
Strobe Input "1" Voltage	V_{CC}=4.75V	2			2			V
Output Short Circuit Current	V_{CC}=5.25V, V_{OUT}=0V	−18		−55	−18		−55	mA
Supply Current I^+	V^+=10V, V^-=−10V, V_{CC}=5.25V, −55°C≤T_A≤125°C			4.5				mA
Supply Current I^+	V^+=10V, V^-=−10V, V_{CC}=5.25V, 0°C≤T_A≤70°C						5	mA
Supply Current I^-	V^+=10V, V^-=−10V, V_{CC}=5.25V, −55°C≤T_A≤125°C			10				mA

Electrical Characteristics (Continued)

(V^+ = +10V, V_{CC} = +5V, V^- = −10V, $T_{MIN} \le T_A \le T_{MAX}$, unless noted)

Parameter	Conditions	Limits						Units
		LM161			LM361			
		Min	Typ	Max	Min	Typ	Max	
Supply Current I^-	V^+=10V, V^-=−10V, V_{CC}=5.25V, 0°C≤T_A≤70°C						10	mA
Supply Current I_{CC}	V^+=10V, V^-=−10V, V_{CC}=5.25V, −55°C≤T_A≤125°C			18				mA
Supply Current I_{CC}	V^+=10V, V^-=−10V, V_{CC}=5.25V, 0°C≤T_A≤70°C						20	mA
Transient Response	V_{IN} = 50 mV overdrive (Note 3)							
Propagation Delay Time ($t_{pd(0)}$)	T_A=25°C		14	20		14	20	ns
Propagation Delay Time ($t_{pd(1)}$)	T_A=25°C		14	20		14	20	ns
Delay Between Output A and B	T_A=25°C		2	5		2	5	ns
Strobe Delay Time ($t_{pd(0)}$)	T_A=25°C		8			8		ns
Strobe Delay Time ($t_{pd(1)}$)	T_A=25°C		8			8		ns

Note 1: The device may be damaged by use beyond the maximum ratings.

Note 2: Typical thermal impedances are as follows:

	H Package	J Package	N Package
θ_{jA}	165°C/W (Still Air) 67°C/W (400 LF/Min Air Flow)	112°C/W	105°C/W
θ_{jC}	25°C/W		

DS005708-17

Note 3: Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.

Note 4: Refer to RETS161X for LM161H and LM161J military specifications.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

National Semiconductor

LM193/LM293/LM393/LM2903
Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

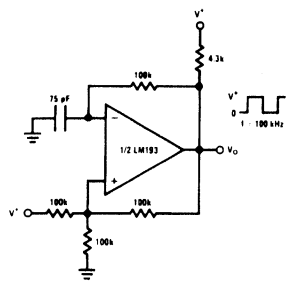
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

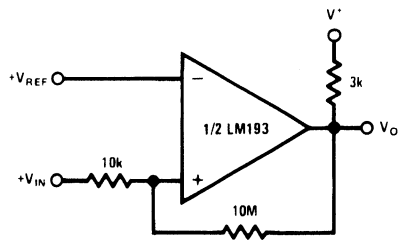
- Wide supply
  - — Voltage range: 2.0V to 36V
  - — single or dual supplies: ±1.0V to ±18V
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current: 25 nA
- Low input offset current: ±5 nA
- Maximum offset voltage: ±3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage,: 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Squarewave Oscillator



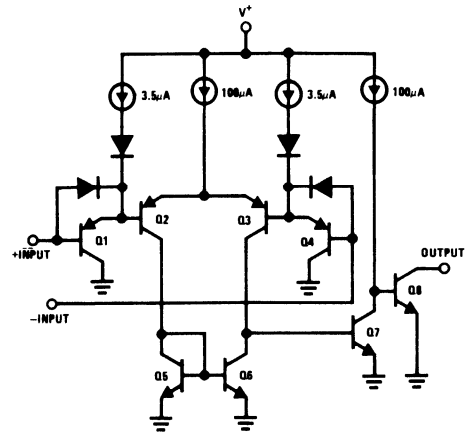
DS005709-38

Non-Inverting Comparator with Hysteresis



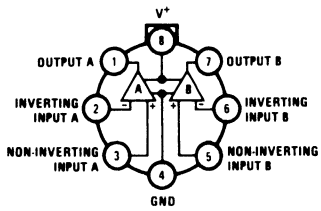
DS005709-9

Schematic and Connection Diagrams



DS005709-2

Metal Can Package

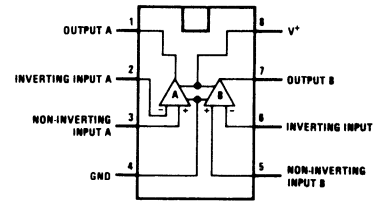


TOP VIEW

DS005709-3

Order Number LM193H *
LM193H/883 , LM193AH-QMLV **
LM193AH, LM193AH/883,
LM293H or LM393H
See NS Package Number H08C

Dual-In-Line Package



TOP VIEW

DS005709-1

Order Number LM193J/883 *
LM193AJ/883, LM193AJ-QMLV **
LM393M, LM393MX, LM2903M,
LM2903MX, LM393N or LM2903N
See NS Package Number J08A,
M08A or N08E

Note: * Also available per JM38510/11202

Note: ** See STD Mil DWG 5962-94526

Absolute Maximum Ratings (Note 10)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V^+	36V
Differential Input Voltage (Note 8)	36V
Input Voltage	−0.3V to +36V
Input Current (V_{IN}<−0.3V) (Note 3)	50 mA
Power Dissipation (Note 1)	
Molded DIP	780 mW
Metal Can	660 mW
Small Outline Package	510 mW
Output Short-Circuit to Ground (Note 2)	Continuous
Operating Temperature Range	
LM393/LM393A	0°C to +70°C
LM293/LM293A	−25°C to +85°C
LM193/LM193A	−55°C to +125°C
LM2903	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
(Soldering, 10 seconds)	+260°C
Soldering Information	
Dual-In-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	215°C
Vapor Phase (60 seconds)	
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating	
(1.5 kΩ in series with 100 pF)	1300V

Electrical Characteristics

(V^+=5V, T_A = 25°C, unless otherwise stated)

Parameter	Conditions		LM193A			LM293A, LM393A			Units
			Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			1.0	2.0		1.0	2.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V (Note 5)			25	100		25	250	nA
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$ V_{CM} = 0V			3.0	25		5.0	50	nA
Input Common Mode Voltage Range	V+ = 30V (Note 6)		0		V^+−1.5	0		V+−1.5	V
Supply Current	R_L=∞	V^+=5V		0.4	1		0.4	1	mA
		V^+=36V		1	2.5		1	2.5	mA
Voltage Gain	R_L≥15 kΩ, V^+=15V V_O = 1V to 11V		50	200		50	200		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V V_{RL}=5V, R_L=5.1 kΩ			300			300		ns
Response Time	V_{RL}=5V, R_L=5.1 kΩ (Note 7)			1.3			1.3		µs
Output Sink Current	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, V_O≈1.5V		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, I_{SINK}≤4 mA			250	400		250	400	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN}(+)$=1V, V_O=5V			0.1			0.1		nA

Electrical Characteristics

(V^+=5V, T_A = 25°C, unless otherwise stated)

Parameter	Conditions		LM193			LM293, LM393			LM2903			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			1.0	5.0		1.0	5.0		2.0	7.0	mV
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output In Linear Range, V_{CM} = 0V (Note 5)			25	100		25	250		25	250	nA
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$ V_{CM} = 0V			3.0	25		5.0	50		5.0	50	nA
Input Common Mode Voltage Range	V+ = 30V (Note 6)		0		V+−1.5	0		V+−1.5	0		V+−1.5	V
Supply Current	R_L=∞	V^+=5V		0.4	1		0.4	1		0.4	1.0	mA
		V^+=36V		1	2.5		1	2.5		1	2.5	mA

Electrical Characteristics (Continued)

(V^+=5V, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Voltage Gain	$R_L \geq 15$ kΩ, V^+=15V V_O = 1V to 11V	50	200		50	200		25	100		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4V V_{RL}=5V, R_L=5.1 kΩ		300			300			300		ns
Response Time	V_{RL}=5V, R_L=5.1 kΩ (Note 7)		1.3			1.3			1.5		μs
Output Sink Current	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $V_O \leq 1.5$V	6.0	16		6.0	16		6.0	16		mA
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK} \leq 4$ mA		250	400		250	400		250	400	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN}(+)$=1V, V_O=5V		0.1			0.1			0.1		nA

Electrical Characteristics

(V+ = 5V) (Note 4)

Parameter	Conditions	LM193A			Units
		Min	Typ	Max	
Input Offset Voltage	(Note 9)			4.0	mV
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, V_{CM}=0V			100	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, V_{CM}=0V (Note 5)			300	nA
Input Common Mode Voltage Range	V^+=30V (Note 6)	0		V^+–2.0	V
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK} \leq 4$ mA			700	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN(+)}$=1V, V_O=30V			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s ≥0V (or V^-, if Used), (Note 8)			36	V

Electrical Characteristics

(V+ = 5V) (Note 4)

Parameter	Conditions	LM193			LM293, LM393			LM2903			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			9			9		9	15	mV
Input Offset Current	$I_{IN(+)}-I_{IN(-)}$, V_{CM}=0V			100			150		50	200	nA
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range, V_{CM}=0V (Note 5)			300			400		200	500	nA
Input Common Mode Voltage Range	V^+=30V (Note 6)	0		V^+–2.0	0		V^+–2.0	0		V^+–2.0	V
Saturation Voltage	$V_{IN}(-)$=1V, $V_{IN}(+)$=0, $I_{SINK} \leq 4$ mA			700			700		400	700	mV
Output Leakage Current	$V_{IN}(-)$=0, $V_{IN(+)}$=1V, V_O=30V			1.0			1.0			1.0	μA
Differential Input Voltage	Keep All V_{IN}'s ≥0V (or V^-, if Used), (Note 8)			36			36			36	V

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V.

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM193/LM193A. With the LM293/LM293A all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$ and the LM393/LM393A temperature specifications are limited to $0°C \leq T_A \leq +70°C$. The LM2903 is limited to $-40°C \leq T_A \leq +85°C$.

Electrical Characteristics (Continued)

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+–1.5V at 25˚C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used).

Note 9: At output switch point, $V_O \cong 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+–1.5V), at 25˚C.

Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

National Semiconductor

LM392
Low Power Operational Amplifier/Voltage Comparator

General Description

The LM392 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM392 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM358 dual op amp and the LM393 dual comparator

Features

- Wide power supply voltage range
  Single supply: 3V to 32V
  Dual supply: ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage: 600 µA
- Low input biasing current: 50 nA
- Low input offset voltage: 2 mV
- Low input offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

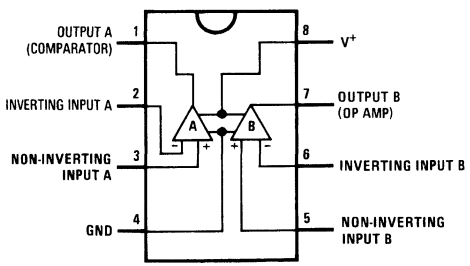
- Internally frequency compensated for unity gain
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1 MHz
- Large output voltage swing: 0V to V^+ − 1.5V

ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage: 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Connection Diagram

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)
Dual-In-Line Package



(Top View)
Order Number LM392M or LM392MX
See NS Package Number M08A
Order Number LM392N
See NS Package Number N08E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM392
Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (Note 2)	
Molded DIP (LM392N)	820 mW
Small Outline Package (LM392M)	530 mW
Output Short-Circuit to Ground (Note 3)	Continuous
Input Current (V_{IN} < −0.3 V_{DC}) (Note 4)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD rating to be determined.	
Soldering Information	
Dual-in-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

(V^+ = 5 V_{DC}; specifications apply to both amplifiers unless otherwise stated) (Note 5)

Parameter	Conditions	LM392			Units
		Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, (Note 6)		±2	±5	mV
Input Bias Current	IN(+) or IN(−), T_A =25°C, (Note 7) , V_{CM} = 0V		50	250	nA
Input Offset Current	IN(+) − IN(−), T_A = 25°C		±5	±50	nA
Input Common-Mode Voltage Range	V^+ = 30 V_{DC}, T_A = 25°C, (Note 8)	0		V^+−1.5	V
Supply Current	R_L = ∞ , V^+= 30 V		1	2	mA
Supply Current	R_L = ∞ , V^+= 5 V		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, T_A = 25°C, Input Referred, (Note 9)		−100		dB
Input Offset Voltage	(Note 6)			±7	mV
Input Bias Current	IN(+) or IN(−)			400	nA
Input Offset Current	IN(+) − IN(−)			150	nA
Input Common-Mode Voltage Range	V^+ = 30 V_{DC}, (Note 8)	0		V^+−2	V
Differential Input Voltage	Keep All V_{IN}'s≥ 0 V_{DC} (or V^-, if used) (Note 10)			32	V

Electrical Characteristics (Continued)

(V^+ = 5 V_{DC}; specifications apply to both amplifiers unless otherwise stated) (Note 5)

Parameter	Conditions	LM392			Units
		Min	Typ	Max	
OP AMP ONLY					
Large Signal Voltage Gain	V^+ = 15 V_{DC}, V_o swing = 1 V_{DC} to 11 V_{DC}, R_L = 2 kΩ, T_A = 25°C	25	100		V/mV
Output Voltage Swing	R_L = 2 kΩ, T_A = 25°C	0		V^+−1.5	V
Common-Mode Rejection Ratio	DC, T_A = 25°C, V_{CM}= 0, V_{DC} to V^+−1.5 V_{DC}	65	70		dB
Power Supply Rejection Ratio	DC, T_A = 25°C	65	100		dB
Output Current Source	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(-)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o = 2 V_{DC}, T_A = 25°C	20	40		mA
Output Current Sink	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o =2V_{DC}, T_A = 25°C	10	20		mA
	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o =200 mV, T_A = 25°C	12	50		µA
Input Offset Voltage Drift	R_S = 0Ω		7		µV/°C
Input Offset Current Drift	R_S = 0Ω		10		pA_{DC}/°C
COMPARATOR ONLY					
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC}, T_A = 25°C	50	200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC} V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		1.3		µs
Output Sink Current	$V_{IN(-)}$ =1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V_O ≥1.5 V_{DC}, T_A = 25°C	6	16		mA
Saturation Voltage	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400	mV
	$V_{IN(-)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA			700	mV
Output Leakage Current	$V_{IN(-)}$ = 0, $V_{IN(+)}$ ≥ 1 V_{DC}, V_o = 5 V_{DC}, T_A = 25°C		0.1		nA
	$V_{IN(-)}$ = 0, $V_{IN(+)}$ ≥ 1 V_{DC}, V_o = 30 V_{DC}			1.0	µA

Note 1: "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For operating at temperatures above 25°C, the LM392 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Note 5: These specifications apply for V^+ = 5V, unless otherwise stated. For the LM392, temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.

Note 6: At output switch point, V_O ≅ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V).

Note 7: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 8: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to 32V without damage.

Note 9: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

Note 10: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 11: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

National Semiconductor

LM397
Single General Purpose Voltage Comparator

General Description

The LM397 is a single voltage comparator with an input common mode that includes ground. The LM397 is designed to operate from a single 5V to 30V power supply or a split power supply. Its low supply current is virtually independent of the magnitude of the supply voltage.

The LM397 features an open collector output stage. This allows the connection of an external resistor at the output. The output can directly interface with TTL, CMOS and other logic levels, by tying the resistor to different voltage levels (level translator).

The LM397 is available in space saving SOT23-5 package and pin compatible to TI's TL331, single differential comparator.

Features

(T_A = 25°C. Typical values unless otherwise specified).

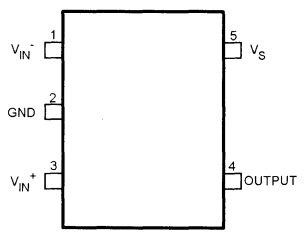
- SOT23-5 package
- Industrial operating range −40°C to +85°C
- Single or dual power supplies
- Wide supply voltage range 5V to 30V
- Low supply current 300µA
- Low input bias current 7nA
- Low input offset current ±1nA
- Low input offset voltage ±2mV
- Response time 440ns (50mV overdrive)
- Input common mode voltage 0 to V_S - 1.5V

Applications

- A/D converters
- Pulse, square wave generators
- Peak detector
- Industrial applications

Connection Diagram

SOT23-5



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Top View

Typical Circuit

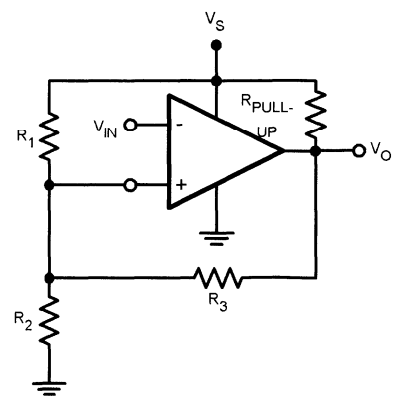

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FIGURE 1. Inverting Comparator with Hysteresis

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SOT-23	LM397MF	C397	1k Units Tape and Reel	MF05A
	LM397MFX		3k Units Tape and Reel	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	
Human Body Model	2KV (Note 2)
Machine Model	200V (Note 3)
V_{IN} Differential	30V
Supply Voltages	30V or ±15V
Voltage at Input Pins	−0.3V to 30V
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C

Operating Ratings (Note 1)

Supply Voltage, V_S	5V to 30V
Junction Temperature Range (Note 4)	−40°C to +85°C
Package Thermal Resistance (Note 4)	
SOT23-5	168°C/W

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V_S = 5V. **Boldface** limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
V_{OS}	Input Offset Voltage	V_S = 5V to 30V, V_O = 1.4V, V_{CM} = 0V		2	7 **10**	mV
I_{OS}	Input Offset Current	V_O = 1.4V, V_{CM} = 0V		1.6	50 **250**	nA
I_B	Input Bias Current	V_O = 1.4V, V_{CM} = 0V		10	250 **400**	nA
I_S	Supply Current	R_L = Open, V_S = 5V		0.25	0.7	mA
		R_L = Open, V_S = 30V		0.30	2	
I_O	Output Sink Current	V_{IN^+} = 1V, V_{IN^-} = 0V, V_O = 1.5V	6	13		mA
$I_{LEAKAGE}$	Output Leakage Current	V_{IN^+} = 1V, V_{IN^-} = 0V, V_O = 5V		0.1		nA
		V_{IN^+} = 1V, V_{IN^-} = 0V, V_O = 30V		1		µA
V_{OL}	Output Voltage Low	I_O = −4mA, V_{IN^+} = 0V, V_{IN^-} = 1V		180	400 **700**	mV
V_{CM}	Common-Mode Input Voltage Range	V_S = 5V to 30V (Note 7)	V_S - 1.5V **V_S - 2V**		0 **0**	V

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for at T_J = 25°C, V_S = 5V. **Boldface** limits apply at temperature extremes. (Continued)

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
A_V	Voltage Gain	V_S = 15V, V_O = 1.4V to 11.4V, R_L > = 15kΩ connected to V_S		120		V/mV
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 5mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		900		ns
		Input Overdrive = 50mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		250		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 5mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		940		µs
		Input Overdrive = 50mV, R_L = 5.1kΩ connected to 5V, C_L = 15pF		440		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: Machine model, 0Ω in series with 200pF.

Note 4: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: The input common-mode voltage of either input should not be permitted to go below the negative rail by more than 0.3V. The upper end of the common-mode voltage range is V_S - 1.5V at 25°C.

National Semiconductor

LM613
Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

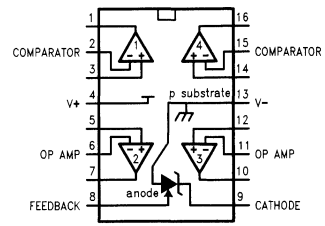
- Low operating current (Op Amp): 300 μA
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+ − 1.8V)
- Wide differential input voltage: ±36V
- Available in plastic package rated for Military Temp. Range Operation

REFERENCE

- Adjustable output voltage: 1.2V to 6.3V
- Tight initial tolerance available: ±0.6%
- Wide operating current range: 17 μA to 20 mA
- Tolerant of load capacitance

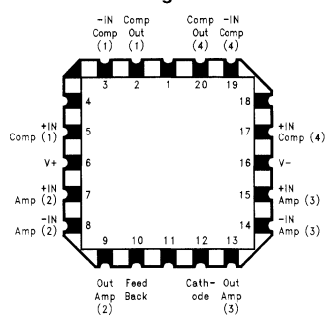
Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

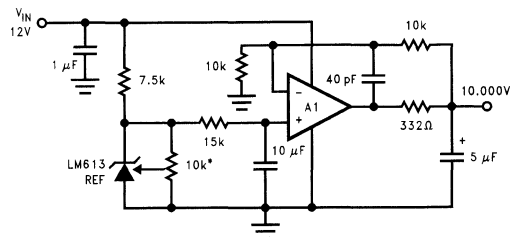


Top View

E Package Pinout



Ultra Low Noise, 10.00V Reference.
Total output noise is typically 14 μV_{RMS}.



*10k must be low t.c. trimpot

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^-pin)	
(Note 2)	36V (Max)
(Note 3)	−0.3V (Min)
Current through Any Input Pin & V_R Pin	±20 mA
Differential Input Voltage	
Military and Industrial	±36V
Commercial	±32V
Storage Temperature Range	$-65°C \le T_J \le +150°C$
Maximum Junction Temp.(Note 4)	150°C
Thermal Resistance, Junction-to-Ambient (Note 5)	
N Package	100°C/W
WM Package	150°C/W
Soldering Information (10 Sec.)	
N Package	260°C
WM Package	220°C
ESD Tolerance (Note 6)	±1 kV

Operating Temperature Range

LM613AI, LM613BI:	$-40°C$ to $+85°C$
LM613AM, LM613M:	$-55°C$ to $+125°C$
LM613C:	$0°C \le T_J \le +70°C$

Electrical Characteristics

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
I_S	Total Supply Current	$R_{LOAD} = \infty$,	450	940	1000	µA (Max)
		$4V \le V^+ \le 36V$ (32V for LM613C)	**550**	**1000**	**1070**	µA (Max)
V_S	Supply Voltage Range		2.2	2.8	2.8	V (Min)
			2.9	**3**	**3**	V (Min)
			46	36	32	V (Max)
			43	**36**	**32**	V (Max)
OPERATIONAL AMPLIFIERS						
V_{OS1}	V_{OS} Over Supply	$4V \le V^+ \le 36V$	1.5	3.5	5.0	mV (Max)
		($4V \le V^+ \le 32V$ for LM613C)	**2.0**	**6.0**	**7.0**	mV (Max)
V_{OS2}	V_{OS} Over V_{CM}	V_{CM} = 0V through V_{CM} =	1.0	3.5	5.0	mV (Max)
		($V^+ - 1.8V$), V^+ = 30V, V^- = 0V	**1.5**	**6.0**	**7.0**	mV (Max)
$\frac{V_{OS3}}{\Delta T}$	Average V_{OS} Drift	(Note 8)	**15**			µV/°C (Max)
I_B	Input Bias Current		10	25	35	nA (Max)
			11	**30**	**40**	nA (Max)
I_{OS}	Input Offset Current		0.2	4	4	nA (Max)
			0.3	**5**	**5**	nA (Max)
$\frac{I_{OS1}}{\Delta T}$	Average Offset Current		**4**			pA/°C
R_{IN}	Input Resistance	Differential	1000			MΩ
C_{IN}	Input Capacitance	Common-Mode	6			pF
e_n	Voltage Noise	f = 100 Hz, Input Referred	74			$nV/\sqrt{Hz}$
I_n	Current Noise	f = 100 Hz, Input Referred	58			$fA/\sqrt{Hz}$
CMRR	Common-Mode	V^+ = 30V, $0V \le V_{CM} \le (V^+ - 1.8V)$	95	80	75	dB (Min)
	Rejection Ratio	$CMRR = 20 \log (\Delta V_{CM}/\Delta V_{OS})$	**90**	**75**	**70**	dB (Min)

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, V_{CM} = V_{OUT} = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
OPERATIONAL AMPLIFIERS						
PSRR	Power Supply Rejection Ratio	4V ≤ V^+ ≤ 30V, V_{CM} = V^+/2, PSRR = 20 log ($\Delta V^+/V_{OS}$)	110 **100**	80 **75**	75 **70**	dB (Min) dB (Min)
A_V	Open Loop Voltage Gain	R_L = 10 kΩ to GND, V^+ = 30V, 5V ≤ V_{OUT} ≤ 25V	500 **50**	100 **40**	94 **40**	V/mV (Min)
SR	Slew Rate	V^+ = 30V (Note 9)	0.70 **0.65**	0.55 **0.45**	0.50 **0.45**	V/µs
GBW	Gain Bandwidth	C_L = 50 pF	0.8 **0.5**			MHz MHz
V_{O1}	Output Voltage Swing High	R_L = 10 kΩ to GND, V^+ = 36V (32V for LM613C)	V^+ − 1.4 **V^+ − 1.6**	V^+ − 1.7 **V^+ − 1.9**	V^+ − 1.8 **V^+ − 1.9**	V (Min) V (Min)
V_{O2}	Output Voltage Swing Low	R_L = 10 kΩ to V^+, V^+ = 36V (32V for LM613C)	V^- + 0.8 **V^- + 0.9**	V^- + 0.9 **V^- + 1.0**	V^- + 0.95 **V^- + 1.0**	V (Max) V (Max)
I_{OUT}	Output Source Current	V_{OUT} = 2.5V, V^+_{IN} = 0V, V^-_{IN} = −0.3V	25 **15**	20 **13**	16 **13**	mA (Min) mA (Min)
I_{SINK}	Output Sink Current	V_{OUT} = 1.6V, V^+_{IN} = 0V, V^-_{IN} = 0.3V	17 **9**	14 **8**	13 **8**	mA (Min) mA (Min)
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V, V^+_{IN} = 3V, V^-_{IN} = 2V	30 **40**	50 **60**	50 **60**	mA (Max) mA (Max)
		V_{OUT} = 5V, V^+_{IN} = 2V, V^-_{IN} = 3V	30 **32**	60 **80**	70 **90**	mA (Max) mA (Max)
COMPARATORS						
V_{OS}	Offset Voltage	4V ≤ V^+ ≤ 36V (32V for LM613C), R_L = 15 kΩ	1.0 **2.0**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{V_{CM}}$	Offset Voltage over V_{CM}	0V ≤ V_{CM} ≤ 36V V^+ = 36V, (32V for LM613C)	1.0 **1.5**	3.0 **6.0**	5.0 **7.0**	mV (Max) mV (Max)
$\frac{V_{OS}}{\Delta T}$	Average Offset Voltage Drift		**15**			µV/°C (Max)
I_B	Input Bias Current		5 **8**	25 **30**	35 **40**	nA (Max) nA (Max)
I_{OS}	Input Offset Current		0.2 **0.3**	4 **5**	4 **5**	nA (Max) nA (Max)
A_V	Voltage Gain	R_L = 10 kΩ to 36V (32V for LM613C) 2V ≤ V_{OUT} ≤ 27V	500 **100**			V/mV V/mV
t_r	Large Signal Response Time	V^+_{IN} = 1.4V, V^-_{IN} = TTL Swing, R_L = 5.1 kΩ	1.5 **2.0**			µs µs
I_{SINK}	Output Sink Current	V^+_{IN} = 0V, V^-_{IN} = 1V, V_{OUT} = 1.5V	20 **13**	10 **8**	10 **8**	mA (Min) mA (Min)
		V_{OUT} = 0.4V	2.8 **2.4**	1.0 **0.5**	0.8 **0.5**	mA (Min) mA (Min)

Electrical Characteristics (Continued)

These specifications apply for V^- = GND = 0V, V^+ = 5V, $V_{CM} = V_{OUT}$ = 2.5V, I_R = 100 µA, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for T_J = 25°C; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (Note 7)	LM613AM LM613AI Limits (Note 8)	LM613M LM613I LM613C Limits (Note 8)	Units
COMPARATORS						
I_{LEAK}	Output Leakage Current	V^+_{IN} = 1V, V^-_{IN} = 0V, V_{OUT} = 36V (32V for LM613C)	0.1 **0.2**	10	10	µA (Max) µA (Max)
VOLTAGE REFERENCE						
V_R	Voltage Reference	(Note 10)	1.244	1.2365 1.2515 (±0.6%)	1.2191 1.2689 (±2%)	V (Min) V (Max)
$\frac{\Delta V_R}{\Delta T}$	Average Temp. Drift	(Note 11)	**10**	**80**	**150**	ppm/°C (Max)
$\frac{\Delta V_R}{\Delta T_J}$	Hysteresis	(Note 12)	**3.2**			µV/°C
$\frac{\Delta V_R}{\Delta I_R}$	V_R Change with Current	$V_{R(100\ \mu A)} - V_{R(17\ \mu A)}$	0.05 **0.1**	1 **1.1**	1 **1.1**	mV (Max) mV (Max)
		$V_{R(10\ mA)} - V_{R(100\ \mu A)}$ (Note 13)	1.5 **2.0**	5 **5.5**	5 **5.5**	mV (Max) mV (Max)
R	Resistance	$\Delta V_{R(10 \rightarrow 0.1\ mA)}$/9.9 mA $\Delta V_{R(100 \rightarrow 17\ \mu A)}$/83 µA	**0.2** **0.6**	**0.56** **13**	**0.56** **13**	Ω (Max) Ω (Max)
$\frac{V_R}{\Delta V_{RO}}$	V_R Change with High V_{RO}	$V_{R(Vro\ =\ Vr)} - V_{R(Vro\ =\ 6.3V)}$ (5.06V between Anode and FEEDBACK)	2.5 **2.8**	7 **10**	7 **10**	mV (Max) mV (Max)
$\frac{V_R}{\Delta V^+}$	V_R Change with V_{ANODE} Change	$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 36V)}$ (V^+ = 32V for LM613C)	0.1 **0.1**	1.2 **1.3**	1.2 **1.3**	mV (Max) mV (Max)
		$V_{R(V+\ =\ 5V)} - V_{R(V+\ =\ 3V)}$	0.01 **0.01**	1 **1.5**	1 **1.5**	mV (Max) mV (Max)
I_{FB}	FEEDBACK Bias Current	$V_{ANODE} \leq V_{FB} \leq 5.06V$	22 **29**	35 **40**	50 **55**	nA (Max) nA (Max)
e_n	V_R Noise	10 Hz to 10 kHz, $V_{RO} = V_R$	30			μV_{RMS}

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^-, a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is 90°C/W for the N package, and 135°C/W for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 7: Typical values in standard typeface are for T_J = 25°C; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes **(bold type face)**.

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

Electrical Characteristics (Continued)

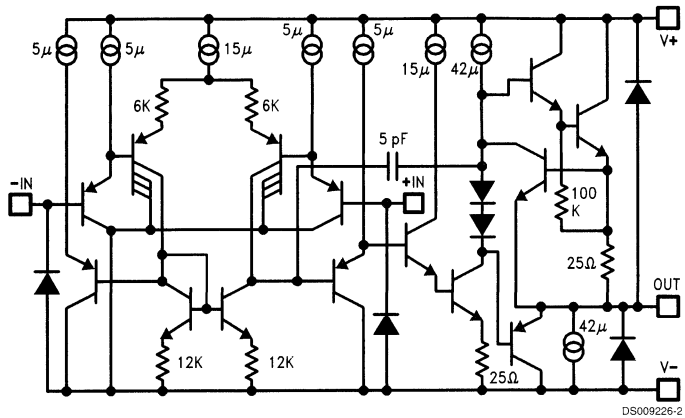
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \cdot \Delta V_R / (V_{R[25°C]} \cdot \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_{R[25°C]}$ is the value at 25°C, and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 12: Hysteresis is the change in V_R caused by a change in T_J, after the reference has been "dehysterized". To dehysterize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C: 25°C, 85°C, −40°C, 70°C, 0°C, 25°C.

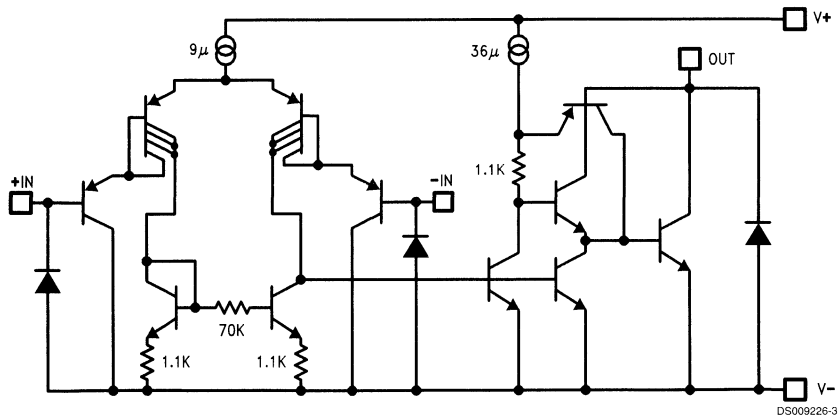
Note 13: Low contact resistance is required for accurate measurement.

Simplified Schematic Diagrams

Op Amp

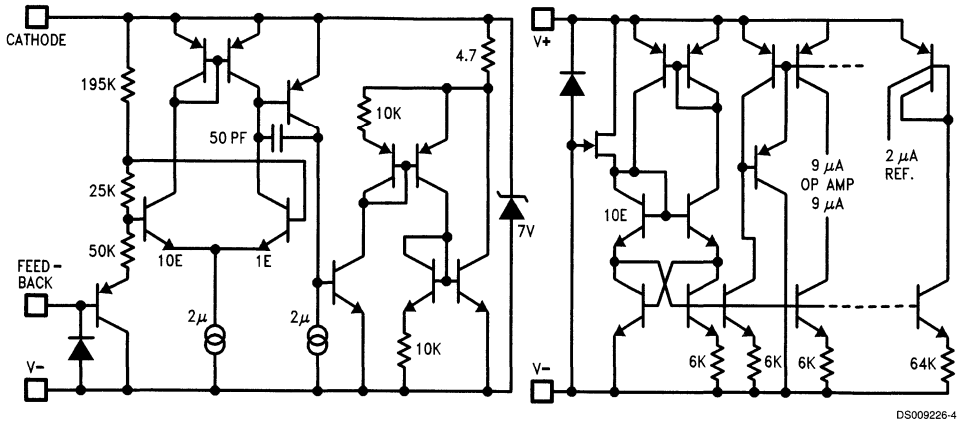


Comparator



Simplified Schematic Diagrams (Continued)

Reference/Bias



DS009226-4

National Semiconductor

LM6511
180 ns 3V Comparator

General Description

The LM6511 voltage comparator is ideal for analog-digital interface circuitry when only a +3V or +3.3V supply is available. The open-collector output permits signal compatibility with a wide variety of digital families: +5V CMOS, +3V CMOS, TTL and so on. Supply voltage may range from 2.7V to 36V between supply voltage leads. The LM6511 operates with little power consumption (P_{diss} < 9.45 mW at V^+ = +2.7V and V^- = 0V).

This voltage comparator offers many features that are available in traditional sub-microsecond comparators: output sync strobe, inputs and output may be isolated from system ground, and wire-ORing. Also, the LM6511 uses the industry-standard, single comparator pinout configuration.

Features

(Typical unless otherwise noted)

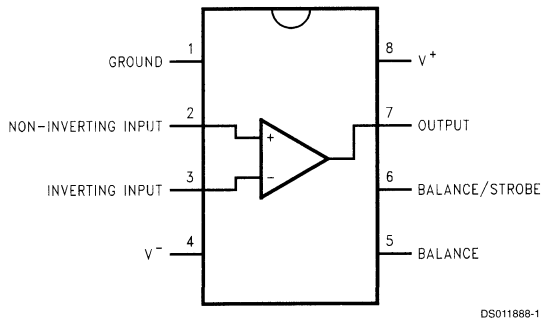
- Operates at +2.7V, +3V, +3.3V, +5V
- Low Power consumption <9.45 mW @ V^+ = 2.7V (max)
- Fast Response Time of 180 ns

Applications

- Portable Equipment
- Cellular Phones
- Digital Level Shifting

Connection Diagram

8-Pin SO



DS011888-1

Ordering Information

Package	Industrial Temperature Range −40°C to +85°C	NSC Package Drawing
8-Pin Small Outline	LM6511IM, LM6511IMX	M08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	−0.3 to +36V
Output to Negative Supply Voltage	50V
Ground to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Input Voltage	(Note 2)
Storage Temperature Range	−65°C to +150°C
Soldering Information:	
SO Package (Vapor Phase in 60 sec)	215°C
SO Package (Infrared in 15 sec)	220°C
Power Dissipation	500 mW
Output Short Circuit Duration	10s
Junction Temperature	150°C
ESD Rating (C = +100 pF, R = 1.5 kΩ)	300V

Operating Ratings (Note 1)

Supply Voltage	2.5V to 30V
Temperature Range	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
SO Package	170°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I Limit	Units (Limits)
V_{OS}	Offset Voltage	$R_S \le 50$ kΩ	1.5	5	mV
		(Note 3)		**8**	max
I_B	Input Bias Current		38	130	
				200	nA
I_{OS}	Input Offset Current	$R_S \le 50$ kΩ	1.5	20	max
		(Note 3)		**50**	
I_S	Positive Supply Current		2.7	3.5	
				5	mA
	Negative Supply Current		1.5	2.0	max
				2.5	
V_{SAT}	Saturation Voltage	$V_{IN} \le 10$ mV	0.23	0.4	V
		I_{SINK} = 8 mA		**0.4**	max
A_V	Large Signal Voltage Gain	ΔV_{OUT} = 2V	40		V/mV
CMRR	Common Mode Rejection Ratio		72		dB
I_{STROBE}	Strobe ON Current	(Note 5)	2.0	5.0	mA max
V_{IN}	Input Voltage Range			0.50	V min
				$V^+ - 1.25$	V max
	Output Leakage Current	$V_{IN} \ge 10$ mV, V_{OUT} = 35V,	0.2		nA
		I_{STROBE} = 3 mA			max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I Limit	Units (Limits)
T_R	Response Time	(Note 4)	180		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: The positive input voltage limit is 30V above the negative supply voltage. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply voltage, whichever is less.

Note 3: The offset voltage and offset current limits are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Therefore, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 4: This specification is for a 100 mV input step with a 25 mV overdrive.

Note 5: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 mA to 5 mA.

National Semiconductor

LMC6762
Dual MicroPower Rail-To-Rail Input CMOS Comparator with Push-Pull Output

General Description

The LMC6762 is an ultra low power dual comparator with a maximum supply current of 10 µA/comparator. It is designed to operate over a wide range of supply voltages, from 2.7V to 15V. The LMC6762 has guaranteed specs at 2.7V to meet the demands of 3V digital systems.

The LMC6762 has an input common-mode voltage range which exceeds both supplies. This is a significant advantage in low-voltage applications. The LMC6762 also features a push-pull output that allows direct connections to logic devices without a pull-up resistor.

A quiescent power consumption of 50 µW/amplifier (@ V^+ = 5V) makes the LMC6762 ideal for applications in portable phones and hand-held electronics. The ultra-low supply current is also independent of power supply voltage. Guaranteed operation at 2.7V and a rail-to-rail performance makes this device ideal for battery-powered applications.

Refer to the LMC6772 datasheet for an open-drain version of this device.

Features

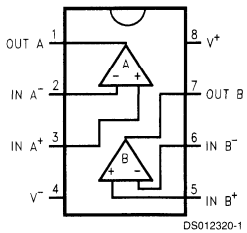
(Typical unless otherwise noted)

- Low power consumption (max): I_S = 10 µA/comp
- Wide range of supply voltages: 2.7V to 15V
- Rail-to-rail input common mode voltage range
- Rail-to-rail output swing (Within 100 mV of the supplies, @ V^+ = 2.7V, and I_{LOAD} = 2.5 mA)
- Short circuit protection: 40 mA
- Propagation delay (@ V^+ = 5V, 100 mV overdrive): 4 µs

Applications

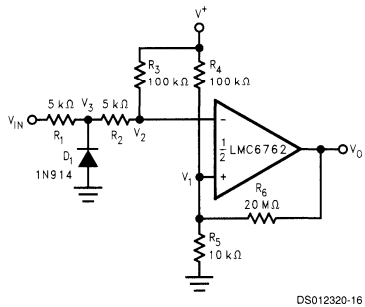
- Laptop computers
- Mobile phones
- Metering systems
- Hand-held electronics
- RC timers
- Alarm and monitoring circuits
- Window comparators, multivibrators

Connection Diagram
8-Pin DIP/SO



Top View

Typical Application



Zero Crossing Detector

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 KV
Differential Input Voltage	$(V^+)+0.3V$ to $(V^-)-0.3V$
Voltage at Input/Output Pin	$(V^+)+0.3V$ to $(V^-)-0.3V$
Supply Voltage (V^+-V^-)	16V
Current at Input Pin	±5 mA
Current at Output Pin (Notes 7, 3)	±30 mA
Current at Power Supply Pin, LMC6762	40 mA
Lead Temperature (Soldering, 10 seconds)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7 \le V_S \le 15V$
Junction Temperature Range	
LMC6762AI, LMC6762BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	100°C/W
M Package, 8-Pin Surface Mount	172°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6762AI Limit (Note 6)	LMC6762BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		2.0			µV/°C
	Input Offset Voltage Average Drift	(Note 8)	3.3			µV/Month
I_B	Input Current		0.02			pA
I_{OS}	Input Offset Current		0.01			pA
CMRR	Common Mode Rejection Ratio		75			dB
PSRR	Power Supply Rejection Ratio	$\pm1.35V < V_S < \pm7.5V$	80			dB
A_V	Voltage Gain	(By Design)	100			dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	I_{LOAD} = 2.5 mA	2.5	2.4 **2.3**	2.4 **2.3**	V min
V_{OL}	Output Voltage Low	I_{LOAD} = 2.5 mA	0.2	0.3 **0.4**	0.3 **0.4**	V max
I_S	Supply Current	For Both Comparators (Output Low)	12	20 **25**	20 **25**	µA max

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15.0V, V^- = 0V, V_{CM} = $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6762AI Limit (Note 6)	LMC6762BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift	V^+ = 5V	2.0			µV/°C
		V^+ = 15V	4.0			
	Input Offset Voltage Average Drift	V^+ = 5V (Note 8)	3.3			µV/Month
		V^+ = 15V (Note 8)	4.0			
I_B	Input Current	V = 5V	0.04			pA
I_{OS}	Input Offset Current	V^+ = 5V	0.02			pA
CMRR	Common Mode Rejection Ratio	V^+ = 5V	75			dB
		V^+ = 15V	82			dB
PSRR	Power Supply Rejection Ratio	±2.5V < V_S < ±5V	80			dB
A_V	Voltage Gain	(By Design)	100			dB
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5.0V CMRR > 55 dB	5.3	5.2 **5.0**	5.2 **5.0**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
		V^+ = 15.0V CMRR > 55 dB	15.3	15.2 **15.0**	15.2 **15.0**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	V^+ = 5V I_{LOAD} = 5mA	4.8	4.6 **4.45**	4.6 **4.45**	V min
		V^+ = 15V I_{LOAD} = 5 mA	14.8	14.6 **14.45**	14.6 **14.45**	V min
V_{OL}	Output Voltage Low	V^+ = 5V I_{LOAD} = 5 mA	0.2	0.4 **0.55**	0.4 **0.55**	V max
		V^+ = 15V I_{LOAD} = 5 mA	0.2	0.4 **0.55**	0.4 **0.55**	V max
I_S	Supply Current	For Both Comparators (Output Low)	12	20 **25**	20 **25**	µA max
I_{SC}	Short Circuit Current	Sourcing	30			mA
		Sinking, V_O = 12V (Note 7)	45			

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6762AI Limit (Note 6)	LMC6762BI Limit (Note 6)	Units
t_{RISE}	Rise Time	f = 10 kHz, C_L = 50 pF, Overdrive = 10 mV (Notes 9, 10)		0.3			µs
t_{FALL}	Fall Time	f = 10 kHz, C_L = 50 pF, Overdrive = 10 mV (Notes 9, 10)		0.3			µs
t_{PHL}	Propagation Delay (High to Low)	f = 10 kHz, C_L = 50 pF (Notes 9, 10)	Overdrive = 10 mV	10			µs
			Overdrive = 100 mV	4			µs
		V^+ = 2.7V, f = 10 kHz, C_L = 50 pF (Notes 9, 10)	Overdrive = 10 mV	10			µs
			Overdrive = 100 mV	4			µs
t_{PLH}	Propagation Delay (Low to High)	f = 10 kHz, C_L = 50 pF (Notes 9, 10)	Overdrive = 10 mV	6			µs
			Overdrive = 100 mV	4			µs
		V^+ = 2.7V, f = 10 kHz, C_L = 50 pF (Notes 9, 10)	Overdrive = 10 mV	7			µs
			Overdrive = 100 mV	4			µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the electrical characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Do not short circuit output to V^+, when V^+ is greater than 12V or reliability will be adversely affected.

Note 8: Input Offset Voltage Average Drift is calculated by dividing the accelerated operating life drift average by the equivalent operational time. The Input Offset Voltage Average Drift represents the input offset voltage change at worst-case input conditions.

Note 9: C_L includes the probe and jig capacitance.

Note 10: The rise and fall times are measured with a 2V input step. The propagation delays are also measured with a 2V input step.

National Semiconductor

LMC6772
Dual Micropower Rail-To-Rail Input CMOS Comparator with Open Drain Output

General Description

The LMC6772 is an ultra low power dual comparator with a maximum 10 µA/comparator power supply current. It is designed to operate over a wide range of supply voltages, with a minimum supply voltage of 2.7V.

The common mode voltage range of the LMC6772 exceeds both the positive and negative supply rails, a significant advantage in single supply applications. The open drain output of the LMC6772 allows for wired-OR configurations. The open drain output also offers the advantage of allowing the output to be pulled to any voltage rail up to 15V, regardless of the supply voltage of the LMC6772.

The LMC6772 is targeted for systems where low power consumption is the critical parameter. Guaranteed operation at supply voltages of 2.7V and rail-to-rail performance makes this comparator ideal for battery-powered applications.

Refer to the LMC6762 datasheet for a push-pull output stage version of this device.

Features

(Typical unless otherwise noted)

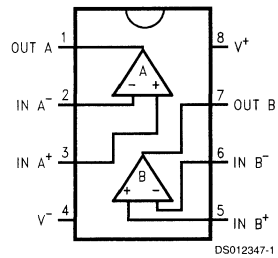
- Low power consumption (max): I_S = 10 µA/comp
- Wide range of supply voltages: 2.7V to 15V
- Rail-to-Rail Input Common Mode Voltage Range
- Open drain output
- Short circuit protection: 40 mA
- Propagation delay (@V_S = 5V, 100 mV overdrive): 5 µs

Applications

- Laptop computers
- Mobile phones
- Metering systems
- Hand-held electronics
- RC timers
- Alarm and monitoring circuits
- Window comparators, multivibrators

Connection Diagram

8-Pin DIP/SO/MSOP



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	1.5 kV
Differential Input Voltage	$(V^+)+0.3V$ to $(V^-)-0.3V$
Voltage at Input/Output Pin	$(V^+)+0.3V$ to $(V^-)-0.3V$
Supply Voltage (V^+-V^-)	16V
Current at Input Pin (Note 8)	±5 mA
Current at Output Pin (Notes 3, 7)	±30 mA
Current at Power Supply Pin, LMC6772	40 mA
Lead Temperature (Soldering, 10 seconds)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7 \le V_S \le 15V$
Junction Temperature Range	
LMC6772AI, LMC6772BI	$40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
N Package, 8-Pin Molded DIP	100°C/W
M Package, 8-Pin Surface Mount	172°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6772AI Limit (Note 6)	LMC6772BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		2.0			µV/°C
	Input Offset Voltage Average Drift	(Note 10)	3.3			µV/Month
I_B	Input Current		0.02			pA
I_{OS}	Input Offset Current		0.01			pA
CMRR	Common Mode Rejection Ratio		75			dB
PSRR	Power Supply Rejection Ratio	$\pm1.35V < V_S < \pm7.5V$	80			dB
A_V	Voltage Gain	(By Design)	100			dB
V_{CM}	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OL}	Output Voltage Low	I_{LOAD} = 2.5 mA	0.2	0.3 **0.4**	0.3 **0.4**	V max
I_S	Supply Current	For Both Comparators (Output Low)	12	20 **25**	20 **25**	µA max
$I_{Leakage}$	Output Leakage Current	$V_{IN}(+) = 0.5V$, $V_{IN}(-) = 0V$, $V_O = 15V$	0.1	500	500	nA

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15.0V, V^- = 0V, $V_{CM} = V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6772AI Limit (Note 6)	LMC6772BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max

5.0V and 15.0V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15.0V, V^- = 0V, V_{CM} = $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC6772AI Limit (Note 6)	LMC6772BI Limit (Note 6)	Units
TCV_{OS}	Input Offset Voltage Temperature Drift	V^+ = 5V	2.0			µV/°C
		V^+ = 15V	4.0			
	Input Offset Voltage Average Drift	V^+ = 5V (Note 10)	3.3			µV/Month
		V^+ = 15V (Note 10)	4.0			
I_B	Input Current	V = 5V	0.04			pA
I_{OS}	Input Offset Current	V^+ = 5V	0.02			pA
CMRR	Common Mode Rejection Ratio	V^+ = 5V	75			dB
		V^+ = 15V	82			dB
PSRR	Power Supply Rejection Ratio	±2.5V < V_S < ±5V	80			dB
A_V	Voltage Gain	(By Design)	100			dB
V_{CM}	Input Common-Mode Voltage Range	V^+ = 5.0V CMRR > 55 dB	5.3	5.2 **5.0**	5.2 **5.0**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
		V^+ = 15.0V CMRR > 55 dB	15.3	15.2 **15.0**	15.2 **15.0**	V min
			−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OL}	Output Voltage Low	V^+ = 5V I_{LOAD} = 5 mA	0.2	0.4 **0.55**	0.4 **0.55**	V max
		V^+ = 15V I_{LOAD} = 5 mA	0.2	0.4 **0.55**	0.4 **0.55**	V max
I_S	Supply Current	For Both Comparators (Output Low)	12	20 **25**	20 **25**	µA max
I_{SC}	Short Circuit Current	V^+ = 15V, Sinking, V_O = 12V (Note 7)	45			mA

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6772AI Limit (Note 6)	LMC6772BI Limit (Note 6)	Units
t_{RISE}	Rise Time	f = 10 kHz, C_L = 50 pF, Overdrive = 10 mV (Note 9)		0.3			µs
t_{FALL}	Fall Time	f = 10 kHz, C_L = 50 pF, Overdrive = 10 mV (Note 9)		0.3			µs
t_{PHL}	Propagation Delay (High to Low)	f = 10 kHz, C_L = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			µs
		V^+ = 2.7V, f = 10 kHz, C_L = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			µs

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, $V_{CM} = V_O = V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC6772AI Limit (Note 6)	LMC6772BI Limit (Note 6)	Units
t_{PLH}	Propagation Delay (Low to High)	f = 10 kHz, C_L = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			µs
		V^+ = 2.7V, f = 10 kHz, C_L = 50 pF (Note 9)	10 mV	8			µs
			100 mV	4			µs

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the electrical characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF. The output pins of the two comparators (pin 1 and pin 7) have an ESD tolerance of 1.5 kV. All other pins have an ESD tolerance of 2 kV.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Do not short circuit output to V^+, when V+ is > 12V or reliability will be adversely affected.

Note 8: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 9: C_L inlcudes the probe and jig capacitance. The rise time, fall time and propagation delays are measured with a 2V input step.

Note 10: Input offset voltage Average Drift is calculated by dividing the accelerated operating life drift average by the equivalent operational time. The input offset voltage average drift represents the input offset voltage change at worst-case input conditions.

National Semiconductor

LMC7211
Tiny CMOS Comparator with Rail-to-Rail Input and Push-Pull Output

General Description

The LMC7211 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes the comparator ideal for space and weight critical designs. The LMC7211 is supplied in two offset voltage grades, 5 mV and 15 mV.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the LMC7211 a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

The Tiny Comparator's outside dimensions (length x width x height) of 3.05mm x 3.00mm x 1.43mm allow it to fit into tight spaces on PC boards.

See the LMC7221 for a comparator with an open-drain output.

Features

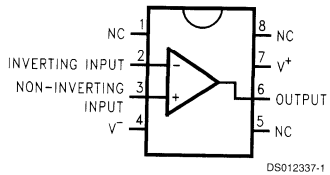
- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 7 µA at 5V
- Response time of 4 µs at 5V
- Push-pull output
- Input common-mode range beyond V− and V+
- Low input current

Applications

- Battery Powered Products
- Notebooks and PDAs
- PCMCIA cards
- Mobile Communications
- Alarm and Security circuits
- Direct Sensor Interface
- Replaces amplifiers used as comparators with better performance and lower current

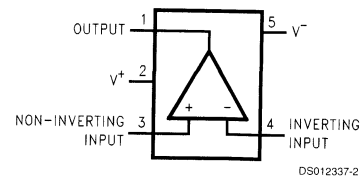
Connection Diagrams

8-Pin SO-8



Top View

5-Pin SOT23-5



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	(V_{CC}) +0.3V to $(-V_{CC})$−0.3V
Voltage at Input/Output Pin	(V_{CC}) + 0.3V to $(-V_{CC})$−0.3V
Supply Voltage (V^+–V^-)	16V
Current at Input Pin (Note 7)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7 \le V_{CC} \le 15V$
Junction Temperature Range LMC7211AI, LMC7211BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
SO-8 Package, 8-Pin Surface Mount	180°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		1.0			µV/°C
	Input Offset Voltage Average Drift	(Note 10)	3.3			µV/Month
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$	75			dB
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 15V$	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	V min
		CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OH}	Output Voltage High	I_{load} = 2.5 mA	2.5	2.4 **2.3**	2.4 **2.3**	V min
V_{OL}	Output Voltage Low	I_{load} = 2.5 mA	0.2	0.3 **0.4**	0.3 **0.4**	V max
I_S	Supply Current	V_{OUT} = Low	7	12 **14**	12 **14**	µA max

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5	15	mV
				8	**18**	max
TCV_{OS}	Input Offset Voltage	V^+ = 5V	1.0			µV/°C
	Temperature Drift	V^+ = 15V	4.0			
	Input Offset Voltage	V^+ = 5V	3.3			µV/Month
	Average Drift	V^+ = 15V	4.0			
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode	V+ = 5.0V	75			dB
	Rejection Ration	V+ = 15.0V	82			dB
PSRR	Power Supply Rejection Ratio	5V ≤ V^+ ≤ 10V	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	V+ = 5.0V	5.3	5.2	5.2	V
		CMRR > 55 dB		**5.0**	**5.0**	min
		V+ = 5.0V	−0.3	−0.2	−0.2	V
		CMRR > 55 dB		**0.0**	**0.0**	max
		V+ = 15.0V	15.3	15.2	15.2	V
		CMRR > 55 dB		**15.0**	**15.0**	min
		V+ = 15.0V	−0.3	−0.2	−0.2	V
		CMRR > 55 dB		**0.0**	**0.0**	max
V_{OH}	Output Voltage High	V+ = 5V	4.8	4.6	4.6	mV
		I_{load} = 5 mA		**4.45**	**4.45**	min
		V+ = 15V	14.8	14.6	14.6	mV
		I_{load} = 5 mA		**14.45**	**14.45**	min
V_{OL}	Output Voltage Low	V+ = 5V	0.2	0.40	0.40	mV
		I_{load} = 5 mA		**0.55**	**0.55**	max
		V+ = 15V	0.2	0.40	0.40	mV
		I_{load} = 5 mA		**0.55**	**0.55**	max
I_S	Supply Current	V_{OUT} = Low	7	14	14	µA
				18	**18**	max
I_{SC}	Short Circuit Current	Sourcing	30			mA
		Sinking (Note 8)	45			mA

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
t_{rise}	Rise Time	f = 10 kHz, Cl = 50 pF, Overdrive = 10 mV (Note 9)	0.3			µs
t_{fall}	Fall Time	f = 10 kHz, Cl = 50 pF, Overdrive = 10 mV (Note 9)	0.3			µs

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extreme.

Symbol	Parameter	Conditions		Typ (Note 5)	LMC7211AI Limit (Note 6)	LMC7211BI Limit (Note 6)	Units
t_{PHL}	Propagation Delay (High to Low) (Note 11)	f = 10 kHz, Cl = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, Cl = 50 pF (Note 9)	10 mV	10			µs
			100 mV	4			
t_{PLH}	Propagation Delay (Low to High) (Note 11)	f = 10 kHz, Cl = 50p (Note 9)	10 mV	6			µs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, Cl = 50 pF (Note 9)	10 mV	7			µs
			100 mV	4			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage rating.

Note 8: Do not short circuit output to V+, when V+ is greater than 12V or reliability will be adversely affected.

Note 9: C_L includes the probe and jig capacitance.

Note 10: Input offset voltage average drift is calculated by dividing the accelerated operating life V_{OS} drift by the equivalent operational time. This represents worst case input conditions and includes the first 30 days of drift.

Note 11: Input step voltage for propagation delay measurement is 2V.

National Semiconductor

LMS33460
3V Under Voltage Detector

General Description

The LMS33460 is an under voltage detector with a 3.0V threshold and extremely low power consumption. The LMS33460 is specifically designed to accurately monitor power supplies. It is especially suited to battery powered systems where low quiescent current and small size are required. This IC generates an active output whenever the input voltage drops below 3.0 Volts.

This part uses a precision on-chip voltage reference and a comparator to measure the input voltage. Built in hysteresis helps to prevent erratic operation in the presence of noise. The UVD is available in the ultra-miniature SC70-5 package.

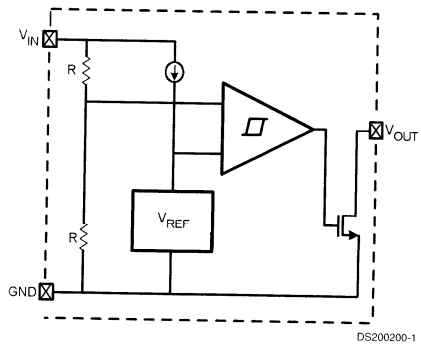
Features

- Ultra low Power
- 3.0V detection
- V_{IN} Range: 0.8V to 7.0V
- Open drain output
- Ultra-small SC70-5 package
- Extended Temperature range (−40˚C to 85˚C)
- Ultra Low Quiescent current (1µA typ)

Applications

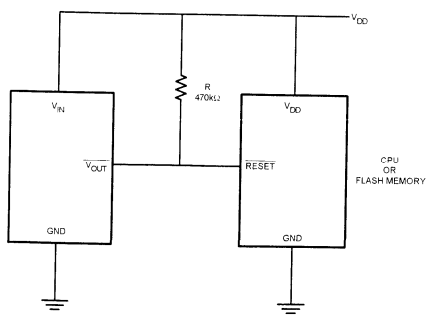
- Low battery voltage detector
- Power Fail Indicator
- Processor Reset Generator
- Battery Backup Control
- Battery Operated Equipment
- Hand-held Instruments

Circuit Block Diagram



DS200200-1

Typical Application



DS200200-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Input Voltage to GND	8.0V
Output Voltage to GND	8.0V
Output Continuous Output Current	30mA
Vapor Phase IR Convection Reflow	240°C
ESD Rating (Note 4)	
Human Body Model	2500V
Machine Model	200V
T_{JMAX} (Note 3)	150°C
θ_{JA} (Note 3)	478°C/W

Temperature Range

Operating Junction	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DET}	Detector Threshold	V_{IN} Falling	2.85	3.0	3.15	V
V_{HYS}	Detector Voltage Hysteresis	V_{IN} Rising	0.095	0.155	0.215	V
I_{IN}	Input Supply Current	V_{IN} = 2.87V	–	1.0	2.2	µA
		V_{IN} = 4.7V	–	1.2	3.6	µA
		V_{IN} = 7.0V (Note 3)	–	25	200	µA
$V_{IN(MAX)}$	Maximum Operating Voltage		–	–	7.0	V
$V_{IN(MIN)}$	Maximum Operating Voltage (Note 2)			0.7 **1.0**	1.1 **1.3**	V
$I_{OUT(LOW)}$	Output Current Low	V_{OUT} = 0.05V, V_{IN} = 1.1V V_{OUT} = 0.50V, V_{IN} = 1.5V	0.01 2	0.6 11		mA
T_{pdHL}	Output Delay Time Output Transition High to Low C_L = 10pF, R_L = 470kΩ		–	70	130	µsec
$\Delta V_{DET}/\Delta T$	Detect Voltage Temperature Coefficient		–	**±120**	–	PPM/°C

Note 1: Absolute maximum ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Temperature range specifications is guaranteed by design.

Note 3: Quiescent current will increase substantially above 5.5 volts, but is very low in the normal range below 5.5 volts.

Note 4: Human body model, 1.5kΩ in series with 100pF. Machine model, 0Ω in series with 200pF.

National Semiconductor

LMC7215/LMC7225
Micro-Power, Rail-to-Rail CMOS Comparators with Push-Pull/Open-Drain Outputs and TinyPak™ Package

General Description

The LMC7215/LMC7225 are ultra low power comparators with a maximum of 1 µA power supply current. They are designed to operate over a wide range of supply voltages, from 2V to 8V.

The LMC7215/LMC7225 have a greater than rail-to-rail common mode voltage range. This is a real advantage in single supply applications.

The LMC7215 features a push-pull output stage. This feature allows operation with absolute minimum amount of power consumption when driving any load.

The LMC7225 features an open drain output. By connecting an external resistor, the output of the comparator can be used as a level shifter to any desired voltage to as high as 15V.

The LMC7215/LMC7225 are designed for systems where low power consumption is the critical parameter.

Guaranteed operation over the full supply voltage range of 2.7V to 5V and rail-to-rail performance makes this comparator ideal for battery-powered applications.

Features

(Typical unless otherwise noted)

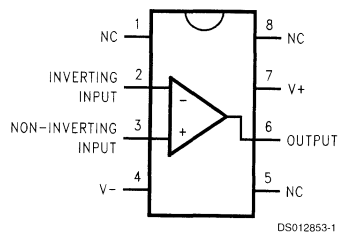
- Ultra low power consumption 0.7 µA
- Wide range of supply voltages 2V to 8V
- Input common-mode range beyond V+ and V−
- Open collector and push-pull output
- High output current drive: (@ V_S = 5V) 45 mA
- Propagation delay (@ V_S = 5V, 10 mV overdrive) 25 µs
- Tiny SOT23-5 package
- Latch-up resistance >300 mA

Applications

- Laptop computers
- Mobile phones
- Metering systems
- Hand-held electronics
- RC timers
- Alarm and monitoring circuits
- Window comparators, multivibrators

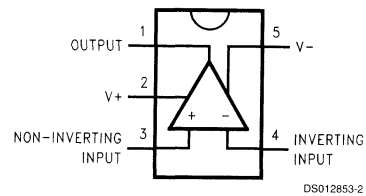
Connection Diagrams

8–Pin SO–8



Top View

5–Pin SOT23-5



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	$(V_{CC})+0.3V$ to $(-V_{CC})-0.3V$
Voltage at Input/Output Pin	$(V_{CC})+0.3V$ to $(-V_{CC})-0.3V$
Supply Voltage (V^+-V^-)	10V
Current at Input Pin	±5 mA
Current at Output Pin (Note 3)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (soldering, 10 sec)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2V \le V_{CC} \le 8V$
Junction Temperature Range	
LMC7215IM, LMC7225IM	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
M Package, 8-Pin Surface Mount	165°C/W
SOT23-5 Package	325°C/W

2.7V to 5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V to 5V, V^- = 0V, $V_{CM} = V_O = V+/2$. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7215 Limit (Note 6)	LMC7225 Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	6	6	mV
				8	**8**	max
TCV_{OS}	Input Offset Voltage Average Drift		2			µV/°C
I_B	Input Current		5			fA
I_{OS}	Input Offset Current		1			fA
CMRR	Common Mode Rejection Ratio	(Note 7)	80	60	60	dB
						min
PSRR	Power Supply Rejection Ratio	V^+ = 2.2V to 8V	90	60	60	dB
						min
A_V	Voltage Gain		140			dB
CMVR	Input Common-Mode Voltage Range	V^+ = 2.7V	3.0	2.9	2.9	V
		CMRR > 50 dB		**2.7**	**2.7**	min
		V^+ = 2.7V	−0.2	0.0	0.0	V
		CMRR > 50 dB		**0.2**	**0.2**	max
		V^+ = 5.0V	5.3	5.2	5.2	V
		CMRR > 50 dB		**5.0**	**5.0**	min
		V^+ = 5.0V	−0.3	−0.2	−0.2	V
		CMRR > 50 dB		**0.0**	**0.0**	max
V_{OH}	Output Voltage High	V^+ = 2.2V	2.05	1.8	NA	V
		I_{OH} = 1.5 mA		**1.7**		min
		V^+ = 2.7V	2.05	2.3	NA	V
		I_{OH} = 2.0 mA		**2.2**		min
		V^+ = 5.0V	4.8	4.6	NA	V
		I_{OH} = 4.0 mA		**4.5**		min
V_{OL}	Output Voltage Low	V^+ = 2.2V	0.17	0.4	0.4	V
		I_{OH} = 1.5 mA		**0.5**	**0.5**	max
		V^+ = 2.7V	0.17	0.4	0.4	V
		I_{OH} = 2.0 mA		**0.5**	**0.5**	max
		V^+ = 5.0V	0.2	0.4	0.4	V
		I_{OH} = 4.0 mA		**0.5**	**0.5**	max
I_{SC+}	Output Short Circuit Current (Note 10)	V^+ = 2.7V, Sourcing	15		NA	mA
		V^+ = 5.0V, Sourcing	50		NA	mA

2.7V to 5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V to 5V, V^- = 0V, V_{CM} = V_O = V+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7215 Limit (Note 6)	LMC7225 Limit (Note 6)	Units
I_{SC-}	Output Short Circuit Current (Note 10)	V^+ = 2.7V, Sinking	12			mA
		V^+ = 5.0V, Sinking	30			mA
$I_{Leakage}$	Output Leakage Current	V^+ = 2.2V $V_{IN}+$ = 0.1V, $V_{IN}-$ = 0V, V_{OUT} = 15V	0.01	NA	500	nA max
I_S	Supply Current	V^+ = 5.0V $V_{IN}+$ = 5V, $V_{IN}-$ = 0V	0.7	1 **1.2**	1 **1.2**	µA max

AC Electrical Characteristics

Unless otherwise specified, T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = $V^+/2$

Symbol	Parameter	Conditions		LMC7215 Typ (Note 5)	LMC7225 Typ (Notes 5, 8)	Units
t_{rise}	Rise Time	Overdrive = 10 mV (Note 8)		1	12.2	µs
t_{fall}	Fall Time	Overdrive = 10 mV (Note 8)		0.4	0.35	µs
t_{PHL}	Propagation Delay (High to Low)	(Notes 8, 9)	Overdrive = 10 mV	24	24	µs
			Overdrive = 100 mV	12	12	
		V^+ = 2.7V (Notes 8, 9)	Overdrive = 10 mV	17	17	µs
			Overdrive = 100 mV	11	11	
t_{PLH}	Propagation Delay (Low to High)	(Notes 8, 9)	Overdrive = 10 mV	24	29	µs
			Overdrive = 100 mV	12	17	
		V^+ = 2.7V (Notes 8, 9)	Overdrive = 10 mV	17	22	µs
			Overdrive = 100 mV	11	16	

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: CMRR measured at V_{CM} = 0V to 2.5V and 2.5V to 5V when V_S = 5V, V_{CM} = 0.2V to 1.35V and 1.35V to 2.7V when V_S = 2.7V. This eliminates units that have large V_{OS} at the V_{CM} extremes and low or opposite V_{OS} at V_{CM} = $V_S/2$.

Note 8: All measurements made at 10 kHz. A 100 kΩ pull-up resistor was used when measuring the LMC7225. C_{LOAD} = 50 pF including the test jig and scope probe. The rise times of the LMC7225 are a function of the R-C time constant.

Note 9: Input step voltage for the propagation measurements is 100 mV.

Note 10: Do not short the output of the LMC7225 to voltages greater than 10V or damage may occur.

National Semiconductor

LMC7221
Tiny CMOS Comparator with Rail-To-Rail Input and Open Drain Output

General Description

The LM7221 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes this comparator ideal for space and weight critical designs. The LMC7221 is also available in the SO-8 package. The LMC7221 is supplied in two offset voltage grades, 5 mV and 15 mV.

The open drain output can be pulled up with a resistor to a voltage which can be higher or lower than the supply voltage—this makes the part useful for mixed voltage systems.

For a tiny comparator with a push-pull output, please see the LMC7211 datasheet.

Features

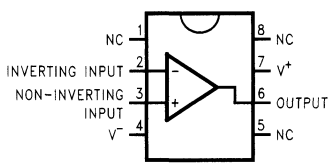
- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 7 µA at 5V
- Response time of 4 µs at 5V
- LMC7221—open drain output
- Input common-mode range beyond V– and V+
- Low input current

Applications

- Mixed voltage battery powered products
- Notebooks and PDAs
- PCMCIA cards
- Mobile communications
- Alarm and security circuits
- Driving low current LEDs
- Direct sensor interface

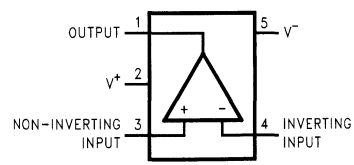
Connection Diagrams

8–Pin SO-8



Top View

5-Pin SOT23-5



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	2 kV
Differential Input Voltage	(V_{CC}) +0.3V to $(-V_{CC})$−0.3V
Voltage at Input	(V_{CC}) + 0.3V to $(-V_{CC})$−0.3V
Voltage at Output Pin	15V
Supply Voltage (V^+–V^-)	16V
Current at Input Pin (Note 7)	±5 mA
Current at Output Pin (Notes 3, 8)	±30 mA
Current at Power Supply Pin	40 mA
Lead Temperature (soldering, 10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	150°C

Operating Ratings (Note 1)

Supply Voltage	$2.7 \le V_{CC} \le 15V$
Junction Temperature Range	
LMC7221AI, LMC7221BI	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
SO-8 Package, 8-Pin Surface Mount	180°C/W
M05A Package, 5-Pin Surface Mount	325°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V, $V_{CM} = V_O = V+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7221AI Limit (Note 6)	LMC7221BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift		1.0			µV/°C
	Input Offset Voltage Average Drift	(Note 10)	3.3			µV/Month
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ratio	$0V \le V_{CM} \le 2.7V$	75			dB
PSRR	Power Supply Rejection Ratio	$2.7V \le V^+ \le 15V$	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	CMRR > 55 dB	3.0	2.9 **2.7**	2.9 **2.7**	V min
		CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OL}	Output Voltage Low	I_{load} = 2.5 mA	0.2	0.3 **0.4**	0.3 **0.4**	V max
I_S	Supply Current	V_{OUT} = low	7	12 **14**	12 **14**	µA max

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5.0V and 15V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extremes

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7221AI Limit (Note 6)	LMC7221BI Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		3	5 **8**	15 **18**	mV max
TCV_{OS}	Input Offset Voltage Temperature Drift	V^+ = 5V	1.0			µV/°C
		V^+ = 15V	4.0			
	Input Offset Voltage Average Drift	V^+ = 5V (Note 10)	3.3			µV/Month
		V^+ = 15V (Note 10)	4.0			
I_B	Input Current		0.04			pA
I_{OS}	Input Offset Current		0.02			pA
CMRR	Common Mode Rejection Ration	V+ = 5.0V	75			dB
		V+ = 15.0V	82			dB
PSRR	Power Supply Rejection Ratio	5V ≤ V^+ ≤ 10V	80			dB
A_V	Voltage Gain		100			dB
CMVR	Input Common-Mode Voltage Range	V+ = 5.0V CMRR > 55 dB	5.3	5.2 **5.0**	5.2 **5.0**	V min
		V+ = 5.0V CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
		V+ = 15.0V CMRR > 55 dB	15.3	15.2 **15.0**	15.2 **15.0**	V min
		V+ = 15.0V CMRR > 55 dB	−0.3	−0.2 **0.0**	−0.2 **0.0**	V max
V_{OL}	Output Voltage Low	V+ = 5V I_{load} = 5 mA	0.2	0.40 **0.55**	0.40 **0.55**	mV max
		V+ = 15V I_{load} = 5 mA	0.2	0.40 **0.55**	0.40 **0.55**	mV max
I_S	Supply Current	V_{OUT} = Low	7	14 **18**	14 **18**	µA max
I_{SC}	Short Circuit Current	Sinking (Note 8)	45			mA

Leakage Characteristics

T_J = 25°C

Symbol	Parameter	Conditions	Typ (Note 5)	LMC7221AI Limit (Note 6)	LMC7221BI Limit (Note 6)	Units
$I_{LEAKAGE}$	Output Leakage Current	V+ = 2.7V V_{IN}(+) = 0.5V V_{IN}(−) = 0V V_{OUT} = 15V	0.1	500	500	nA

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V, V_{CM} = V_O = $V^+/2$. **Boldface** limits apply at the temperature extreme

Symbol	Parameter	Conditions		Typ (Note 5)	LMC7221AI Limit (Note 6)	LMC7221BI Limit (Note 6)	Units
t_{rise}	Rise Time	f = 10 kHz, C_L = 50 pF, (Note 9) Overdrive = 10 mV, 5 kΩ Pullup		0.3			µs
t_{fall}	Fall Time	f = 10 kHz, C_L = 50 pF, (Note 9) Overdrive = 10 mV, 5 kΩ Pullup		0.3			µs
t_{PHL}	Propagation Delay (High to Low) (Note 11)	f = 10 kHz, C_L = 50 pF, 5 kΩ Pullup (Note 9)	10 mV	10			µs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, C_L = 50 pF, 5 kΩ Pullup (Note 9)	10 mV	10			µs
			100 mV	4			
t_{PLH}	Propagation Delay (Low to High) (Note 11)	f = 10 kHz, C_L = 50 pF, 5 kΩ Pullup (Note 9)	10 mV	6			µs
			100 mV	4			
		V+ = 2.7V, f = 10 kHz, C_L = 50 pF, 5 kΩ Pullup (Note 9)	10 mV	7			µs
			100 mV	4			

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 kΩ in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30 mA may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is

Note 5: $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 6: Typical values represent the most likely parametric norm.

Note 7: All limits are guaranteed by testing or statistical analysis.

Note 8: Limiting input pin current is only necessary for input voltages which exceed the absolute maximum input voltage rating.

Note 9: Do not short circuit the output to V+ when V+ is greater than 12V or reliability will be adversely affected.

Note 10: C_L includes the probe and test jig capacitance.

Note 11: Input offset voltage average drift is calculated by dividing the accelerated operating life V_{OS} drift by the equivalent operational time. This represents worst case input conditions and includes the first 30 days of drift.

Note 12: Input step voltage for propagation delay measurement is 2V.

National Semiconductor

LMV331 Single / LMV393 Dual / LMV339 Quad General Purpose, Low Voltage, TinyPack Comparators

General Description

The LMV393 and LMV339 are low voltage (2.7-5V) versions of the dual and quad comparators, LM393/339, which are specified at 5-30V. The LMV331 is the single version, which is available in space saving SC70-5 and SOT23-5 packages. SC70-5 is approximately half the size of SOT23-5.

The LMV393 is available in 8-pin SOIC and 8-pin MSOP. The LMV339 is available in 14-pin SOIC and 14-pin TSSOP.

The LMV331/393/339 is the most cost-effective solution where space, low voltage, low power and price are the primary specification in circuit design for portable consumer products. They offer specifications that meet or exceed the familiar LM393/339 at a fraction of the supply current.

The chips are built with National's advanced Submicron Silicon-Gate BiCMOS process. The LMV331/393/339 have bipolar input and output stages for improved noise performance.

Features

(For 5V Supply, Typical Unless Otherwise Noted)

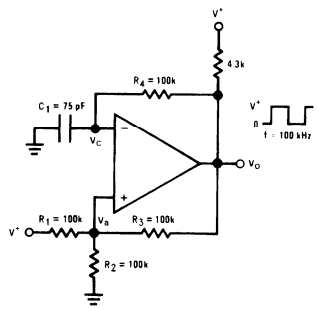
- Space Saving SC70-5 Package (2.0 x 2.1 x 1.0 mm)
- Space Saving SOT23-5 Package (3.00 x 3.01 x1.43 mm)
- Guaranteed 2.7V and 5V Performance
- Industrial Temperature Range −40°C to +85°C
- Low Supply Current 60µA/Channel
- Input Common Mode Voltage Range Includes Ground
- Low Output Saturation Voltage 200 mV

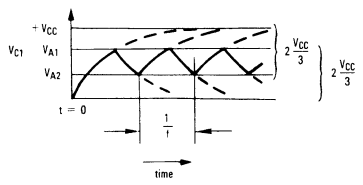
Applications

- Mobile Communications
- Notebooks and PDA's
- Battery Powered Electronics
- General Purpose Portable Device
- General Purpose Low Voltage Applications

Typical Applications

Squarewave Oscillator





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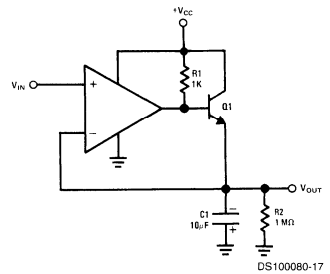


DS100080-17

Positive Peak Detector

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	
LMV331/ 393/ 339	800V
Machine Model LMV331/339/393	120V
Differential Input Voltage	± Supply Voltage
Voltage on any pin (referred to V^- pin)	5.5V
Soldering Information	
Infrared or Convection (20 sec)	235°C
Storage Temp. Range	−65°C to +150°C
Junction Temperature (Note 3)	150°C

Operating Ratings (Note 1)

Supply Voltage	2.7V to 5.0V
Temperature Range	
LMV393, LMV339, LMV331	$-40°C \le T_J \le +85°C$
Thermal Resistance (θ_{JA})	
M Package, 8-pin Surface Mount	190°C/W
M Package, 14-pin Surface Mount	145°C/W
MTC Package, 14-pin TSSOP	155°C/W
MAA05 Package, 5-pin SC70-5	478°C/W
M05A Package 5 -pin SOT23-5	265°C/W
MM Package, 8-pin Mini Surface Mount	235°C/W

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V+ = 2.7V, V− = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 4)	LMV331/ 393/339 Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		1.7	7	mV max
TCV_{OS}	Input Offset Voltage Average Drift		**5**		µV/°C
I_B	Input Bias Current		10	250 **400**	nA max
I_{OS}	Input Offset Current		5	50 **150**	nA max
V_{CM}	Input Voltage Range		−0.1		V
			2.0		V
V_{SAT}	Saturation Voltage	$I_{sink} \le 1mA$	200		mV
I_O	Output Sink Current	$V_O \le 1.5V$	23	5	mA min
I_S	Supply Current	LMV331	40	100	µA max
		LMV393 Both Comparators	70	140	µA max
		LMV339 All four Comparators	140	200	µA max
	Output Leakage Current		.003	**1**	µA max

2.7V AC Electrical Characteristics

T_J = 25°C, V+ = 2.7V, R_L = 5.1 kΩ, V− = 0V.

Symbol	Parameter	Conditions	Typ (Note 4)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive =10 mV	1000	ns
		Input Overdrive =100 mV	350	ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive =10 mV	500	ns
		Input Overdrive =100 mV	400	ns

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V+ = 5V, V− = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 4)	LMV331/ 393/339 Limit (Note 5)	Units
V_{OS}	Input Offset Voltage		1.7	7 **9**	mV max
TCV_{OS}	Input Offset Voltage Average Drift		5		µV/˚C
I_B	Input Bias Current		25	250 **400**	nA max
I_{OS}	Input Offset Current		2	50 **150**	nA max
V_{CM}	Input Voltage Range		−0.1		V
			4.2		V
A_V	Voltage Gain		50	20	V/mV min
V_{sat}	Saturation Voltage	$I_{sink} \leq 4$ mA	200	400 **700**	mV max
I_O	Output Sink Current	$V_O \leq 1.5V$	84	10	mA
I_S	Supply Current	LMV331	60	120 **150**	µA max
		LMV393 Both Comparators	100	200 **250**	µA max
		LMV339 All four Comparators	170	300 **350**	µA max
	Output Leakage Current		.003	**1**	µA max

5V AC Electrical Characteristics

T_J = 25˚C, V+ = 5V, R_L = 5.1 kΩ, V− = 0V.

Symbol	Parameter	Conditions	Typ (Note 4)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive =10 mV	600	ns
		Input Overdrive =100 mV	200	ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive =10 mV	450	ns
		Input Overdrive =100 mV	300	ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: : Human body model, 1.5kΩ in series with 100 pF. Machine model, 200Ω in series with 100 pF.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: Typical Values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

National Semiconductor

LMV7219
7 nsec, 2.7V to 5V Comparator with Rail-to-Rail Output

General Description

The LMV7219 is a low-power, high-speed comparator with internal hysteresis. The LMV7219 operating voltage ranges from 2.7V to 5V with push/pull rail-to-rail output. This device achieves a 7ns propagation delay while consuming only 1.1mA of supply current at 5V.

The LMV7219 inputs have a common mode voltage range that extends 200mV below ground, allowing ground sensing. The internal hysteresis ensures clean output transitions even with slow-moving inputs signals.

The LMV7219 is available in the SC70-5 and SOT23-5 packages, which are ideal for systems where small size and low power are critical.

Features

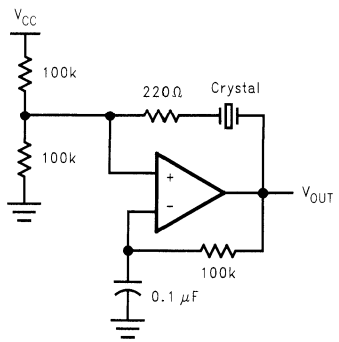
(V_S = 5V, T_A = 25°C, Typical values unless specified)

- Propagation delay 7ns
- Low supply current 1.1mA
- Input common mode voltage range extends 200mv below ground
- Ideal for 2.7V and 5V single supply applications
- Internal hysteresis ensures clean switching
- Fast rise and fall time 1.3ns
- Available in space-saving packages: 5-pin SC70-5 and SOT23-5

Applications

- Portable and battery-powered systems
- Scanners
- Set top boxes
- High speed differential line receiver
- Window comparators
- Zero-crossing detectors
- High-speed sampling circuits

Typical Application



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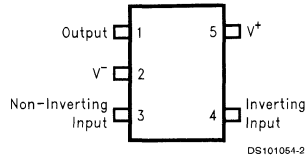
Connection Diagram

SC70-5/SOT23-5

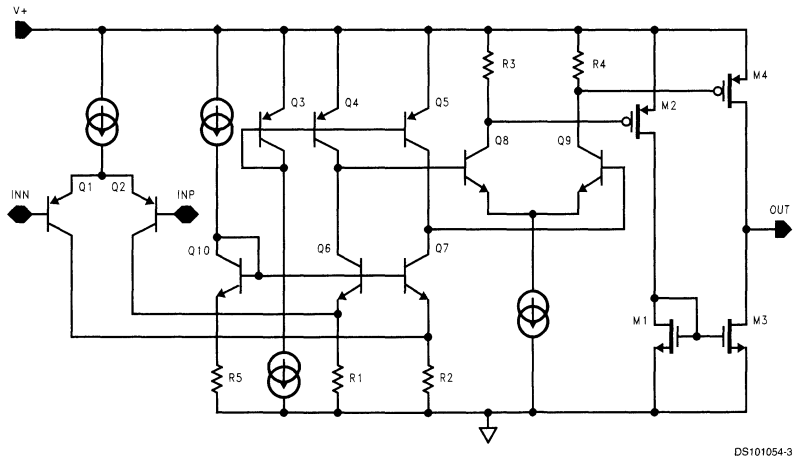


Top View

Ordering Information

Package	Part Number	Marking	Supplied as	NSC Drawing
5-pin SC70-5	LMV7219M7	C15	1k Units Tape and Reel	MAA05A
	LMV7219M7X	C15	3k Units Tape and Reel	
5-pin SOT23-5	LMV7219M5	C14A	1k Units Tape and Reel	MA05B
	LMV7219M5X	C14A	3k Units Tape and Reel	

Simplified Schematic



Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Body	150V
Human Model Body	2000V
Differential Input Voltage	± Supply Voltage
Output Short Circuit Duration	(Note 3)
Supply Voltage (V^+ - V^-)	5.5V
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C (lead temp)
Voltage at Input/Output pins	(V^+) + 0.4V (V^-) − 0.4V
Current at Input Pin (Note 9)	±10mA

Operating Ratings

Supply voltages (V^+ - V^-)	2.7V to 5V
Junction temperature range (Note 4)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Thermal Resistance	
SC70-5	478°C/W
SOT23-5	265°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 2.7V, V^- = 0V, C_L = 10pF and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	6 **8**	mV max
I_B	Input Bias Current		450	950 **2000**	nA max
I_{OS}	Input Offset Current		50	200 **400**	nA max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 1.50V	85	62 **55**	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	85	65 **55**	dB min
V_{CM}	Input Common-Voltage Range	CMRR > 50dB	V_{CC} −1	V_{CC} −1.2 **V_{CC} −1.3**	V min
			−0.2	−0.1 **0**	V max
V_O	Output Swing High	I_L = 4mA, V_{ID} = 500mV	V_{CC} −0.22	V_{CC} −0.3 **V_{CC} −0.4**	V min
		I_L = 0.4mA, V_{ID} = 500mV	V_{CC} −0.02	V_{CC} −0.05 **V_{CC} −0.15**	
	Output Swing Low	I_L = −4mA, V_{ID} = −500mV	130	200 **300**	mV max
		I_L = −0.4mA, V_{ID} = −500mV	15	50 **150**	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (Note 3)	20		mA
		Sinking, V_O = 2.7V (Note 3)	20		
I_S	Supply Current	No load	0.9	1.6 **2.2**	mA max
V_{HYST}	Input Hysteresis Voltage	(Note 10)	7		mV
V_{TRIP^+}	Input Referred Positive Trip Point	(see *Figure 1*)	3	8	mV max
V_{TRIP^-}	Input Referred Negative Trip Point	(see *Figure 1*)	−4	−8	mV min

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_{CM} = V^+/2, V^+ = 2.7V, V^- = 0V, C_L = 10pF and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
t_{PD}	Propagation Delay	Overdrive = 5mV V_{CM} = 0V (Note 7)	12		ns max
		Overdrive = 15mV V_{CM} = 0V (Note 7)	11		
		Overdrive = 50mV V_{CM} = 0V (Note 7)	10	20	
t_{SKEW}	Propagation Delay Skew	(Note 8)	1		ns
t_r	Output Rise Time	10% to 90%	2.5		ns
t_f	Output Fall Time	90% to 10%	2		ns

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C, V_{CM} = V^+/2, V^+ = 5V, V^- = 0V, C_L = 10pF and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
V_{OS}	Input Offset Voltage		1	6 **8**	mV max
I_B	Input Bias Current		500	950 **2000**	nA max
I_{OS}	Input Offset Current		50	200 **400**	nA max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 3.8V	85	65 **55**	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	85	65 **55**	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB	V_{CC} −1	V_{CC} −1.2 V_{CC} −1.3	V min
			−0.2	−0.1 0	V max
V_O	Output Swing High	I_L = 4mA, V_{ID} = 500mV	V_{CC} −0.13	V_{CC} −0.2 V_{CC} −0.3	V min
		I_L = 0.4mA, V_{ID} = 500mV	V_{CC} −0.02	V_{CC} −0.05 V_{CC} −0.15	
	Output Swing Low	I_L = −4mA, V_{ID} = −500mV	80	180 **280**	mV max
		I_L = −0.4mA, V_{ID} = −500mV	10	50 **150**	
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (Note 3)	68	30 **20**	mA min
		Sinking, V_O = 5V (Note 3)	65	30 **20**	
I_S	Supply Current	No load	1.1	1.8 **2.4**	mA max
V_{HYST}	Input Hysteresis Voltage	(Note 10)	7.5		mV
V_{Trip^+}	Input Referred Positive Trip Point	(See figure 1)	3.5	8	mV max
V_{Trip^-}	Input Referred Negative Trip Point	(See figure 1)	−4	−8	mV min

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5V, V^- = 0V, C_L = 10pF and R_L > 1MΩ to V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limit (Note 6)	Units
t_{PD}	Propagation Delay	Overdrive = 5mV V_{CM} = 0V (Note 7)	9		ns max
		Overdrive = 15mV V_{CM} = 0V (Note 7)	8	20	
		Overdrive = 50mV V_{CM} = 0V (Note 7)	7	19	
t_{SKEW}	Propagation Delay Skew	(Note 8)	0.4		ns
t_r	Output Rise Time	10% to 90%	1.3		ns
t_f	Output Fall Time	90% to 10%	1.25		ns

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 200Ω in series with 100pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Propagation delay measurements made with 100mV steps. Overdrive is measure relative to V_{Trip}.

Note 8: Propagation Delay Skew is defined as absolute value of the difference between t_{PDLH} and t_{PDHL}.

Note 9: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 10: The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{trip^+} and V_{trip^-}, while the hysteresis voltage is the difference of these two.

National Semiconductor

LMV7235/LMV7239
45ns, Ultra Low Power, Low Voltage, Rail-to-Rail Input Comparator with Open-Drain/Push-Pull Output

General Description

The LMV7235/39 are ultra low power, low voltage, 45ns comparators. They are guaranteed to operate over the full supply voltage range of 2.7V to 5V. These devices achieve a 45ns propagation delay while consuming only 65µA of supply current at 5V.

The LMV7235/39 have a greater than rail-to-rail common mode voltage range. The input common mode voltage range extends 200mV below ground and 200mV above supply, allowing both ground and supply sensing.

The LMV7235 features an open drain output. By connecting an external resistor, the output of the comparator can be used as a level shifter.

The LMV7239 features a push-pull output stage. This feature allows operation without the need of an external pull-up resistor.

The LMV7235/39 are available in the SC70-5 and SOT23-5 packages, which are ideal for systems where small size and low power is critical.

Features

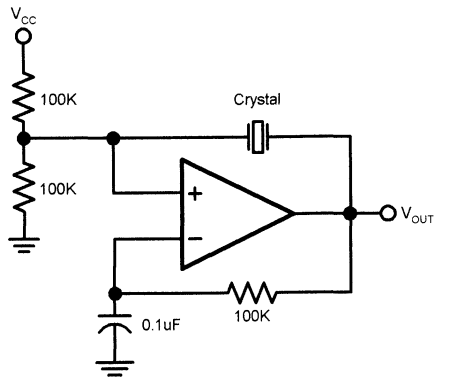
(V_S = 5V, T_A = 25°C, Typical values unless otherwise specified)

- Propagation delay 45ns
- Low supply current 65µA
- Rail-to-Rail input
- Open drain and push-pull output
- Ideal for 2.7V and 5V single supply applications
- Available in space saving packages: 5-pin SOT23-5 and 5-pin SC70-5

Applications

- Portable and battery powered systems
- Scanners
- Set top boxes
- High speed differential line receiver
- Window comparators
- Zero-crossing detectors
- High speed sampling circuits

Typical Application



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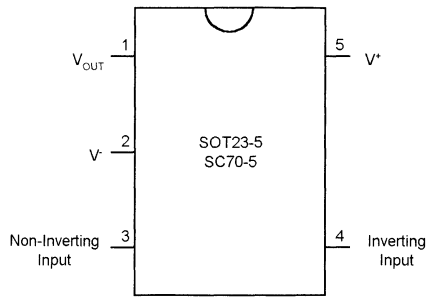
Connection Diagram

SC70-5/SOT23-5



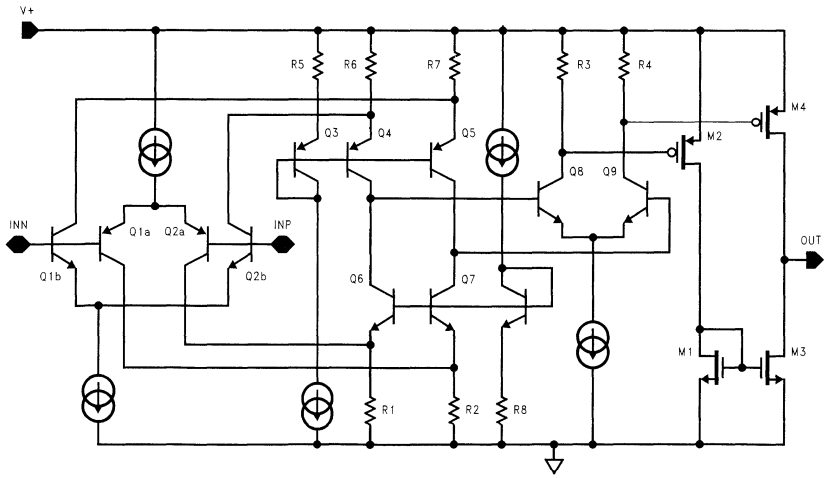
10135903

Top View

Ordering Information

Package	Part Number	Marking	Supplied as	NSC Drawing
5-pin SC70-5	LMV7235M7	C21	1k Units Tape and Reel	MAA05A
	LMV7235M7X	C21	3k Units Tape and Reel	
	LMV7239M7	C20	1k Units Tape and Reel	
	LMV7239M7X	C20	3k Units Tape and Reel	
5-pin SOT23-5	LMV7235M5	C21A	1k Units Tape and Reel	MF05A
	LMV7235M5X	C21A	3k Units Tape and Reel	
	LMV7239M5	C20A	1k Units Tape and Reel	
	LMV7239M5X	C20A	3k Units Tape and Reel	

Simplified Schematic



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Machine Body	100V
Human Model Body	1000V
Differential Input Voltage	± Supply Voltage
Output Short Circuit Duration	(Note 3)
Supply Voltage (V^+ - V^-)	5.5V
Soldering Information	
Infrared or Convection(20 sec)	235°C
Wave Soldering (10 sec)	260°C (lead temp)
Voltage between any two pins	5.5V
Current at Input Pin(Note 9)	

Operating Ratings

Supply Voltages (V^+ - V^-)	2.7V to 5V
Junction Temperature Range (Note 4)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Thermal Resistance	
SC70-5	478°C/W
SOT23-5	265°C/W

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = $V^+/2$, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		0.8	6 **8**	mV max
I_B	Input Bias Current		30	400 **600**	nA max
I_{OS}	Input Offset Current		5	200 **400**	nA max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 2.7V (Note 7)	62	52	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	85	65	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB	V^+ +0.2	V^+ +0.1 **V^+**	V min
			−0.2	−0.1 **0**	V max
V_O	Output Swing High (LMV7239 only)	I_L = 4mA, V_{ID} = 500mV	V^+ −0.26	V^+ −0.35	V min
		I_L = 0.4mA, V_{ID} = 500mV	V^+ −0.02		V min
	Output Swing Low (LMV7239/LMV7235)	I_L = −4mA, V_{ID} = −500mV	230	350 **450**	mV max
		I_L = −0.4mA, V_{ID} = −500mV	15		mV max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (LMV7239 only) (Note 3)	15		mA
		Sinking, V_O = 2.7V (LMV7235 R_L = 10k) (Note 3)	20		mA
I_S	Supply Current	No load	52	85 **100**	µA max

2.7V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 2.7V, V^- = 0V^-. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limits (Note 6)	Units
t_{PD}	Propagation Delay	Overdrive = 20mV (Note 10)	68		ns
		Overdrive = 50mV (Note 10)	63		ns
		Overdrive = 100mV (Note 10)	50		ns
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	(Note 8)	5		ns
t_r	Output Rise Time	LMV7239 10% to 90%	1.7		ns
		LMV7235 10% to 90% (Note 10)	112		ns
t_f	Output Fall Time	90% to 10%	1.7		ns
$I_{LEAKAGE}$	Output Leakage Current (LMV7235 only)		3		nA

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		1	6 **8**	mV max
I_B	Input Bias Current		30	400 **600**	nA max
I_{OS}	Input Offset Current		5	200 **400**	nA max
CMRR	Common Mode Rejection Ratio	0V < V_{CM} < 5V	67	52	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 2.7V to 5V	85	65	dB min
V_{CM}	Input Common-Mode Voltage Range	CMRR > 50dB	V^+ +0.2	V^+ +0.1 **V^+**	V min
			−0.2	−0.1 **0**	V max
V_O	Output Swing High (LMV7239 only)	I_L = 4mA, V_{ID} = 500mV	V^+ −0.15	V^+ −0.25	V min
		I_L = 0.4mA, V_{ID} = 500mV	V^+ −0.01		V min
	Output Swing Low (LMV7239/LMV7235)	I_L = −4mA, V_{ID} = −500mV	230	350 **450**	mV max
		I_L = −0.4mA, V_{ID} = −500mV	10		mV max

5V Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V_{CM} = V^+/2, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limits (Note 6)	Units
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0V (LMV7239 only) (Note 3)	55	25 **15**	mA min
		Sinking, V_O = 5V (LMV7235 R_L = 10k) (Note 3)	60	30 **20**	mA min
I_S	Supply Current	No load	65	95 **110**	µA max
t_{PD}	Propagation Delay	Overdrive = 20mV (Note 10)	62		ns max
		Overdrive = 50mV (Note 10)	57		ns max
		Overdrive = 100mV (Note 10)	45		ns max
t_{SKEW}	Propagation Delay Skew (LMV7239 only)	(Note 8)	5		ns
t_r	Output Rise Time	LMV7239 10% to 90%	1.2		ns
		LMV7235 10% to 90% (Note 10)	100		ns
t_f	Output Fall Time	90% to 10%	1.2		ns
$I_{LEAKAGE}$	Output Leakeage Current (LMV7235 only)		3		nA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF. Machine model, 200pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: CMRR is not linear over the common mode range. Limits are guaranteed over the worst case from 0 to $V_{CC/2}$ or $V_{CC/2}$ to V_{CC}.

Note 8: Propagation Delay Skew is defined as the absolute value of the difference between t_{PDLH} and t_{PDHL}.

Note 9: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

Note 10: A 10k pull-up resistor was used when measuring the LMV7235. The rise time of the LMV7235 is a function of the R-C time constant.

National Semiconductor

LMV7251/LMV7255
1.8V Low Voltage Comparator with Rail-to-Rail Input

General Description

The LMV7251/LMV7255 are rail-to-rail input low voltage comparators, which can operate at supply voltage range of 1.8V to 5.0V. The LMV7251/LMV7255 are available in space saving SC-70 or SOT23-5 packages. These comparators are ideal for low voltage and space critical designs.

The LMV7251 features a push-pull output stage. This feature allows operation with minimum power consumption when driving a load.

The LMV7255 features an open drain output. This allows the connection of an external resistor at the output. The output of the comparator can be used as a level shifter.

The IC's are built with National Semiconductor's advance Submicron Silicon-Gate BiCMOS process. The LMV7251/LMV7255 have bipolar inputs for improved noise performance and CMOS outputs for better rail-to-rail output performance.

Features

(V_S = 1.8V, T_A = 25°C, Typical values unless specified).

- Single or Dual Supplies
- Low supply voltage — 1.8V to 5.0V
- Ultra low supply current — 11µA
- Low input bias current — 14nA
- Low input offset current — 200pA
- Low input offset voltage — +/−0.3mV
- Response time — 670ns (20mV overdrive)
- Input common mode voltage — 0.1V beyond rails

Applications

- Mobile communications
- Laptops and PDA's
- Battery powered electronics
- General purpose low voltage applications

Typical Circuit

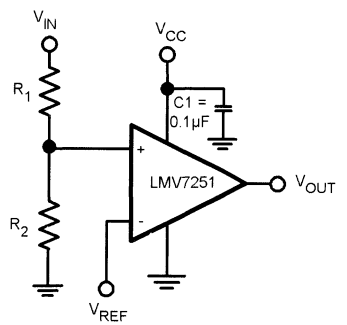
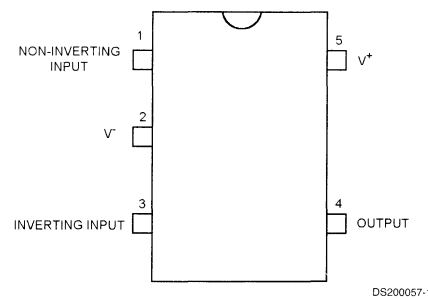


FIGURE 1. Threshold Detector

Connection Diagram



Top View

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance	1KV (Note 2)
	200V (Note 6)
V_{IN} Differential	+/−Supply Voltage
Supply Voltage (V^+ - V^-)	5.5V
Voltage at Input/Output pins	V^+ +0.1V, V^- −0.1V
Soldering Information	
Infrared or Convection (20 sec.)	235°C
Wave Soldering (10 sec.)	260°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (Note 4)	+150°C

Operating Ratings (Note 1)

Supply Voltage V^+	1.8V to 5.0V
Junction Temperature Range (Note 3)	−40°C to +85°C
Package Thermal Resisance (Note 3)	
SOT23-5	325°C/W
SC-70	265°C/W

1.8V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 4)	Limits (Note 5)	Units
V_{OS}	Input Offset Voltage		0.3	6 **8**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 0.9V (Note 7)	10		uV/C
I_B	Input Bias Current		14		nA
I_{OS}	Input Offset Current		200		pA
I_S	Supply Current		11	15 **17**	µA max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 0.9V (LMV7251 only)	8	4	mA min
		Sinking, V_O = 0.9V	11.6	5	
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8V (LMV7255 only)	300		pA
V_{OH}	Output Voltage High	I_O = 1.5mA (LMV7251 only)	1.72	1.675	V min
V_{OL}	Output Voltage Low	I_O = −1.5mA	65	125	mV max
V_{CM}	Input Common Voltage Range	CMRR > 45 dB		1.9	V max
				−0.1	V min
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 1.8V	72	47	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	79	55	dB min

1.8V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ	720		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ	380		ns

1.8V AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 1.8V, V^- = 0V, V_{CM} = 0.5V, V_O = V^+/2. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ	670		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ	400		ns

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		0.03	6 **8**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 1.35V (Note 7)	10		µV/C
I_B	Input Bias Current		15		nA
I_{OS}	Input offset Current		210		pA
I_S	Supply Current		11	18 **22**	µA max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 1.35V (LMV7251 only)	28	15	mA
		Sinking, V_O = 1.35V	28	15	
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7V, (LMV7255 only)	320		pA
V_{OH}	Output Voltage High	I_O = 2mA (LMV7251 only)	2.63	2.575	V min
V_{OL}	Output Voltage Low	I_O = −2mA	61	125	mV max
V_{CM}	Input Common Voltage Range	CMRR > 45dB		2.8	V max
				−0.1	V min
CMRR	Common Mode Rejection Ratio	0 < V_{CM} < 2.7V	75	46	dB min
PSRR	Power Supply Rejection Ratio	V^+ = 1.8V to 5V	79	55	dB min

2.7V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 2.7V, V^- = 0V.**Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Condition	Typ (Note 5)	Limits (Note 6)	Units
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20mV Load = 50pF//5kΩ	830		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ	430		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20mV Load = 50pF//5kΩ	730		ns
		Input Overdrive = 50mV Load = 50pF//5kΩ	410		ns

5V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C, V^+ = 5V, V^- = 0V. **Boldface** limits apply at the temperature extremes.

Symbol	Parameter	Conditions	Typ (Note 5)	Limits (Note 6)	Units
V_{OS}	Input Offset Voltage		0.03	6 **8**	mV max
TC V_{OS}	Input Offset Average Drift	V_{CM} = 2.5V (Note 7)	10		µV/C
I_B	Input Bias Current		16		nA
I_{OS}	Input Offset Current		220		pA
I_S	Supply Current		12	20 **25**	µA max
I_{SC}	Output Short Circuit Current	Sourcing, V_O = 2.5V (LMV7251 only)	82	50	mA min
		Sinking, V_O = 2.5V	78	50	
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5V, (LMV7255 only)	375		pA
V_{OH}	Output Voltage High	I_O = 4mA	4.9	4.82	V min
V_{OL}	Output Voltage Low	I_O = −4mA	90	180	mV max

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5kΩ in series with 100pF.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: Machine Model, 0Ω in series with 200pF.

Note 7: Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

National Semiconductor

LP339
Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 µA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

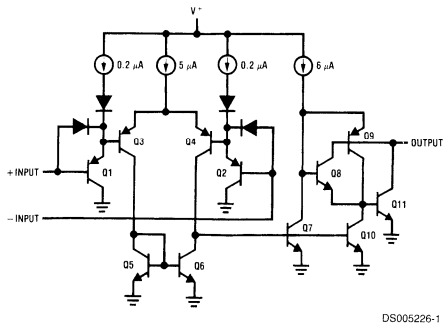
Advantages

- Ultra-low power supply drain suitable for battery applications
- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Features

- Ultra-low power supply current drain (60 µA)—independent of the supply voltage (75 µW/comparator at +5 V_{DC})
- Low input biasing current: 3 nA
- Low input offset current: ±0.5 nA
- Low input offset voltage: ±2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O=2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



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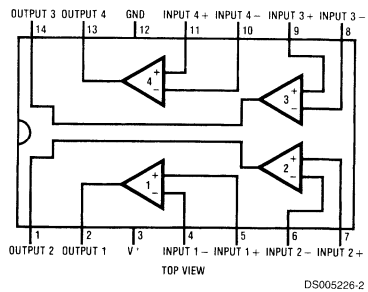
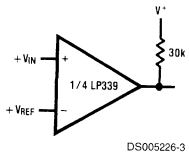


DS005226-2

Order Number LP339M for S.O. Package
See NS Package Number M14A
Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

Typical Applications (V^+= 5.0 V_{DC})

Basic Comparator



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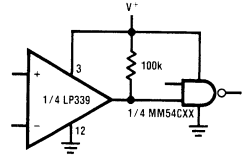
Driving CMOS



DS005226-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	36 V_{DC} or ±18 V_{DC}
Differential Input Voltage	±36 V_{DC}
Input Voltage	−0.3 V_{DC} to 36 V_{DC}
Power Dissipation (Note 2)	
Molded DIP	570 mW
Output Short Circuit to GND (Note 3)	Continuous
Input Current V_{IN}<−0.3 V_{DC} (Note 4)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65° to +150°C
Soldering Information:	
Dual-In-Line Package (10 sec.)	+260°C
S.O. Package:	
Vapor Phase (60 sec.)	+215°C
Infrared (15 sec.)	+220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics

(V+=5 V_{DC}) (Note 5)

Parameter	Conditions	Min	Typ	Max	Units
Input Offset Voltage	T_A=25°C (Note 10)		±2	±5	mV_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with the Output in the Linear Range, T_A=25°C (Note 6)		2.5	25	nA_{DC}
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$, T_A=25°C		±0.5	±5	nA_{DC}
Input Common Mode Voltage Range	T_A=25°C (Note 7)	0		V+−1.5	V_{DC}
Supply Current	R_L=Infinite on all Comparators, T_A=25°C		60	100	μA_{DC}
Voltage Gain	V_O = 1 V_{DC} to 11 V_{DC}, R_L=15 kΩ, V^+=15 V_{DC}, T_A=25°C		500		V/mV
Large Signal Response Time	V_{IN}=TTL Logic Swing, V_{REF}=1.4 V_{DC}, V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25°C		1.3		µSec
Response Time	V_{RL}=5 V_{DC}, R_L=5.1 kΩ, T_A=25°C (Note 8)		8		µSec
Output Sink Current	$V_{IN}(-)$=1 V_{DC}, $V_{IN}(+)$=0, V_O=2 V_{DC}, T_A=25°C (Note 12)	15	30		mA_{DC}
	V_O=0.4 V_{DC}	0.20	0.70		mA_{DC}
Output Leakage Current	$V_{IN}(+)$=1 V_{DC}, $V_{IN}(-)$=0, V_O=5 V_{DC}, T_A=25°C		0.1		nA_{DC}
Input Offset Voltage	(Note 10)			±9	mV_{DC}
Input Offset Current	$I_{IN}(+)-I_{IN}(-)$		±1	±15	nA_{DC}
Input Bias Current	$I_{IN}(+)$ or $I_{IN}(-)$ with Output in Linear Range		4	40	nA_{DC}
Input Common Mode Voltage Range	Single Supply	0		V+−2.0	V_{DC}
Output Sink Current	$V_{IN}(-)$=1 V_{DC}, $V_{IN}(+)$=0, V_O=2 V_{DC}	10			mA_{DC}
Output Leakage Current	$V_{IN}(+)$=1 V_{DC}, $V_{IN}(-)$=0, V_O=30 V_{DC}			1.0	μA_{DC}
Differential Input Voltage	All $V_{IN's} \geq 0$ V_{DC} (or V^- on split supplies) (Note 9)			36	V_{DC}

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: For elevated temperature operation, T_j max is 125°C for the LP339. θ_{ja} (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq$ 100 mW), provided the output transistors are allowed to saturate.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V+ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than −0.3 V_{DC} (T_A=25°C).

Note 5: These specifications apply for V^+=5V_{DC} and 0°C≤T_A≤70° C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 7: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+−1.5V (T_A=25°C), but either or both inputs can go to 30 V_{DC} without damage.

Note 8: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 µs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics (Continued)

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at T_A=25˚C.

Note 10: At output switch point, V_O=1.4V, R_S=0Ω with V^+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+−1.5 V_{DC}).

Note 11: For input signals that exceed V^+, only the overdriven comparator is affected. With a 5V supply, V_{IN} should be limited to 25V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Note 12: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).

Section 6

Converters - A/D, D/A, and Data Acquisition Systems

Section 6 Contents

National Semiconductor

A/D Converter Selection Guide

(Sorted by Resolution and Speed)

Device	Resolution (Bits)	Speed (MSPS)	Conversion Time (max)	Supply Voltage (V)	Power Consumption (mW, typ)	INL (LSB, typ)	DNL (LSB, typ)	SINAD (dB, typ)	ENOB (Bits, typ)
ADC08200	8	200	-	+3.3	1.05 mW/MSPS	±1.0	±0.4	46	7.3
ADC08100	8	100	-	3	130	±0.5	±0.4	42.8	7.4
ADC08060	8	60	-	+3.3	1.3 mW/MSPS	±0.5	±0.4	47	7.6
ADC1175-50	8	50	-	+5	125	±0.8	±0.7	45	7.2
ADC08351	8	42	-	+3	36	±0.7	±0.6	45	7.2
ADC1175	8	20	-	+5	60	±0.5	±0.35	45	7.2
ADC1173	8	15	-	+3	33	±0.5	±0.4	46	7.6
ADC0820	8	-	1.2 µs	+5	75	±0.5	-	-	-
ADC08131/4/8	8	-	2 µs	+5	20	±0.5	±8	48.3	7.7
ADC08831/2	8	-	4 µs	+5	5.5	±0.2	±0.2	48.0	7.7
ADC08031/4/8	8	-	8 µs	+5	20	±1.0	±8	-	-
ADC08131/4/8	8	-	8	5	20	±0.5	-	-	-
ADCV0831	8	-	16 µs	+5	0.72	±1.5	-	-	-
ADC0831/2/4/8	8	-	32 µs	+5	15	±1.0	-	-	-
ADC0844/8	8	-	40 µs	+5	13	±0.5	-	-	-
ADC0801/2/3/4/5	8	-	110 µs	+5	12.5	±0.25	-	-	-
ADC0808/9	8	-	100 µs	+5	15	±0.5	-	-	-
ADC0816/7	8	-	100 µs	+5	15	±0.5	-	-	-
ADC08061/2	8	-	560 ns	+5	100	±0.5	-	-	-
ADC08161	8	-	560 ns	+5	100	±0.5	-	60	7.1
ADC10D040	2 x 10	40	-	+3.3	250	±0.5	±0.35	59	9.5
ADC10030	10	27	-	+5	121	±0.45	±0.4	59	9.4
ADC10D020	2 x 10	20	-	+3.3	150	±0.7	±0.35	59	9.5
ADC10321	10	20	-	+5	98	±0.45	±0.35	60	9.6
ADC10221	10	15	-	+5	98	±0.45	±0.35	60	9.6
ADC1061	10	-	1.8 µs	+5	235	±0.3	±1.0	-	-
ADC10154/8	10	-	4.4 µs	+5 or ±5	33	±1.0	-	60	9.6
ADC10731/2/4/8	10	-	5 µs	+5	37	±1.25	-	67	10.8
ADC1038	10	-	13.7 µs	+5	15	-	±1.0	-	-
ADC1005	10	-	50 µs	+5	15	±0.5	-	-	-
ADC1001	10		200 µs	+5	25	±2.0	-	-	-
ADC10662/4	10	-	470 ns	+5	235	±0.5	-	60	9.6
ADC10061/2/4	10	1.1	900 ns	+5	235	±0.5	-	60	9.6
ADC10461/2/4	10	1.1	900 ns	+5	235	±0.5	-	60	9.6
CLC5957	12	70	-	5	640	±1.5	±0.65	65.5	10.5
CLC5956	12	65	-	+5	615	±1.7	±0.65	65.5	10.5
ADC12L063	12	62	-	+3.0	354	±1.0	±0.5	65	10.3
ADC12040	12	40	-	+5.0	340	±0.7	±0.4	69.5	11.2
ADC12281	12	20	-	+5	443	±1.0	±0.4	65	10.5
ADC12181	12	10	-	+5	235	±0.7	±0.4	64.5	10.4
ADC12191	12	10	-	+5	235	±0.7	±0.5	62	10.0
ADC12081	12	5	-	+5	105	±0.6	±0.35	67.6	10.9
ADC12662	12	1.5	0.58	5	200	±0.4	±0.4	70	11.3
ADC12062	12	1	1	5	75	±0.4	±0.4	71	11.5
ADC12041/8	12	-	3.6 µs	+5	33	±0.6	±1.0	-	-

Device	Resolution (Bits)	Speed (MSPS)	Conversion Time (max)	Supply Voltage (V)	Power Consumption (mW, typ)	INL (LSB, typ)	DNL (LSB, typ)	SINAD (dB, typ)	ENOB (Bits, typ)
ADC12H030/2/4/8	12	-	5.5 µs	+5	36	±0.5	±1.0	69.4	11.2
ADC12451	12	-	7.7	5	113	1.5	-	-	-
ADC1251	12	-	8	5	113	1.5	-	-	-
ADC12030/2/4/8	12	-	8.8 µs	+5	33	±0.5	±1.0	69.4	11.2
ADC12L030/2/4/8	12	-	8.8 µs	+5	15	±0.5	±1.0	69.4	11.2
ADC12130/2/8	12	-	8.8 µs	+5	33	±0.5	±1.0	69.4	11.2
ADC1241	12	-	13.8	5	70	±0.5	-	-	-
CLC5958	14	52	-	+5	1,330	±1.5	±0.3	69	11.2
ADC14071	14	7	-	5	380	±2.2	±1.0	78	12.7
ADC14061	14	2.5	-	+5	390	±0.75	±0.3	79	12.8
ADC14161	14	2.5	-	+5	390	±0.75	±0.3	79	12.8
ADC16061	16	2.5	-	+5	390	±0.3	±1.0	79	12.8

National Semiconductor

D/A Converter Selection Guide

Device	Resolution (Bits)	Linearity (%)	Settling Time (½ LSB)	Supply Voltages (V)	Power Consumption (mW, typ)
DAC0800/1/2	8	0.19	100 ns	±5 to ±15	33
DAC0806/7/8	8	0.78/0.39/0.19	100 ns	±5 to ±15	33
DAC0830/1/2	8	0.05/0.1/0.2	1 μs	±5 to ±15	20

National Semiconductor

Data Acquisition System Selection Guide

Device	Reso-lution (Bits)	Maximum Clock Freq (MHz)	Through-put Rate (ksps, min)	Supply Voltage (V)	Power Con-sumption (mW, max)	INL (LSB, max)	DNL (LSB, max)	Difer-ential SINAD (dB, typ)	ENOB (Bits, typ)
LM12454	12 + Sign	5	88	+5	30	±1.0	±0.75	76	12.3
LM12458	12 + Sign	5	88	+5	30	±1.0	±0.75	76	12.3
LM12H458	12 + Sign	8	140	+5	34	±1.0	±0.75	76	12.3
LM12L458	12 + Sign	6	106	+3V to +5V	15	±1.0	±1.0	76	12.3

National Semiconductor

A/D Converter Definition Of Terms

APERTURE DELAY See Sampling Delay.

APERTURE JITTER is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

BOTTOM OFFSET is the difference between the input voltage that just causes the output code to transition to the first code and the negative reference voltage. Bottom Offset is defined as $E_{OB} = V_{ZT} - V_{RB}$, where V_{ZT} is the first code transition input voltage and V_{RB} is the lower reference voltage. Note that this is different from the normal Offset Error.

CLOCK DUTY CYCLE is the ratio of the time that the clock waveform is high to the total time for one clock cycle.

COMMON MODE VOLTAGE (V_{CM}) is the d.c. input voltage that is common to both pins of a differential input.

CONVERSION LATENCY See PIPELINE DELAY.

CONVERSION TIME is the time required for a complete measurement by an analog-to-digital converter. Since the Conversion Time does not include acquisition time, multiplexer set up time, or other elements of a complete conversion cycle, the conversion time may be less than the Throughput Time.

DC COMMON-MODE ERROR is a specification which applies to ADCs with differential inputs. It is the change in the output code that occurs when the analog voltages on the two inputs are changed by an equal amount. It is usually expressed in LSBs.

DIFFERENTIAL GAIN ERROR is the percentage difference between the output amplitudes of a specified small signal, high frequency sine wave input at two different dc input levels.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB. DNL is commonly measured at the rated clock frequency with a ramp input.

DIFFERENTIAL PHASE ERROR is the difference in the output phase of a reconstructed small signal sine wave at two different dc input levels.

DYNAMIC SPECIFICATIONS of an ADC are those pertaining to an AC input signal. These include S/N ratio (SNR), SINAD (S/(N+D)), ENOB, THD, IMD, FPBW, and SSBW.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD - 1.76)/6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

FULL SCALE (FS) INPUT RANGE of the ADC is the input range of voltages over which the ADC will digitize that input without going underrange or overrange. For $V_{REF^+} = 3.5V$ and $V_{REF^-} = 1.5V$, $FS = (V_{REF^+}) - (V_{REF^-}) = 2.0V$.

FULL SCALE ERROR is a measure of how far the last code transition is from the ideal 1½ LSB below V_{REF^+} and is defined as:

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF^+}$$

where V_{max} is the voltage at which the transition to the max code occurs and can be expressed in Volts, LSB or percent of ful scale range.

FULL SCALE STEP RESPONSE is defined as the time required after V_{IN} goes from V_{REF^-} to V_{REF^+}, or V_{REF^+} to V_{REF^-}, and settles sufficiently for the converter to recover and make a conversion with its rated accuracy.

GAIN ERROR is the difference between the ideal and actual differences between the input levels at which the first and last code transitions occur. That is, how far this difference is from full scale - 2LSB.

GAIN TEMPERATURE COEFFICIENT (FULL SCALE TEMPERATURE COEFFICIENT) is the change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

INTEGRAL NON-LINEARITY (INL) is a measure of the maximum deviation of each individual code from a line drawn from zero scale or negative full scale (½ LSB below the first code transition) through positive full scale (1½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. INL is commonly measured at rated clock frequency with a ramp input.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components that are not present at the input as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the intermodulation products to the total power in one of the original frequencies. IMD is usually expressed in dB.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is $m^*V_{REF}/2^n$ where 'm' is the reference scale factor (which is most often unity) and 'n' is the ADC resolution.

MISSING CODES are those output codes that are skipped or will never appear at the ADC outputs. These codes cannot be reached by any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

OFFSET ERROR of an offset binary ADC is a measure of how far the mid-scale transition point is from the ideal zero voltage input.

OUTPUT DELAY is the time delay after the edge of the input clock before the data update is present at the output pins.

OUTPUT HOLD TIME is the length of time that the output data is valid after the edge of the input clock.

OVERRANGE RECOVERY TIME is the time required after V_{IN} goes from a specified voltage out of the normal input range to a specified voltage within the normal input range and the converter makes a conversion with its rated accuracy.

PIPELINE DELAY (LATENCY) is the number of clock cycles between initiation of conversion and when that data is pre-

sented to the output driver stage. Data for any given sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the acquisition by the Pipeline Delay plus the Output Delay.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. DC PSRR is the ratio of the change in a specified parameter (e.g., Full Scale Error) that results from a specified change in the power supply voltage. AC PSRR is measured with a signal of specified frequency and amplitude riding upon the power suply and is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is usually specified in dB.

QUANTIZATION ERROR is the error inherent in all A/D conversions. Since even an 'ideal' converter has finite resolution, any analog voltage that falls beween two adjacent output codes will result in an output code that is inaccurate by up to ½ LSB. This is the quantization Error

RATIOMETRIC OPERATION uses the reference voltage that is used for the ADC to drive the signal source such that the ratio of the output of that signal source to the reference is a constant. When the driving voltage for that source is also used as the voltage reference for the ADC, the ADC output code is a function of the ratio of the signal source output to the reference voltage and, for a limited reference voltage range, the ADC output code is independent of the value of that reference voltage.

RESOLUTION is the analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of digital codes is equal to 2^n, where "n" is the number of bits. As an example, a 12-bit converter maps the analog signal into 2^{12} = 4096 digital codes.

SAMPLING (APERTURE) DELAY is that time required after the edge of the clock input for the sampling switch to open. The Sample/Hold circuit effectively stops capturing the input signal and goes into the 'hold' mode the sampling delay after the specified clock.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or dc.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding dc.

SMALL SIGNAL BANDWIDTH (SSBW) is the frequency at which a specified amplitude input signal drops a specified anout below the output level of a specified, low frequency signal of the same input amplitude.

SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal. where a spurious signal is any signal present in the output spectrum that is not present at the input.

STATIC SPECIFICATIONS are the specifications of an ADC pertaining to a DC signal input. These include gain error, offset error, and differential and integral linearity errors.

THROUGHPUT RATE is the maximun continuous conversion rate of the ADC.

THROUGHPUT TIME is the time it takes a converter to do a single conversion. Throuput time includes any multiplexer settling time, acquisition time, conersion time, and output presentation time.

TOP OFFSET is the difference between the positive reference voltage and the input voltage that just causes the output code to transition to full scale and is defined as $E_{OT} = V_{FT} - V_{REF+}$ where V_{FT} is the full scale transition input voltage. Note that this is different from the normal Full Scale Error.

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBc, of the total of the first six harmonic levels to the level of the input signal at the output. THD is caluclated as

$$THD = \sqrt{\frac{f_2^2 + f_3^2 + f_4^2 + f_5^2 + f_6^2 + f_7^2}{f_1^2}}$$

where f_1 is the fundamental (input) frequency and f_2 through f_7 are the first 6 harmonic frequencies.

TOTAL UNADJUSTED ERROR (TUE) is the maximum deviation of the voltage corresponding to the center of a digital code's associated input voltage span from the ideal case. Total unadjusted error includes offset error, Gain error, and differential and integral nonlinearity errors.

ZERO SCALE OFFSET ERROR is the difference between the ideal input voltage (½ LSB) and the actual input voltage that just causes a transition from an output code of zero to an output code of one.

ZERO ERROR see Zero Scale Offset Error

National Semiconductor

D/A Converters Definition Of Terms

Differential Nonlinearity: Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step. For example, a DAC with a 1.5 LSB output change for a 1 LSB digital code change exhibits ½ LSB differential non-linearity. Differential non-linearity may be expressed in fractional bits or as a percentage of full scale. A differential non-linearity greater than 1 LSB will lead to a non-monotonic transfer function in a DAC.

Gain Error (Full Scale Error): The difference between the output voltage (or current) with full scale input code and the ideal voltage (or current) that should exist with a full scale input code.

Gain Temperature Coefficient (Full Scale Temperature Coefficient): Change in gain error divided by change in temperature. Usually expressed in parts per million per degree Celsius (ppm/°C).

Integral Nonlinearity (Linearity Error): Worst case deviation from the line between the endpoints (zero and full scale). Can be expressed as a percentage of full scale or in fraction of an LSB.

LSB (Lease-Significant Bit): In a binary coded system this is the bit that carries the smallest value or weight. Its value is the full scale voltage (or current) divided by 2^n, where n is the resolution of the converter.

Monotonicity: A monotonic function has a slope whose sign does not change. A monotonic DAC has an output that changes in the same direction (or remains constant) for each increase in the input code. the converse is true for decreasing codes.

MSB (Most Significant Bit): In a binary coded system this is the bit that has the largest value or weight. Its value is one half of full scale.

Multiplying DAC: In a sense, every DAC is a multiplying DAC since the output voltage (or current) is equal to the reference voltage times a constant determined by the digital input code divided by 2^n (n is the number of bits of resolution). In a two quadrant multiplying DAC the reference voltage or the digital input code can change the output voltage polarity. If both the reference voltage and the digital code change the output voltage polarity, four quadrant multiplication exists.

Offset Error (Zero Error): The output voltage that exists when the input digital code is set to give an ideal output of zero volts. All the digital codes in the transfer curve are offset by the same value. Offset error is usually expressed in LSBs.

Power supply Rejection (Power Supply Sensitivity): The sensitivity of a converter to changes in the dc power supply voltages.

Resolution: the smallest analog increment corresponding to a 1 LSB converter code change. For converters, resolution is normally expressed in bits, where the number of analog levels is equal to 2^n.

Settling Time: The time from a change in input code until a DAC's output signal remains within ±½ LSB (or some other specified tolerance) of the final value.

National Semiconductor

ADC0801/ADC0802/ADC0803/ADC0804/ADC0805 8-Bit µP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

Features

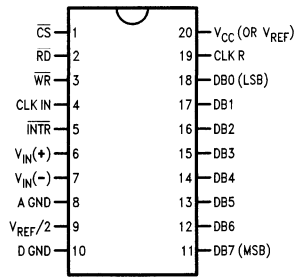
- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

- Resolution 8 bits
- Total error ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time 100 µs

Connection Diagram

ADC080X
Dual-In-Line and Small Outline (SO) Packages

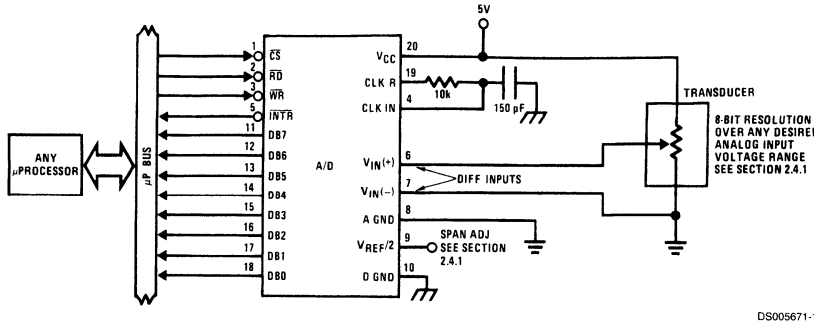


See Ordering Information

Ordering Information

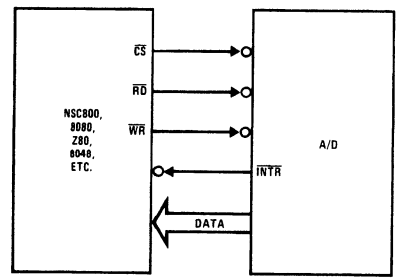
TEMP RANGE		0°C TO 70°C	0°C TO 70°C	−40°C TO +85°C
ERROR	±¼ Bit Adjusted			ADC0801LCN
	±½ Bit Unadjusted	ADC0802LCWM		ADC0802LCN
	±½ Bit Adjusted			ADC0803LCN
	±1Bit Unadjusted	ADC0804LCWM	ADC0804LCN	ADC0805LCN/ADC0804LCJ
PACKAGE OUTLINE		M20B—Small Outline	N20A—Molded DIP	

Typical Applications



DS005671-1

8080 Interface



DS005671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	**Full-Scale Adjusted**	**$V_{REF}/2$=2.500 V_{DC} (No Adjustments)**	**$V_{REF}/2$=No Connection (No Adjustments)**
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

National Semiconductor

ADC08031/ADC08032/ADC08034/ADC08038 8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

General Description

The ADC08031/ADC08032/ADC08034/ADC08038 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

The ADC08034 and ADC08038 provide a 2.6V band-gap derived reference. For devices offering guaranteed voltage reference performance over temperature see ADC08131, ADC08134 and ADC08138.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Applications

- Digitizing automotive sensors
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Test systems
- Embedded diagnostics

Features

- Serial digital data link requires few I/O pins
- Analog input track/hold function
- 2-, 4-, or 8-channel input multiplexer options with address logic
- 0V to 5V analog input range with single 5V power supply
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- On chip 2.6V band-gap reference
- 0.3" standard width 8-, 14-, or 20-pin DIP package
- 14-, 20-pin small-outline packages

Key Specifications

- Resolution: 8 bits
- Conversion time (f_C = 1 MHz): 8μs (max)
- Power dissipation: 20mW (max)
- Single supply: $5V_{DC}$ (±5%)
- Total unadjusted error: ±½ LSB and ±1LSB
- No missing codes over temperature

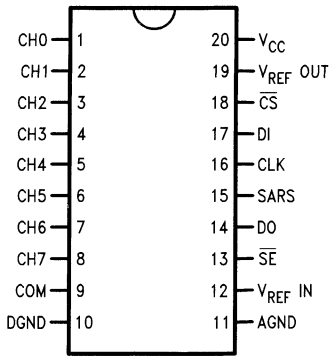
Ordering Information

Industrial ($-40^\circ C \leq T_A \leq +85^\circ C$)	Package
ADC08031CIN*	N08E
ADC08038CIN*	N20A
ADC08031CIWM, ADC08032CIWM, ADC08034CIWM	M14B
ADC08038CIWM	M20B

*Not recomended for new designs.

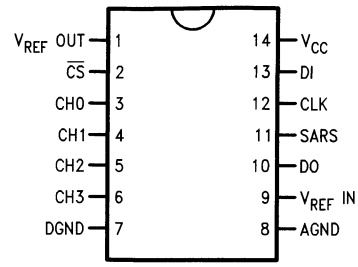
Connection Diagrams

ADC08038



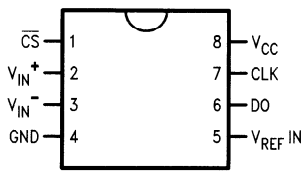
DS010555-2

ADC08034



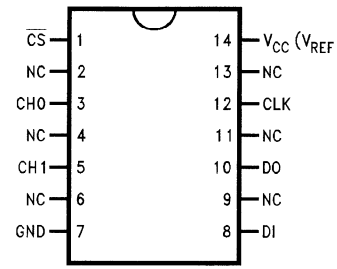
DS010555-3

ADC08031
Dual-In-Line Package



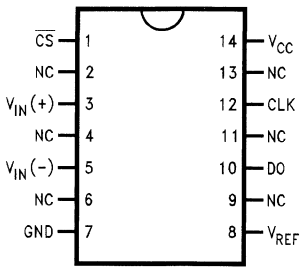
DS010555-5

ADC08032
Small Outline Package



DS010555-30

ADC08031
Small Outline Package



DS010555-31

National Semiconductor

ADC08060
8-Bit, 20 MSPS to 60 MSPS, 1.3 mW/MSPS A/D Converter

General Description

The ADC08060 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 20 MSPS to 70 MSPS with outstanding dynamic performance over its full operating range while consuming just 1.3 mW per MHz of clock frequency. That's just 78 mW of power at 60 MSPS. Raising the PD pin puts the ADC08060 into a Power Down mode where it consumes just 1 mW.

The unique architecture achieves 7.5 Effective Bits with 25 MHz input frequency. The excellent DC and AC characteristics of this device, together with its low power consumption and single +3V supply operation, make it ideally suited for many imaging and communications applications, including use in portable equipment. Furthermore, the ADC08060 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08060's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The digital inputs (CLK and PD) are TTL/CMOS compatible.

The ADC08060 is offered in a 24-lead plastic package (TSSOP) and is specified over the industrial temperature range of −40°C to +85°C.

Features

- Single-ended input
- Internal sample-and-hold function
- Low voltage (single +3V) operation
- Small package
- Power-down feature

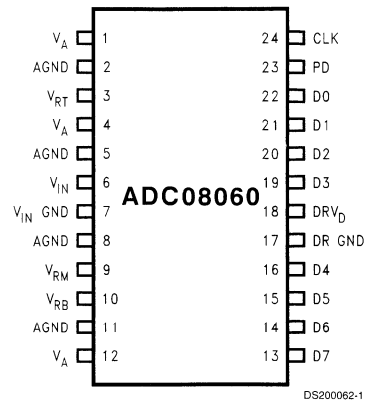
Key Specifications

- Resolution — 8 bits
- Maximum sampling frequency — 60 MSPS (min)
- DNL — 0.4 LSB (typ)
- ENOB — 7.5 bits (typ) at f_{IN} = 25 MHz
- THD — −60 dB (typ)
- Guaranteed no missing codes
- Power consumption
  - — Operating: 1.3 mW/MSPS (typ)
  - — Power down: 1 mW (typ)

Applications

- Digital imaging systems
- Communication systems
- Portable instrumentation
- Viterbi decoders
- Set-top boxes

Pin Configuration

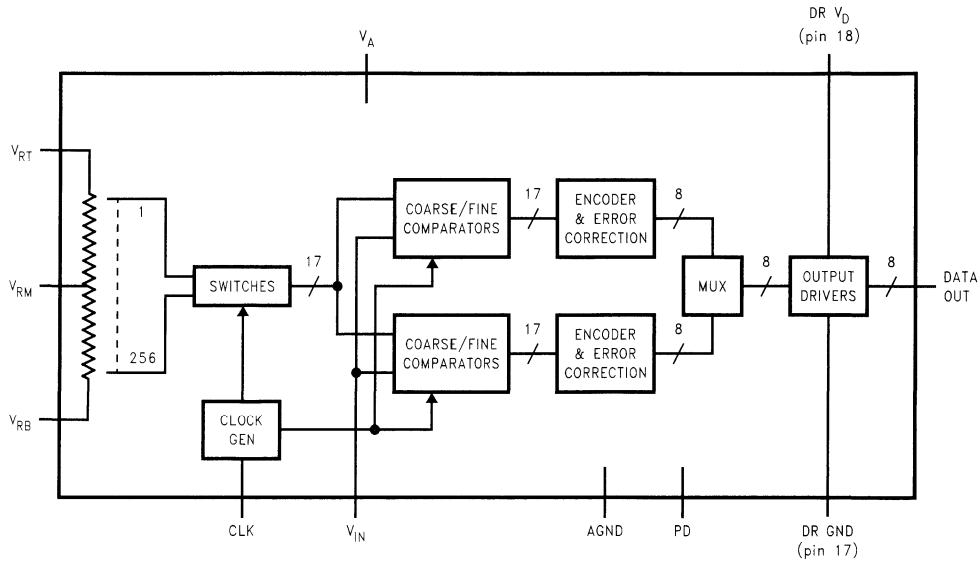


DS200062-1

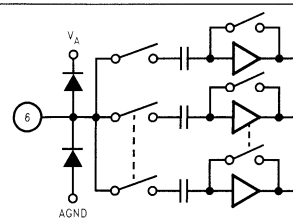
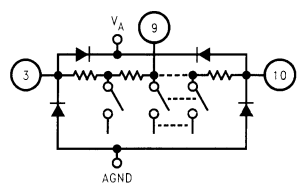
Ordering Information

ADC08060CIMT	TSSOP
ADC08060CIMTX	TSSOP (tape and reel)

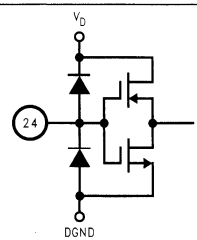
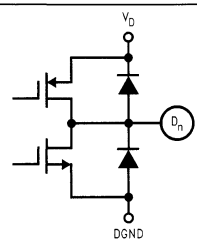
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a clean, quiet point in the analog ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} – 1.0V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See Section 3.0 for more information.
18	DR V_D		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

National Semiconductor

ADC08061/ADC08062
500 ns A/D Converter with S/H Function and Input Multiplexer

General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08061 and ADC08062 CMOS ADCs offer 500 ns (typ) conversion time, internal sample-and-hold (S/H), and dissipate only 125 mW of power. The ADC08062 has a two-channel multiplexer. The ADC08061/2 family performs an 8-bit conversion using a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LSBs.

Input track-and-hold circuitry eliminates the need for an external sample-and-hold. The ADC08061/2 family performs accurate conversions of full-scale input signals that have a frequency range of DC to 300 kHz (full-power bandwidth) without need of an external S/H.

The digital interface has been designed to ease connection to microprocessors and allows the parts to be I/O or memory mapped.

Key Specifications

■ Resolution	8 bits
■ Conversion Time	560 ns max ($\overline{WR}$-$\overline{RD}$ Mode)
■ **Full Power Bandwidth**	**300 kHz**
■ Throughput rate	1.5 MHz
■ Power Dissipation	100 mW max
■ Total Unadjusted Error	±½ LSB and ±1 LSB

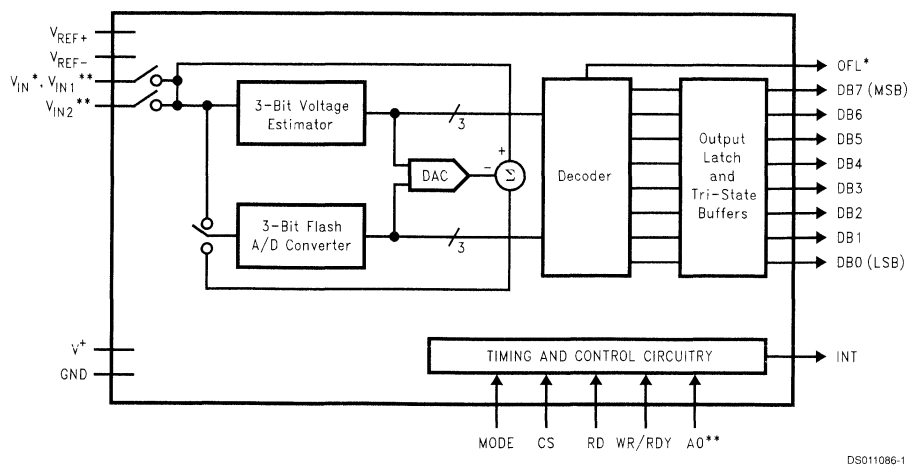
Features

- 1 or 2 input channels
- No external clock required
- Analog input voltage range from GND to V^+
- Overflow output available for cascading (ADC08061)
- ADC08061 pin-compatible with the industry standard ADC0820

Applications

- Mobile telecommunications
- Hard disk drives
- Instrumentation
- High-speed data acquisition systems

Block Diagram



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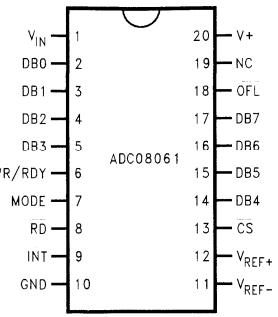
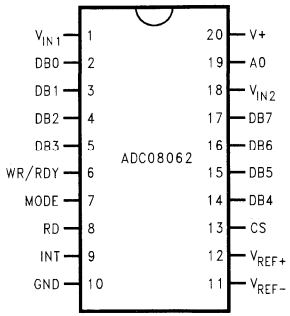
* ADC08061
** ADC08062

Connection Diagrams



Dual-In-Line and Wide-Body Small-Outline Packages N20A or M20B



Dual-In-Line and Wide-Body Small-Outline Packages N20A or M20B

Ordering Information

Industrial ($-40^\circ C \le T_A \le 85^\circ C$)	Package
ADC08061BIN, ADC08062BIN	N20A
ADC08061CIWM, ADC08062CIWM	M20B

Pin Description

V_{IN}, V_{IN1-8} These are analog inputs. The input range is GND−50 mV ≤ V_{INPUT} ≤ V^+ + 50 mV. The ADC08061 has a single input (V_{IN}) and the ADC08062 has a two-channel multiplexer (V_{IN1-2}).

DB0–DB7 TRI-STATE data outputs—bit 0 (LSB) through bit 7 (MSB).

$\overline{WR}$ /RDY **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)

$\overline{WR}$: With $\overline{CS}$ low, the conversion is started on the falling edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (see *Figures 2, 3, 4*).

: **$\overline{RD}$ Mode** (Logic low applied to MODE pin)

RDY: This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and return high at the end of conversion.

MODE **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input—This pin is pulled to a logic low through an internal 50 µA current sink when left unconnected.

$\overline{RD}$ Mode is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.

$\overline{WR}$-$\overline{RD}$ Mode is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.

$\overline{RD}$ **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin) This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (logic low on the MODE pin)

With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion(see *Figures 1, 5*).

$\overline{INT}$ This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.

GND This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.

V_{REF-}, V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} − 1.5 LSB produces an output code of 255.

For the ADC08062, an input voltage on any unselected input that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create errors in a selected channel that is operating within proper operating conditions.

$\overline{CS}$ This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.

$\overline{OFL}$ Overflow Output. If the analog input is higher than V_{REF+} − ½ LSB, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08061s to achieve higher resolution

Pin Description (Continued)

(9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.

NC No connection.

A0 This logic input is used to select one of the ADC08062's input multiplexer channels. A channel is selected as shown in the table below.

ADC08062 A0	Channel
0	V_{IN1}
1	V_{IN2}

V^+ Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 µF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

National Semiconductor

ADC0808/ADC0809
8-Bit µP Compatible A/D Converters with 8-Channel Multiplexer

General Description

The ADC0808, ADC0809 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any of 8-single-ended analog signals.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet. (See AN-247 for more information.)

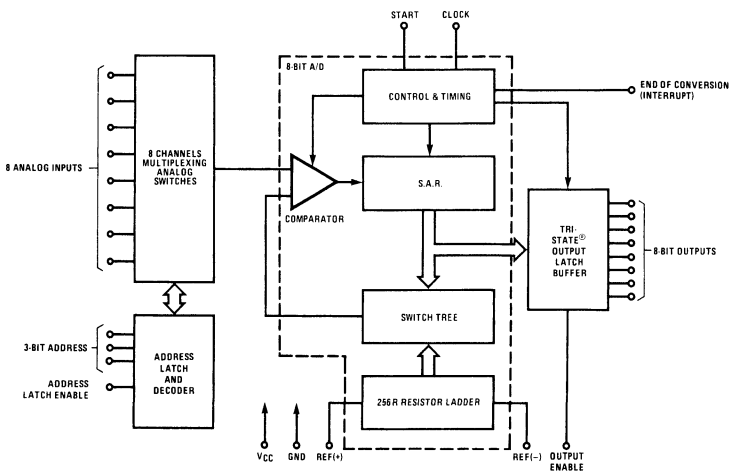
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- No zero or full-scale adjust required
- 8-channel multiplexer with address logic
- 0V to 5V input range with single 5V power supply
- Outputs meet TTL voltage level specifications
- Standard hermetic or molded 28-pin DIP package
- 28-pin molded chip carrier package
- ADC0808 equivalent to MM74C949
- ADC0809 equivalent to MM74C949-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

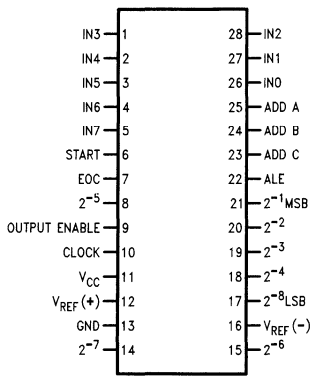
Block Diagram



See Ordering Information

Connection Diagrams

Dual-In-Line Package



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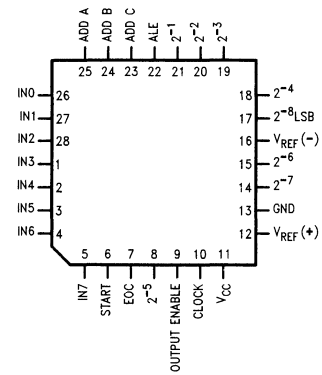
Order Number ADC0808CCN or ADC0809CCN
See NS Package J28A or N28A

Molded Chip Carrier Package



DS005672-12

Order Number ADC0808CCV or ADC0809CCV
See NS Package V28A

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C			−55°C to +125°C
Error	±½ LSB Unadjusted	ADC0808CCN	ADC0808CCV	ADC0808CCJ	ADC0808CJ
	±1 LSB Unadjusted	ADC0809CCN	ADC0809CCV		
Package Outline		N28A Molded DIP	V28A Molded Chip Carrier	J28A Ceramic DIP	J28A Ceramic DIP

National Semiconductor

ADC08100
8-Bit, 20 MSPS to 100 MSPS, 1.3 mW/MSPS A/D Converter

General Description

The ADC08100 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates of 20 MSPS to 100 MSPS with outstanding dynamic performance over its full operating range while consuming just 1.3 mW per MHz of clock frequency. That's just 130 mW of power at 100 MSPS. Raising the PD pin puts the ADC08100 into a Power Down mode where it consumes just 1 mW.

The unique architecture achieves 7.4 Effective Bits with 41 MHz input frequency. The excellent DC and AC characteristics of this device, together with its low power consumption and single +3V supply operation, make it ideally suited for many imaging and communications applications, including use in portable equipment. Furthermore, the ADC08100 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08100's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The digital inputs (CLK and PD) are TTL/CMOS compatible.

The ADC08100 is offered in a 24-lead plastic package (TSSOP) and is specified over the industrial temperature range of −40°C to +85°C.

Features

- Single-ended input
- Internal sample-and-hold function
- Low voltage (single +3V) operation
- Small package
- Power-down feature

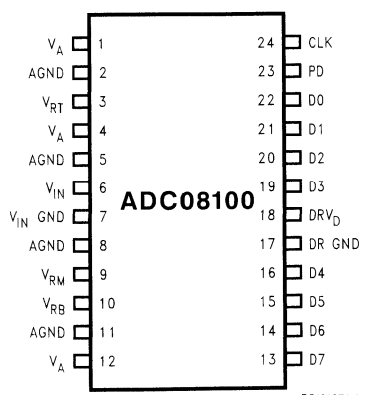
Key Specifications

- Resolution 8 bits
- Maximum sampling frequency 100 MSPS (min)
- DNL 0.4 LSB (typ)
- ENOB 7.4 bits (typ) at f_{IN} = 41 MHz
- THD −60 dB (typ)
- Guaranteed no missing codes
- Power consumption
  - — Operating: 1.3 mW/MSPS (typ)
  - — Power down: 1 mW (typ)

Applications

- Flat panel displays
- Projection systems
- Set-top boxes
- Battery-powered instruments
- Communications
- Medical scan converters
- X-ray imaging
- High speed viterbi decoders
- Astronomy

Pin Configuration

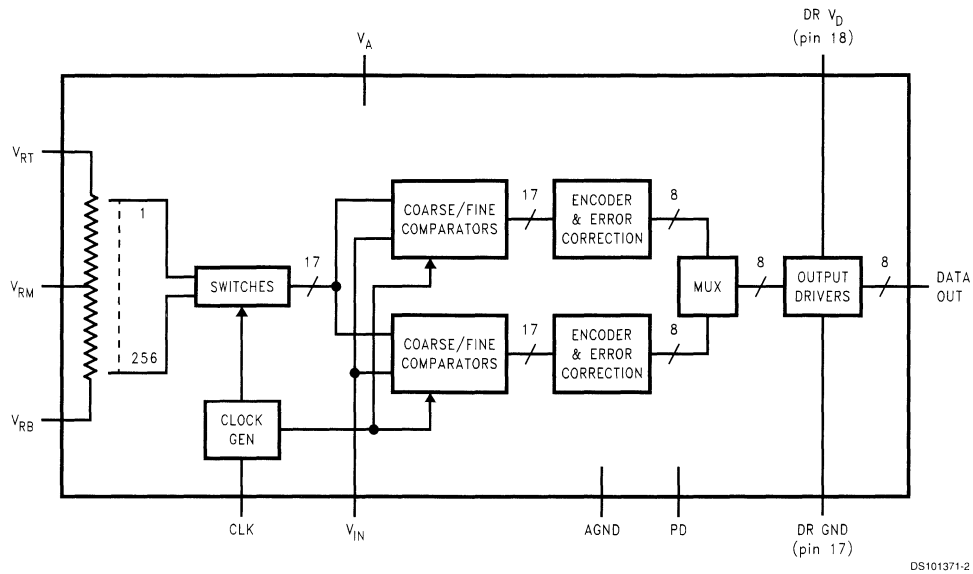


DS101371-1

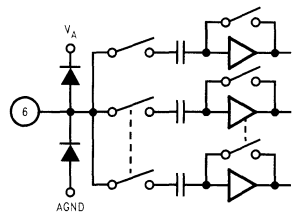
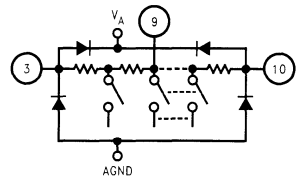
Ordering Information

ADC08100CIMT	TSSOP
ADC08100CIMTX	TSSOP (tape and reel)

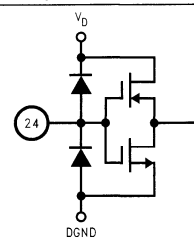
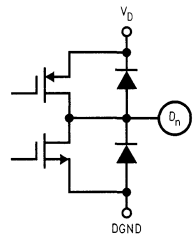
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a clean, quiet point in the analog ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} − 1.0V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See Section 3.0 for more information.
18	DR V_D		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

National Semiconductor

ADC08131/ADC08134/ADC08138
8-Bit High-Speed Serial I/O A/D Converters with Multiplexer Options, Voltage Reference, and Track/Hold Function

General Description

The ADC08131/ADC08134/ADC08138 are 8-bit successive approximation A/D converters with serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of controllers, and can easily interface with standard shift registers or microprocessors.

All three devices provide a 2.5V band-gap derived reference with guaranteed performance over temperature.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. In addition, input voltage spans as small as 1V can be accommodated.

Applications

- Digitizing automotive sensors
- Process control/monitoring
- Remote sensing in noisy environments
- Embedded diagnostics

Features

- Serial digital data link requires few I/O pins
- Analog input track/hold function
- 4- or 8-channel input multiplexer options with address logic
- On-chip 2.5V band-gap reference (±2% over temperature guaranteed)
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- 0V to 5V analog input range with single 5V power supply

Key Specifications

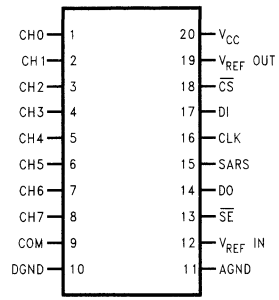
- Resolution — 8 Bits
- Conversion time (f_C = 1 MHz) — 8 µs (Max)
- Power dissipation — 20 mW (Max)
- Single supply — 5 V_{DC} (±5%)
- Total unadjusted error — ±½ LSB and ±1 LSB
- Linearity Error (V_{REF} = 2.5V) — ±½ LSB
- No missing codes (over temperature)
- On-board Reference — +2.5V ±1.5% (Max)

Ordering Information

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC08131CIWM	M14B
ADC08134CIWM	M14B
ADC08138CIWM	M20B

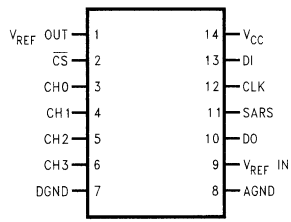
Connection Diagrams

ADC08138CIWM
Small Outline
Packages



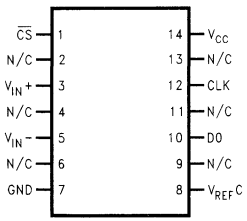
DS010749-2

ADC08134CIWM
Small Outline
Packages



DS010749-3

ADC08131CIWM
Small Outline Package



DS010749-4

National Semiconductor

ADC0816/ADC0817
8-Bit µP Compatible A/D Converters with 16-Channel Multiplexer

General Description

The ADC0816, ADC0817 data acquisition component is a monolithic CMOS device with an 8-bit analog-to-digital converter, 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16-single-ended analog signals, and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the multiplexer output, and to the input of the 8-bit A/D converter.

The device eliminates the need for external zero and full-scale adjustments. Easy interfacing to microprocessors is provided by the latched and decoded multiplexer address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications from process and machine control to consumer and automotive applications. For similar performance in an 8-channel, 28-pin, 8-bit A/D converter, see the ADC0808, ADC0809 data sheet. (See AN-258 for more information.)

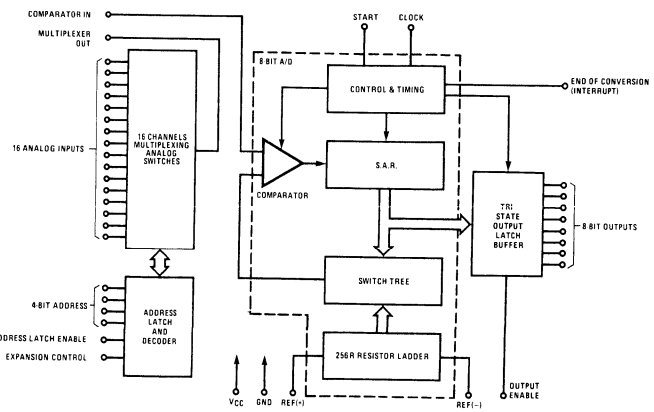
Features

- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} or analog span adjusted voltage reference
- 16-channel multiplexer with latched control logic
- Outputs meet TTL voltage level specifications
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Standard hermetic or molded 40-pin DIP package
- Temperature range −40°C to +85°C or −55°C to +125°C
- Latched TRI-STATE output
- Direct access to "comparator in" and "multiplexer out" for signal conditioning
- ADC0816 equivalent to MM74C948
- ADC0817 equivalent to MM74C948-1

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	100 µs

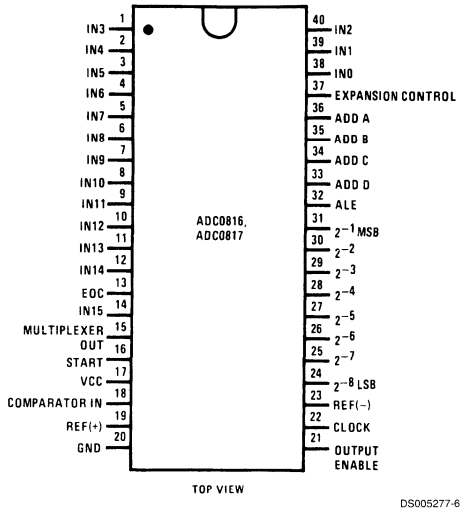
Block Diagram



DS005277-1

Connection Diagram

Dual-In-Line Package



Order Number ADC0816CCN or ADC0817CCN
See NS Package Number N40A

Ordering Information

TEMPERATURE RANGE		−40°C to +85°C	
Error	±½ Bit Unadjusted	ADC0816CCN	ADC0816CCJ
	±1 Bit Unadjusted	ADC0817CCN	
Package Outline		N40A Molded DIP	J40A Hermetic DIP

National Semiconductor

ADC08161
500 ns A/D Converter with S/H Function and 2.5V Bandgap Reference

General Description

Using a patented multi-step A/D conversion technique, the 8-bit ADC08161 CMOS A/D converter offers 500 ns conversion time, internal sample-and-hold (S/H), a 2.5V bandgap reference, and dissipates only 100 mW of power. The ADC08161 performs an 8-bit conversion with a 2-bit voltage estimator that generates the 2 MSBs and two low-resolution (3-bit) flashes that generate the 6 LBSs.

Input signals are tracked and held by the input sampling circuitry, eliminating the need for an external sample-and-hold. The ADC08161 can perform accurate conversions of full-scale input signals at frequencies from DC to typically more than 300 kHz (full power bandwidth) without the need of an external sample-and-hold (S/H).

For ease of interface to microprocessors, this part has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

■ Resolution	8 Bits
■ Conversion time (t_{CONV})	560 ns max ($\overline{WR}$-$\overline{RD}$ Mode)
■ Full power bandwidth	300 kHz (typ)
■ Throughput rate	1.5 MHz min
■ Power dissipation	100 mW max
■ Total unadjusted error	±½ LSB and ±1 LSB max

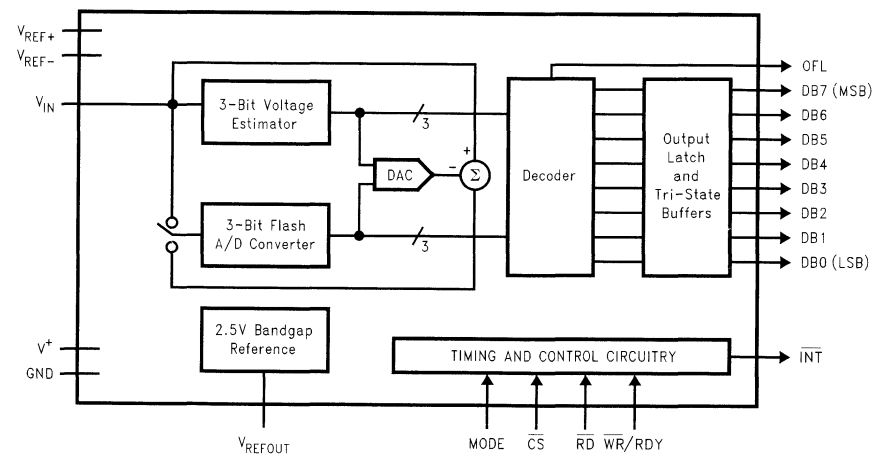
Features

- No external clock required
- Analog input voltage range from GND to V^+
- 2.5V bandgap reference

Applications

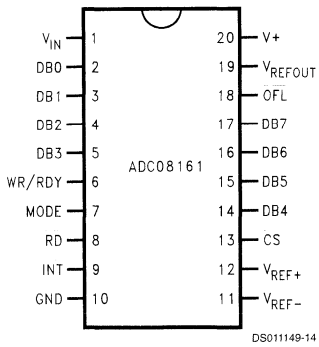
- Mobile telecommunications
- Hard-disk drives
- Instrumentation
- High-speed data acquisition systems

Block Diagram



Connection Diagram

Wide-Body Small-Outline Package



See NS Package Number M20B

Ordering Information

Industrial ($-40^\circ C \le T_A \le 85^\circ C$)	Package
ADC08161CIWM	M20B

Pin Description

V_{IN} This is the analog input. The input range is GND−50 mV ≤ V_{INPUT} ≤ V^+ + 50 mV.

DB0–DB7 TRI-STATE data outputs—bit 0 (LSB) through bit 7 (MSB).

$\overline{WR}$ /RDY **$\overline{WR}$-$\overline{RD}$ Mode** (Logic high applied to MODE pin)

$\overline{WR}$: With $\overline{CS}$ low, the conversion is started on the rising edge of $\overline{WR}$. The digital result will be strobed into the output latch at the end of conversion (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (Logic low applied to MODE pin)

RDY: This is an open drain output (no internal pull-up device). RDY will go low after the falling edge of $\overline{CS}$ and returns high at the end of conversion.

MODE **Mode:** Mode (**$\overline{RD}$ or $\overline{WR}$-$\overline{RD}$**) selection input– This pin is pulled to a logic low through an internal 50 µA current sink when left unconnected.

$\overline{RD}$ Mode is selected if the MODE pin is left unconnected or externally forced low. A complete conversion is accomplished by pulling $\overline{RD}$ low until output data appears.

$\overline{WR}$-$\overline{RD}$ Mode is selected when a high is applied to the MODE pin. A conversion starts with the $\overline{WR}$ signal's rising edge and then using $\overline{RD}$ to access the data.

$\overline{RD}$ **$\overline{WR}$-$\overline{RD}$ Mode** (logic high on the MODE pin)

This is the active low Read input. With a logic low applied to the $\overline{CS}$ pin, the TRI-STATE data outputs (DB0–DB7) will be activated when $\overline{RD}$ goes low (*Figures 2, 3, 4*).

$\overline{RD}$ Mode (logic low on the MODE pin)

With $\overline{CS}$ low, a conversion starts on the falling edge of $\overline{RD}$. Output data appears on DB0–DB7 at the end of conversion (*Figures 1, 5*).

$\overline{INT}$ This is an active low output that indicates that a conversion is complete and the data is in the output latch. $\overline{INT}$ is reset by the rising edge of $\overline{RD}$.

GND This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.

V_{REF-}, V_{REF+} These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V^+ + 50 mV, but V_{REF+} must be greater than V_{REF-}. Ideally, an input voltage equal to V_{REF-} produces an output code of 0, and an input voltage greater than V_{REF+} − 1.5 LSB produces an output code of 255.

For the ADC08161 an input voltage that exceeds V^+ by more than 100 mV or is below GND by more than 100 mV will create conversion errors.

$\overline{CS}$ This is the active low Chip Select input. A logic low signal applied to this input pin enables the $\overline{RD}$ and $\overline{WR}$ inputs. Internally, the $\overline{CS}$ signal is ORed with $\overline{RD}$ and $\overline{WR}$ signals.

$\overline{OFL}$ Overflow Output. If the analog input is higher than V_{REF+}, $\overline{OFL}$ will be low at the end of conversion. It can be used when cascading two ADC08161s to achieve higher resolution (9 bits). This output is always active and does not go into TRI-STATE as DB0–DB7 do. When $\overline{OFL}$ is set, all data outputs remain high when the ADC08061's output data is read.

V^+ Positive power supply voltage input. Nominal operating supply voltage is +5V. The supply pin should be bypassed with a 10 µF bead tantalum in parallel with a 0.1 ceramic capacitor. Lead length should be as short as possible.

V_{REFOUT} The internal bandgap reference's 2.5V output is available on this pin. Use a 220 µF bypass capacitor between this pin and analog ground.

6

National Semiconductor

ADC0820
8-Bit High Speed µP Compatible A/D Converter with Track/Hold Function

General Description

By using a half-flash conversion technique, the 8-bit ADC0820 CMOS A/D offers a 1.5 µs conversion time and dissipates only 75 mW of power. The half-flash technique consists of 32 comparators, a most significant 4-bit ADC and a least significant 4-bit ADC.

The input to the ADC0820 is tracked and held by the input sampling circuitry eliminating the need for an external sample-and-hold for signals moving at less than 100 mV/µs.

For ease of interface to microprocessors, the ADC0820 has been designed to appear as a memory location or I/O port without the need for external interfacing logic.

Key Specifications

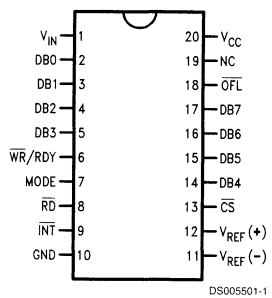
■ Resolution	8 Bits
■ Conversion Time	2.5 µs Max (RD Mode)
	1.5 µs Max (WR-RD Mode)
■ Low Power	75 mW Max
■ Total Unadjusted Error	±½ LSB and ± 1 LSB

Features

- Built-in track-and-hold function
- No missing codes
- No external clocking
- Single supply—5 V_{DC}
- Easy interface to all microprocessors, or operates stand-alone
- Latched STRI-STATE output
- Logic inputs and outputs meet both MOS and T^2L voltage level specifications
- Operates ratiometrically or with any reference value equal to or less than V_{CC}
- 0V to 5V analog input voltage range with single 5V supply
- No zero or full-scale adjust required
- Overflow output available for cascading
- 0.3" standard width 20-pin DIP
- 20-pin molded chip carrier package
- 20-pin small outline package
- 20-pin shrink small outline package (SSOP)

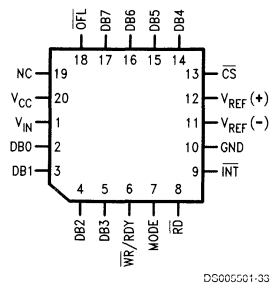
Connection and Functional Diagrams

Dual-In-Line, Small Outline and SSOP Packages



Top View

Molded Chip Carrier Package



Connection and Functional Diagrams (Continued)

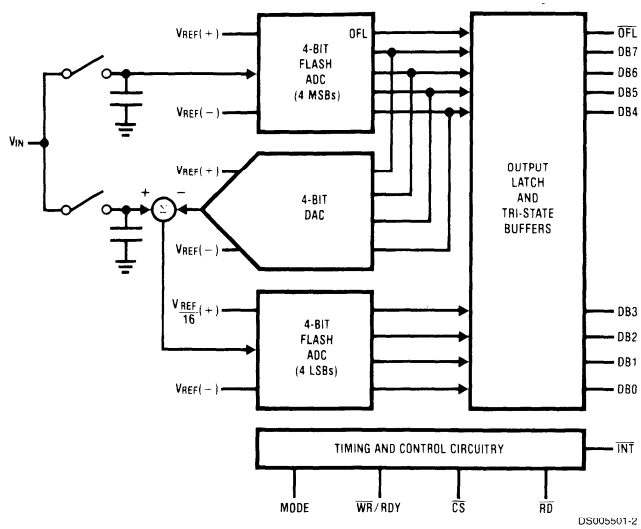


FIGURE 1.

Ordering Information

Part Number	Total Unadjusted Error	Package	Temperature Range
ADC0820BCV	±½ LSB	V20A—Molded Chip Carrier	0°C to +70°C
ADC0820BCWM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820BCN		N20A—Molded DIP	0°C to +70°C
ADC0820CCJ	±1 LSB	J20A—Cerdip	−40°C to +85°C
ADC0820CCWM		M20B—Wide Body Small Outline	0°C to +70°C
ADC0820CIWM		M20B—Wide Body Small Outline	−40°C to +85°C
ADC0820CCN		N20A—Molded DIP	0°C to +70°C

National Semiconductor

ADC08200
8-Bit, 20 MSPS to 200 MSPS, 1.05 mW/MSPS A/D Converter

General Description

The ADC08200 is a low-power, 8-bit, monolithic analog-to-digital converter with an on-chip track-and-hold circuit. Optimized for low cost, low power, small size and ease of use, this product operates at conversion rates up to 230 MSPS while consuming just 1.05 mW per MHz of clock frequency, or 210 mW at 200 MSPS. Raising the PD pin puts the ADC08200 into a Power Down mode where it consumes 1 mW.

The unique architecture achieves 7.3 Effective Bits with 50 MHz input frequency. The ADC08200 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC08200's reference ladder are available for connections, enabling a wide range of input possibilities. The digital outputs are TTL/CMOS compatible with a separate output power supply pin to support interfacing with 3V or 2.5V logic. The digital inputs (CLK and PD) are TTL/CMOS compatible.

The ADC08200 is offered in a 24-lead plastic package (TSSOP) and is specified over the industrial temperature range of −40°C to +85°C.

Features

- Single-ended input
- Internal sample-and-hold function
- Low voltage (single +3V) operation
- Small package
- Power-down feature

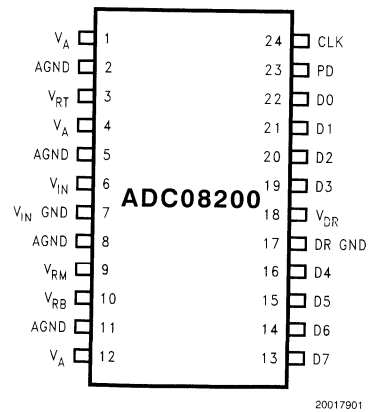
Key Specifications

■ Resolution:	8 bits
■ Maximum sampling frequency:	200 MSPS (min)
■ DNL:	±0.4 LSB (typ)
■ ENOB (f_{IN}= 50 MHz):	7.3 bits (typ)
■ THD (f_{IN}= 50 MHz):	−61 dB (typ)
■ Guaranteed no missing codes	
■ Power consumption	
■ Operating:	1.05 mW/MSPS (typ)
■ Power down:	1 mW (typ)

Applications

- Flat panel displays
- Projection systems
- Set-top boxes
- Battery-powered instruments
- Communications
- Medical scan converters
- X-ray imaging
- High speed viterbi decoders
- Astronomy

Pin Configuration

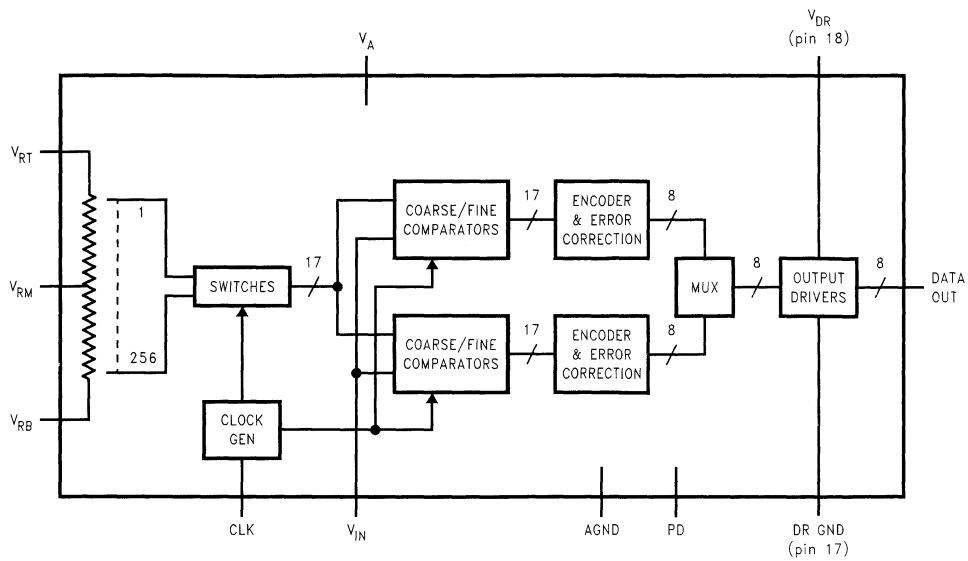


20017901

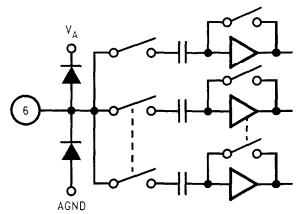
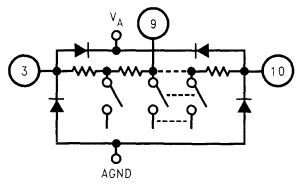
Ordering Information

ADC08200CIMT	TSSOP
ADC08200CIMTX	TSSOP (tape and reel)

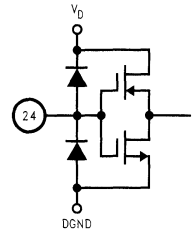
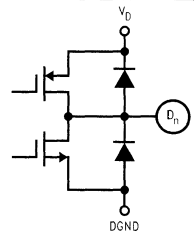
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
6	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
3	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 0.5V to V_A. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
9	V_{RM}		Mid-point of the reference ladder. This pin should be bypassed to a quiet point in the analog ground plane with a 0.1 µF capacitor.
10	V_{RB}		Analog Input that is the low side (bottom) of the reference ladder of the ADC. Nominal range is 0.0V to (V_{RT} – 0.5V). Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
23	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins hold the last conversion result.
24	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
13 thru 16 and 19 thru 22	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input.
7	V_{IN} GND		Reference ground for the single-ended analog input, V_{IN}.
1, 4, 12	V_A		Positive analog supply pin. Connect to a quiet voltage source of +3V. V_A should be bypassed with a 0.1 µF ceramic chip capacitor for each pin, plus one 10 µF capacitor. See Section 3.0 for more information.
18	V_{DR}		Power supply for the output drivers. If connected to V_A, decouple well from V_A.
17	DR GND		The ground return for the output driver supply.
2, 5, 8, 11	AGND		The ground return for the analog supply.

National Semiconductor

ADC0831/ADC0832/ADC0834/ADC0838
8-Bit Serial I/O A/D Converters with Multiplexer Options

General Description

The ADC0831 series are 8-bit successive approximation A/D converters with a serial I/O and configurable input multiplexers with up to 8 channels. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ family of processors, and can interface with standard shift registers or µPs.

The 2-, 4- or 8-channel multiplexers are software configured for single-ended or differential inputs as well as channel assignment.

The differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

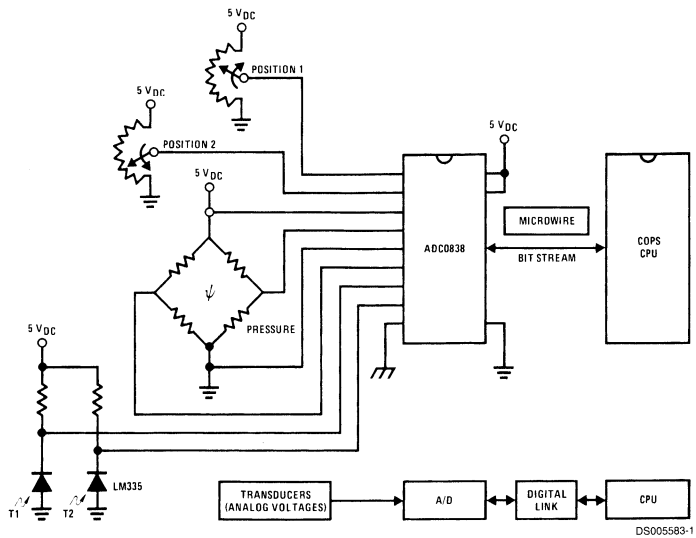
Features

- NSC MICROWIRE compatible—direct interface to COPS family processors
- Easy interface to all microprocessors, or operates "stand-alone"
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 2-, 4- or 8-channel multiplexer options with address logic
- Shunt regulator allows operation with high voltage supplies
- 0V to 5V input range with single 5V power supply
- Remote operation with serial digital data link
- TTL/MOS input/output compatible
- 0.3" standard width, 8-, 14- or 20-pin DIP package
- 20 Pin Molded Chip Carrier Package (ADC0838 only)
- Surface-Mount Package

Key Specifications

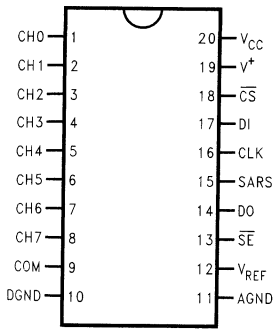
■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ±1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	32 µs

Typical Application



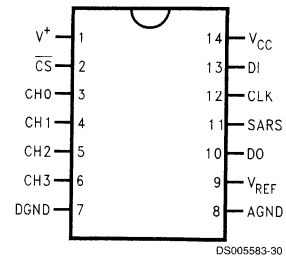
Connection Diagrams

ADC0838 8-Channel Mux
Small Outline/Dual-In-Line Package
(WM and N)



Top View

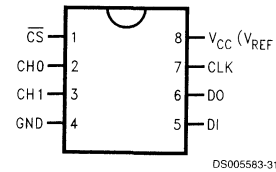
ADC0834 4-Channel MUX
Small Outline/Dual-In-Line Package
(WM and N)



COM internally connected to A GND
Top View

Top View

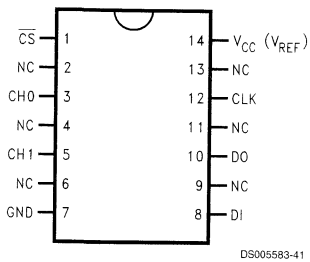
ADC0832 2-Channel MUX
Dual-In-Line Package (N)



COM internally connected to GND.
V_{REF} internally connected to V_{CC}.
Top View

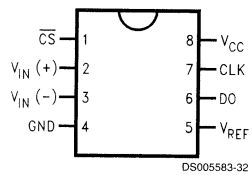
Top View

ADC0832 2-Channel MUX
Small Outline Package (WM)



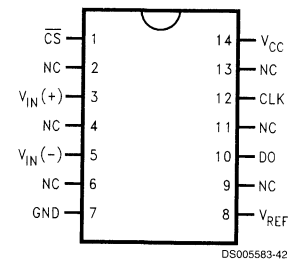
Top View

ADC0831 Single
Differential Input
Dual-In-Line Package (N)



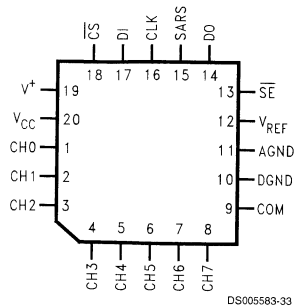
Top View

ADC0831 Single Differential Input
Small Outline Package (WM)



Top View

ADC0838 8-Channel MUX
Molded Chip Carrier (PCC)
Package (V)



Ordering Information

Part Number	Analog Input Channels	Total Unadjusted Error	Package	Temperature Range
ADC0831CCN	1	±1	Molded (N)	0°C to +70°C
ADC0831CCWM			SO(M)	0°C to +70°C
ADC0832CIWM	2	±1	SO(M)	−40°C to +85°C
ADC0832CCN			Molded (N)	0°C to +70°C
ADC0832CCWM			SO(M)	0°C to +70°C
ADC0834BCN	4	±½	Molded (N)	0°C to +70°C
ADC0834CCN		±1	Molded (N)	0°C to +70°C
ADC0834CCWM			SO(M)	0°C to +70°C
ADC0838BCV	8	±½	PCC (V)	0°C to +70°C
ADC0838CCV		±1	PCC (V)	0°C to +70°C
ADC0838CCN			Molded (N)	0°C to +70°C
ADC0838CIWM			SO(M)	−40°C to +85°C
ADC0838CCWM			SO(M)	0°C to +70°C

See NS Package Number M14B, M20B, N08E, N14A, N20A or V20A

National Semiconductor

ADC08351
8-Bit, 42 MSPS, 40 mW A/D Converter

General Description

The ADC08351 is an easy to use low power, low cost, small size, 42 MSPS analog-to-digital converter that digitizes signals to 8 bits. The ADC08351 uses an unique architecture that achieves 7.2 Effective Bits with a 4.4 MHz input and 42 MHz clock frequency and 6.8 Effective Bits with a 21 MHz input and 42 MHz clock frequency. Output formatting is straight binary coding.

To minimize system cost and power consumption, the ADC08351 requires minimal external components and includes input biasing to allow optional a.c. input signal coupling. The user need only provide a +3V supply and a clock. Many applications require no separate reference or driver components.

The excellent dc and ac characteristics of this device, together with its low power consumption and +3V single supply operation, make it ideally suited for many video and imaging applications, including use in portable equipment. Total power consumption is reduced to less than 7 mW in the power-down mode. Furthermore, the ADC08351 is resistant to latch-up and the outputs are short-circuit proof.

Fabricated on a 0.35 micron CMOS process, the ADC08351 is offered in TSSOP and LLP (a molded lead frame-based chip-scale package), and is designed to operate over the industrial temperature range of −40°C to +85°C.

Features

- Low Input Capacitance
- Internal Sample-and-Hold Function
- Single +3V Operation
- Power Down Feature
- TRI-STATE Outputs

Key Specifications

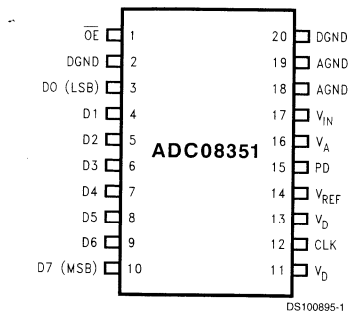
- Resolution — 8 Bits
- Maximum Sampling Frequency — 42 MSPS (min)
- ENOB @ f_{CLK} = 42 MHz, f_{IN} = 4.4 MHz — 7.2 Bits (typ)
- Guaranteed No Missing Codes
- Power Consumption — 40 mW (typ); 48 mW (max) (Excluding Reference Current)

Applications

- Video Digitization
- Digital Still Cameras
- Set Top Boxes
- Digital Camcorders
- Communications
- Medical Imaging
- Personal Computer Video
- CCD Imaging
- Electro-Optics

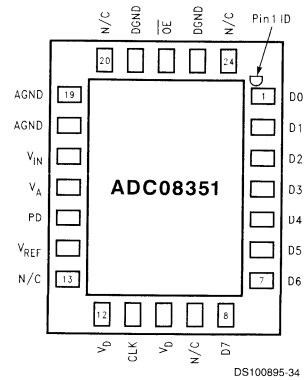
Pin Configuration

20-Pin TSSOP



Top View

24-Pin LLP (CSP)

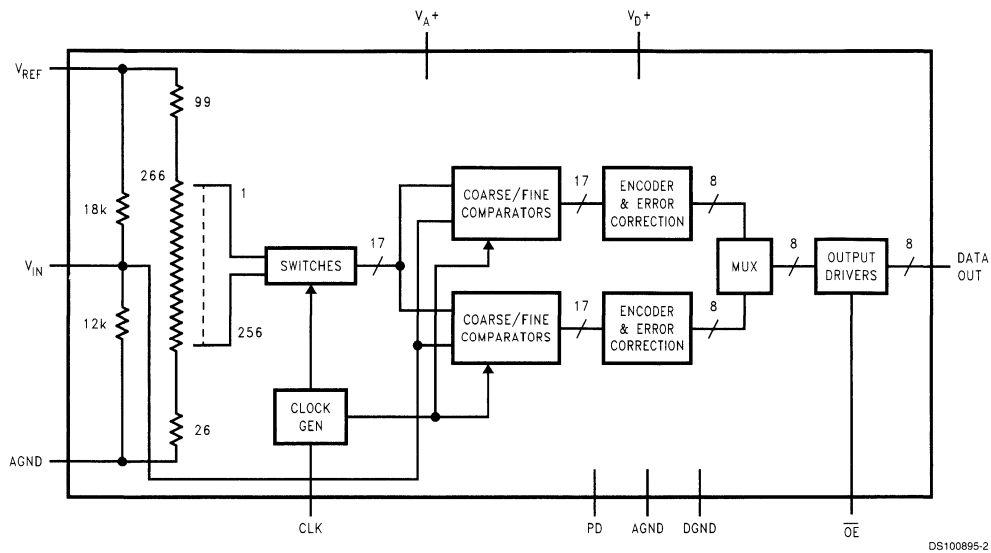


Bottom View

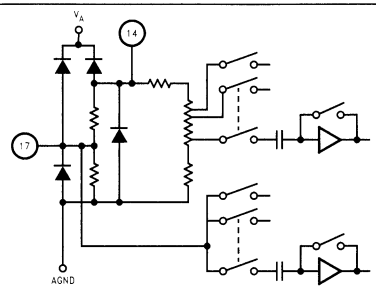
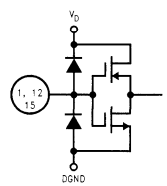
Ordering Information

ADC08351CIMTC	TSSOP
ADC08351CIMTCX	TSSOP (tape & reel)
ADC08351CILQ	LLP (tape & reel - 1, 000 units)
ADC08351CILQX	LLP (tape & reel - 4, 500 units)

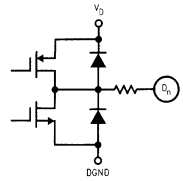
ADC08351 Block Diagram



Pin Descriptions and Equivalent Circuits (LLP pins in parentheses)

Pin No.	Symbol	Equivalent Circuit	Description
17 (17)	V_{IN}		Analog signal input. Conversion range is 0.5 V_{P-P} to 0.68 V_A.
14 (14)	V_{REF}		Positive reference voltage input. Operating range of this voltage is 0.75V to V_A. This pin should be bypassed with a 10 µF tantalum or aluminum electrolytic capacitor and a 0.1 µF ceramic chip capacitor.
1 (22)	$\overline{OE}$		CMOS/TTL compatible digital input that, when low, enables the digital outputs of the ADC08351. When high, the outputs are in a high impedance state.
12 (11)	CLK		CMOS/TTL compatible digital clock input. V_{IN} is sampled on the falling edge of CLK input.
15 (15)	PD		CMOS/TTL compatible digital input that, when high, puts the ADC08351 into the power down mode, where it consumes minimal power. When this pin is low, the ADC08351 is in the normal operating mode.

Pin Descriptions and Equivalent Circuits (LLP pins in parentheses) (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
3 thru 10 (1 thru 8)	D0–D7		Conversion data digital output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are enabled by bringing the $\overline{OE}$ pin low.
11, 13 (10, 12)	V_D		Positive digital supply pin. Connect to a clean, quiet voltage source of +3V. V_A and V_D should have a common supply and be separately bypassed with a 10 µF tantalum or aluminum electrolytic capacitor and a 0.1 µF ceramic chip capacitor. See Section 3.0 for more information.
2, 20 (21, 23)	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC08351.
16 (16)	V_A		Positive analog supply pin. Connected to a clean, quiet voltage source of +3V. V_A and V_D should have a common supply and be separately bypassed with a 10 µF tantalum or aluminum electrolytic capacitor and a 0.1 µF ceramic chip capacitor. See Section 3.0 for more information.
18, 19 (18, 19)	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC08351 package.

National Semiconductor

ADC0844/ADC0848
8-Bit µP Compatible A/D Converters with Multiplexer Options

General Description

The ADC0844 and ADC0848 are CMOS 8-bit successive approximation A/D converters with versatile analog input multiplexers. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/Ds are designed to operate from the control bus of a wide variety of microprocessors. TRI-STATE output latches that directly drive the data bus permit the A/Ds to be configured as memory locations or I/O devices to the microprocessor with no interface logic necessary.

Features

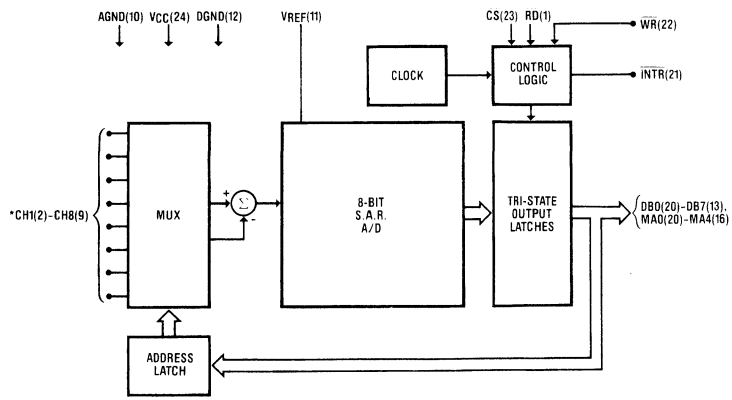
- Easy interface to all microprocessors
- Operates ratiometrically or with 5 V_{DC} voltage reference
- No zero or full-scale adjust required
- 4-channel or 8-channel multiplexer with address logic
- Internal clock
- 0V to 5V input range with single 5V power supply
- 0.3" standard width 20-pin or 24-pin DIP
- 28 Pin Molded Chip Carrier Package

Key Specifications

■ Resolution	8 Bits
■ Total Unadjusted Error	±½ LSB and ± 1 LSB
■ Single Supply	5 V_{DC}
■ Low Power	15 mW
■ Conversion Time	40 µs

6

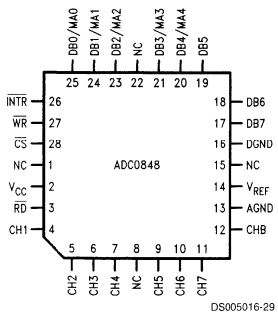
Block and Connection Diagrams



*ADC0848 shown in DIP Package CH5-CH8 not included on the ADC0844

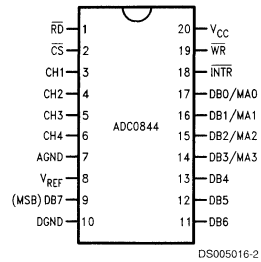
Block and Connection Diagrams (Continued)

Molded Chip Carrier Package



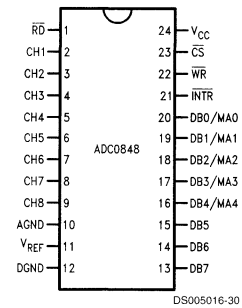
Top View
See Ordering Information

Dual-In-Line Package



Top View

Dual-In-Line Package



Top View

Ordering Information

Temperature Range	Total Unadjusted Error		MUX Channels	Package Outline
	±½ LSB	±1 LSB		
0°C to +70°C		ADC0844CCN	4	N20A Molded Dip
	ADC0848BCN	ADC0848CCN	8	N24C Molded Dip
−40°C to +85°C	ADC0844BCJ	ADC0844CCJ	4	J20A Cerdip
	ADC0848BCV	ADC0848CCV	8	V28A Molded Chip Carrier

National Semiconductor

ADC08831/ADC08832
8-Bit Serial I/O CMOS A/D Converters with Multiplexer and Sample/Hold Function

General Description

The ADC08831/ADC08832 are 8-bit successive approximation Analog to Digital converters with 3-wire serial interfaces and a configurable input multiplexer for 2 channels. The serial I/O will interface to COPS™family of micro-controllers, PLD's, microprocessors, DSP's, or shift registers. The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard.

To minimize total power consumption, the ADC08831/ADC08832 automatically go into low power mode whenever they are not performing conversions.

A track/hold function allows the analog voltage at the positive input to vary during the actual A/D conversion.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. The voltage reference input can be adjusted to allow encoding of small analog voltage spans to the full 8-bits of resolution.

Applications

- Digitizing sensors and waveforms
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Embedded Systems

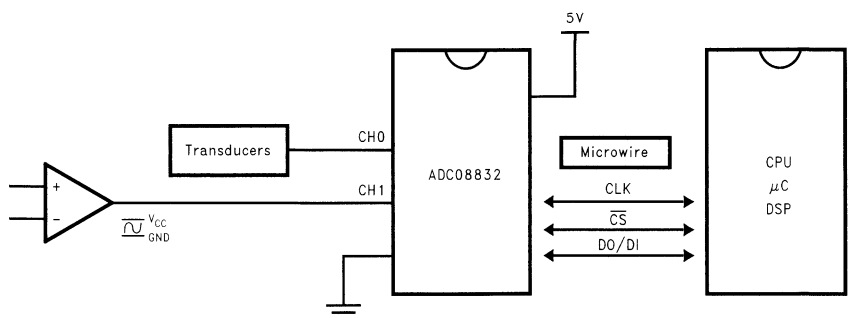
Features

- 3-wire serial digital data link requires few I/O pins
- Analog input track/hold function
- 2-channel input multiplexer option with address logic
- Analog input voltage range from GND to V_{CC}
- No zero or full scale adjustment required
- TTL/CMOS input/output compatible
- Superior pin compatible replacement for ADC0831/2

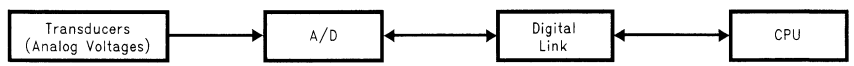
Key Specifications

- Resolution: 8 bits
- Conversion time (f_C = 2 MHz): 4µs (max)
- Power dissipation: 8.5mW (typ)
- Low power mode: 3.0mW (typ)
- Single supply: $5V_{DC}$
- Total unadjusted error: ±1LSB
- No missing codes over temperature

Typical Application



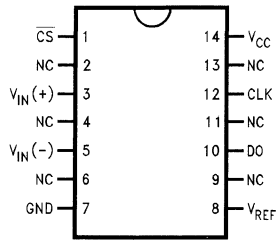
DS100108-44



DS100108-43

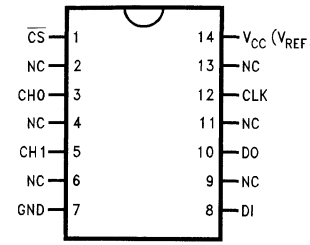
Connection Diagrams

ADC08831
Wide Body SO Packages



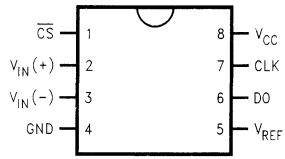
DS100108-4

ADC08832
Wide Body SO Packages



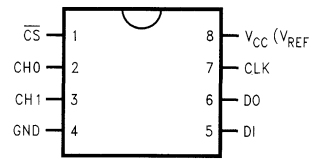
DS100108-3

ADC08831
N,M,MM Packages



DS100108-2

ADC08832
N,M,MM Packages



DS100108-1

Ordering Information

Temperature Range	Package
Industrial ($-40^{\circ}C \leq T_J \leq +85^{\circ}C$)	
ADC08831IN	N08E
ADC08832IN	
ADC08831IWM,	M14B
ADC08832IWM,	
ADC08831IM,	M08A
ADC08832IM,	
ADC08831IMM,	MUA08A
ADC08832IMM,	

National Semiconductor

ADC1001
10-Bit µP Compatible A/D Converter

General Description

The ADC1001 is a CMOS, 10-bit successive approximation A/D converter. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

Differential inputs provide low frequency input common mode rejection and allow offsetting the analog range of the converter. In addition, the reference input can be adjusted enabling the conversion of reduced analog ranges with 10-bit resolution.

Key Specifications

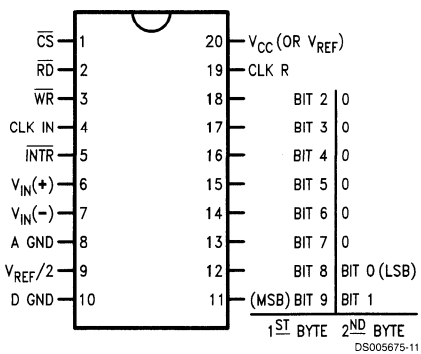
- Resolution 10 bits
- Linearity error ±1 LSB
- Conversion time 200µS

Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D converters
- Compatible with NSC800 and 8080 µP derivatives—no interfacing logic needed
- Easily interfaced to 6800 µP derivatives
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3" standard width 20-pin DIP package

Connection Diagram

ADC1001
Dual-In-Line Package



Top View

Ordering Information

Temperature Range	0°C to +70°C	−40°C to +85°C
Order Number	ADC1001CCJ-1	ADC1001CCJ
Package Outline	J20A	J20A

National Semiconductor

ADC10030
10-Bit, 30 MSPS, 125 mW A/D Converter with Internal Sample and Hold

General Description

The ADC10030 is a low power, high performance CMOS analog-to-digital converter that digitizes signals to 10 bits resolution at sampling rates up to 30 Msps while consuming a typical 125 mW from a single 5V supply. Reference force and sense pins allow the user to connect an external reference buffer amplifier to ensure optimal accuracy. No missing codes is guaranteed over the full operating temperature range. The unique two-stage architecture achieves 9.1 Effective Bits with a 15 MHz input signal and a 30 MHz clock frequency. Output formatting is straight binary coding.

To ease interfacing to 3V systems, the digital I/O power pins of the ADC10030 can be tied to a 3V power source, making the outputs 3V compatible. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power standby state, where it typically consumes less than 4 mW. The ADC10030's speed, resolution and single supply operation makes it well suited for a variety of applications in video, imaging, communications, multimedia and high speed data acquisition. Low power, single supply operation ideally suit the ADC10030 for high speed portable applications, and its speed and resolution are ideal for charge coupled device (CCD) input systems.

The ADC10030 comes in a space saving 32-pin TQFP and operates over the industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$) temperature range.

Features

- Internal Sample-and-Hold
- Single +5V Operation
- Low Power Standby Mode
- Guaranteed No Missing Codes
- TRI-STATE Outputs
- TTL/CMOS or 3V Logic Input/Output Compatible

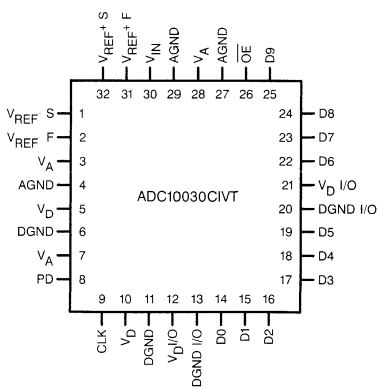
Key Specifications

■ Resolution	10 Bits
■ Conversion Rate	30 Msps
■ ENOB @ 15 MHz Input	9.1 Bits (typ)
■ DNL	0.40 LSB (typ)
■ Conversion Latency	2 Clock Cycles
■ PSRR	56 dB
■ Power Consumption	125 mW (typ)
■ Low Power Standby Mode	<3.5 mW (typ)

Applications

- Digital Video
- Communications
- Document Scanners
- Medical Imaging
- Electro-Optics
- Plain Paper Copiers
- CCD Imaging

Connection Diagram

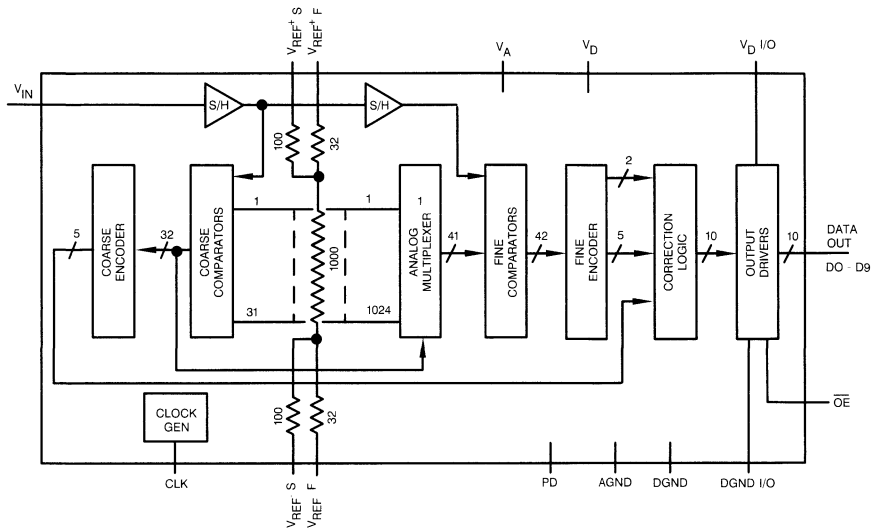


DS101064-1

Ordering Information

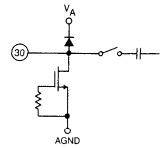
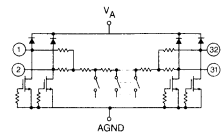
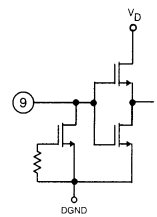
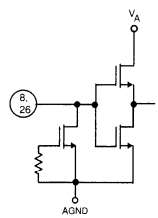
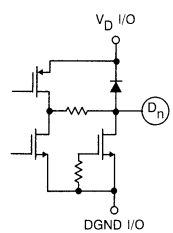
Commercial Temperature Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10030CIVT	TQFP

Block Diagram



DS101064-2

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
30	V_{IN}		Analog Input signal to be converted. Conversion range is V_{REF^+} S to V_{REF^-} S.
31	V_{REF^+} F		Analog input that goes to the high side of the reference ladder of the ADC. This voltage should force V_{REF^+} S to be in the range of 2.6V to 3.8V.
32	V_{REF^+} S		Analog output used to sense the voltage near the top of the ADC reference ladder.
2	V_{REF^-} F		Analog input that goes to the low side of the reference ladder of the ADC. This voltage should force V_{REF-} S to be in the range of 1.7V to 2.8V.
1	V_{REF-} S		Analog output used to sense the voltage near the bottom of the ADC reference ladder.
9	CLK		Converter digital clock input. V_{IN} is sampled on the falling edge of CLK input.
8	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins are in a high impedance state.
26	$\overline{OE}$		Output Enable pin. When this pin and the PD pin are low, the output data pins are active. When this pin or the PD pin is high, the data output pins are in a high impedance state.
14 thru 19 and 22 thru 25	D0–D9		Digital Output pins providing the 10-bit conversion results. D0 is the LSB, D9 is the MSB. Data is acquired on the falling edge of the CLK input and valid data is present 2.0 clock cycles plus t_{OD} later.
3, 7, 28	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.
5, 10	V_D		Positive digital supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
12, 21	V_D I/O		Positive supply pins for the digital output drivers. These pins should be connected to a clean, quiet voltage source of +3V to +5V and be separately bypassed with 10 µF to 50 µF capacitors.
4, 27, 29	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10030 package.
6, 11	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10030 package.
13, 20	DGND I/O		The ground return of the digital output drivers.

National Semiconductor

ADC1005
10-Bit µP Compatible A/D Converter

General Description

The ADC1005 is a CMOS 10-bit successive approximation A/D converter. The 20-pin ADC1005 outputs 10-bit data in a two-byte format for interface with 8-bit microprocessors.

The ADC1005 has differential inputs to permit rejection of common-mode signals, allow the analog input range to be offset, and also to permit the conversion of signals not referred to ground. In addition, the reference voltage can be adjusted, allowing smaller voltage spans to be measured with 10-bit resolution.

Features

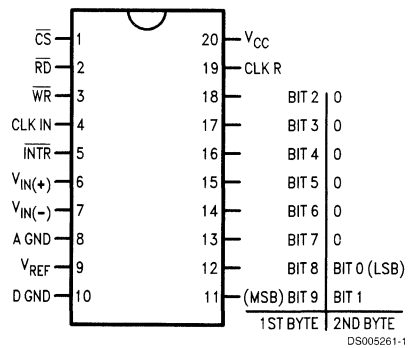
- Easy interface to all microprocessors
- Differential analog voltage inputs
- Operates ratiometrically or with 5 V_{DC} voltage reference or analog span adjusted voltage reference
- 0V to 5V analog input voltage range with single 5V supply
- On-chip clock generator
- TLL/MOS input/output compatible
- 0.3" standard width 20-pin DIP

Key Specifications

- Resolution — 10 bits
- Linearity Error — ±½ LSB and ±1 LSB
- Conversion Time — 50 µs

Connection Diagram

ADC 1005 (for an 8–bit data bus)
Dual-In-Line Package



Top View

Ordering Information

Part Number	Package Outline	Temperature Range	Linearity Error
ADC1005BCJ-1	J20A	0°C to +70°C	±½ LSB
ADC1005BCJ	J20A	−40°C to +85°C	
ADC1005CCJ-1	J20A	0°C to +70°C	±1 LSB
ADC1005CCJ	J20A	−40°C to +85°C	

National Semiconductor

ADC10061/ADC10062/ADC10064
10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep* conversion technique, the 10-bit ADC10061, ADC10062, and ADC10064 CMOS analog-to-digital converters offer sub-microsecond conversion times yet dissipate a maximum of only 235 mW. The ADC10061, ADC10062, and ADC10064 perform a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. The ADC10061 is pin-compatible with the ADC1061 but much faster, thus providing a convenient upgrade path for the ADC1061.

The analog input voltage to the ADC10061, ADC10062, and ADC10064 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 200 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10062 and ADC10064 include a "speed-up" pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 350 ns with only a small increase in linearity error.

For ease of interface to microprocessors, the ADC10061, ADC10062, and ADC10064 have been designed to appear as a memory location or I/O port without the need for external interface logic.

*U.S. Patent Number 4918449

Features

- Built-in sample-and-hold
- Single +5V supply
- 1, 2, or 4-input multiplexer options
- No external clock required
- Speed adjust pin for faster conversions (ADC10062 and ADC10064). See ADC10662/4 for high speed guaranteed performance.

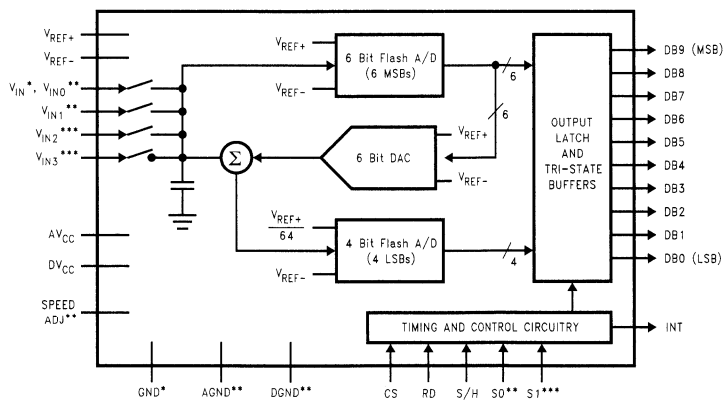
Key Specifications

- Conversion time to 10 bits — 600 ns typical, 900 ns max over temperature
- Sampling Rate — 800 kHz
- Low power dissipation — 235 mW (max)
- Total unadjusted error — ±1.0 LSB (max)
- No missing codes over temperature

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Simplified Block Diagram



*ADC10061 Only

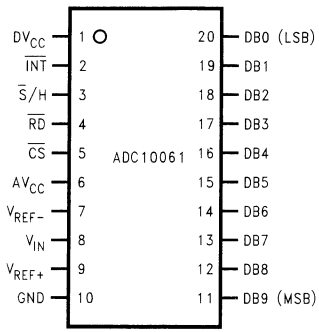
**ADC10062 and ADC10064 Only

***ADC10064 Only

Ordering Information

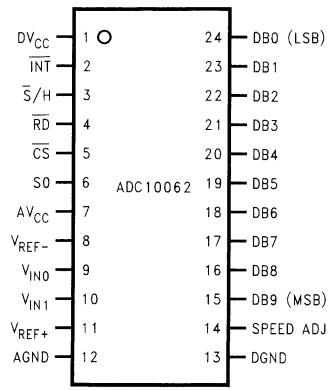
Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC10061CIWM	M20B Small Outline
ADC10062CIWM	M24B Small Outline
ADC10064CIWM	M28B Small Outline

Connection Diagrams



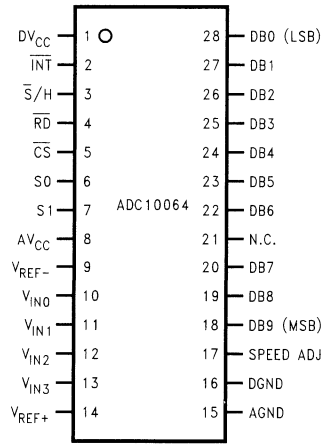
01102011

Top View



01102012

Top View



01102013

Top View

Pin Descriptions

DV_{CC}, AV_{CC} These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}$/H This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}$/H pins.

S0, S1 On the multiple-input devices (ADC10062 and ADC10064), these pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}$/H makes its High-to-Low transition (See the Timing Diagrams). The ADC10064 includes both S0 and S1. The ADC10062 includes just S0, and the ADC10061 includes neither.

V_{REF-}, V_{REF+}
These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to (V_{REF+} − 1 LSB) produces an output code of 1023.

V_{IN}, V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3}
These are the analog input pins. The ADC10061 has one input (V_{IN}), the ADC10062 has two inputs (V_{IN0} and V_{IN1}), and the ADC10064 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND
These are the power supply ground pins. The ADC10061 has a single ground pin (GND), and the ADC10062 and ADC10064 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. For the devices with two ground pins, both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE® output pins.

SPEED ADJ (ADC10062 and ADC10064 only). This pin is normally left unconnected, but by connecting a resistor between this pin and ground, the conversion time can be reduced. See the Typical Performance Curves and the table of Electrical Characteristics.

National Semiconductor

ADC10154/ADC10158
10-Bit Plus Sign 4 µs ADCs with 4- or 8-Channel MUX, Track/Hold and Reference

General Description

The ADC10154 and ADC10158 are CMOS 10-bit plus sign successive approximation A/D converters with versatile analog input multiplexers, track/hold function and a 2.5V band-gap reference. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The input track/hold is implemented using a capacitive array and sampled-data comparator.

Resolution can be programmed to be 8-bit, 8-bit plus sign, 10-bit or 10-bit plus sign. Lower-resolution conversions can be performed faster.

The variable resolution output data word is read in two bytes, and can be formatted left justified or right justified, high byte first.

Applications

- Process control
- Instrumentation
- Test equipment

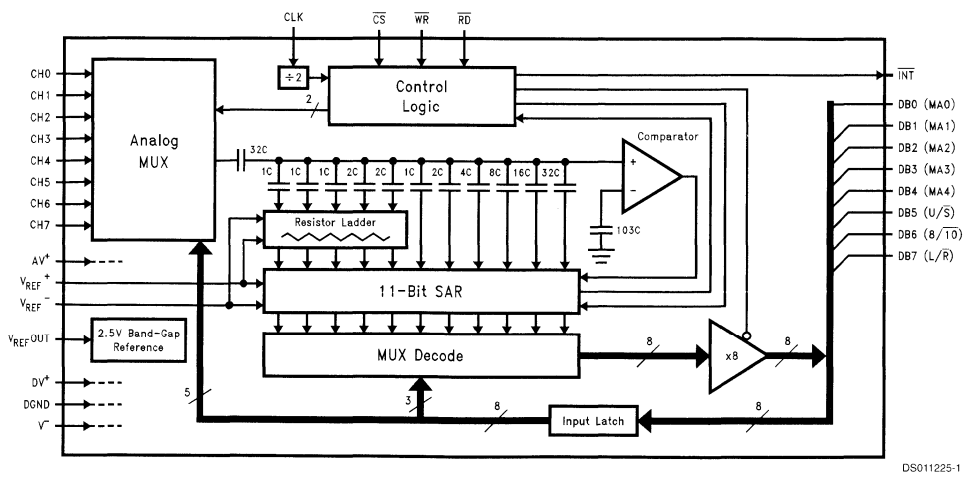
Features

- 4- or 8- channel configurable multiplexer
- Analog input track/hold function
- 0V to 5V analog input range with single +5V power supply
- −5V to +5V analog input voltage range with ±5V supplies
- Fully tested in unipolar (single +5V supply) and bipolar (dual ±5V supplies) operation
- Programmable resolution/speed and output data format
- Ratiometric or Absolute voltage reference operation
- No zero or full scale adjustment required
- No missing codes over temperature
- Easy microprocessor interface

Key Specifications

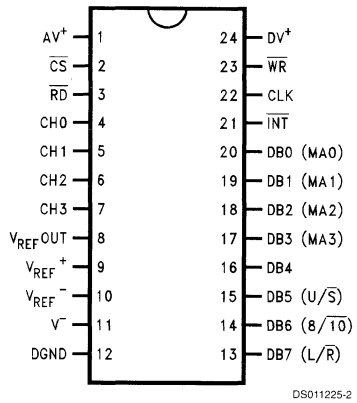
Resolution	10-bit plus sign
Integral linearity error	±1 LSB (max)
Unipolar power dissipation	33 mW (max)
Conversion time (10-bit + sign)	4.4 µs (max)
Conversion time (8-bit)	3.2 µs (max)
Sampling rate (10-bit + sign)	166 kHz
Sampling rate (8-bit)	207 kHz
Band-gap reference	2.5V ±2.0% (max)

ADC10158 Simplified Block Diagram



Connection Diagrams

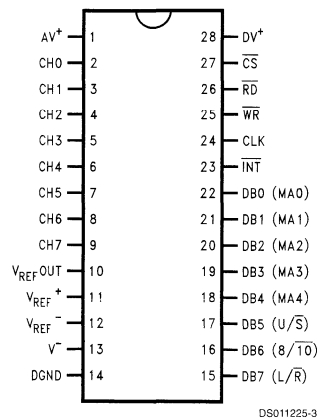
Dual-in-Line and SO Packages



DS011225-2

Top View
Order Number ADC10154
NS Package Number M24B

Dual-in-Line and SO Packages



DS011225-3

Top View
Order Number ADC10158
NS Package Numbers
M28B or N28B

Pin Descriptions

AV^+ — This is the positive analog supply. This pin should be bypassed with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor to the system analog ground.

DV^+ — This is the positive digital supply. This supply pin also needs to be bypassed with 0.1 µF ceramic and 10 µF tantalum capacitors to the system digital ground. AV^+ and DV^+ should be bypassed separately and tied to same power supply.

DGND — This is the digital ground. All logic levels are referred to this ground.

V^- — This is the negative analog supply. For unipolar operation this pin may be tied to the system analog ground or to a negative supply source. It should not go above DGND by more than 50 mV. When bipolar operation is required, the voltage on this pin will limit the analog input's negative voltage level. In bipolar operation this supply pin needs to be bypassed with 0.1 µF ceramic and 10 µF tantalum capacitors to the system analog ground.

V_{REF}^+, V_{REF}^- — These are the positive and negative reference inputs. The voltage difference between V_{REF}^+ and V_{REF}^- will set the analog input voltage span.

V_{REF}Out — This is the internal band-gap voltage reference output. For proper operation of the voltage reference, this pin needs to be bypassed with a 330 µF tantalum or electrolytic capacitor.

$\overline{CS}$ — This is the chip select input. When a logic low is applied to this pin the $\overline{WR}$ and $\overline{RD}$ pins are enabled.

$\overline{RD}$ — This is the read control input. When a logic low is applied to this pin the digital outputs are enabled and the $\overline{INT}$ output is reset high.

$\overline{WR}$ — This is the write control input. The rising edge of the signal applied to this pin selects the multiplexer channel and initiates a conversion.

$\overline{INT}$ — This is the interrupt output. A logic low at this output indicates the completion of a conversion.

CLK — This is the clock input. The clock frequency directly controls the duration of the conversion time (for example, in the 10-bit bipolar mode $t_C = 22/f_{CLK}$) and the acquisition time ($t_A = 6/f_{CLK}$).

DB0(MA0) –DB7 (L/$\overline{R}$) — These are the digital data inputs/outputs. DB0 is the least significant bit of the digital output word; DB7 is the most significant bit in the digital output word (see the Output Data Configuration table). MA0 through MA4 are the digital inputs for the multiplexer channel selection (see the Multiplexer Addressing tables). U/$\overline{S}$ (Unsigned/Signed), 8/$\overline{10}$, (8/10-bit resolution) and L/$\overline{R}$ (Left/Right justification) are the digital input bits that set the A/D's output word format and resolution (see the Output Data Configuration table). The conversion time is modified by the chosen resolution (see Electrical AC Characteristics table). The lower the resolution, the faster the conversion will be.

CH0–CH7 — These are the analog input multiplexer channels. They can be configured as single-ended inputs, differential input pairs, or pseudo-differential inputs (see the Multiplexer Addressing tables for the input polarity assignments).

National Semiconductor

ADC10221
10-Bit, 15 MSPS, 98 mW A/D Converter with Internal Sample and Hold

General Description

The ADC10221 is the first in a family of low power, high performance CMOS analog-to-digital converters. It can digitize signals to 10 bits resolution at sampling rates up to 20 MSPS (15 MSPS guaranteed) while consuming a typical 98 mW from a single 5V supply. Reference force and sense pins allow the user to connect an external reference buffer amplifier to ensure optimal accuracy. The ADC10221 is guaranteed to have no missing codes over the full operating temperature range. The unique two stage architecture achieves 9.2 Effective Bits with a 10MHz input signal and a 20MHz clock frequency. Output formatting is straight binary coding.

To ease interfacing to 3V systems, the digital I/O power pins of the ADC10221 can be tied to a 3V power source, making the outputs 3V compatible. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power standby state, where it typically consumes less than 4 mW. The ADC10221's speed, resolution and single supply operation make it well suited for a variety of applications in video, imaging, communications, multimedia and high speed data acquisition. Low power, single supply operation ideally suit the ADC10221 for high speed portable applications, and its speed and resolution are ideal for charge coupled device (CCD) input systems.

The ADC10221 comes in a space saving 32-pin TQFP and operates over the industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$) temperature range.

Features

- Internal Sample-and-Hold
- Single +5V Operation
- Low Power Standby Mode
- Guaranteed No Missing Codes
- TTL/CMOS or 3V Logic Input/Output Compatible

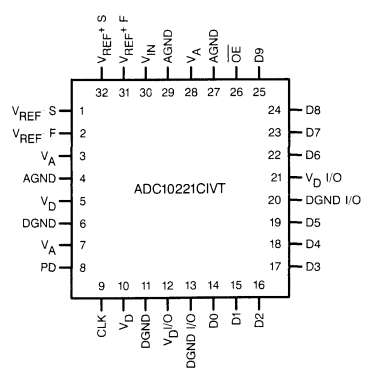
Key Specifications

■ Resolution	10 Bits
■ Conversion Rate	20 MSPS (typ)
	15 MSPS (min)
■ ENOB @ 10 MHz Input, 20 MHz Clock	9.2 Bits (typ)
■ DNL	0.35 LSB (typ)
■ Power Consumption	98 mW (typ)
■ Low Power Standby Mode	<4 mW (typ)

Applications

- Digital Video
- Document Scanners
- Medical Imaging
- Electro-Optics
- Plain Paper Copiers
- CCD Imaging

Connection Diagram

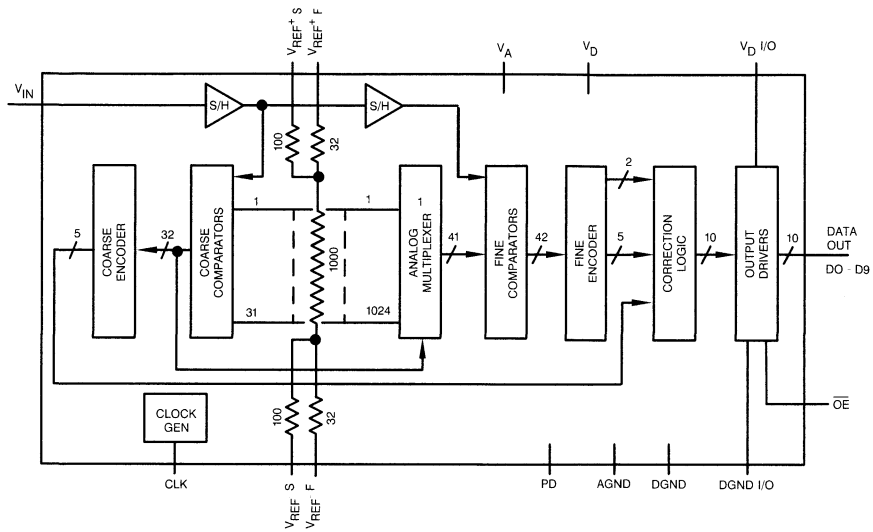


DS101038-1

Ordering Information

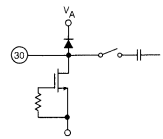
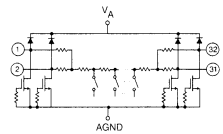
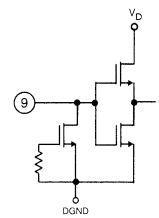
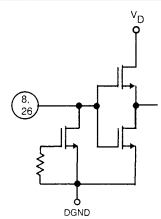
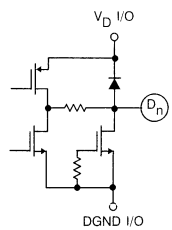
Commercial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10221CIVT	TQFP

Block Diagram



DS101038-2

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
30	V_{IN}		Analog Input signal to be converted. Conversion range is V_{REF^+} S to V_{REF^-} S.
31	V_{REF^+} F		Analog input that goes to the high side of the reference ladder of the ADC. This voltage should force V_{REF^+} S to be in the range of 2.3V to 4.0V.
32	V_{REF^+} S		Analog output used to sense the voltage near the top of the ADC reference ladder.
2	V_{REF^-} F		Analog input that goes to the low side of the reference ladder of the ADC. This voltage should force V_{REF-} S to be in the range of 1.3V to 3.0V.
1	V_{REF-} S		Analog output used to sense the voltage near the bottom of the ADC reference ladder.
9	CLK		Converter digital clock input. V_{IN} is sampled on the falling edge of CLK input.
8	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins are in a high impedance state.
26	$\overline{OE}$		Output Enable pin. When this pin and the PD pin are low, the output data pins are active. When this pin or the PD pin is high, the output data pins are in a high impedance state.
14 thru 19 and 22 thru 25	D0 -D9		Digital Output pins providing the 10 bit conversion results. D0 is the LSB, D9 is the MSB. Valid data is present just after the falling edge of the CLK input.
3, 7, 28	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10µF to 50µF capacitors in parallel with 0.1µF capacitors.
5, 10	V_D		Positive digital supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10µF to 50µF capacitors in parallel with 0.1µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
12, 21	V_D I/O		Positive supply pins for the digital output drivers. These pins should be connected to a clean, quiet voltage source of +3V to +5V and be separately bypassed with 10µF capacitors.
4, 27, 29	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10221 package.
6, 11	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10221 pacjage.
13, 20	DGND I/O		The ground return of the digital output drivers.

National Semiconductor

ADC10321
10-Bit, 20MSPS, 98mW A/D Converter with Internal Sample and Hold

General Description

The ADC10321 is a low power, high performance CMOS analog-to-digital converter that digitizes signals to 10 bits resolution at sampling rates up to 25Msps while consuming a typical 98mW from a single 5V supply. Reference force and sense pins allow the user to connect an external reference buffer amplifier to ensure optimal accuracy. No missing codes is guaranteed over the full operating temperature range. The unique two stage architecture achieves 9.2 Effective Bits with a 10MHz input signal and a 20MHz clock frequency. Output formatting is straight binary coding.

To ease interfacing to 3V systems, the digital I/O power pins of the ADC10321 can be tied to a 3V power source, making the outputs 3V compatible. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power standby state, where it typically consumes less than 4mW. The ADC10321's speed, resolution and single supply operation makes it well suited for a variety of applications in video, imaging, communications, multimedia and high speed data acquisition. Low power, single supply operation ideally suit the ADC10321 for high speed portable applications, and its speed and resolution are ideal for charge coupled device (CCD) input systems.

The ADC10321 comes in a space saving 32-pin TQFP and operates over the industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$) temperature range.

Features

- Internal Sample-and-Hold
- Single +5V Operation
- Low Power Standby Mode
- Guaranteed No Missing Codes
- Tri-State Outputs
- TTL/CMOS or 3V Logic Input/Output Compatible

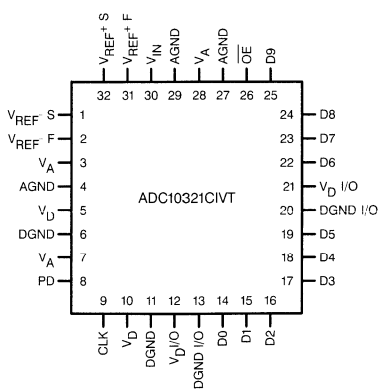
Key Specifications

■ Resolution	10 Bits
■ Conversion Rate	20 Msps
■ ENOB@ 10MHz Input	9.2 Bits (typ)
■ DNL	0.35 LSB (typ)
■ Conversion Latency	2 Clock Cycles
■ PSRR	56dB
■ Power Consumption	98mW (typ)
■ Low Power Standby Mode	<4mW (typ)

Applications

- Digital Video
- Communications
- Document Scanners
- Medical Imaging
- Electro-Optics
- Plain Paper Copiers
- CCD Imaging

Connection Diagram

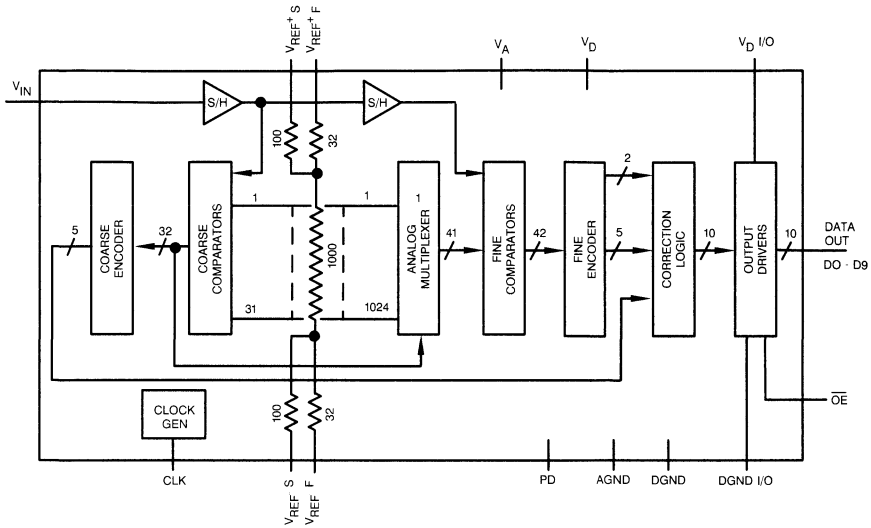


DS100897-1

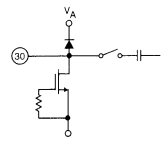
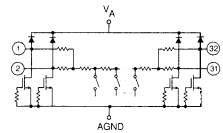
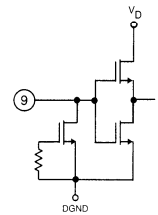
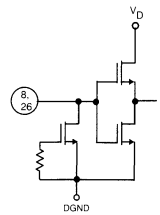
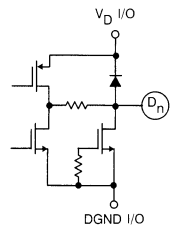
Ordering Information

Commercial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10321CIVT	TQFP

Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
30	V_{IN}		Analog Input signal to be converted. Conversion range is V_{REF^+} S to V_{REF^-} S.
31	V_{REF^+} F		Analog input that goes to the high side of the reference ladder of the ADC. This voltage should force V_{REF^+} S to be in the range of 2.3V to 4.0V.
32	V_{REF^+} S		Analog output used to sense the voltage near the top of the ADC reference ladder.
2	V_{REF^-} F		Analog input that goes to the low side of the reference ladder of the ADC. This voltage should force V_{REF-} S to be in the range of 1.3V to 3.0V.
1	V_{REF-} S		Analog output used to sense the voltage near the bottom of the ADC reference ladder.
9	CLK		Converter digital clock input. V_{IN} is sampled on the falling edge of CLK input.
8	PD		Power Down input. When this pin is high, the converter is in the Power Down mode and the data output pins are in a high impedance state.
26	$\overline{OE}$		Output Enable pin. When this pin and the PD pin are low, the output data pins are active. When this pin or the PD pin is high, the output data pins are in a high impedance state.
14 thru 19 and 22 thru 25	D0 -D9		Digital Output pins providing the 10 bit conversion results. D0 is the LSB, D9 is the MSB. Valid data is present just after the falling edge of the CLK input.
3, 7, 28	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10µF to 50µF capacitors in parallel with 0.1µF capacitors.
5, 10	V_D		Positive digital supply pins. These pins should be connected to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with 10µF to 50µF capacitors in parallel with 0.1µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
12, 21	V_D I/O		Positive supply pins for the digital output drivers. These pins should be connected to a clean, quiet voltage source of +3V to +5V and be separately bypassed with 10µF capacitors.
4, 27, 29	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10321 package.
6, 11	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10321 pacjage.
13, 20	DGND I/O		The ground return of the digital output drivers.

National Semiconductor

ADC10461/ADC10462/ADC10464
10-Bit 600 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep* conversion technique, the 10-bit ADC10461, ADC10462, and ADC10464 CMOS analog-to-digital converters offer sub-microsecond conversion times yet dissipate a maximum of only 235 mW. The ADC10461, ADC10462, and ADC10464 perform a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. Dynamic performance (THD, S/N) is guaranteed. The ADC10461 is pin-compatible with the ADC1061 but much faster, thus providing a convenient upgrade path for the ADC1061.

The analog input voltage to the ADC10461, ADC10462, and ADC10464 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 200 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10462 and ADC10464 include a "speed-up" pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 350 ns with only a small increase in linearity error.

For ease of interface to microprocessors, the ADC10461, ADC10462, and ADC10464 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Features

- Built-in sample-and-hold
- Single +5V supply
- 1, 2, or 4-input multiplexer options
- No external clock required
- Speed adjust pin for faster conversions (ADC10462 and ADC10464)

Key Specifications

■ Conversion time to 10 bits	600 ns typical
■ Sampling Rate	800 kHz
■ Low power dissipation	235 mW (max)
■ Total harmonic distortion (50 kHz)	−60 dB (max)
■ No missing codes over temperature	

Applications

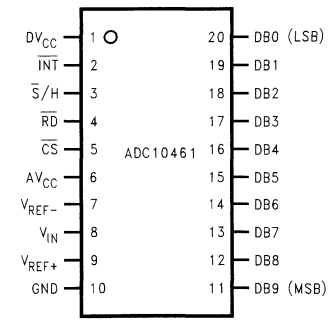
- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Note: *U.S. Patent Number 4918449

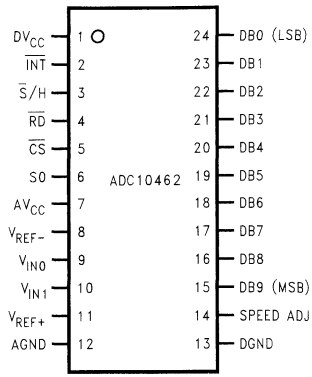
Ordering Information

Industrial Temp Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC20461CIWM	M20B Small Outline
ADC20462CIWM	M24B Small Outline
ADC20464CIWM	M28B Small Outline

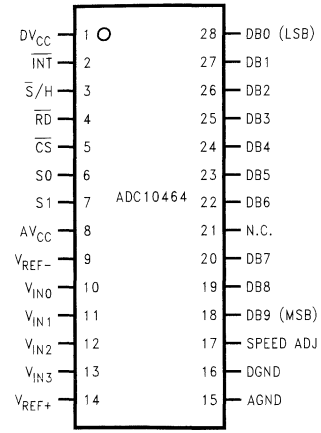
Connection Diagrams



Top View



Top View



Top View

Pin Descriptions

DV_{CC}, AV_{CC} These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}$ /H This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}$ /H pins.

S0, S1 On the multiple-input devices (ADC10462 and ADC10464), these pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}$ /H makes its High-to-Low transition (See the Timing Diagrams). The ADC10464 includes both S0 and S1. The ADC10462 includes just S0, and the ADC10461 includes neither.

V_{REF-}, V_{REF+}
These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to (V_{REF+} − 1 LSB) produces an output code of 1023.

V_{IN}, V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3}
These are the analog input pins. The ADC10461 has one input (V_{IN}), the ADC10462 has two inputs (V_{IN0} and V_{IN1}), and the ADC10464 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND
These are the power supply ground pins. The ADC10461 has a single ground pin (GND), and the ADC10462 and ADC10464 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. For the devices with two ground pins, both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE output pins.

SPEED ADJ (ADC10462 and ADC10464 only). This pin is normally left unconnected, but by connecting a resistor between this pin and ground, the conversion time can be reduced. See the Typical Performance Curves and the table of Electrical Characteristics.

6

National Semiconductor

ADC1061
10-Bit High-Speed µP-Compatible A/D Converter with Track/Hold Function

General Description

Using a modified half-flash conversion technique, the 10-bit ADC1061 CMOS analog-to-digital converter offers very fast conversion times yet dissipates a maximum of only 235 mW. The ADC1061 performs a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches.

The analog input voltage to the ADC1061 is tracked and held by an internal sampling circuit. Input signals at frequencies from DC to greater than 160 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

For ease of interface to microprocessors, the ADC1061 has been designed to appear as a memory location or I/O port without the need for external interface logic.

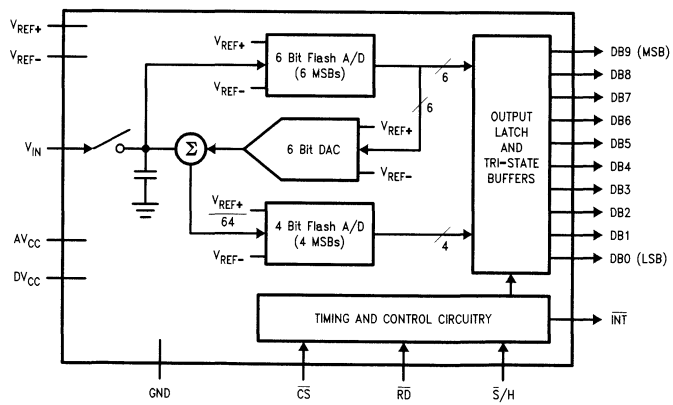
Features

- 1.8 µs maximum conversion time to 10 bits
- Low power dissipation: 235 mW (maximum)
- Built-in track-and-hold
- No external clock required
- Single +5V supply
- No missing codes over temperature

Applications

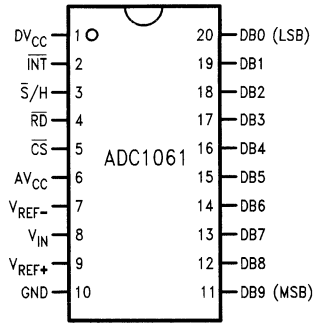
- Waveform digitizers
- Disk drives
- Digital signal processor front ends
- Mobile telecommunications

Simplified Block and Connection Diagrams



Simplified Block and Connection Diagrams (Continued)

Dual-In-Line Package



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Top View
Order Number
ADC1061CIN or ADC1061CIWM
See NS Package J20A,
M20B or N20A

Ordering Information

Industrial ($-40^{\circ}C \leq T_A \leq 85^{\circ}C$)	Package
ADC1061CIN	N20A
ADC1061CIWM	M20B

Pin Descriptions

Symbol	Function
DV_{CC}, AV_{CC} (1, 6)	These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.
$\overline{INT}$ (2)	This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.
$\overline{S}$ /H (3)	This is the Sample/Hold control input. When this pin is forced low, it causes the analog input signal to be sampled and initiates a new conversion.
$\overline{RD}$ (4)	This is the active low Read control input. When this pin is low, any data present in the ADC1061's output registers will be placed on the data bus. In Mode 2, the Read signal must be low until $\overline{INT}$ goes low. Until $\overline{INT}$ goes low, the data at the output pins will be incorrect.
$\overline{CS}$ (5)	This is the active low Chip Select control input. This pin enables the $\overline{S}$ /H and $\overline{RD}$ inputs.
V_{REF-}, V_{REF+} (7, 9)	These are the reference voltage inputs. They may be placed at any voltage between GND − 50 mV and V_{CC} + 50 mV, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to V_{REF+} − 1LSB produces an output code of 1023.
V_{IN} (8)	This is the analog input pin. The impedance of the source should be less than 500Ω for best accuracy and conversion speed. To avoid damage to the ADC1061, V_{IN} should not be allowed to extend beyond the power supply voltages by more than 300 mV unless the drive current is limited. For accurate conversions, V_{IN} should not extend more than 50 mV beyond the supply voltages.
GND (10)	This is the power supply ground pin. The ground pin should be connected to a "clean" ground reference point.
DB0–DB9 (11-20)	These are the TRI-STATE output pins.

National Semiconductor

ADC10662/ADC10664
10-Bit 360 ns A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative, patented multistep® conversion technique, the 10-bit ADC10662 and ADC10664 are 2- and 4-input CMOS analog-to-digital converters offering sub-microsecond conversion times yet dissipating a maximum of only 235 mW. The ADC10662 and ADC10664 perform a 10-bit conversion in two lower-resolution "flashes", thus yielding a fast A/D without the cost, power dissipation, and other problems associated with true flash approaches. In addition to standard static performance specifications (Linearity, Full-Scale Error, etc.) dynamic performance (THD, S/N) is guaranteed.

The analog input voltage to the ADC10662 and ADC10664 is sampled and held by an internal sampling circuit. Input signals at frequencies from dc to over 250 kHz can therefore be digitized accurately without the need for an external sample-and-hold circuit.

The ADC10662 and ADC10664 include a "speed-up" pin. Connecting an external resistor between this pin and ground reduces the typical conversion time to as little as 360 ns.

For ease of interface to microprocessors, the ADC10662 and ADC10664 have been designed to appear as a memory location or I/O port without the need for external interface logic.

Features

- Built-in sample-and-hold
- Single +5V supply
- 2- or 4-input multiplexer options
- No external clock required

Key Specifications

- Conversion time to 10 bits: 360 ns typical, 466 ns max over temperature
- Sampling Rate: 1.5 MHz (min)
- Low power dissipation: 235 mW (max)
- Total harmonic distortion (50 kHz): −60 dB (max)
- No missing codes over temperature

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications

Ordering Information

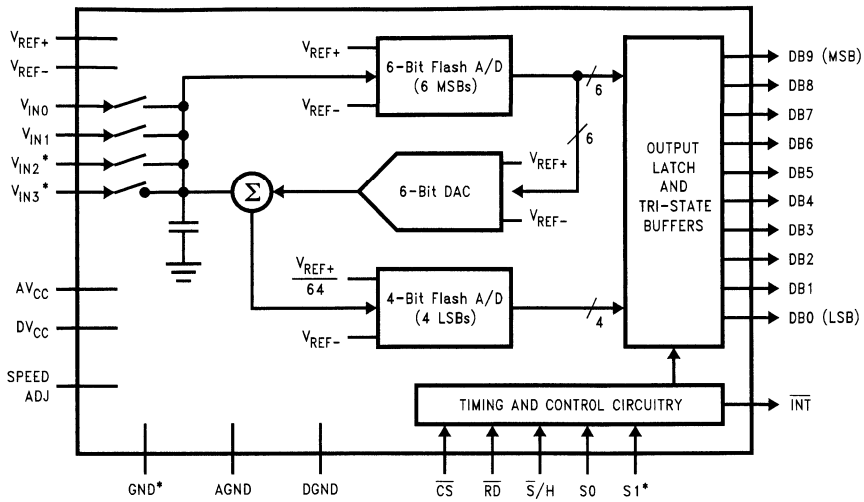
ADC10662

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC10662CIWM	M24B Small Outline

ADC10664

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC10664CIWM	M28B Small Outline

Simplified Block Diagram



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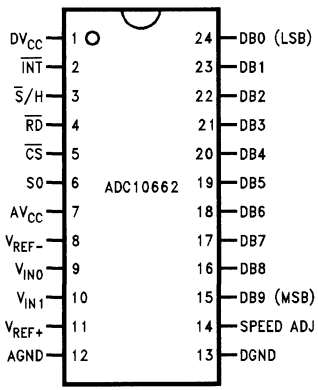
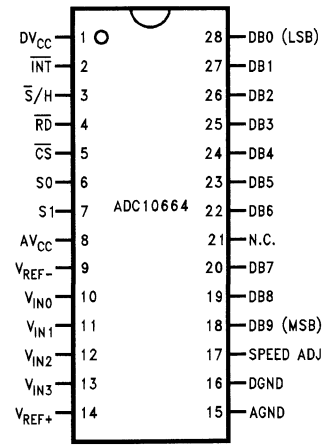
*ADC10664 Only

Connection Diagrams



01119210

Top View



01119211

Top View

Pin Descriptions

DV_{CC}, AV_{CC}
These are the digital and analog positive supply voltage inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor to ground.

$\overline{INT}$ This is the active low interrupt output. $\overline{INT}$ goes low at the end of each conversion, and returns to a high state following the rising edge of $\overline{RD}$.

$\overline{S}$ /H This is the Sample/Hold control input. When this pin is forced low (and $\overline{CS}$ is low), it causes the analog input signal to be sampled and initiates a new conversion.

$\overline{RD}$ This is the active low Read control input. When this $\overline{RD}$ and $\overline{CS}$ are low, any data present in the output registers will be placed on the data bus.

$\overline{CS}$ This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$ and $\overline{S}$ /H pins.

S0, S1 These pins select the analog input that will be connected to the A/D during the conversion. The input is selected based on the state of S0 and S1 when $\overline{S}$ /H makes its High-to-Low transition (See the Timing Diagrams). The ADC10664 includes both S0 and S1. The ADC10662 includes just S0.

V_{REF-}, V_{REF+}
These are the reference voltage inputs. They may be placed at any voltage between GND and V_{CC}, but V_{REF+} must be greater than V_{REF-}. An input voltage equal to V_{REF-} produces an output code of 0, and an input voltage equal to (V_{REF+} − 1 LSB) produces an output code of 1023.

V_{IN0}, V_{IN1}, V_{IN2}, V_{IN3}
These are the analog input pins. The ADC10662 has two inputs (V_{IN0} and V_{IN1}) and the ADC10664 has four inputs (V_{IN0}, V_{IN1}, V_{IN2} and V_{IN3}). The impedance of the source should be less than 500Ω for best accuracy and conversion speed. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV above V_{CC} or 50 mV below ground.

GND, AGND, DGND
These are the power supply ground pins. The ADC10662 and ADC10664 have separate analog and digital ground pins (AGND and DGND) for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. Both pins should be returned to the same potential.

DB0–DB9 These are the TRI-STATE output pins.

SPEED ADJ
By connecting a resistor between this pin and ground, the conversion time can be reduced. The specifications listed in the table of Electrical Characteristics apply for a speed adjust resistor (R_{SA}) equal to 14.0 kΩ (Mode 1) or 8.26 kΩ (Mode 2). See the Typical Performance Curves and the table of Electrical Characteristics.

National Semiconductor

ADC10731/ADC10732/ADC10734/ADC10738 10-Bit Plus Sign Serial I/O A/D Converters with Mux, Sample/Hold and Reference

General Description

This series of CMOS 10-bit plus sign successive approximation A/D converters features versatile analog input multiplexers, sample/hold and a 2.5V band-gap reference. The 1-, 2-, 4-, or 8-channel multiplexers can be software configured for single-ended or differential mode of operation.

An input sample/hold is implemented by a capacitive reference ladder and sampled-data comparator. This allows the analog input to vary during the A/D conversion cycle.

In the differential mode, valid outputs are obtained even when the negative inputs are greater than the positive because of the 10-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE™ serial data exchange standard for easy interface to the COPS™ and HPC™ families of controllers, and can easily interface with standard shift registers and microprocessors.

Features

- 0V to 5V analog input range with single 5V power supply
- Serial I/O (MICROWIRE compatible)
- 1-, 2-, 4-, or 8-channel differential or single-ended multiplexer
- Software or hardware power down
- Analog input sample/hold function
- Ratiometric or absolute voltage referencing
- No zero or full scale adjustment required
- No missing codes over temperature
- TTL/CMOS input/output compatible
- Standard DIP and SO packages

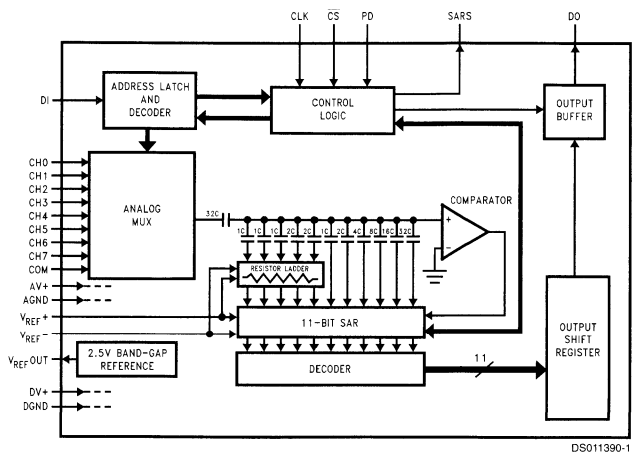
Key Specifications

■ Resolution	10 bits plus sign
■ Single supply	5V
■ Power dissipation	37 mW (Max)
■ In powerdown mode	18 µW
■ Conversion time	5µs (Max)
■ Sampling rate	74 kHz (Max)
■ Band-gap reference	2.5V ±2% (Max)

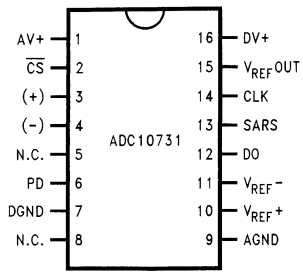
Applications

- Medical instruments
- Portable and remote instrumentation
- Test equipment

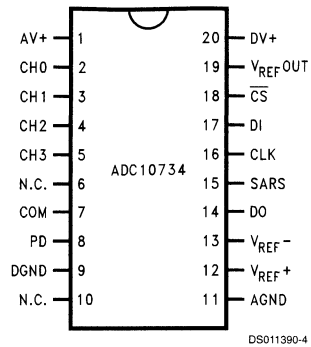
ADC10738 Simplified Block Diagram



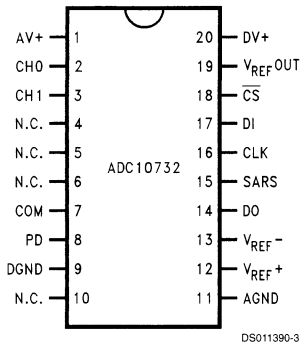
Connection Diagrams



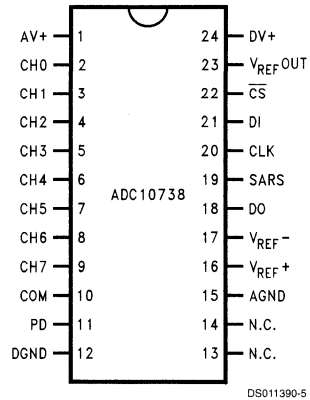
Top View
See NS Package Number M16B



Top View
See NS Package Number M20B

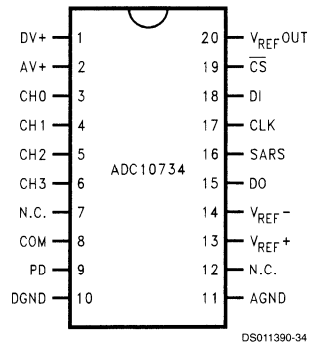


Top View
See NS Package Number M20B



Top View
See NS Package Number M24B

SSOP Package



See NS Package Number MSA20

Ordering Information

Industrial Temperature Range $-40^{\circ}C \leq T_A \leq +85^{\circ}C$	Package
ADC10731CIWM	M16B
ADC10732CIWM	M20B
ADC10734CIMSA	MSA20
ADC10734CIWM	M20B
ADC10738CIWM	M24B

Pin Descriptions

CLK — The clock applied to this input controls the successive approximation conversion time interval, the acquisition time and the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address shift register. This address controls which channel of the analog input multiplexer (MUX) is selected. The falling edge shifts the data resulting from the A/D conversion out on DO. $\overline{CS}$ enables or disables the above functions. The clock frequency applied to this input can be between 5 kHz and 3 MHz.

DI — This is the serial data input pin. The data applied to this pln is shifted by CLK into the multiplexer address register. *Tables 1, 2, 3* show the multiplexer address assignment.

DO — The data output pin. The A/D conversion result (DB0-SIGN) are clocked out by the failing edge of CLK on this pin.

$\overline{CS}$ — This is the chip select input pin. When a logic low is applied to this pin, the rising edge of CLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE after a conversion has been completed.

PD — This is the power down input pin. When a logic high is applied to this pin the A/D is powered down. When a low is applied the A/D is powered up.

SARS — This is the successive approximation register status output pin. When $\overline{CS}$ is high this pin is in TRI-STATE. With $\overline{CS}$ low this pin is active high when a conversion is in progress and active low at all other times.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of CLK into the address register (see *Tables 1, 2, 3*).

The voltage applied to these inputs should not exceed AV^+ or go below GND by more than 50 mV. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input pln. It can be used as a "pseudo ground" when the analog multiplexer is single-ended.

$V_{REF}+$ — This is the positive analog voltage reference input. In order to malntaln accuracy, the voltage range V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is 0.5 V_{DC} to 5.0 V_{DC} and the voltage at $V_{REF}+$ cannot exceed AV^+ +50 mV.

$V_{REF}-$ — The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND – 50 mV or exceed AV^+ + 50 mV.

AV^+, DV^+ — These are the analog and digital power supply pins. These pins should be tied to the same power supply and bypassed separately. The operating voltage range of AV^+ and DV^+ is 4.5 V_{DC} to 5.5 V_{DC}.

DGND — This is the digital ground pin.

AGND — This is the analog ground pin.

National Semiconductor

ADC10D020
Dual 10-Bit, 20 MSPS, 150 mW A/D Converter

General Description

The ADC10D020 is a dual low power, high performance CMOS analog-to-digital converter that digitizes signals to 10 bits resolution at sampling rates up to 30 MSPS while consuming a typical 150 mW from a single 3.0V supply. No missing codes is guaranteed over the full operating temperature range. The unique two stage architecture achieves 9.5 Effective Bits over the entire Nyquist band at 20 MHz sample rate. An output formatting choice of straight binary or 2's complement coding and a choice of two gain settings eases the interface to many systems. Also allowing great flexibility of use is a selectable 10-bit multiplexed or 20-bit parallel mode. An offset correction feature nulls the offset error to less than 1 LSB.

To ease interfacing to most low voltage systems, the digital output power pins of the ADC10D020 can be tied to a separate supply voltage of 1.5V to 3.6V, making the outputs compatible with other low voltage systems. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power state where it typically consumes less than 1 mW and from which recovery is about 1 ms. Bringing the STBY (Standby) pin high places the converter into a standby mode where power consumption is about 27 mW and from which recovery is 800 ns.

The ADC10D020's speed, resolution and single supply operation makes it well suited for a variety of applications, including high speed portable applications.

Operating over the industrial ($-40^\circ \leq T_A \leq +85^\circ C$) temperature range, the ADC10D020 is available in a 48-pin TQFP. An evaluation board is available to ease the design effort.

Features

- Internal sample-and-hold
- Dual gain settings
- Offset correction
- Selectable straight binary or 2's complement output
- Multiplexed or parallel output bus
- Single +2.7V to 3.6V operation
- Power down and standby modes
- 3V TTL Logic input/output compatible

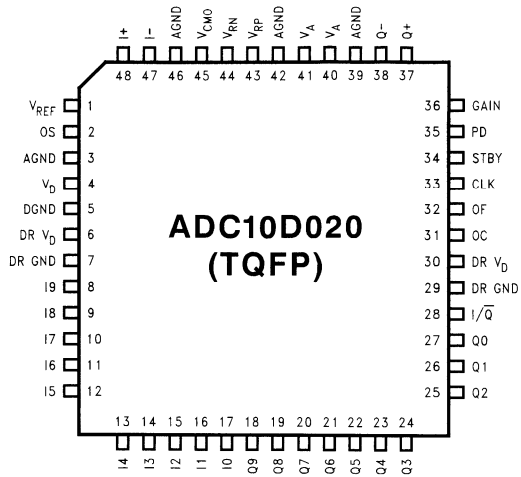
Key Specifications

■ Resolution	10 Bits
■ Conversion Rate	20 MSPS
■ ENOB	9.5 Bits (typ)
■ DNL	0.35 LSB (typ)
■ Conversion Latency Parallel Outputs	2.5 Clock Cycles
— Multiplexed Outputs, I Data Bus	2.5 Clock Cycles
— Multiplexed Outputs, Q Data Bus	3 Clock Cycles
■ PSRR	50 dB
■ Power Consumption—Normal Operation	150 mW (typ)
— Power Down Mode	1 mW (typ)
— Fast Recovery Standby Mode	27 mW (typ)

Applications

- Digital Video
- CCD Imaging
- Portable Instrumentation
- Communications
- Medical Imaging
- Ultrasound

Connection Diagram

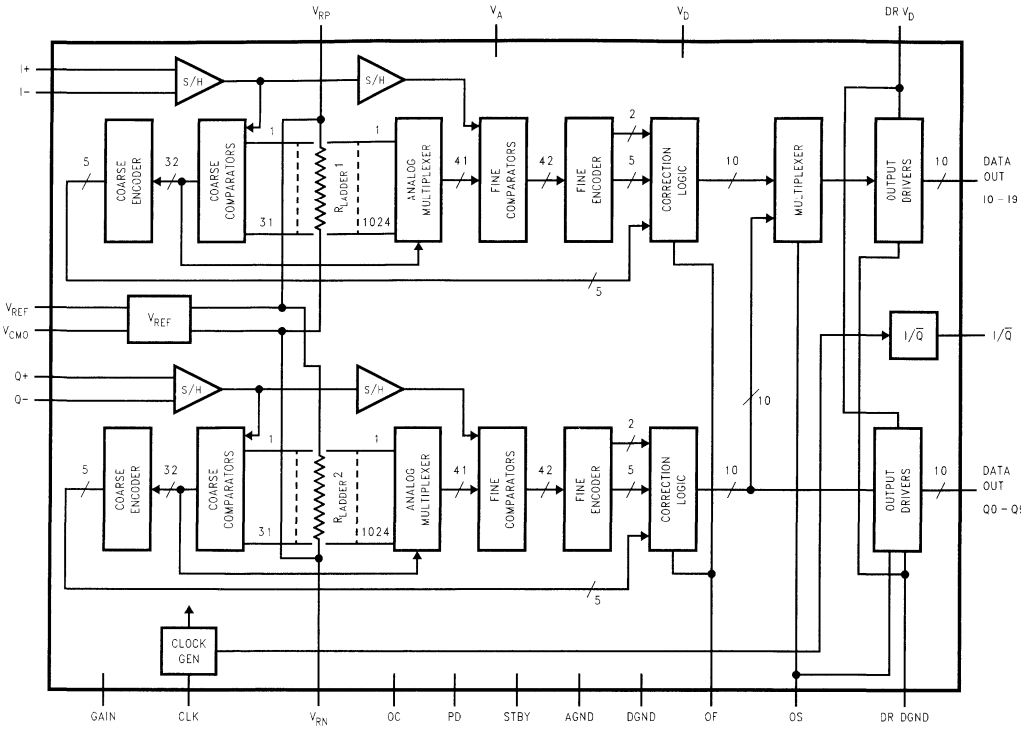


TOP VIEW

Ordering Information

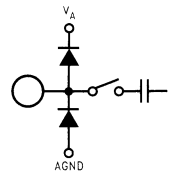
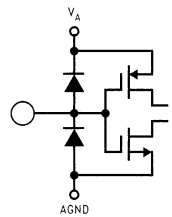
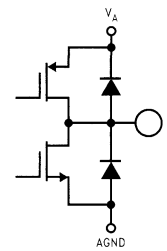
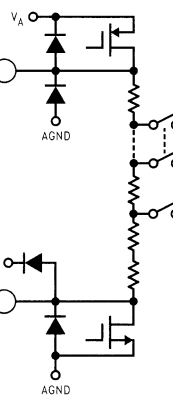
Industrial Temperature Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10D020CIVS	TQFP
ADC10D020EVAL	Evaluation Board

Block Diagram

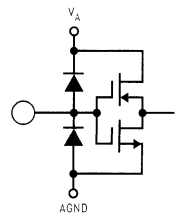
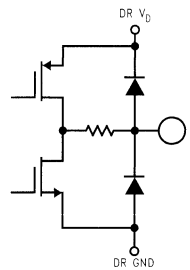


20025502

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
48 47	I+ I−		Analog inputs to "I" ADC. Nominal conversion range is 1.25V to 1.75V with GAIN pin low, or 1.0V to 2.0V with GAIN pin high.
37 38	Q+ Q−		Analog inputs to "Q" ADC. Nominal conversion range is 1.25V to 1.75V with GAIN pin low, or 1.0V to 2.0V with GAIN pin high.
1	V_{REF}		Analog Reference Voltage input. The voltage at this pin should be in the range of 0.8V to 1.5V. With 1.0V at this pin and the GAIN pin *low*, the full scale differential inputs are 1 V_{P-P}. With 1.0V at this pin and the GAIN pin *high*, the full scale differential inputs are 2 V_{P-P}. This pin should be bypassed with a 1 µF capacitor.
45	V_{CMO}		This is an analog output which can be used to set the common mode voltage of the input. It should be bypassed with a minimum of 2 µF low ESR capacitor in parallel with a 0.1 µF capacitor. This pin has a nominal output voltage of 1.5V and has a 1 mA output capability.
43	V_{RP}		Top of the reference ladder. **Do not drive this pin.** Bypass this pin with a 10 µF low ESR capacitor and a 0.1 µF capacitor.
44	V_{RN}		Bottom of the reference ladder. **Do not drive this pin.** Bypass this pin with a 10 µF low ESR capacitor and a 0.1 µF capacitor.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
33	CLK		Digital clock input for both converters. The analog inputs are sampled on the falling edge of this clock input.
2	OS		Output Bus Select. With this pin at a logic high, both the "I" and the "Q" data are present on their respective 10-bit output buses (Parallel mode of operation). When this pin is at a logic low, the "I" and "Q" data are multiplexed onto the "I" output bus and the "Q" output lines all remain at a logic low (multiplexed mode).
31	OC		Offset Correct pin. A low-to-high transition on this pin initiates an independent offset correction sequence for each converter, which takes 34 clock cycles to complete. During this time 32 conversions are taken and averaged. The result is subtracted from subsequent conversions. Each input pair should have 0V differential value during this entire 34 clock period.
32	OF		Output Format pin. When this pin is LOW the output format is Straight Binary. When this pin is HIGH the output format is 2's complement. This pin may be changed "on the fly", but this will result in errors for one or two conversions.
34	STBY		Standby pin. The device operates normally with a logic low on this and the PD (Power Down) pin. With this pin at a logic high and the PD pin at a logic low, the device is in the standby mode where it consumes just 27 mW of power. It takes just 800 ns to come out of this mode after the STBY pin is brought low.
35	PD		Power Down pin that, when high, puts the converter into the Power Down mode where it consumes just 1 mW of power. It takes 1 ms to recover from this mode after the PD pin is brought low. If both the STBY and PD pins are low simultaneously, the PD pin dominates.
36	GAIN		This pin sets the internal signal gain at the inputs to the ADCs. With this pin low the full scale differential input peak-to-peak signal is equal to V_{REF}. With this pin high the full scale differential input peak-to-peak signal is equal to 2 x V_{REF}.
8 thru 27	I0–I9 and Q0–Q9		3V TTL/CMOS-compatible Digital Output pins that provide the conversion results of the I and Q inputs. I0 and Q0 are the LSBs, I9 and Q9 are the MSBs. Valid data is present just after the rising edge of the CLK input in the Parallel mode. In the multiplexed mode, valid data is present just after the rising edge of the CLK input for I0–I9 and just after the falling edge of the CLK input for Q0–Q9.
28	$I/\overline{Q}$		Output data valid signal. In the multiplexed mode, this pin transitions from low to high when the data bus transitions from Q-data to I-data, and from high to low when the data bus transitions from I-data to Q-data. In the Parallel mode, this pin transitions from low to high as the output data changes.
40, 41	V_A		Positive analog supply pin. This pin should be connected to a quiet voltage source of +2.7V to +3.6V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
4	V_D		Positive digital supply pins. These pins should be connected to a quiet voltage source of +2.7V to +3.6V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.
6, 30	DR V_D		Positive digital output pins. These pins should be connected to a clean, quiet voltage source of +1.5V to V_D and be bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors. These pins should also be well decoupled from V_A and V_D and never exceed V_D.
3, 39, 42, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10D020 package.
5	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10D020 package.
7, 29	DR GND		The ground return of the digital output drivers.

National Semiconductor

PRELIMINARY

ADC10D040
Dual 10-Bit, 40 MSPS, 210 mW A/D Converter

General Description

The ADC10D040 is a dual low power, high performance CMOS analog-to-digital converter that digitizes signals to 10 bits resolution at sampling rates up to 45 MSPS while consuming a typical 210 mW from a single 3.0V supply. No missing codes is guaranteed over the full operating temperature range. The unique two stage architecture achieves 9.2 Effective Bits over the entire Nyquist band at 40 MHz sample rate. An output formatting choice of straight binary or 2's complement coding and a choice of two gain settings eases the interface to many systems. Also allowing great flexibility of use is a selectable 10-bit multiplexed or 20-bit parallel mode. An offset correction feature nulls the offset error to less than 1 LSB.

To ease interfacing to most low voltage systems, the digital output power pins of the ADC10D040 can be tied to a separate supply voltage of 1.5V to 3.6V, making the outputs compatible with other low voltage systems. When not converting, power consumption can be reduced by pulling the PD (Power Down) pin high, placing the converter into a low power state where it typically consumes less than 1 mW and from which recovery is about 1 ms. Bringing the STBY (Standby) pin high places the converter into a standby mode where power consumption is about 27 mW and from which recovery is 800 ns.

The ADC10D040's speed, resolution and single supply operation makes it well suited for a variety of applications, including high speed portable applications.

Operating over the industrial ($-40^\circ \le T_A \le +85^\circ C$) temperature range, the ADC10D040 is available in a 48-pin TQFP. An evaluation board is available to ease the design effort.

Features

- Internal sample-and-hold
- Dual gain settings
- Offset correction
- Selectable straight binary or 2's complement output
- Multiplexed or parallel output bus
- Single +2.7V to 3.6V operation
- Power down and standby modes
- 3V TTL Logic input/output compatible

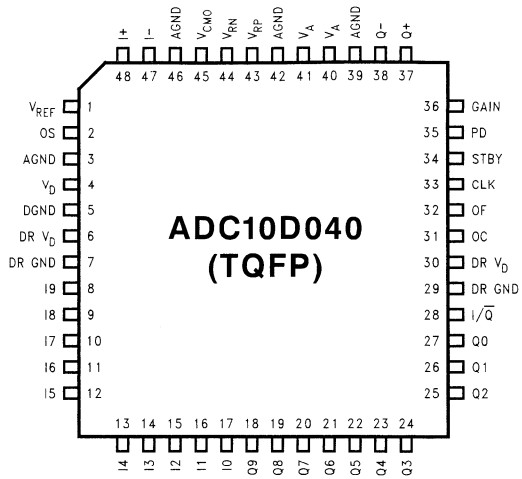
Key Specifications

■ Resolution	10 Bits
■ Conversion Rate	40 MSPS
■ ENOB	9.2 Bits (typ)
■ DNL	0.35 LSB (typ)
■ Conversion Latency Parallel Outputs	2.5 Clock Cycles
— Multiplexed Outputs, I Data Bus	2.5 Clock Cycles
— Multiplexed Outputs, Q Data Bus	3 Clock Cycles
■ PSRR	50 dB
■ Power Consumption — Normal Operation	210 mW (typ)
— Power Down Mode	1 mW (typ)
— Fast Recovery Standby Mode	27 mW (typ)

Applications

- Digital Video
- CCD Imaging
- Portable Instrumentation
- Communications
- Medical Imaging
- Ultrasound

Connection Diagram

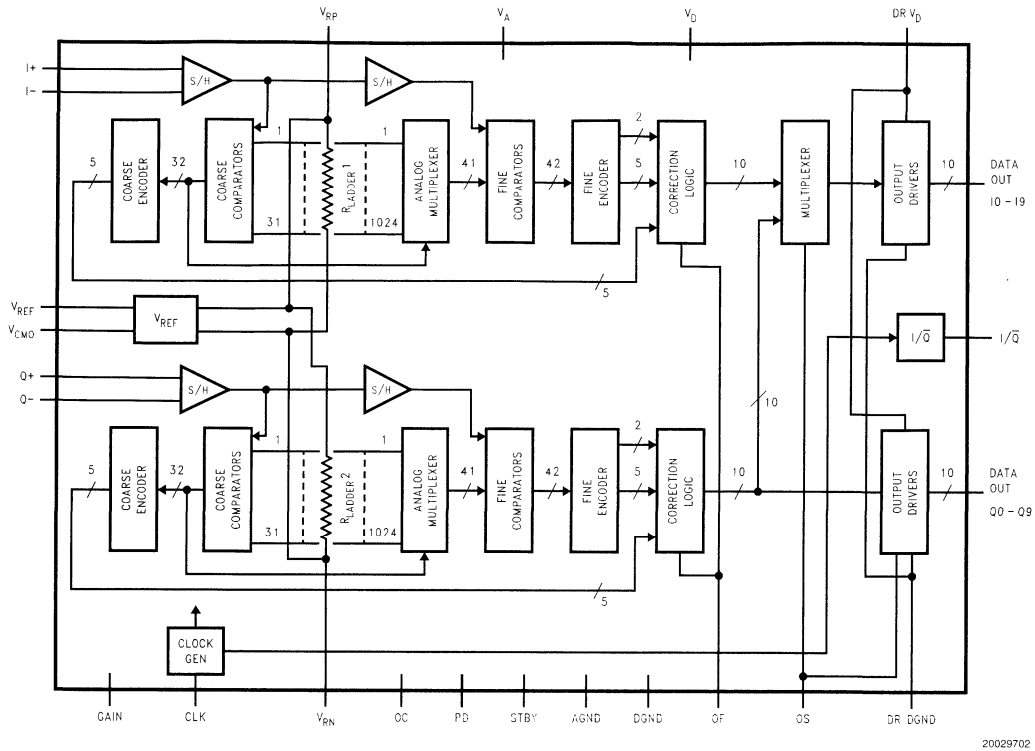


TOP VIEW

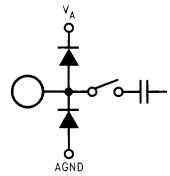
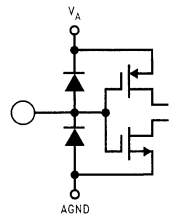
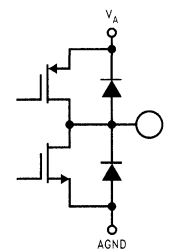
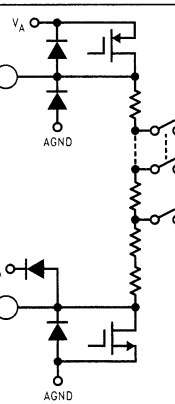
Ordering Information

Industrial Temperature Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC10D040CIVS	TQFP
ADC10D040EVAL	Evaluation Board

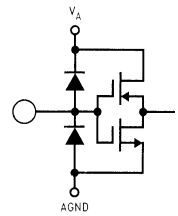
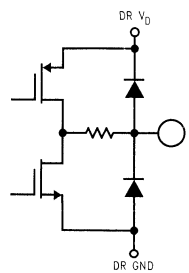
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
48 47	I+ I−		Analog inputs to "I" ADC. Nominal conversion range is 1.25V to 1.75V with GAIN pin low, or 1.0V to 2.0V with GAIN pin high.
37 38	Q+ Q−		Analog inputs to "Q" ADC. Nominal conversion range is 1.25V to 1.75V with GAIN pin low, or 1.0V to 2.0V with GAIN pin high.
1	V_{REF}		Analog Reference Voltage input. The voltage at this pin should be in the range of 0.8V to 1.5V. With 1.0V at this pin and the GAIN pin *low*, the full scale differential inputs are 1 V_{P-P}. With 1.0V at this pin and the GAIN pin *high*, the full scale differential inputs are 2 V_{P-P}. This pin should be bypassed with a 1 µF capacitor.
45	V_{CMO}		This is an analog output which can be used to set the common mode voltage of the input. It should be bypassed with a minimum of 2 µF low ESR capacitor in parallel with a 0.1 µF capacitor. This pin has a nominal output voltage of 1.5V and has a 1 mA output capability.
43	V_{RP}		Top of the reference ladder. **Do not drive this pin.** Bypass this pin with a 10 µF low ESR capacitor and a 0.1 µF capacitor.
44	V_{RN}		Bottom of the reference ladder. **Do not drive this pin.** Bypass this pin with a 10 µF low ESR capacitor and a 0.1 µF capacitor.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
33	CLK		Digital clock input for both converters. The analog inputs are sampled on the falling edge of this clock input.
2	OS		Output Bus Select. With this pin at a logic high, both the "I" and the "Q" data are present on their respective 10-bit output buses (Parallel mode of operation). When this pin is at a logic low, the "I" and "Q" data are multiplexed onto the "I" output bus and the "Q" output lines all remain at a logic low (multiplexed mode).
31	OC		Offset Correct pin. A low-to-high transition on this pin initiates an independent offset correction sequence for each converter, which takes 34 clock cycles to complete. During this time 32 conversions are taken and averaged. The result is subtracted from subsequent conversions. Each input pair should have 0V differential value during this entire 34 clock period.
32	OF		Output Format pin. When this pin is LOW the output format is Straight Binary. When this pin is HIGH the output format is 2's complement. This pin may be changed "on the fly", but this will result in errors for one or two conversions.
34	STBY		Standby pin. The device operates normally with a logic low on this and the PD (Power Down) pin. With this pin at a logic high and the PD pin at a logic low, the device is in the standby mode where it consumes just 27 mW of power. It takes just 800 ns to come out of this mode after the STBY pin is brought low.
35	PD		Power Down pin that, when high, puts the converter into the Power Down mode where it consumes just 1 mW of power. It takes 1 ms to recover from this mode after the PD pin is brought low. If both the STBY and PD pins are low simultaneously, the PD pin dominates.
36	GAIN		This pin sets the internal signal gain at the inputs to the ADCs. With this pin low the full scale differential input peak-to-peak signal is equal to V_{REF}. With this pin high the full scale differential input peak-to-peak signal is equal to 2 x V_{REF}.
8 thru 27	I0–I9 and Q0–Q9		3V TTL/CMOS-compatible Digital Output pins that provide the conversion results of the I and Q inputs. I0 and Q0 are the LSBs, I9 and Q9 are the MSBs. Valid data is present just after the rising edge of the CLK input in the Parallel mode. In the multiplexed mode, valid data is present just after the rising edge of the CLK input for I0–I9 and just after the falling edge of the CLK input for Q0–Q9.
28	$I/\overline{Q}$		Output data valid signal. In the multiplexed mode, this pin transitions from low to high when the data bus transitions from Q-data to I-data, and from high to low when the data bus transitions from I-data to Q-data. In the Parallel mode, this pin transitions from low to high as the output data changes.
40, 41	V_A		Positive analog supply pin. This pin should be connected to a quiet voltage source of +2.7V to +3.6V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
4	V_D		Positive digital supply pins. These pins should be connected to a quiet voltage source of +2.7V to +3.6V. V_A and V_D should have a common supply and be separately bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors.
6, 30	DR V_D		Positive digital output pins. These pins should be connected to a clean, quiet voltage source of +1.5V to V_D and be bypassed with 10 µF to 50 µF capacitors in parallel with 0.1 µF capacitors. These pins should also be well decoupled from V_A and V_D and never exceed V_D.
3, 39, 42, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC10D040 package.
5	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC10D040 package.
7, 29	DR GND		The ground return of the digital output drivers.

National Semiconductor

ADC1173
8-Bit, 3-Volt, 15MSPS, 33mW A/D Converter

General Description

The ADC1173 is a low power, 15 MSPS analog-to-digital converter that digitizes signals to 8 bits while consuming just 33 mW of power (typ). The ADC1173 uses a unique architecture that achieves 7.6 Effective Bits. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +3V single supply operation, make it ideally suited for many video, imaging and communications applications, including use in portable equipment. Furthermore, the ADC1173 is resistant to latchup and the outputs are short-circuit proof. The top and bottom of the ADC1173's reference ladder is available for connections, enabling a wide range of input possibilities.

The ADC1173 is offered in SOIC (EIAJ) and TSSOP. It is designed to operate over the commercial temperature range of -20°C to +75°C.

Features

- Internal Sample-and-Hold Function
- Single +3V Operation
- Internal Reference Bias Resistors
- Industry Standard Pinout
- TRI-STATE Outputs

Key Specifications

■ Resolution	8 Bits
■ Maximum Sampling Frequency	15 MSPS (min)
■ THD	−56 dB (typ)
■ DNL	±0.8 LSB (max)
■ ENOB at 3.58 MHz Input	7.6 Bits (typ)
■ Guaranteed No Missing Codes	
■ Differential Phase	0.5 Degree (max)
■ Differential Gain	1.5% (typ)
■ Power Consumption	33mW (typ)
■	(excluding reference current)

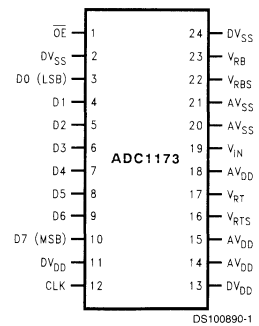
Applications

- Video Digitization
- Digital Still Cameras
- Set Top Boxes
- Camcorders
- Personal Computer Video
- Digital Television
- CCD Imaging
- Electro-Optics

Ordering Information

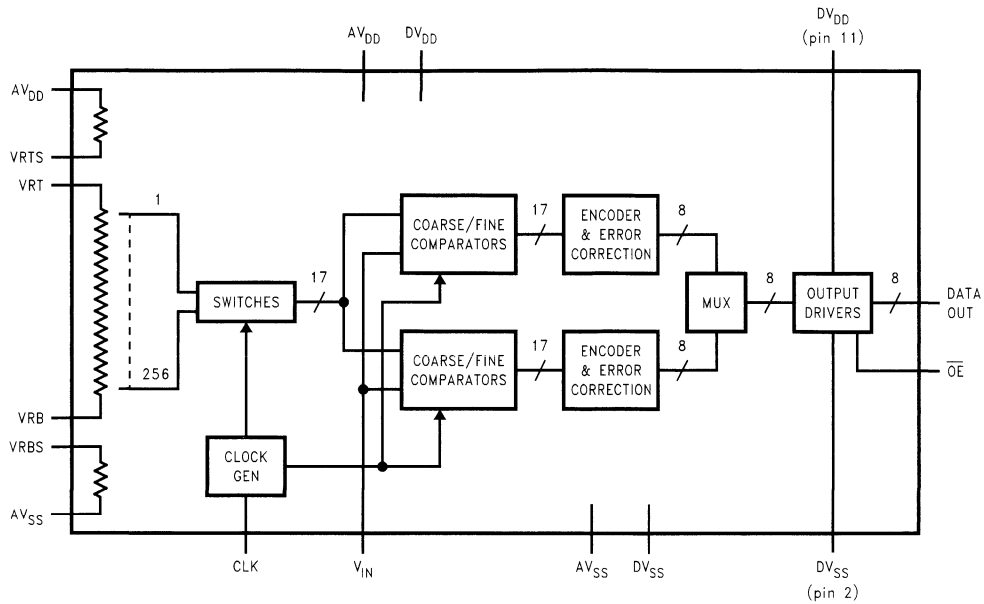
ADC1173CIJM	SOIC (EIAJ)
ADC1173CIJMX	SOIC (EIAJ) (tape & reel)
ADC1173CIMTC	TSSOP
ADC1173CIMTCX	TSSOP (tape & reel)

Pin Configuration



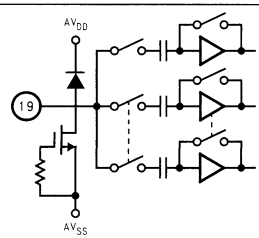
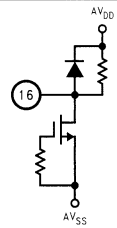
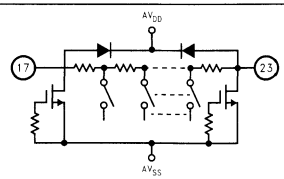
DS100890-1

Block Diagram

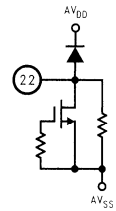
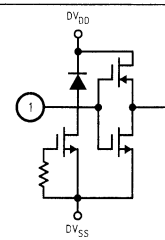
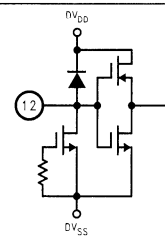
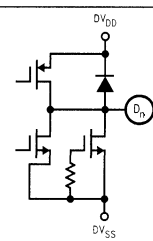


DS100890-2

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
19	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
16	V_{RTS}		Reference Top Bias with internal pull-up resistor. Short this pin to V_{RT} to self bias the reference ladder.
17	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to AV_{DD}. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
23	V_{RB}		Analog Input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0V to 2.0V. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
22	V_{RBS}		Reference Bottom Bias with internal pull down resistor. Short to V_{RB} to self bias the reference ladder.
1	$\overline{OE}$		CMOS/TTL compatible Digital input that, when low, enables the digital outputs of the ADC1173. When high, the outputs are in a high impedance state.
12	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
3 thru 10	D0-D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are enabled by bringing the $\overline{OE}$ pin low.
11, 13	DV_{DD}		Positive digital supply pin. Connect to a clean, quiet voltage source of +3V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10µF capacitor and a 0.1µF ceramic chip capacitor. See Section 3.0 for more information.
2, 24	DV_{SS}		The ground return for the digital supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1173.
14, 15, 18	AV_{DD}		Positive analog supply pin. Connected to a clean, quiet voltage source of +3V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See Section 3.0 for more information.
20, 21	AV_{SS}		The ground return for the analog supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1173 package.

National Semiconductor

ADC1175
8-Bit, 20MHz, 60mW A/D Converter

General Description

The ADC1175 is a low power, 20 Msps analog-to-digital converter that digitizes signals to 8 bits while consuming just 60 mW of power (typ). The ADC1175 uses a unique architecture that achieves 7.5 Effective Bits. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video, imaging and communications applications, including use in portable equipment. Furthermore, the ADC1175 is resistant to latchup and the outputs are short-circuit proof. The top and bottom of the ADC1175's reference ladder is available for connections, enabling a wide range of input possibilities.

The ADC1175 is offered in SOIC (EIAJ) and TSSOP. It is designed to operate over the commercial temperature range of -20°C to +75°C.

Features

- Internal Sample-and-Hold Function
- Single +5V Operation
- Internal Reference Bias Resistors
- Industry Standard Pinout
- TRI-STATE Outputs

Key Specifications

■ Resolution	8 Bits
■ Maximum Sampling Frequency	20 Msps (min)
■ THD	−55 dB (typ)
■ DNL	0.75 LSB (max)
■ ENOB	7.5 Bits (typ)
■ Guaranteed No Missing Codes	
■ Differential Phase	0.5 Degree (typ)
■ Differential Gain	0.4% (typ)
■ Power Consumption (excluding reference current)	60mW (typ)

Applications

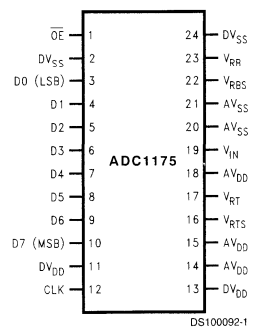
- Video Digitization
- Digital Still Cameras
- Set Top Boxes
- Communications
- Medical Imaging
- Personal Computer Video Cameras
- Digital Television
- CCD Imaging
- Electro-Optics

Ordering Information

ADC1175CIJM	SOIC (EIAJ)
ADC1175CIJMX	SOIC (EIAJ) (tape & reel)
ADC1175CIMTC	TSSOP
ADC1175CIMTCX	TSSOP (tape & reel)

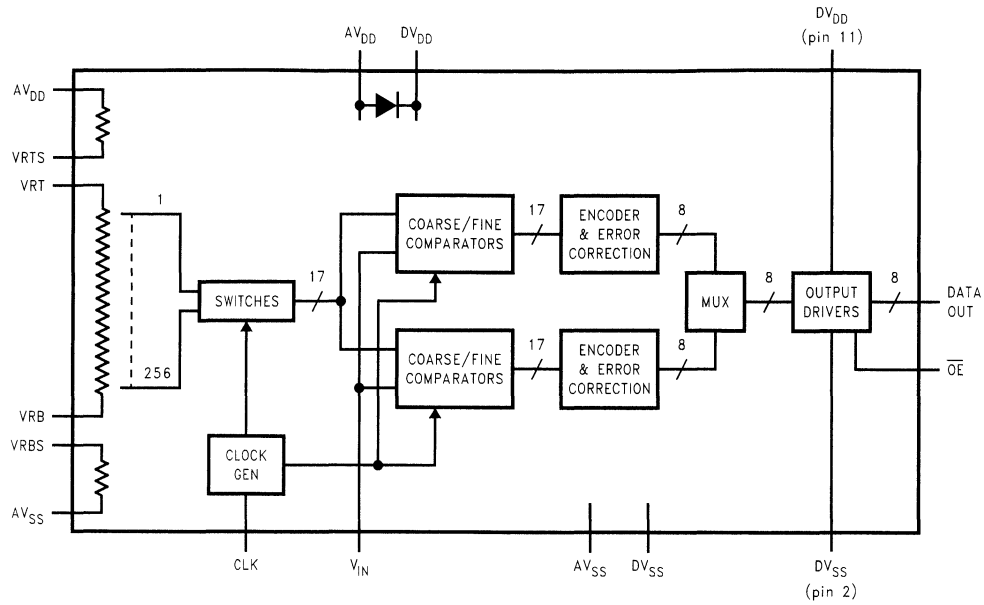
Pin Configuration

ADC1175 Pin Configuration

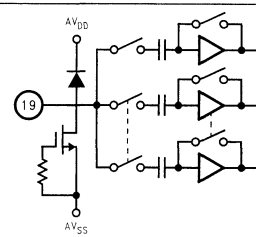
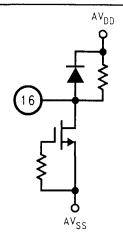
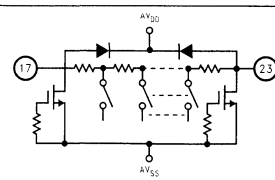


DS100092-1

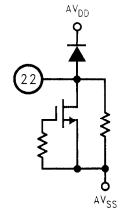
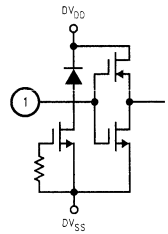
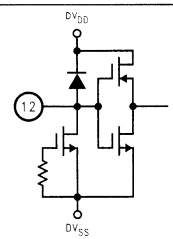
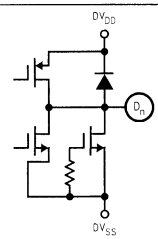
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
19	V_{IN}		Analog signal input. Conversion range is V_{RB} to V_{RT}.
16	V_{RTS}		Reference Top Bias with internal pull-up resistor. Short this pin to V_{RT} to self bias the reference ladder.
17	V_{RT}		Analog Input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to AV_{DD}. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
23	V_{RB}		Analog Input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0V to 4.0V. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
22	V_{RBS}		Reference Bottom Bias with internal pull down resistor. Short to V_{RB} to self bias the reference ladder.
1	$\overline{OE}$		CMOS/TTL compatible Digital input that, when low, enables the digital outputs of the ADC1175. When high, the outputs are in a high impedance state.
12	CLK		CMOS/TTL compatible digital clock Input. V_{IN} is sampled on the falling edge of CLK input.
3 thru 10	D0-D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are enabled by bringing the $\overline{OE}$ pin low.
11, 13	DV_{DD}		Positive digital supply pin. Connect to a clean, quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10µF capacitor and a 0.1µF ceramic chip capacitor. See Section 3.0 for more information.
2, 24	DV_{SS}		The ground return for the digital supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175.
14, 15, 18	AV_{DD}		Positive analog supply pin. Connected to a clean, quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See Section 3.0 for more information.
20, 21	AV_{SS}		The ground return for the analog supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175 package.

National Semiconductor

ADC1175-50
8-Bit, 50 MSPS, 125 mW A/D Converter

General Description

The ADC1175-50 is a low power, 50 MSPS analog-to-digital converter that digitizes signals to 8 bits while consuming just 125 mW (typ). The ADC1175-50 uses a unique architecture that achieves 6.8 Effective Bits at 25 MHz input and 50 MHz clock frequency. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video and imaging applications, including use in portable equipment. Furthermore, the ADC1175-50 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC1175-50's reference ladder is available for connections, enabling a wide range of input possibilities. The low input capacitance (7 pF, typical) makes this device easier to drive than conventional flash converters and the power down mode reduces power consumption to less than 5 mW.

The ADC1175-50 is offered in SOIC (EIAJ), TSSOP and LLP (a molded lead frame-based chip-scale package.) It is designed to operate over the commercial temperature range of −20˚C to +75˚C.

Features

- Internal Track-and-Hold function
- Single +5V operation
- Internal reference bias resistors
- Industry standard pinout
- Power-down mode (<5 mW)

Key Specifications

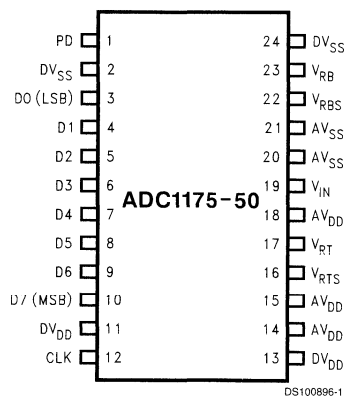
■ Resolution	8 Bits
■ Maximum Sampling Frequency	50 MSPS (min)
■ THD	54 dB (typ)
■ DNL	0.7 LSB (typ)
■ ENOB @ f_{IN} = 25 MHz	6.8 Bits (typ)
■ Guaranteed No Missing Codes	
■ Differential Phase	0.5˚ (typ)
■ Differential Gain	1.0% (typ)
■ Power Consumption (Excluding Reference Current)	125 mW (typ), 190 mW (max)

Applications

- Digital Still Cameras
- CCD Imaging
- Electro-Optics
- Medical Imaging
- Communications
- Video Digitization
- Digital Television
- Multimedia

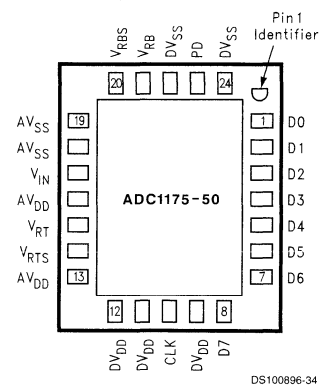
Connection Diagrams

24-pin SOLC and TSSOP



Top View

24-pin LLP (CSP)

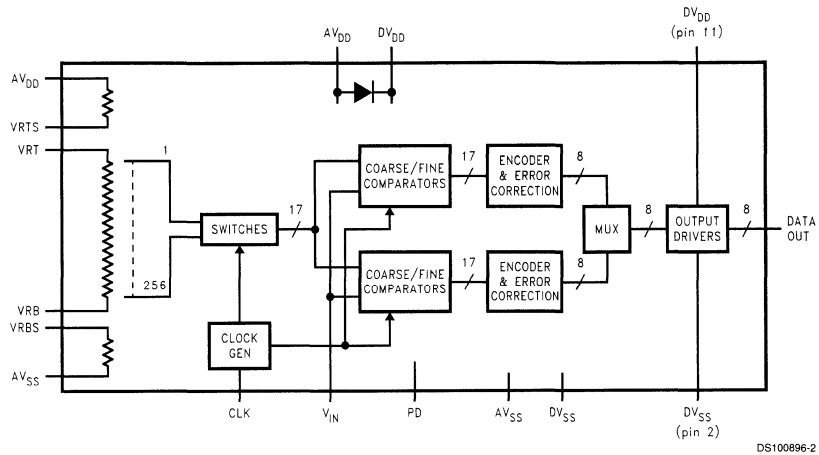


Bottom View

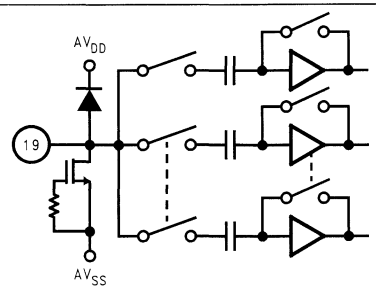
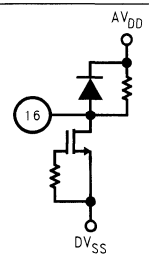
Ordering Information

ADC1175-50CIJM	SOIC (EIAJ)
ADC1175-50CIJMX	SOIC (EIAJ) (tape and reel)
ADC1175-50CIMT	TSSOP
ADC1175-50CIMTX	TSSOP (tape and reel)
ADC1175-50CILQ	LLP (tape and reel - 1, 000 units)
ADC1175-50CILQX	LLP (tape and reel - 4, 500 units)

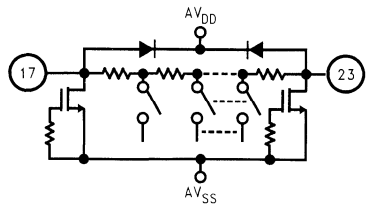
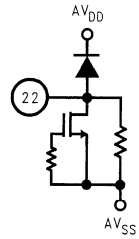
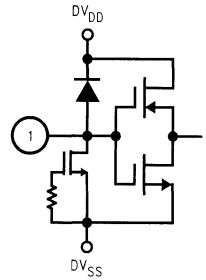
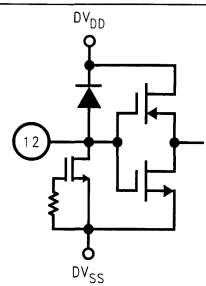
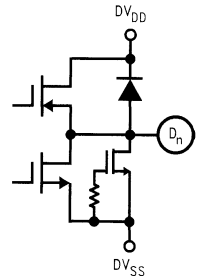
Block Diagram



Pin Descriptions and Equivalent Circuits (LLP pins in parentheses)

Pin No.	Symbol	Equivalent Circuit	Description
19 (17)	V_{IN}		Analog signal input. Conversion range is V_{RT} to V_{RB}.
16 (14)	V_{RTS}		Reference Top Bias with internal pull up resistor. Short this pin to V_{RT} to self-bias the reference ladder.

Pin Descriptions and Equivalent Circuits (LLP pins in parentheses) (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
17 (15)	V_{RT}		Analog input that is the high (top) side of the reference ladder of the ADC. Nominal range is 1.0V to AV_{DD}, optimized value of 2.6V. Voltages on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
23 (21)	V_{RB}		Analog input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0.0V to 4.0V, with optimized value of 0.6V. Voltage on V_{RT} and V_{RB} inputs define the V_{IN} conversion range. Bypass well. See Section 2.0 for more information.
22 (20)	V_{RBS}		Reference Bottom Bias with internal pull down resistor. Short to V_{RB} to self-bias the reference ladder. Bypass well if not grounded. See Section 2.0 for more information.
1 (23)	PD		CMOS/TTL compatible Digital input that, when high, puts the ADC1175-50 into a power-down mode where total power consumption is typically less than 5 mW. With this pin low, the device is in the normal operating mode.
12 (10)	CLK		CMOS/TTL compatible digital clock input. V_{IN} is sampled on the falling edge of CLK input.
3 thru 10 (1 thru 8)	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are in a high impedance mode when the PD pin is low.

Pin Descriptions and Equivalent Circuits (LLP pins in parentheses) (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
11, 13, 14 (9, 11, 12)	DV_{DD}		Positive digital supply pin. Connect to a clean, quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See Section 4.0 for more information.
2, 24 (22, 24)	DV_{SS}		The ground return for the digital supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175-50.
15, 18 (13, 16)	AV_{DD}		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. AV_{DD} and DV_{DD} should have a common source and be separately bypassed with a 10 µF capacitor and a 0.1 µF ceramic chip capacitor. See Section 4.0 for more information.
20, 21 (18, 19)	AV_{SS}		The ground return for the analog supply. AV_{SS} and DV_{SS} should be connected together close to the ADC1175-50 package.

National Semiconductor

ADC12H030/ADC12H032/ADC12H034/ADC12H038, ADC12030/ADC12032/ADC12034/ADC12038 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12030, and ADC12H030 families are 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexers. The ADC12032/ ADC12H032, ADC12034/ADC12H034 and ADC12038/ ADC12H038 have 2, 4 and 8 channel multiplexers, respectively. The differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12030/ADC12H030 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. The ADC12030 family is tested with a 5 MHz clock, while the ADC12H030 family is tested with an 8 MHz clock. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to less than ±1 LSB each.

The analog inputs can be configured to operate in varicus combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +5V) can be accommodated with a single +5V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE. For voltage references see the LM4040 or LM4041.

Applications

- Medical instruments
- Process control systems
- Test equipment

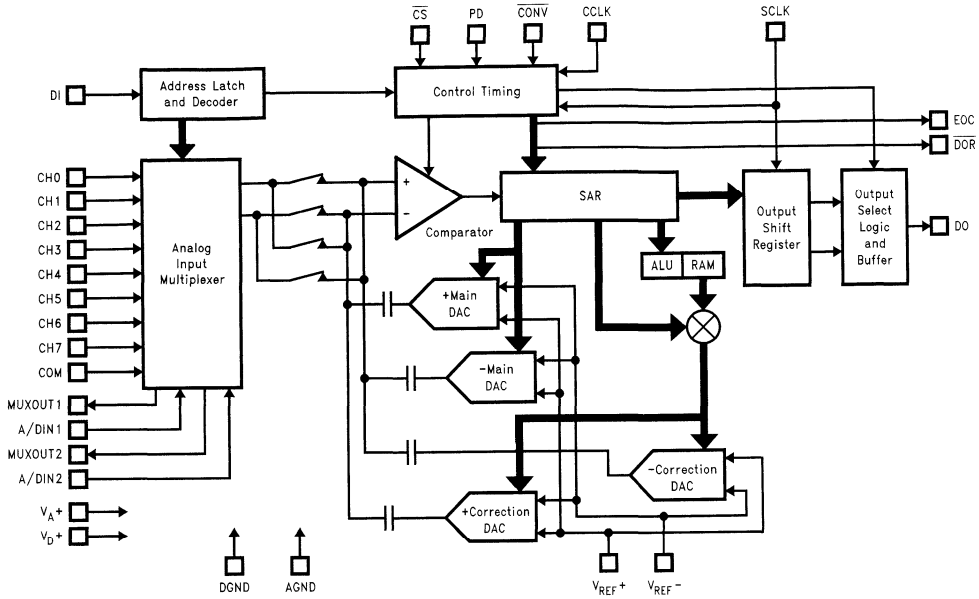
Features

- Serial I/O (MICROWIRE Compatible)
- 2, 4, or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Variable resolution and conversion rate
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- Fully tested and guaranteed with a 4.096V reference
- 0V to 5V analog input range with single 5V power supply
- No Missing Codes over temperature

Key Specifications

■ Resolution	12-bit plus sign
■ 12-bit plus sign conversion time	
– ADC12H30 family	5.5 µs (max)
– ADC12030 family	8.8 µs (max)
■ 12-bit plus sign throughput time	
– ADC12H30 family	8.6 µs (max)
– ADC12030 family	14 µs (max)
■ Integral linearity error	±1 LSB (max)
■ single supply	5V ±10%
■ Power consumption	33 mV (max)
– Power down	100 µW (typ)

ADC12038 Simplified Block Diagram



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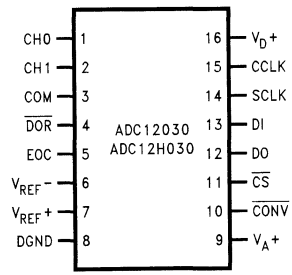
Connection Diagrams

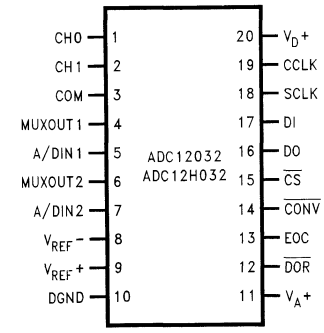
16-Pin Wide Body SO Packages



01135406

Top View

20-Pin Wide Body SO Packages



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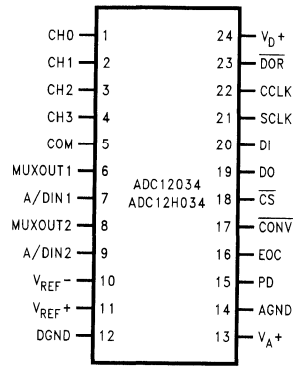
Top View

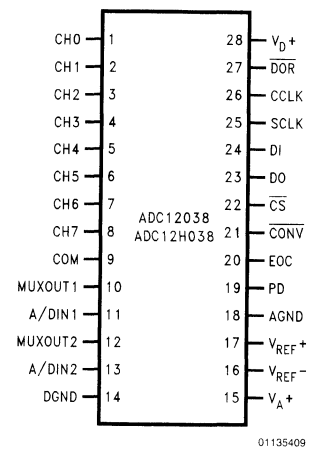
Connection Diagrams (Continued)

24-Pin Wide Body
SO, SSOP-EIAJ Packages



Top View

28-Pin Wide Body
SO Packages



Top View

Ordering Information

Industrial Temperature Range $-40^{\circ}C \le T_A \le +85^{\circ}C$	Package
ADC12H030CIWM, ADC12030CIWM	M16B
ADC12H032CIWM, ADC12032CIWM	M20B
ADC12H034CIN, ADC12034CIN	N24C
ADC12H034CIWM, ADC12034CIWM	M24B
ADC12H034CIMSA	MSA24
ADC12H038CIWM, ADC12038CIWM	M28B

Pin Descriptions

CCLK — The clock applied to this input controls the sucessive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 µs.

SCLK — This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 µs.

DI — This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. *Table 2* through *Table 5* show the assignment of the multiplexer address and the mode select data.

DO — The data output pin. This pin is an active push/pull output when $\overline{CS}$ is low. When $\overline{CS}$ is high, this output is TRI-STATE. The A/D conversion result (D0–D12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see *Table 1*). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see *Table 5*).

EOC — This pin is an active push/pull output and indicates the status of the ADC12030/2/4/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{CS}$ — This is the chip select pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data on DI into the address regis-

Pin Descriptions (Continued)

ter. This low also brings DO out of TRI-STATE. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought back low during a conversion, that conversion is prematurely terminated. The data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought back low during a conversion in progress the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. *Table 5* details the data required.

$\overline{DOR}$ This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{CONV}$ A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming *Table 5* such as 12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.

PD This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 250 µs to power up after the command is given.

CH0–CH7 These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (See *Tables 2, 3, 4*).

The voltage applied to these inputs should not exceed V_A+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2
These are the multiplexer output pins.

A/DIN1, /DIN2 These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_A^+ or go below AGND (see *Figure 5*).

V_{REF}+ This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range of V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is 1 V_{DC} to 5.0 V_{DC} and the voltage at V_{REF}+ cannot exceed V_A+. See *Figure 6* for recommended bypassing.

V_{REF}– The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND or exceed V_A+. (See *Figure 6*).

V_A+, V_D+ These are the analog and digital power supply pins. V_A^+ and V_D^+ are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see *Figure 6*). The operating voltage range of V_A+ and V_D+ is 4.5 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin (see *Figure 6*).

AGND This is the analog ground pin (see *Figure 6*).

National Semiconductor

ADC12040
12-Bit, 40 MSPS, 340 mW A/D Converter with Internal Sample-and-Hold

General Description

The ADC12040 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 40 Megasamples per second (MSPS), minimum. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 5V power supply, this device consumes just 340 mW at 40 MSPS, including the reference current. The Power Down feature reduces power consumption to 40 mW.

The differential inputs provide a full scale input swing equal to V_{REF} with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of −40°C to +85°C.

Features

- Single supply operation
- Internal sample-and-hold
- Outputs 2.5V to 5V compatible
- TTL/CMOS compatible input/outputs
- Low power consumption
- Power down mode
- On-chip reference buffer

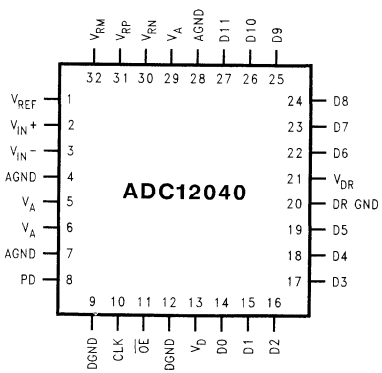
Key Specifications

■ Resolution	12 Bits
■ Conversion Rate	40 MSPS(min)
■ DNL	±0.4 LSB(typ)
■ INL	±0.7 LSB(typ)
■ SNR (f_{IN} = 10MHz)	69 dB(typ)
■ ENOB (f_{IN} = 10MHz)	11.2 bits(typ)
■ Data Latency	6 Clock Cycles
■ Supply Voltage	+5V ±5%
■ Power Consumption, 40 MHz	340 mW(typ)

Applications

- Ultrasound and Imaging
- Instrumentation
- Cellular Base Stations/Communications Receivers
- Sonar/Radar
- xDSL
- Wireless Local Loops/Cable Modems
- HDTV/DTV
- DSP Front Ends

Connection Diagram

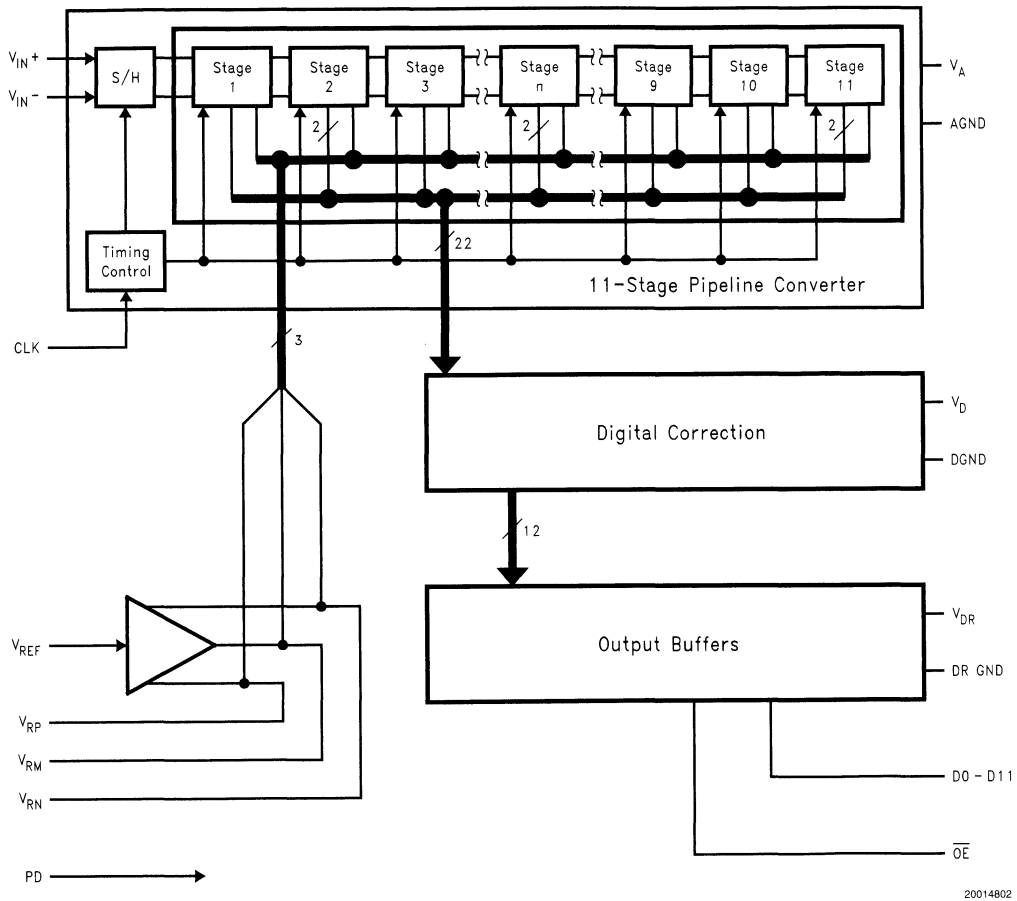


20014801

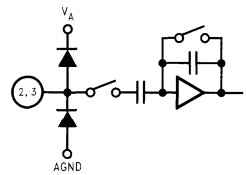
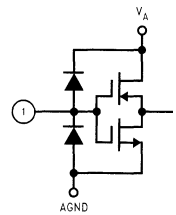
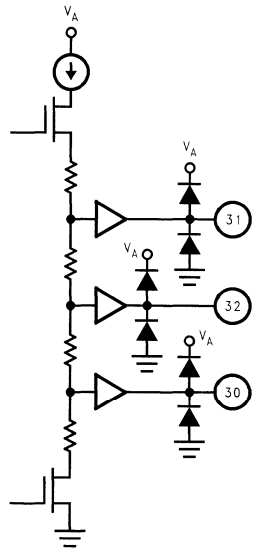
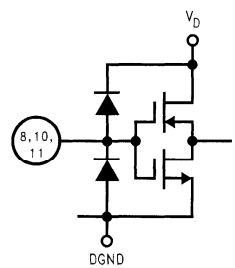
Ordering Information

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC12040CIVY	32 Pin LQFP
ADC12040CIVYX	32 Pin LQFP Tape and Reel
ADC12040EVAL	Evaluation Board

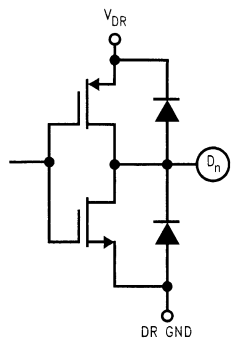
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	V_{IN^+}		Non-Inverting analog signal Input. With a 2.0V reference voltage, the differential input signal level is 2.0 V_{P-P} centered on V_{CM}.
3	V_{IN^-}		Inverting analog signal Input. With a 2.0V reference voltage the input signal level is 2.0 V_{P-P} centered on V_{CM}. This pin may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
1	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 2.0V nominal and should be between 1.0V to 2.2V.
31	V_{RP}		These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to AGND. DO NOT connect anything else to these pins.
32	V_{RM}		
30	V_{RN}		
DIGITAL I/O			
10	CLK		Digital clock input. The range of frequencies for this input is 100 kHz to 50 MHz (typical) with guaranteed performance at 40 MHz. The input is sampled on the rising edge of this input.
11	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE data output pins. When this pin is high, the outputs are in a high impedance state.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the offset binary output word. Output levels are TTL/CMOS compatible.
ANALOG POWER			
5, 6, 29	V_A		Positive analog supply pins. These pins should be connected to a quiet +5V voltage source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to the same quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin.
9, 12	DGND		The ground return for the digital supply.
21	V_{DR}		Positive digital supply pin for the ADC12040's output drivers. This pin should be connected to a voltage source of +2.5V to +5V and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor. V_{DR} should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12040's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12040's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.

National Semiconductor

ADC12041
12-Bit Plus Sign 216 kHz Sampling Analog-to-Digital Converter

General Description

Operating from a single 5V power supply, the ADC12041 is a 12 bit + sign, parallel I/O, self-calibrating, sampling analog-to-digital converter (ADC). The maximum sampling rate is 216 kHz. On request, the ADC goes through a self-calibration process that adjusts linearity, zero and full-scale errors.

The ADC12041 can be configured to work with many popular microprocessors/microcontrollers and DSPs including National's HPC family, Intel386 and 8051, TMS320C25, Motorola MC68HC11/16, Hitachi 64180 and Analog Devices ADSP21xx.

For complementary voltage references see the LM4040, LM4041 or LM9140.

Features

- Fully differential analog input
- Programmable acquisition times and user-controllable throughput rates
- Programmable data bus width (8/13 bits)
- Built-in Sample-and-Hold
- Programmable auto-calibration and auto-zero cycles
- Low power standby mode
- No missing codes

Key Specifications

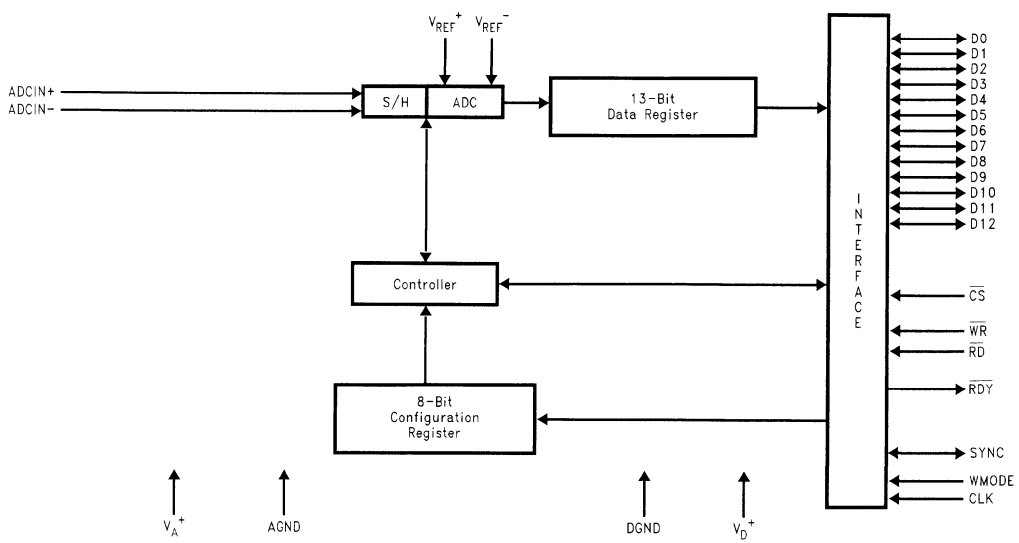
(f_{CLK} = 12 MHz)

■ Resolution	12-bits + sign
■ 13-bit conversion time	3.6 µs, max
■ 13-bit throughput rate	216 ksamples/s, min
■ Integral Linearity Error (ILE)	±1 LSB, max
■ Single supply	+5V ± 10%
■ V_{IN} range	GND to V_A+
■ Power consumption	
— Normal operation	33 mW, max
— Stand-by mode	75 µw, max

Applications

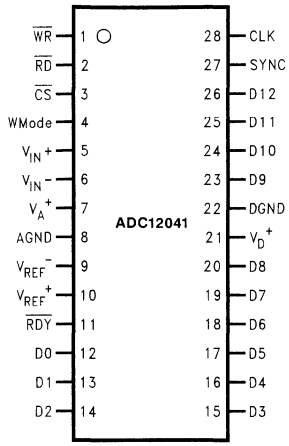
- Medical instrumentation
- Process control systems
- Test equipment
- Data logging
- Inertial guidance

Block Diagram



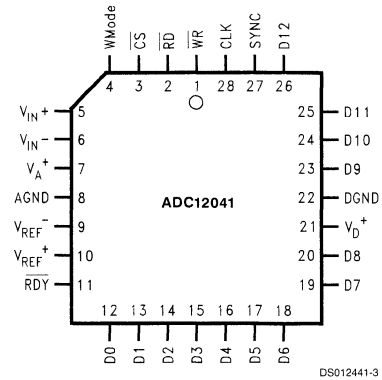
Connection Diagrams

28-Pin SSOP



Order Number ADC12041CIMSA
See NS Package Number MSA28

28-Pin PLCC



Order Number ADC12041CIV
See NS Package Number V28A

Ordering Information

Industrial Temperature Range $-40^{\circ}C \leq T_A \leq +85^{\circ}C$	NS Package Number
ADC12041CIV	PLCC
ADC12041CIMSA	SSOP

Pin Descriptions

PLCC and SSOP Pkg. Pin Number	Pin Name	Description
5 6	$V_{IN}+$ $V_{IN}-$	The analog ADC inputs. $V_{IN}+$ is the non-inverting (positive) input and $V_{IN}-$ is the inverting (negative) input into the ADC.
10	$V_{REF}+$	Positive reference input. The operating voltage range for this input is $1V \leq V_{REF}+ \leq V_A+$ (see *Figure 3* and *Figure 4*). This pin should be bypassed to AGND at least with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
9	$V_{REF}-$	Negative reference input. The operating voltage range for this input is $0V \leq V_{REF}- \leq V_{REF}+ -1$ (see *Figure 3* and *Figure 4*). This pin should be bypassed to AGND at least with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
4	WMODE	The logic state of this pin at power-up determines which edge of the write signal ($\overline{WR}$) will latch in data from the data bus. If tied low, the ADC12041 will latch in data on the rising edge of the $\overline{WR}$ signal. If tied to a logic high, data will be latched in on the falling edge of the $\overline{WR}$ signal. The state of this pin should not be changed after power-up.
27	SYNC	The SYNC pin can be programmed as an **input** or an **output**. The Configuration register's bit b4 controls the function of this pin. When programmed as an input pin (b4 = 1), a rising edge on this pin causes the ADC's sample-and-hold to hold the analog input signal and begin conversion. When programmed as an output pin (b4 = 0), the SYNC pin goes high when a conversion begins and returns low when completed.
12–20 23–26	D0–D8 D9–D12	13-bit Data bus of the ADC12041. D12 is the most significant bit and D0 is the least significant. The BW(bus width) bit of the Configuration register (b3) selects between an 8-bit or 13-bit data bus width. When the **BW** bit is **cleared** (BW = 0), D7–D0 are active and D12–D8 are always in TRI-STATE® . When the BW bit is set (BW = 1), D12–D0 are active.
28	CLK	The clock input pin used to drive the ADC12041. The operating range is 0.05 MHz to 12 MHz.
1	$\overline{WR}$	$\overline{WR}$ is the active low WRITE control input pin. A logic low on this pin and the $\overline{CS}$ will enable the input buffers of the data pins D12–D0. The signal at this pin is used by the ADC12041 to latch in data on D12–D0. The sense of the WMODE pin at power-up will determine which edge of the $\overline{WR}$ signal the ADC12041 will latch in data. See WMODE pin description.
2	$\overline{RD}$	$\overline{RD}$ is the active low read control input pin. A logic low on this pin and $\overline{CS}$ will enable the active output buffers to drive the data bus.
3	$\overline{CS}$	$\overline{CS}$ is the active low Chip Select input pin. Used in conjunction with the $\overline{WR}$ and $\overline{RD}$ signals to control the active data bus input/output buffers of the data bus.
11	$\overline{RDY}$	$\overline{RDY}$ is an active low output pin. The signal at this pin indicates when a requested function has begun or ended. Refer to section **Functional Description** and the digital timing diagrams for more detail.
7	V_A+	Analog supply input pin. The device operating supply voltage range is +5V ± 10%. Accuracy is guaranteed only if the V_A+ and V_D+ are connected to the same potential. This pin should be bypassed to AGND with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible.
8	AGND	Analog ground pin. This is the device's analog supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.
21	V_D+	Digital supply input pins. The device operating supply voltage range is +5V ± 10%. Accuracy is guaranteed only if the V_A+ and V_D+ are connected to the same potential. This pin should be bypassed to DGND with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible.
22	DGND	Digital ground pin. This is the device's digital supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.

National Semiconductor

ADC12048
12-Bit Plus Sign 216 kHz 8-Channel Sampling Analog-to-Digital Converter

General Description

Operating from a single 5V power supply, the ADC12048 is a 12 bit + sign, parallel I/O, self-calibrating, sampling analog-to-digital converter (ADC) with an eight input fully differential analog multiplexer. The maximum sampling rate is 216 kHz. On request, the ADC goes through a self-calibration process that adjusts linearity, zero and full-scale errors.

The ADC12048's 8-channel multiplexer is software programmable to operate in a variety of combinations of single-ended, differential, or pseudo-differential modes. The fully differential MUX and the 12-bit + sign ADC allows for the difference between two signals to be digitized.

The ADC12048 can be configured to work with many popular microprocessors/microcontrollers and DSPs including National's HPC family, Intel386 and 8051, TMS320C25, Motorola MC68HC11/16, Hitachi 64180 and Analog Devices ADSP21xx.

For complementary voltage references see the LM4040, LM4041 or LM9140.

Features

- 8-channel programmable Differential or Single-Ended multiplexer
- Programmable Acquisition Times and user-controllable Throughput Rates
- Programmable data bus width (8/13 bits)
- Built-in Sample-and-Hold
- Programmable Auto-Calibration and Auto-Zero cycles
- Low power standby mode
- No missing codes

Key Specifications

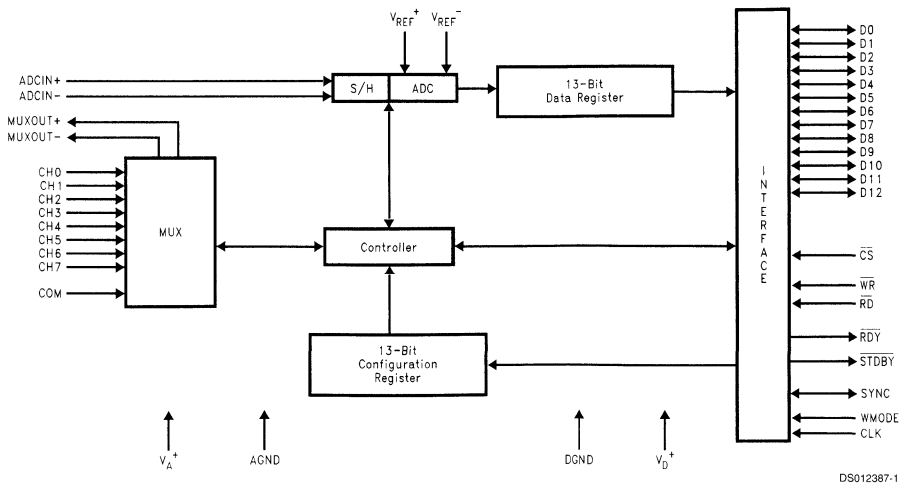
(f_{CLK} = 12 MHz)

■ Resolution	12-bits + sign
■ 13-bit conversion time	3.6 µs, max
■ 13-bit throughput rate	216 ksamples/s, min
■ Integral Linearity Error (ILE)	±1 LSB, max
■ Single Supply	+5V ±10%
■ V_{IN} Range	GND to V_A+
■ Power consumption	
— Normal operation	34 mW, max
— Stand-by mode	75 µw, max

Applications

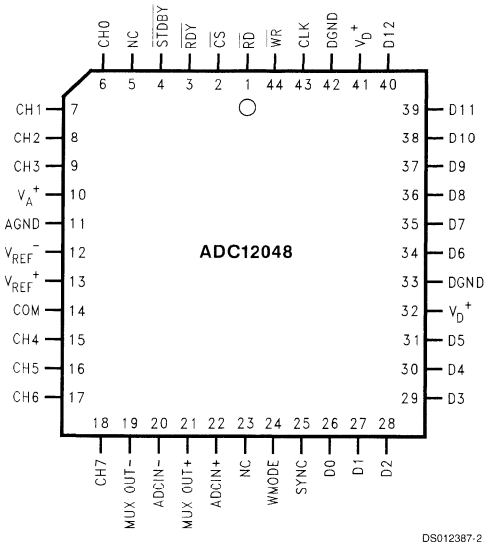
- Medical instrumentation
- Process control systems
- Test equipment
- Data logging
- Inertial guidance

Block Diagram



Connection Diagrams

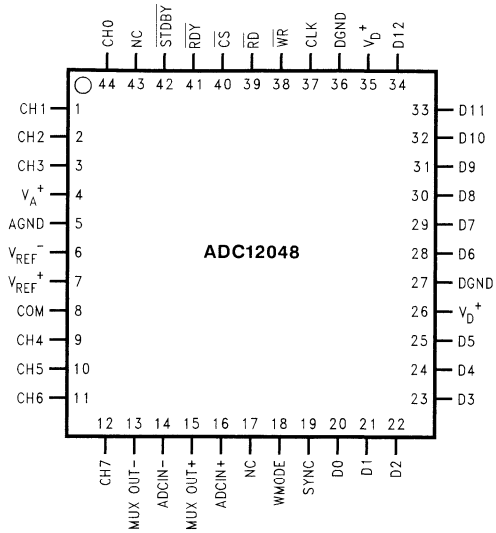
PLCC Package



DS012387-2

Order Number ADC12048CIV
See NS Package Number V44A

PQFP Package



DS012387-3

Order Number ADC12048CIVF
See NS Package Number VGZ44A

Ordering Information

Industrial Temperature Range $-40^\circ C \leq T_A \leq +85^\circ C$	Package
ADC12048CIV	PLCC
ADC12048CIVF	PQFP
ADC12048EVAL	Evaluation board

Pin Description

PLCC Pkg. Pin Number	PQFP Pkg. Pin Number	Pin Name	Description
6	44	CH0	The eight analog inputs to the Multiplexer. Active channels are selected based on the contents of bits b3–b0 of the Configuration register. Refer to section titled MUX for more details.
7	1	CH1	
8	2	CH2	
9	3	CH3	
15	9	CH4	
16	10	CH5	
17	11	CH6	
18	12	CH7	
14	8	COM	This pin is another analog input pin used as a pseudo ground when the multiplexer is configured in single-ended mode.
13	7	$V_{REF}+$	Positive reference input. The operating voltage range for this input is $1V \leq V_{REF}+ \leq V_A+$ (see *Figure 3* and *4*). This pin should be bypassed to AGND at least with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitors. The capacitors should be placed as close to the part as possible.

Pin Description (Continued)

PLCC Pkg. Pin Number	PQFP Pkg. Pin Number	Pin Name	Description
12	6	$V_{REF}-$	Negative reference input. The operating voltage range for this input is $0V \le V_{REF}- \le V_{REF}+ -1$ (see *Figure 3* and *4*). This pin should be bypassed to AGND at least with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the part as possible.
19 21	13 15	MUX OUT− MUX OUT+	The inverting (negative) and non-inverting (positive) outputs of the multiplexer. The analog inputs to the MUX selected by bits b3–b0 of the Configuration register appear at these pins.
20 22	14 16	ADCIN− ADCIN+	ADC inputs. The inverting (negative) and non-inverting (positive) inputs into the ADC.
24	18	WMODE	The logic state of this pin at power-up determines which edge of the write signal ($\overline{WR}$) will latch in data from the data bus. If tied low, the ADC12048 will latch in data on the **rising** edge of the $\overline{WR}$ signal. If tied to a logic **high**, data will be latched in on the **falling** edge of the $\overline{WR}$ signal. The state of this pin should not be changed after power-up.
25	19	SYNC	The SYNC pin can be programmed as an **input** or an **output**. The Configuration register's bit b8 controls the function of this pin. When programmed as an **input** pin (b8 = 1), a rising edge on this pin causes the ADC's sample-and-hold to hold the analog input signal and begin conversion. When programmed as an **output** pin (b8 = 0), the SYNC pin goes high when a conversion begins and returns low when completed.
26–31 34–40	20–25 29–34	D0–D5 D6–D12	13-bit Data bus of the ADC12048. D12 is the most significant bit and D0 is the least significant. The BW (bus width) bit of the Configuration register (b12) selects between an 8-bit or 13-bit data bus width. When the **BW** bit is **cleared** (BW = 0), D7–D0 are active and D12–D8 are always in TRI-STATE. When the **BW** bit is **set** (BW = 1), D12–D0 are active.
43	37	CLK	The clock input pin used to drive the ADC12048. The operating range is 0.05 MHz to 12 MHz.
44	38	$\overline{WR}$	$\overline{WR}$ is the active low WRITE control input pin. A logic low on this pin and the $\overline{CS}$ will enable the input buffers of the data pins D12–D0. The signal at this pin is used by the ADC12048 to latch in data on D12–D0. The sense of the WMODE pin at power-up will determine which edge of the $\overline{WR}$ signal the ADC12048 will latch in data. See WMODE pin description.
1	39	$\overline{RD}$	$\overline{RD}$ is the active low read control input pin. A logic low on this pin and $\overline{CS}$ will enable the active output buffers to drive the data bus.
2	40	$\overline{CS}$	$\overline{CS}$ is the active low Chip Select input pin. Used in conjunction with the $\overline{WR}$ and $\overline{RD}$ signals to control the active data bus input/output buffers of the data bus.
3	41	$\overline{RDY}$	$\overline{RDY}$ is an active low output pin. The signal at this pin indicates when a requested function has begun or ended. Refer to section **Functional Description** and the digital timing diagrams for more detail.
4	42	$\overline{STDBY}$	This is the standby active low output pin. This pin is low when the ADC12048 is in the standby mode and high when the ADC12048 is out of the standby mode or has been requested to leave the standby mode.
10	4	V_A+	Analog supply input pin. The device operating supply voltage range is +5V ±10%. Accuracy is guaranteed only if the V_A+ and V_D+ are connected to the same potential. This pin should be bypassed to AGND with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible.

Pin Description (Continued)

PLCC Pkg. Pin Number	PQFP Pkg. Pin Number	Pin Name	Description
11	5	AGND	Analog ground pin. This is the device's analog supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.
32 and 41	26 and 35	V_D+	Digital supply input pins. The device operating supply voltage range is +5V ±10%. Accuracy is guaranteed only if the V_A+ and V_D+ are connected to the same potential. This pin should be bypassed to DGND with a parallel combination of a 10 µF and a 0.1 µF (ceramic) capacitor. The capacitors should be placed as close to the supply pins of the part as possible.
33 and 42	27 and 36	DGND	Digital ground pin. This is the device's digital supply ground connection. It should be connected through a low resistance and low inductance ground return to the system power supply.

National Semiconductor

ADC12062
12-Bit, 1 MHz, 75 mW A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative multistep conversion technique, the 12-bit ADC12062 CMOS analog-to-digital converter digitizes signals at a 1 MHz sampling rate while consuming a maximum of only 75 mW on a single +5V supply. The ADC12062 performs a 12-bit conversion in three lower-resolution "flash" conversions, yielding a fast A/D without the cost and power dissipation associated with true flash approaches.

The analog input voltage to the ADC12062 is tracked and held by an internal sampling circuit, allowing high frequency input signals to be accurately digitized without the need for an external sample-and-hold circuit. The multiplexer output is available to the user in order to perform additional external signal processing before the signal is digitized.

When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 100 µW.

Features

- Built-in sample-and-hold
- Single +5V supply
- Single channel or 2 channel multiplexer operation
- Low Power Standby mode

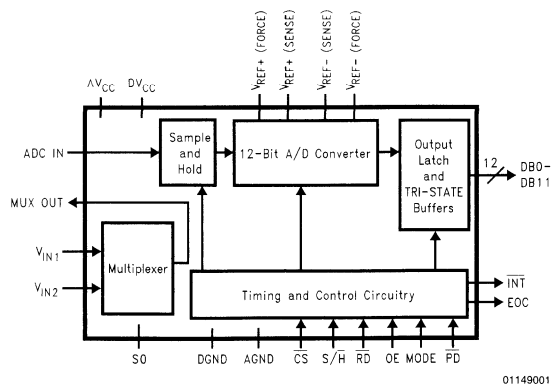
Key Specifications

- Sampling rate: 1 MHz (min)
- Conversion time: 740 ns (typ)
- Signal-to-Noise Ratio, f_{IN} = 100 kHz: 69.5 dB (min)
- Power consumption (f_s = 1 MHz): 75 mW (max)
- No missing codes over temperature: Guaranteed

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications
- Waveform digitizers

Block Diagram



Ordering Information

Industrial ($-40^\circ C \le T_A \le +85^\circ$)	Package
ADC12062BIVF	VGZ44A Plastic Quad Flat Package
ADC12062CIV	V44 Plastic Leaded Chip Carrier
ADC12062CIVF	VGZ44A Plastic Quad Flat Package

National Semiconductor

ADC12081
12-Bit, 5 MHz Self-Calibrating, Pipelined A/D Converter with Internal Sample & Hold

General Description

The ADC12081 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 5 megasamples per second (MSPS). The ADC12081 utilizes an innovative pipeline architecture to minimize die size and power consumption. The ADC12081 uses self-calibration and error correction to maintain accuracy and performance over temperature.

The ADC12081 converter operates on a 5V power supply and can digitize analog input signals in the range of 0 to 2V. A single convert clock controls the conversion operation. All digital I/O is TTL compatible.

The ADC12081 is designed to minimize external components necessary for the analog input interface. An internal sample-and-hold circuit samples the analog input and an internal amplifier buffers the reference voltage input.

The ADC12081 is available in the 32-lead LQFP package and is designed to operate over the extended commercial temperature range of -40°C to +85°C.

Features

- Single 5V power supply
- Simple analog input interface
- Internal Sample-and-hold
- Internal Reference buffer amplifier
- Low power consumption

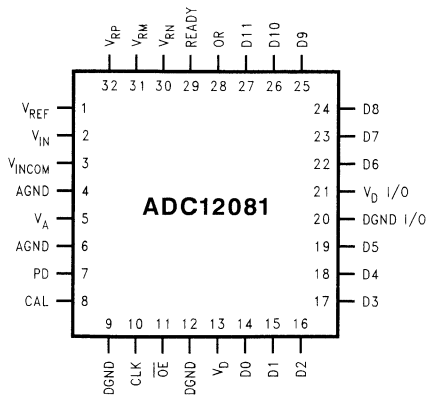
Key Specifications

■ Resolution	12 Bits
■ Conversion Rate	5 Msps (min)
■ DNL	±0.35 LSB (typ)
■ SNR	68 dB (typ)
■ ENOB	10.9 Bits (typ)
■ Analog Input Range	2 Vpp (min)
■ Supply Voltage	+5V ±5%
■ Power Consumption, 5 MHz	105 mW (typ)

Applications

- Image processing front end
- PC-based data acquisition
- Scanners
- Fax machines
- Waveform digitizer

Connection Diagram

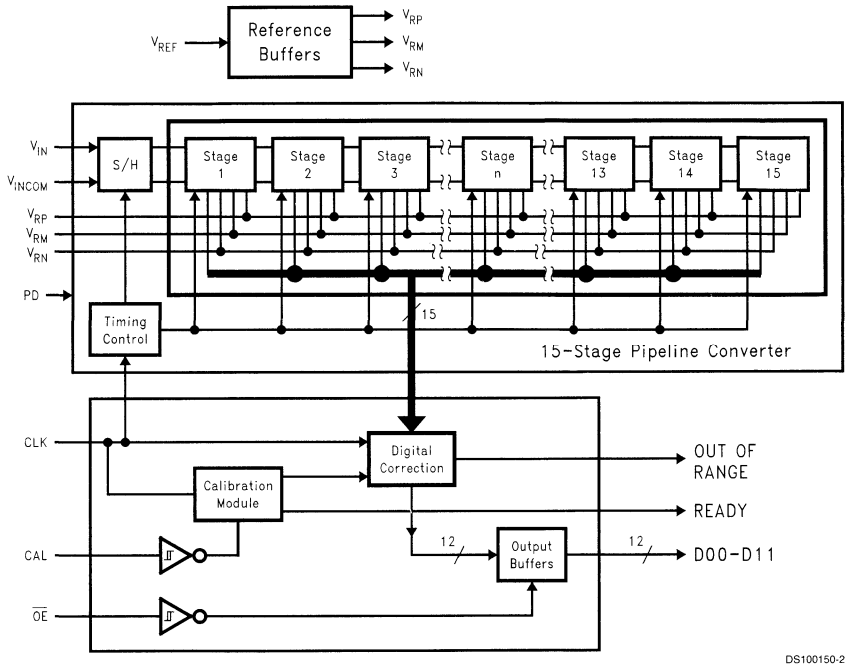


DS100150-1

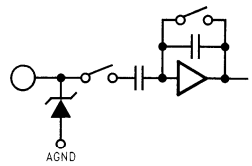
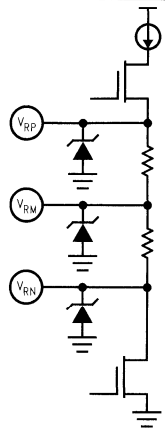
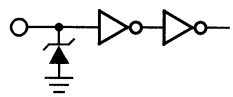
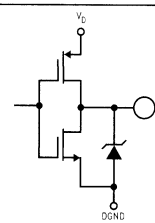
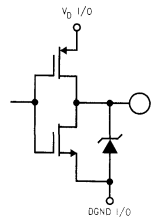
Ordering Information

Industrial ($-40^{\circ}C \leq TA \leq +85^{\circ}C$)	Package
ADC12081CIVT	32 pin LQFP
ADC12181 EVAL	Evaluation Board

Simplified Block Diagram



Pin Descriptions and Equivalent Circuits #2

No.	Symbol	Equivalent Circuit	Description
2	V_{IN}		Analog signal input. With a 2.0V reference voltage, input signal voltages in the range of 0 to 2.0 Volts will be converted. See section 1.2.
1	V_{REF}		Reference voltage input. This pin should be driven from an accurate, stable reference source in the range of 1.8 to 2.2V and bypassed to a low-noise analog ground with a monolithic ceramic capacitor, nominally 0.01µF. See section 1.1.
32	V_{RP}		Positive reference bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
31	V_{RM}		Reference midpoint bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
30	V_{RN}		Negative reverence bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
10	CLOCK		Sample Clock input, TTL compatible. Maximum amplitude should not exceed 3V.
8	CAL		Calibration request, active High. Calibration cycle starts when CAL returns to logic low. CAL is ignored during power-down mode. See section 2.2.
7	PD		Power-down, active High, ignored during calibration cycle. See paragraph 2.4
11	$\overline{OE}$		Output enable control, active low. When this pin is high the data outputs are in Tri-state (high-impedance) mode.
28	OR		Over range indicator. This pin is at a logic High for $V_{IN} < 0$ or for $V_{IN} > V_{REF}$.
29	READY		Device ready indicator, active High. This pin is at a logic Low during a calibration cycle and while the device is in the power down mode.
14-19, 22-27	D0 - D11		Digital output word, CMOS compatible. D0 (pin 14) is LSB, D11 (pin 27) is MSB. Load with no more than 50pF.

Pin Descriptions and Equivalent Circuits #2 (Continued)

No.	Symbol	Equivalent Circuit	Description
3	$V_{IN\ com}$		Analog input common. Connect to a quiet point in analog ground near the driving device. See section 1.2.
5	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1µF chip capacitor.
4, 6	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12081 package. See section 5.0.
13	V_D		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1 µF chip capacitor.
9, 12	DGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12081 package. See section 5.0
21	V_D I/O		The digital output driver supply pin. This pin can be operated from a supply voltage of 3V to 5V, but the voltage on this pin should never exceed the V_D supply pin voltage.
20	DGND I/O		The ground return for the output drivers. This pin should be returned to a point in the digital ground that is removed from the other ground pins of the ADC12081.

National Semiconductor

ADC12130/ADC12132/ADC12138 Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12130, ADC12132 and ADC12138 are 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexer. The ADC12132 and ADC12138 have a 2 and an 8 channel multiplexer, respectively. The differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12130 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. The ADC12130 family is tested with a 5 MHz clock. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to typically less than ±1 LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +5V) can be accommodated with a single +5V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign output data format.

The serial I/O is configured to comply with the NSC MICROWIRE™. For voltage references, see the LM4040 or LM4041.

Features

- Serial I/O (MICROWIRE, SPI and QSPI Compatible)
- 2 or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- 0V to 5V analog input range with single 5V power supply

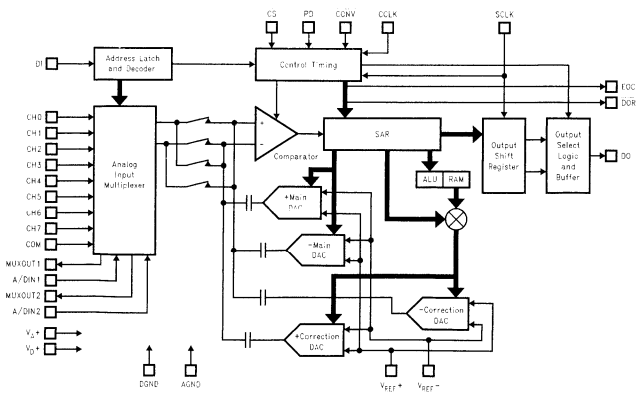
Key Specifications

- Resolution: 12-bit plus sign
- 12-bit plus sign conversion time: 8.8 µs (max)
- 12-bit plus sign throughput time: 14 µs (max)
- Integral linearity error: ±2 LSB (max)
- Single supply: 3.3V or 5V ±10%
- Power consumption
  - — 3.3V 15 mW (max)
  - — 3.3V power down 40 µW (typ)
  - — 5V 33 mW (max)
  - — 5V power down 100 µW (typ)

Applications

- Pen-based computers
- Digitizers
- Global positioning systems

ADC12138 Simplified Block Diagram



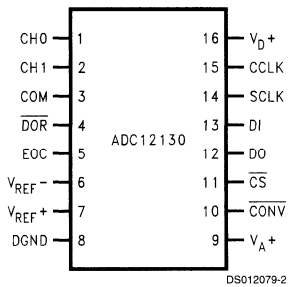
DS012079-1

Ordering Information

Industrial Temperature Range $-40^{\circ}C \leq T_A \leq +85^{\circ}C$	NS Package Number
ADC12130CIN	N16E, Dual-In-Line
ADC12130CIWM	M16B, Wide Body SO
ADC12132CIMSA	MSA20, SSOP
ADC12138CIN	N28B, Dual-In-Line
ADC12138CIWM	M28B
ADC12138CIMSA	MSA28, SSOP

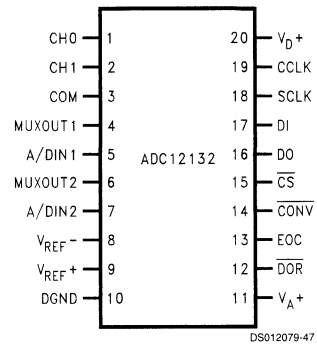
Connection Diagrams

16-Pin Dual-In-Line and Wide Body SO Packages



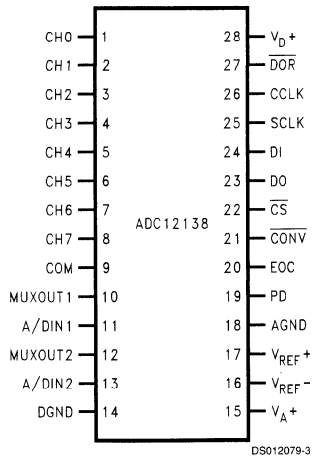
Top View

20-Pin SSOP Package



Top View

28-Pin Dual-In-Line, SSOP and Wide Body SO Packages



Top View

Pin Descriptions

CCLK — The clock applied to this input controls the sucessive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 µs.

SCLK — This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{CS}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled, the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 µs.

DI — This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. *Table 2* through *Table 4* show the assignment of the multiplexer address and the mode select data.

DO — The data output pin. This pin is an active push/pull output when $\overline{CS}$ is low. When $\overline{CS}$ is high, this output is TRI-STATE. The A/D conversion result (DB0–DB12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see *Table 1*). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see *Table 4*).

EOC — This pin is an active push/pull output and indicates the status of the ADC12130/2/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{CS}$ — This is the chip select pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE. With $\overline{CS}$ low, the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled, the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought back low during a conversion, that conversion is prematurely terminated. The data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought back low during a conversion in progress the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. *Table 4* details the data required.

$\overline{DOR}$ — This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{CONV}$ — A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming Table (*Table 4*) such as 12-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.

PD — This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 700 µs to power up after the command is given.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (see *Table 2* and *Table 3*).

The voltage applied to these inputs should not exceed V_A+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2 — These are the multiplexer output pins.

A/DIN1, A/DIN2 — These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed V_A^+ or go below AGND (see *Figure 5*).

$V_{REF}+$ — This is the positive analog voltage reference input. In order to maintain accuracy, the voltage range of V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is

Pin Descriptions (Continued)

1 V_{DC} to 5.0 V_{DC} and the voltage at $V_{REF}+$ cannot exceed V_A+. See *Figure 6* for recommended bypassing.

$V_{REF}-$ The negative voltage reference input. In order to maintain accuracy, the voltage at this pin must not go below GND or exceed V_A+. (See *Figure 6*).

V_A+, V_D+ These are the analog and digital power supply pins. $V_A{}^+$ and $V_D{}^+$ are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see *Figure 6*). The operating voltage range of V_A+ and V_D+ is 3.0 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin (see *Figure 6*).

AGND This is the analog ground pin (see *Figure 6*).

National Semiconductor

ADC12181
12-Bit, 10 MHz Self-Calibrating, Pipelined A/D Converter with Internal Sample & Hold

General Description

The ADC12181 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 10 megasamples per second (MSPS). The ADC12181 utilizes an innovative pipeline architecture to minimize die size and power consumption. Self-calibration and error correction maintain accuracy and performance over temperature.

The ADC12181 converter operates on a 5V power supply and can digitize analog input signals in the range of 0 to 2V. A single convert clock controls the conversion operation. All digital I/O is TTL compatible.

The ADC12181 is designed to minimize external components necessary for the analog input interface. An internal sample-and-hold circuit samples the analog input and an internal amplifier buffers the reference voltage input.

The ADC12181 is available in the 32-lead TQFP package and is designed to operate over the extended commercial temperature range of -40°C to +85°C.

Features

- Single 5V power supply
- Simple analog input interface
- Internal Sample-and-hold
- Internal Reference buffer amplifier
- Low power consumption

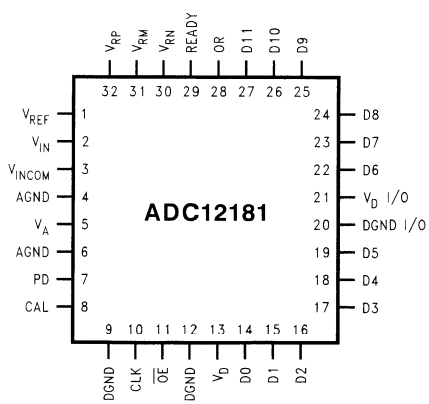
Key Specifications

■ Resolution	12 Bits
■ Conversion Rate	10 Msps (min)
■ DNL	±0.4 LSB (typ)
■ SNR	65 dB (typ)
■ ENOB	10.4 Bits (typ)
■ Analog Input Range	2 Vpp (min)
■ Supply Voltage	+5V ±5%
■ Power Consumption, 10 MHz	235 mW (typ)

Applications

- Image processing front end
- PC-based data acquisition
- Scanners
- Fax machines
- Waveform digitizer

Connection Diagram



DS101039-1

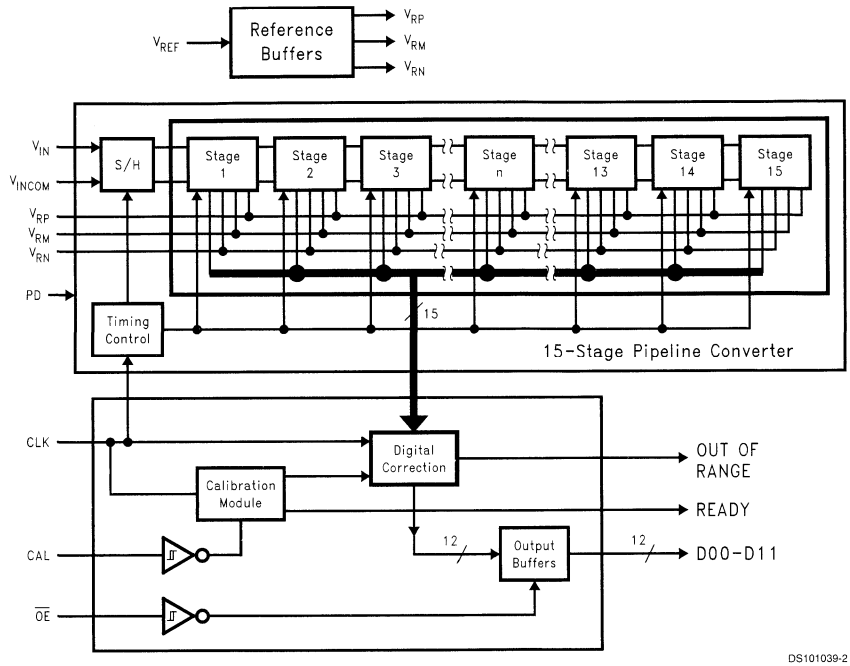
Ordering Information

Industrial (−40°C ≤ TA ≤ +85°C)	Package
ADC12181CIVT	32 pin TQFP

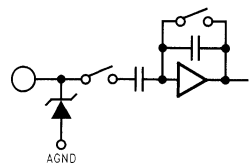
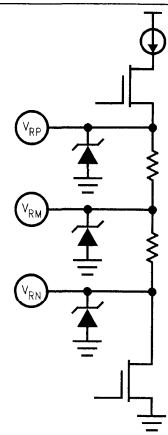
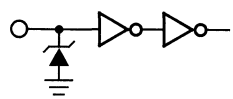
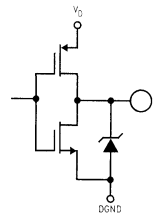
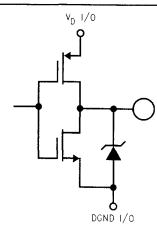
Ordering Information (Continued)

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC12181 EVAL	Evaluation Board

Simplified Block Diagram



Pin Descriptions and Equivalent Circuits #2

No.	Symbol	Equivalent Circuit	Description
2	V_{IN}		Analog signal input. With a 2.0V reference voltage, input signal voltages in the range of 0 to 2.0 Volts will be converted. See section 1.2.
1	V_{REF}		Reference voltage input. This pin should be driven from an accurate, stable reference source in the range of 1.8 to 2.2V and bypassed to a low-noise analog ground with a monolithic ceramic capacitor, nominally 0.01µF. See section 1.1.
32	V_{RP}		Positive reference bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
31	V_{RM}		Reference midpoint bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
30	V_{RN}		Negative reverence bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
10	CLOCK		Sample Clock input, TTL compatible. Maximum amplitude should not exceed 3V.
8	CAL		Calibration request, active High. Calibration cycle starts when CAL returns to logic low. CAL is ignored during power-down mode. See section 2.2.
7	PD		Power-down, active High, ignored during calibration cycle. See paragraph 2.4
11	$\overline{OE}$		Output enable control, active low. When this pin is high the data outputs are in Tri-state (high-impedance) mode.
28	OR		Over range indicator. This pin is at a logic High for $V_{IN} < 0$ or for $V_{IN} > V_{REF}$.
29	READY		Device ready indicator, active High. This pin is at a logic Low during a calibration cycle and while the device is in the power down mode.
14-19, 22-27	D0 - D11		Digital output word, CMOS compatible. D0 (pin 14) is LSB, D11 (pin 27) is MSB. Load with no more than 50pF.

Pin Descriptions and Equivalent Circuits #2 (Continued)

No.	Symbol	Equivalent Circuit	Description
3	$V_{IN\ com}$		Analog input common. Connect to a quiet point in analog ground near the driving device. See section 1.2.
5	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1µF chip capacitor.
4, 6	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12181 package. See section 5.0.
13	V_D		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1 µF chip capacitor.
9, 12	DGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12181 package. See section 5.0
21	V_D I/O		The digital output driver supply pin. This pin can be operated from a supply voltage of 3V to 5V, but the voltage on this pin should never exceed the V_D supply pin voltage.
20	DGND I/O		The ground return for the output drivers. This pin should be returned to a point in the digital ground that is removed from the other ground pins of the ADC12181.

National Semiconductor

ADC12191
12-Bit, 10 MHz Self-Calibrating, Pipelined A/D Converter with Internal Sample & Hold

General Description

The ADC12191 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 10 megasamples per second (MSPS). The ADC12191 utilizes an innovative pipeline architecture to minimize die size and power consumption. The ADC12191 uses self-calibration and error correction to maintain accuracy and performance over temperature.

The ADC12191 converter operates on a 5V power supply and can digitize analog input signals in the range of 0 to 2V. A single convert clock controls the conversion operation. All digital I/O is TTL compatible.

The ADC12191 is designed to minimize external components necessary for the analog input interface. An internal sample-and-hold circuit samples the analog input and an internal amplifier buffers the reference voltage input.

The ADC12191 is available in the 32-lead TQFP package and is designed to operate over the extended commercial temperature range of -40°C to +85°C.

Features

- Single 5V power supply
- Simple analog input interface
- Internal Sample-and-hold
- Internal Reference buffer amplifier
- Low power consumption

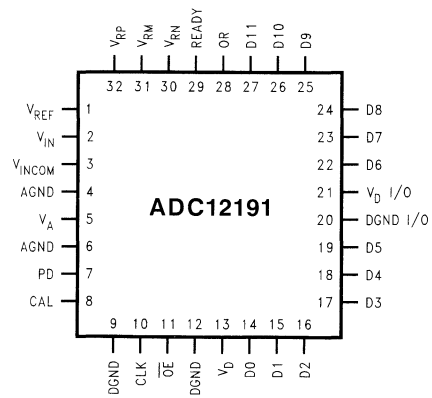
Key Specifications

■ Resolution	12 Bits
■ Conversion Rate	10 Msps (min)
■ DNL	±0.5 LSB (typ)
■ SNR	63 dB (typ)
■ ENOB	10 Bits (typ)
■ Analog Input Range	2 Vpp (min)
■ Supply Voltage	+5V ±5%
■ Power Consumption, 10 MHz	235 mW (typ)

Applications

- Image processing front end
- PC-based data acquisition
- Scanners
- Fax machines
- Waveform digitizer

Connection Diagram

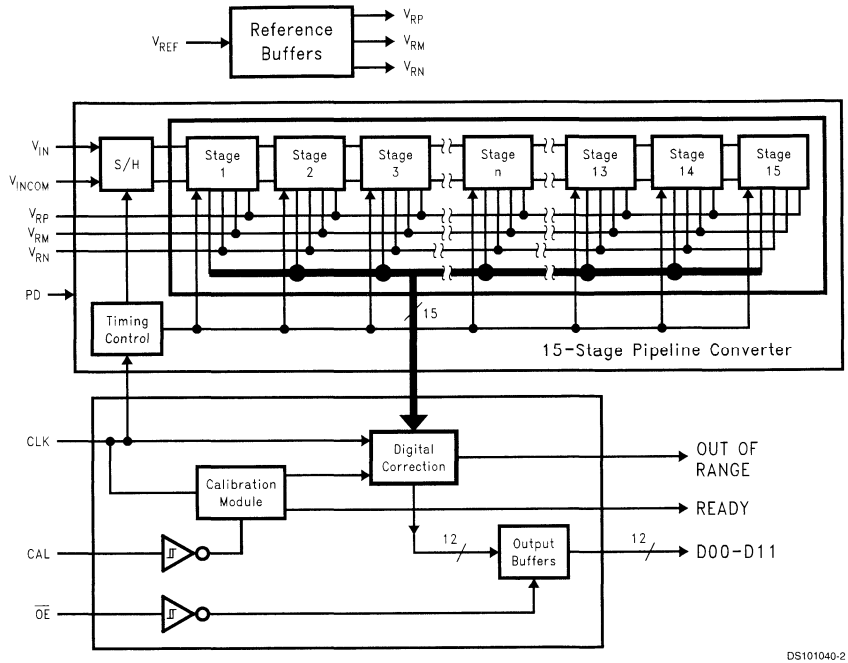


DS101040-1

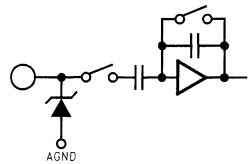
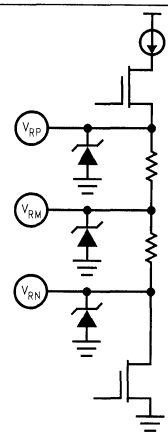
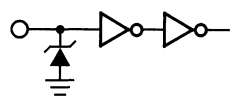
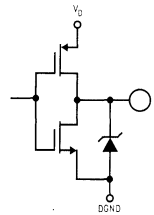
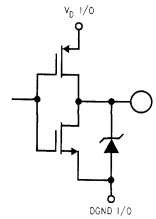
Ordering Information

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC12191CIVT	32 pin TQFP
ADC12181 EVAL	Evaluation Board

Simplified Block Diagram



Pin Descriptions and Equivalent Circuits #2

No.	Symbol	Equivalent Circuit	Description
2	V_{IN}		Analog signal input. With a 2.0V reference voltage, input signal voltages in the range of 0 to 2.0 Volts will be converted. See section 1.2.
1	V_{REF}		Reference voltage input. This pin should be driven from an accurate, stable reference source in the range of 1.8 to 2.2V and bypassed to a low-noise analog ground with a monolithic ceramic capacitor, nominally 0.01µF. See section 1.1.
32	V_{RP}		Positive reference bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
31	V_{RM}		Reference midpoint bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
30	V_{RN}		Negative reverence bypass pin. Bypass with a 0.1µF capacitor. Do not connect anything else to this pin. See section 3.1
10	CLOCK		Sample Clock input, TTL compatible. Maximum amplitude should not exceed 3V.
8	CAL		Calibration request, active High. Calibration cycle starts when CAL returns to logic low. CAL is ignored during power-down mode. See section 2.2.
7	PD		Power-down, active High, ignored during calibration cycle. See paragraph 2.4
11	$\overline{OE}$		Output enable control, active low. When this pin is high the data outputs are in Tri-state (high-impedance) mode.
28	OR		Over range indicator. This pin is at a logic High for $V_{IN} < 0$ or for $V_{IN} > V_{REF}$.
29	READY		Device ready indicator, active High. This pin is at a logic Low during a calibration cycle and while the device is in the power down mode.
14-19, 22-27	D0 - D11		Digital output word, CMOS compatible. D0 (pin 14) is LSB, D11 (pin 27) is MSB. Load with no more than 50pF.

Pin Descriptions and Equivalent Circuits #2 (Continued)

No.	Symbol	Equivalent Circuit	Description
3	$V_{IN\ com}$		Analog input common. Connect to a quiet point in analog ground near the driving device. See section 1.2.
5	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1µF chip capacitor.
4, 6	AGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12191 package. See section 5.0.
13	V_D		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5µF to 10µF capacitor and a 0.1 µF chip capacitor.
9, 12	DGND		The ground return for the analog supply. AGND and DGND should be connected together close to the ADC12191 package. See section 5.0
21	V_D I/O		The digital output driver supply pin. This pin can be operated from a supply voltage of 3V to 5V, but the voltage on this pin should never exceed the V_D supply pin voltage.
20	DGND I/O		The ground return for the output drivers. This pin should be returned to a point in the digital ground that is removed from the other ground pins of the ADC12191.

National Semiconductor

ADC12281
12-Bit, 20 MSPS Single-Ended Input, Pipelined A/D Converter

General Description

The ADC12281 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 20 megasamples per second (MSPS). It utilizes a pipeline architecture to minimize die size and power dissipation. Self-calibration and error correction maintain accuracy and performance over temperature.

The ADC12281 operates on a 5V power supply and can digitize single-ended analog input signals in the range of 0V to 2V. A single convert clock controls the conversion operation and all digital I/O is TTL compatible.

The ADC12881 is designed to minimize external components necessary for the analog input interface. An internal sample-and-hold circuit samples the single-ended analog input and an internal amplifier buffers the reference voltage input.

The Power Down feature reduces power consumption to 20 mW, typical.

The ADC12281 is available in the 32-lead TQFP package and is designed to operate over the industrial temperature range of −40°C to +85°C.

Features

- Single 5V power supply
- Single-ended analog input
- Internal sample-and-hold
- Internal reference buffer amplifier
- Low offset and gain errors

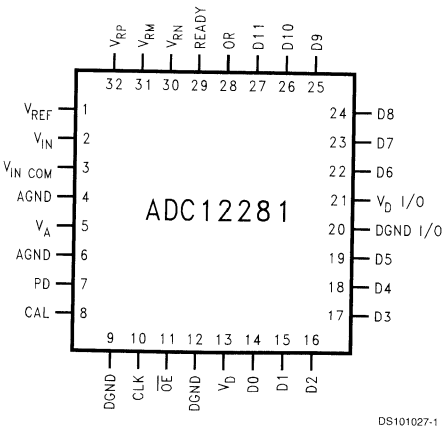
Key Specifications

■ Resolution	12 bits
■ Conversion rate	up to 20 MSPS
■ DNL	0.35 LSB (typ)
■ SNR	65.5 dB (typ)
■ ENOB	10.5 bits (typ)
■ Analog input range	2 V_{PP} (min)
■ Supply voltage	+5V ±5%
■ Power consumption, 20 MHz	443 mW (typ)

Applications

- Digital signal processing front end
- Digital television
- Radar
- High speed data links
- Waveform digitizers
- Quadrature demodulation

Connection Diagram



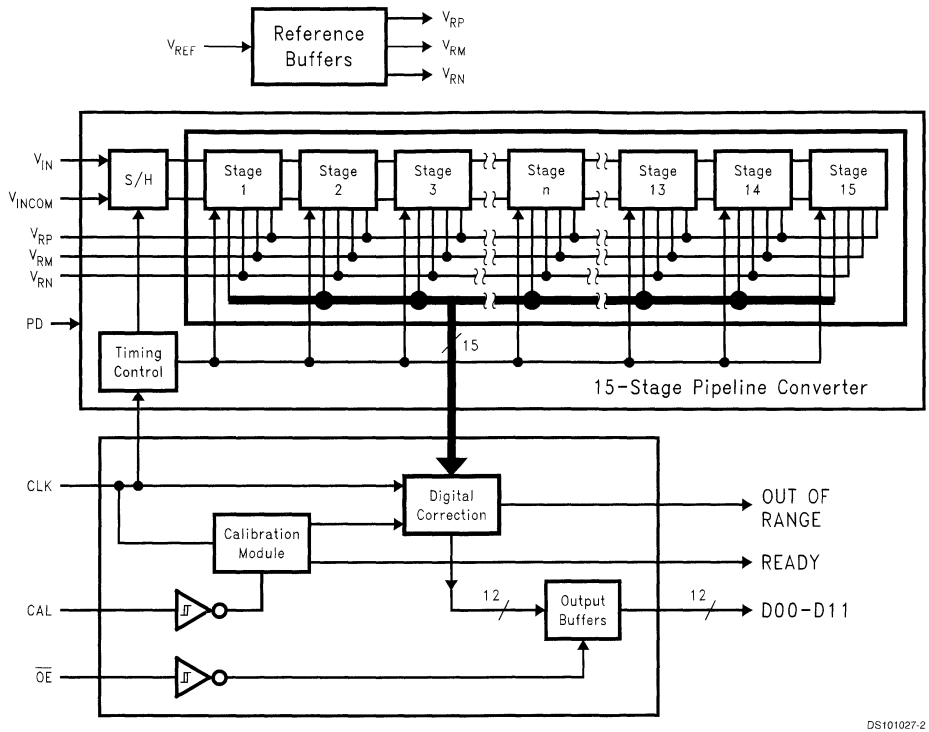
DS101027-1

32-Lead TQFP Package
Order Number ADC12281CIVT
See NS Package Number VBE32A

Ordering Information

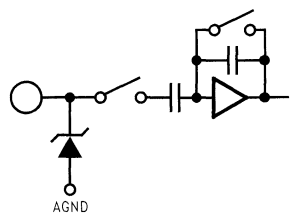
Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC12281CIVT	32-Pin TQFP

Simplified Block Diagram

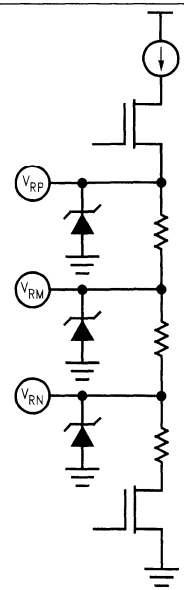
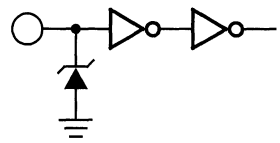
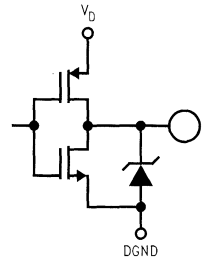
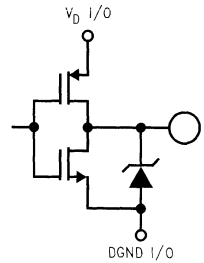


DS101027-2

Pin Descriptions and Equivalent Circuits

Pin	Symbol	Equivalent Circuit	Description
2	V_{IN}		Single-ended analog signal input. With a 2.0V reference voltage, input signal voltages in the range of 0V to 2.0V will be converted. See Section 1.2.
1	V_{REF}		Reference voltage input. This pin should be driven from an accurate, stable reference source in the range of 1.8V to 2.2V and bypassed to a low-noise ground with a monolithic ceramic capacitor, nominally 0.01 µF. See Section 1.1.

Pin Descriptions and Equivalent Circuits (Continued)

Pin	Symbol	Equivalent Circuit	Description
32	V_{RP}		Positive reference bypass pin. Bypass with a 0.1 µF capacitor. Do not connect anything else to this pin. See Section 3.1.
31	V_{RM}		Reference midpoint bypass pin. Bypass with a 0.1 µF capacitor. Do not connect anything else to this pin. See Section 3.1.
30	V_{RN}		Negative reference bypass pin. Bypass with a 0.1 µF capacitor. Do not connect anything else to this pin. See Section 3.1.
10	CLOCK		Sample clock input, TTL compatible. Amplitude should not exceed 3 V_{P-P}.
8	CAL		Calibration request, active High. Calibration cycle starts when CAL returns to logic low. CAL is ignored during power-down mode. See Section 2.2.
7	PD		Power-down, active High, ignored during calibration cycle. See paragraph 2.4.
11	$\overline{OE}$		Output enable control, active low. When this pin is high the data outputs are in TRI-STATE (high-impedance) mode.
28	OR		Over-range indicator. This pin is at a logic High, for $V_{IN} < 0$ or for $V_{IN} > V_{REF}$.
29	READY		Device ready indicator, active High. This pin will be at a logic Low during a calibration cycle and while the device is in the power down mode.
14–19, 22–27	D0–D11		Digital output word, CMOS compatible. D0 (pin 19) is LSB, D11 (pin 36) is MSB. Load with no more than 25 pF.

Pin Descriptions and Equivalent Circuits (Continued)

Pin	Symbol	Equivalent Circuit	Description
3	$V_{IN\ COM}$		Analog input common. Connect to a quiet point in analog ground near the driving device. See Section 1.2.
5	V_A		Positive analog supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5 µF to 10 µF capacitor and a 0.1 µF chip capacitor.
4, 6	AGND		The ground return for the analog supply, AGND and DGND should be connected together close to the ADC12281 package. See Section 5.0.
13	V_D		Positive digital supply pin. Connect to a clean, quiet voltage source of +5V. V_A and V_D should have a common supply and be separately bypassed with a 5 µF to 10 µF capacitor and a 0.1 µF chip capacitor.
9, 12	DGND		The ground return for the digital supply. AGND and DGND should be connected together close to the ADC12281 package. See Section 5.0.
21	V_D I/O		The digital output driver supply pins. This pin can be operated from a supply voltage of 3V to 5V, but the voltage on this pin should never exceed the V_D supply pin voltage. See Section 3.4.
20	DGND I/O		The ground return for the digital output drivers. This pin should be returned to a point in the digital ground that is removed from the other ground pins of the ADC12281.

National Semiconductor

ADC12662
12-Bit, 1.5 MHz, 200 mW A/D Converter with Input Multiplexer and Sample/Hold

General Description

Using an innovative multistep conversion technique, the 12-bit ADC12662 CMOS analog-to-digital converter digitizes signals at a 1.5 MHz sampling rate while consuming a maximum of only 200 mW on a single +5V supply. The ADC12662 performs a 12-bit conversion in three lower-resolution "flash" conversions, yielding a fast A/D without the cost and power dissipation associated with true flash approaches.

The analog input voltage to the ADC12662 is tracked and held by an internal sampling circuit, allowing high frequency input signals to be accurately digitized without the need for an external sample-and-hold circuit. The ADC12662 features two sample-and-hold/flash comparator sections which allow the converter to acquire one sample while converting the previous. This pipelining technique increases conversion speed without sacrificing performance. The multiplexer output is available to the user in order to perform additional external signal processing before the signal is digitized.

When the converter is not digitizing signals, it can be placed in the Standby mode; typical power consumption in this mode is 250 µW.

Features

- Built-in sample-and-hold
- Single +5V supply
- Single channel or 2 channel multiplexer operation
- Low Power Standby mode

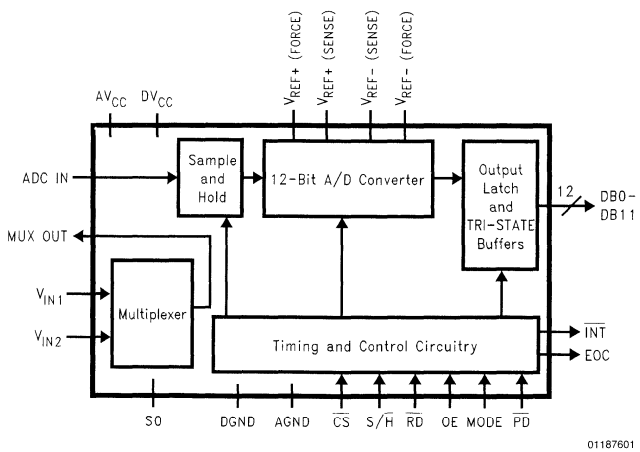
Key Specifications

■ Sampling rate	1.5 MHz (min)
■ Conversion time	580 ns (typ)
■ Signal-to-Noise Ratio, f_{IN}= 100 kHz	67.5 dB (min)
■ Power consumption (f_s= 1.5 MHz)	200 mW (max)
■ No missing codes over temperature	Guaranteed

Applications

- Digital signal processor front ends
- Instrumentation
- Disk drives
- Mobile telecommunications
- Waveform digitizers

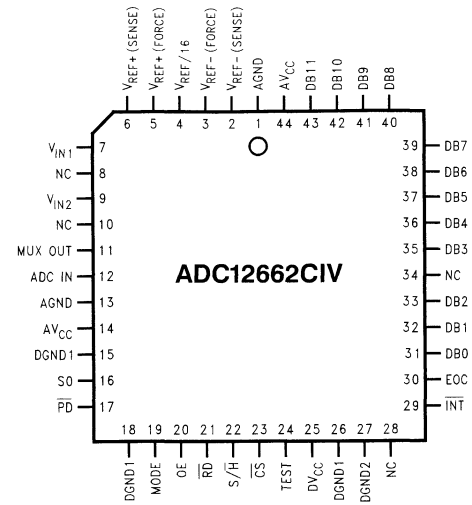
ADC12662 Block Diagram



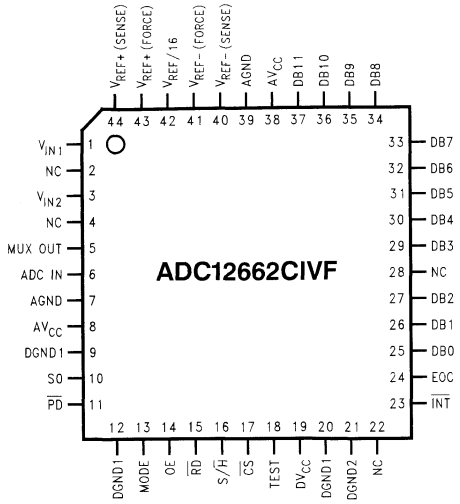
Ordering Information

Industrial (−40°C ≤ T_A ≤ +85°)	Package
ADC12662CIV	V44 Plastic Leaded Chip Carrier
ADC12662CIVF	VGZ44A Plastic Quad Flat Package

Connection Diagrams



Top View



Top View

Pin Descriptions

AV_{CC} — These are the two positive analog supply inputs. They should always be connected to the same voltage source, but are brought out separately to allow for separate bypass capacitors. Each supply pin should be bypassed to AGND with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

DV_{CC} — This is the positive digital supply input. It should always be connected to the same voltage as the analog supply, AV_{CC}. It should be bypassed to DGND2 with a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor.

AGND, DGND1, DGND2 — These are the power supply ground pins. There are separate analog and digital ground pins for separate bypassing of the analog and digital supplies. The ground pins should be connected to a stable, noise-free system ground. All of the ground pins should be returned to the same potential. AGND is the analog ground for the converter. DGND1 is the ground pin for the digital control lines. DGND2 is the ground return for the output databus. See Section 6.0 LAYOUT AND GROUNDING for more information.

DB0–DB11 — These are the TRI-STATE output pins, enabled by $\overline{RD}$, $\overline{CS}$, and OE.

V_{IN1}, V_{IN2} — These are the analog input pins to the multiplexer. For accurate conversions, no input pin (even one that is not selected) should be driven more than 50 mV below ground or 50 mV above V_{CC}.

MUX OUT — This is the output of the on-board analog input multiplexer.

ADC IN — This is the direct input to the 12-bit sampling A/D converter. For accurate conversions, this pin should not be driven more than 50 mV below ground or 50 mV above V_{CC}.

S0 — This pin selects the analog input that will be connected to the ADC12662 during the conversion. The input is selected based on the state of S0 when EOC makes its high-to-low transition. Low selects V_{IN1}, high selects V_{IN2}.

MODE — This pin should be tied to DGND1.

$\overline{CS}$ — This is the active low Chip Select control input. When low, this pin enables the $\overline{RD}$, S/$\overline{H}$, and OE inputs. This pin can be tied low.

$\overline{INT}$ — This is the active low Interrupt output. When using the Interrupt Interface Mode (*Figure 1*), this output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. This output is always high when $\overline{RD}$ is held low (*Figure 2*).

$\overline{EOC}$ — This is the End-of-Conversion control output. This output is low during a conversion.

$\overline{RD}$ — This is the active low Read control input. When $\overline{RD}$ is low (and $\overline{CS}$ is low), the $\overline{INT}$ output is reset and (if OE is high) data appears on the data bus. This pin can be tied low.

OE — This is the active high Output Enable control input. This pin can be thought of as an inverted version of the $\overline{RD}$ input (see *Figure 6*). Data output pins DB0–DB11 are TRI-STATE when OE is low. Data appears on DB0–DB11 only when OE is high and $\overline{CS}$ and $\overline{RD}$ are both low. This pin can be tied high.

S/$\overline{H}$ — This is the Sample/$\overline{Hold}$ control input. The analog input signal is held and a new conver-

Pin Descriptions (Continued)

sion is initiated by the falling edge of this control input (when $\overline{CS}$ is low).

$\overline{PD}$ This is the Power Down control input. This pin should be held high for normal operation. When this pin is pulled low, the device goes into a low power standby mode.

$V_{REF+(FORCE)}$, $V_{REF-(FORCE)}$ These are the positive and negative voltage reference force inputs, respectively. See Section 4, REFERENCE INPUTS, for more information.

$V_{REF+(SENSE)}$, $V_{REF-(SENSE)}$ These are the positive and negative voltage reference sense pins, respectively. See Section 4, REFERENCE INPUTS, for more information.

$V_{REF}/16$ This pin should be bypassed to AGND with a 0.1 µF ceramic capacitor.

TEST This pin should be tied to DV_{CC}.

National Semiconductor

ADC12L030/ADC12L032/ADC12L034/ADC12L038 3.3V Self-Calibrating 12-Bit Plus Sign Serial I/O A/D Converters with MUX and Sample/Hold

General Description

The ADC12L030 family is 12-bit plus sign successive approximation A/D converters with serial I/O and configurable input multiplexers. These devices are fully tested with a single 3.3V power supply. The ADC12L032, ADC12L034 and ADC12L038 have 2, 4 and 8 channel multiplexers, respectively. Differential multiplexer outputs and A/D inputs are available on the MUXOUT1, MUXOUT2, A/DIN1 and A/DIN2 pins. The ADC12L030 has a two channel multiplexer with the multiplexer outputs and A/D inputs internally connected. On request, these A/Ds go through a self calibration process that adjusts linearity, zero and full-scale errors to less than ±½ LSB each.

The analog inputs can be configured to operate in various combinations of single-ended, differential, or pseudo-differential modes. A fully differential unipolar analog input range (0V to +3.3V) can be accommodated with a single +3.3V supply. In the differential modes, valid outputs are obtained even when the negative inputs are greater than the positive because of the 12-bit plus sign two's compliment output data format.

The serial I/O is configured to comply with NSC's MICROWIRE™ and Motorola's SPI standards. For voltage references, see the LM4040 or LM4041 data sheets.

Features

- 0V to 3.3V analog input range with single 3.3V power supply
- Serial I/O (MICROWIRE and SPI Compatible)
- 2, 4, or 8 channel differential or single-ended multiplexer
- Analog input sample/hold function
- Power down mode
- Variable resolution and conversion rate
- Programmable acquisition time
- Variable digital output word length and format
- No zero or full scale adjustment required
- Fully tested and guaranteed with a 2.5V reference
- No Missing Codes over temperature

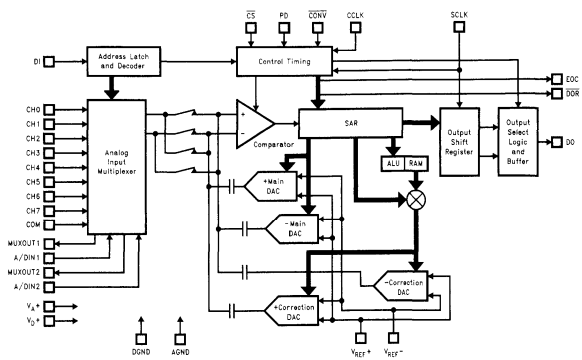
Key Specifications

■ Resolution	12-bit plus sign
■ 12-bit plus sign conversion time	8.8 µs (min)
■ 12-bit plus sign sampling rate	73 kHz (max)
■ Integral linearity error	±1 LSB (max)
■ Single supply	3.3V ±10%
■ Power dissipation	15 mW (max)
■ Power down	40 µW (typ)

Applications

- Portable Medical instruments
- Portable computing
- Portable Test equipment

ADC12L038 Simplified Block Diagram



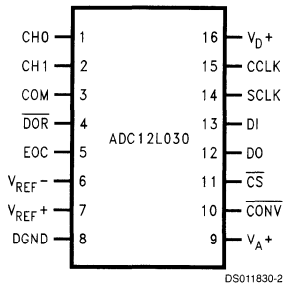
DS011830-1

Ordering Information

Industrial Temperature Range $-40^{\circ}C \leq T_A \leq +85^{\circ}C$	NS Package Number
ADC12L030CIWM	M16B
ADC12L032CIWM	M20B
ADC12L034CIWM	M24B
ADC12L038CIWM	M28B

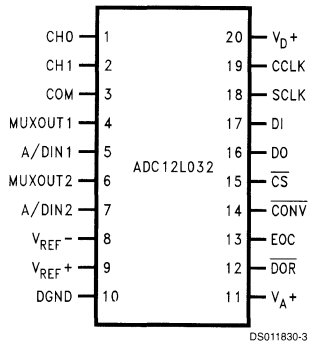
Connection Diagrams

16-Pin Wide Body SO Packages



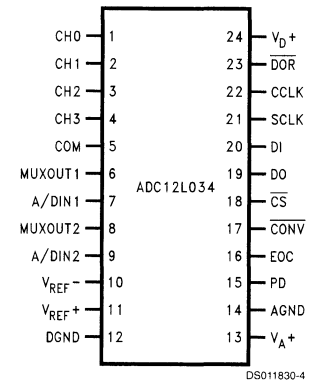
Top View

20-Pin Wide Body SO Packages



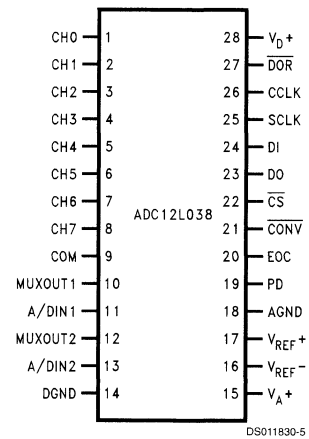
Top View

24-Pin Wide Body SO Packages



Top View

248-Pin Wide Body SO Packages



Top View

Pin Descriptions

CCLK — The clock applied to this input controls the sucessive approximation conversion time interval and the acquisition time. The rise and fall times of the clock edges should not exceed 1 µs.

SCLK — This is the serial data clock input. The clock applied to this input controls the rate at which the serial data exchange occurs. The rising edge loads the information on the DI pin into the multiplexer address and mode select shift register. This address controls which channel of the analog input multiplexer (MUX) is selected and the mode of operation for the A/D. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The rise and fall times of the clock edges should not exceed 1 µs.

DI — This is the serial data input pin. The data applied to this pin is shifted by the rising edge of SCLK into the multiplexer address and mode select register. *Tables 2, 3, 4, 5* show the assignment of the multiplexer address and the mode select data.

DO — The data output pin. This pin is an active push/pull output when $\overline{CS}$ is Low. When $\overline{CS}$ is High this output is in TRI-STATE. The A/D conversion result (D0–D12) and converter status data are clocked out by the falling edge of SCLK on this pin. The word length and format of this result can vary (see *Table 1*). The word length and format are controlled by the data shifted into the multiplexer address and mode select register (see *Table 5*).

EOC — This pin is an active push/pull output and indicates the status of the ADC12L030/2/4/8. When low, it signals that the A/D is busy with a conversion, auto-calibration, auto-zero or power down cycle. The rising edge of EOC signals the end of one of these cycles.

$\overline{CS}$ — This is the chip select pin. When a logic low is applied to this pin, the rising edge of SCLK shifts the data on DI into the address register. This low also brings DO out of TRI-STATE. With $\overline{CS}$ low the falling edge of SCLK shifts the data resulting from the previous ADC conversion out on DO, with the exception of the first bit of data. When $\overline{CS}$ is low continuously, the first bit of the data is clocked out on the rising edge of EOC (end of conversion). When $\overline{CS}$ is toggled the falling edge of $\overline{CS}$ always clocks out the first bit of data. $\overline{CS}$ should be brought low when SCLK is low. The falling edge of $\overline{CS}$ resets a conversion in progress and starts the sequence for a new conversion. When $\overline{CS}$ is brought back low during a conversion, that conversion is prematurely ended. The data in the output latches may be corrupted. Therefore, when $\overline{CS}$ is brought back low during a conversion in progress the data output at that time should be ignored. $\overline{CS}$ may also be left continuously low. In this case it is imperative that the correct number of SCLK pulses be applied to the ADC in order to remain synchronous. After the ADC supply power is applied, it expects to see 13 clock pulses for each I/O sequence. The number of clock pulses the ADC expects is the same as the digital output word length. This word length can be modified by the data shifted in on the DO pin. *Table 5* details the data required.

$\overline{DOR}$ — This is the data output ready pin. This pin is an active push/pull output. It is low when the conversion result is being shifted out and goes high to signal that all the data has been shifted out.

$\overline{CONV}$ — A logic low is required on this pin to program any mode or change the ADC's configuration as listed in the Mode Programming Table (*Table 5*) such as 12-bit conversion, 8-bit conversion, Auto Cal, Auto Zero etc. When this pin is high the ADC is placed in the read data only mode. While in the read data only mode, bringing $\overline{CS}$ low and pulsing SCLK will only clock out on DO any data stored in the ADCs output shift register. The data on DI will be neglected. A new conversion will not be started and the ADC will remain in the mode and/or configuration previously programmed. Read data only cannot be performed while a conversion, Auto-Cal or Auto-Zero are in progress.

PD — This is the power down pin. When PD is high the A/D is powered down; when PD is low the A/D is powered up. The A/D takes a maximum of 700 µs to power up after the command is given.

CH0–CH7 — These are the analog inputs of the MUX. A channel input is selected by the address information at the DI pin, which is loaded on the rising edge of SCLK into the address register (see *Tables 2, 3, 4*).

The voltage applied to these inputs should not exceed V_A+ or go below GND. Exceeding this range on an unselected channel will corrupt the reading of a selected channel.

COM — This pin is another analog input pin. It is used as a pseudo ground when the analog multiplexer is single-ended.

MUXOUT1, MUXOUT2 — These are the multiplexer output pins.

A/DIN1, A/DIN2 — These are the converter input pins. MUXOUT1 is usually tied to A/DIN1. MUXOUT2 is usually tied to A/DIN2. If external circuitry is placed between MUXOUT1 and A/DIN1, or MUXOUT2 and A/DIN2 it may be necessary to protect these pins. The voltage at these pins should not exceed $V_A{}^+$ or go below AGND (see *Figure 5*).

$V_{REF}+$ — This is the positive analog voltage reference input. In order to maintain accuracy the voltage range of V_{REF} ($V_{REF} = V_{REF}+ - V_{REF}-$) is

Pin Descriptions (Continued)

1 V_{DC} to 3.3 V_{DC} and the voltage at $V_{REF}+$ cannot exceed V_A+. See *Figure 6* for recommended bypassing.

$V_{REF}-$ The negative voltage reference input. In order to maintain accuracy the voltage at this pin must not go below GND or exceed V_A+. (See *Figure 6*).

V_A+, V_D+ These are the analog and digital power supply pins. $V_A{}^+$ and $V_D{}^+$ are not connected together on the chip. These pins should be tied to the same power supply and bypassed separately (see *Figure 6*). The operating voltage range of V_A+ and V_D+ is 3.0 V_{DC} to 5.5 V_{DC}.

DGND This is the digital ground pin (see *Figure 6*).

AGND This is the analog ground pin (see *Figure 6*).

National Semiconductor

ADC12L063
12-Bit, 62 MSPS, 354 mW A/D Converter with Internal Sample-and-Hold

General Description

The ADC12L063 is a monolithic CMOS analog-to-digital converter capable of converting analog input signals into 12-bit digital words at 62 Megasamples per second (MSPS), minimum. This converter uses a differential, pipelined architecture with digital error correction and an on-chip sample-and-hold circuit to minimize die size and power consumption while providing excellent dynamic performance. Operating on a single 3.3V power supply, this device consumes just 354 mW at 62 MSPS, including the reference current. The Power Down feature reduces power consumption to just 50 mW.

The differential inputs provide a full scale input swing equal to $\pm V_{REF}$ with the possibility of a single-ended input. Full use of the differential input is recommended for optimum performance. For ease of use, the buffered, high impedance, single-ended reference input is converted on-chip to a differential reference for use by the processing circuitry. Output data format is 12-bit offset binary.

This device is available in the 32-lead LQFP package and will operate over the industrial temperature range of −40°C to +85°C.

Features

- Single supply operation
- Low power consumption
- Power down mode
- On-chip reference buffer

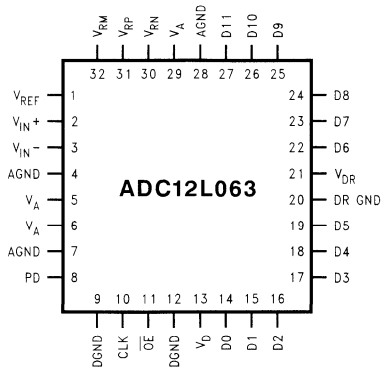
Key Specifications

Resolution	12 Bits
Conversion Rate	62 MSPS(min)
Bandwidth	170MHz
DNL	±0.5 LSB(typ)
INL	±1.0 LSB(typ)
SNR	66 dB(typ)
SFDR	78 dB(typ)
Data Latency	6 Clock Cycles
Supply Voltage	+3.3V ± 300 mV
Power Consumption, 40 MHz	354 mW(typ)

Applications

- Ultrasound and Imaging
- Instrumentation
- Cellular Base Stations/Communications Receivers
- Sonar/Radar
- xDSL
- Wireless Local Loops
- Data Acquisition Systems
- DSP Front Ends

Connection Diagram

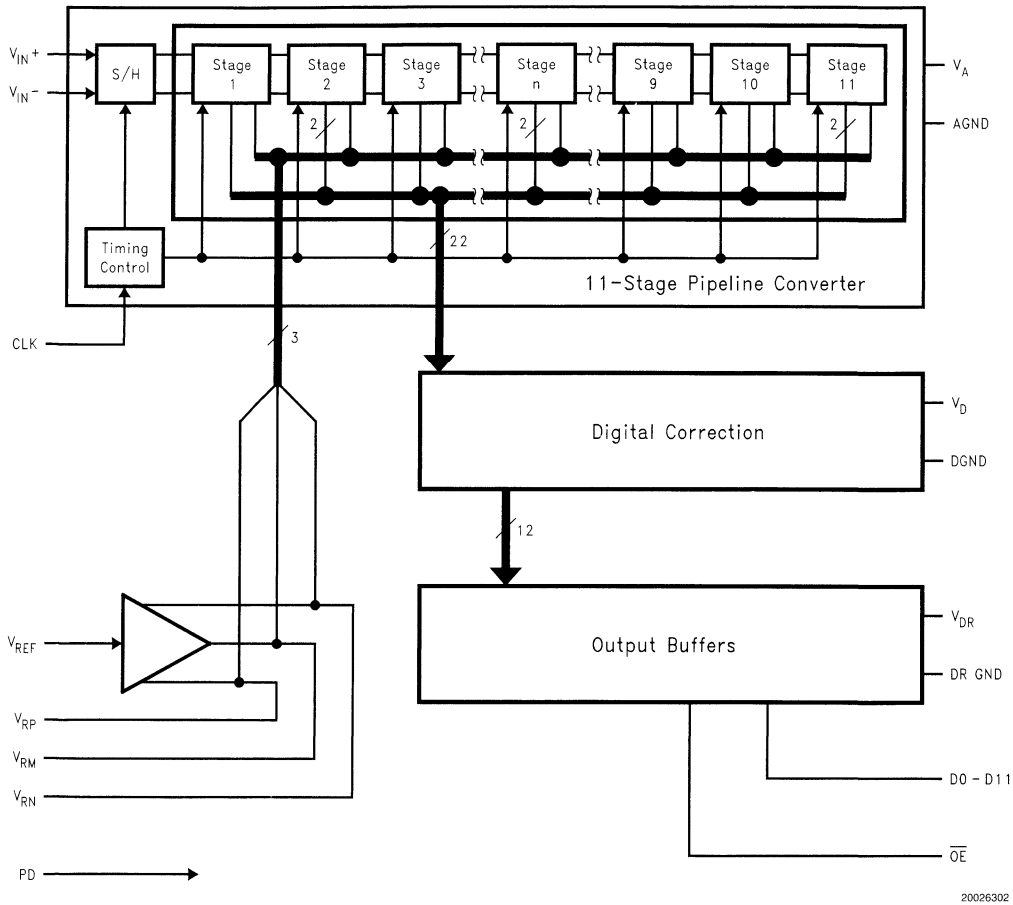


20026301

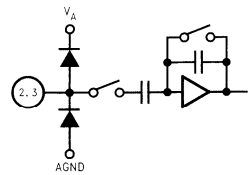
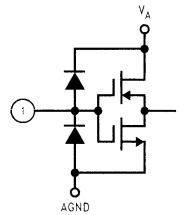
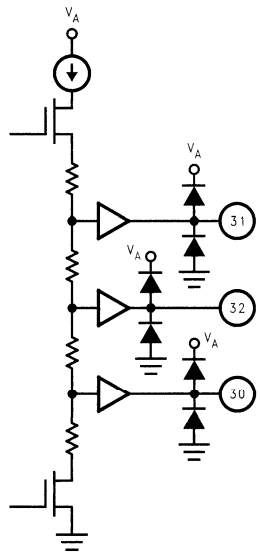
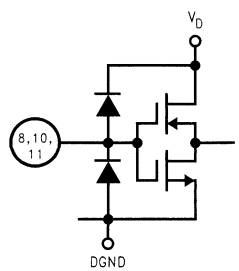
Ordering Information

Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	Package
ADC12L063CIVY	32 Pin LQFP
ADC12L063CIVYX	32 Pin LQFP Tape and Reel
ADC12L063EVAL	Evaluation Board

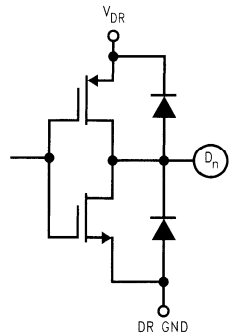
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	V_{IN^+}		Non-Inverting analog signal Input. With a 1.0V reference voltage the input signal level is 1.0 V_{P-P}.
3	V_{IN^-}		Inverting analog signal Input. With a 1.0V reference voltage the input signal level is 1.0 V_{P-P}. This pin may be connected to V_{CM} for single-ended operation, but a differential input signal is required for best performance.
1	V_{REF}		Reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 1.0V nominal and should be between 0.8V and 1.2V.
31	V_{RP}		These pins are high impedance reference bypass pins only. Connect a 0.1 µF capacitor from each of these pins to AGND. DO NOT connect anything else to these pins.
32	V_{RM}		
30	V_{RN}		
DIGITAL I/O			
10	CLK		Digital clock input. The range of frequencies for this input is 1 MHz to 70 MHz (typical) with guaranteed performance at 62 MHz. The input is sampled on the rising edge of this input.
11	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE data output pins. When this pin is high, the outputs are in a high impedance state.
8	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
14–19, 22–27	D0–D11		Digital data output pins that make up the 12-bit conversion results. D0 is the LSB, while D11 is the MSB of the offset binary output word.
ANALOG POWER			
5, 6, 29	V_A		Positive analog supply pins. These pins should be connected to a quiet +3.3V source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and with a 10 µF capacitor.
4, 7, 28	AGND		The ground return for the analog supply.
DIGITAL POWER			
13	V_D		Positive digital supply pin. This pin should be connected to the same quiet +3.3V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin. Decouple this pin from the V_A pins.
9, 12	DGND		The ground return for the digital supply.
21	V_{DR}		Positive digital supply pin for the ADC12L063's output drivers. This pin should be connected to a voltage source of +2.5V to V_D and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor. The voltage at this pin should never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
20	DR GND		The ground return for the digital supply for the ADC12L063's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC12L063's DGND or AGND pins. See Section 5.0 (Layout and Grounding) for more details.

National Semiconductor

ADC14061
Self-Calibrating 14-Bit, 2.5 MSPS, 390 mW A/D Converter

General Description

The ADC14061 is a self-calibrating 14-bit, 2.5 Megasample per second analog to digital converter. It operates on a single +5V supply, consuming just 390mW (typ).

The ADC14061 provides an easy and affordable upgrade from 12 bit converters. The ADC14061 may also be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC14061 operates with excellent dynamic performance at input frequencies up to ½ the clock frequency. The calibration feature of the ADC14061 can be used to get more consistent and repeatable results over the entire operating temperature range. On-command self-calibration reduces many of the effects of temperature-induced drift, resulting in more repeatable conversions.

The Power Down feature reduces power consumption to less than 2mW.

The ADC14061 comes in a TQFP and is designed to operate over the commercial temperature range of 0°C to +70°C.

Features

- Single +5V Operation
- Auto-Calibration
- Power Down Mode
- TTL/CMOS Input/Output compatible

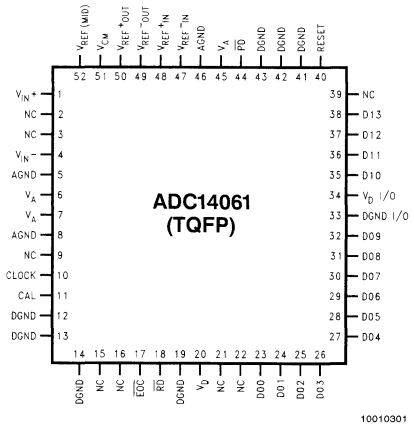
Key Specifications

■ Resolution	14 Bits
■ Conversion Rate	2.5 Msps (min)
■ DNL	0.3 LSB (typ)
■ SNR (f_{IN} = 500 kHz)	80 dB (typ)
■ ENOB	12.8 Bits (typ)
■ Supply Voltage	+5V ±5%
■ Power Consumption	390mW (typ)

Applications

- Instrumentation
- PC-Based Data Acquisition
- Data Communications
- Blood Analyzers
- Sonar/Radar

Connection Diagram

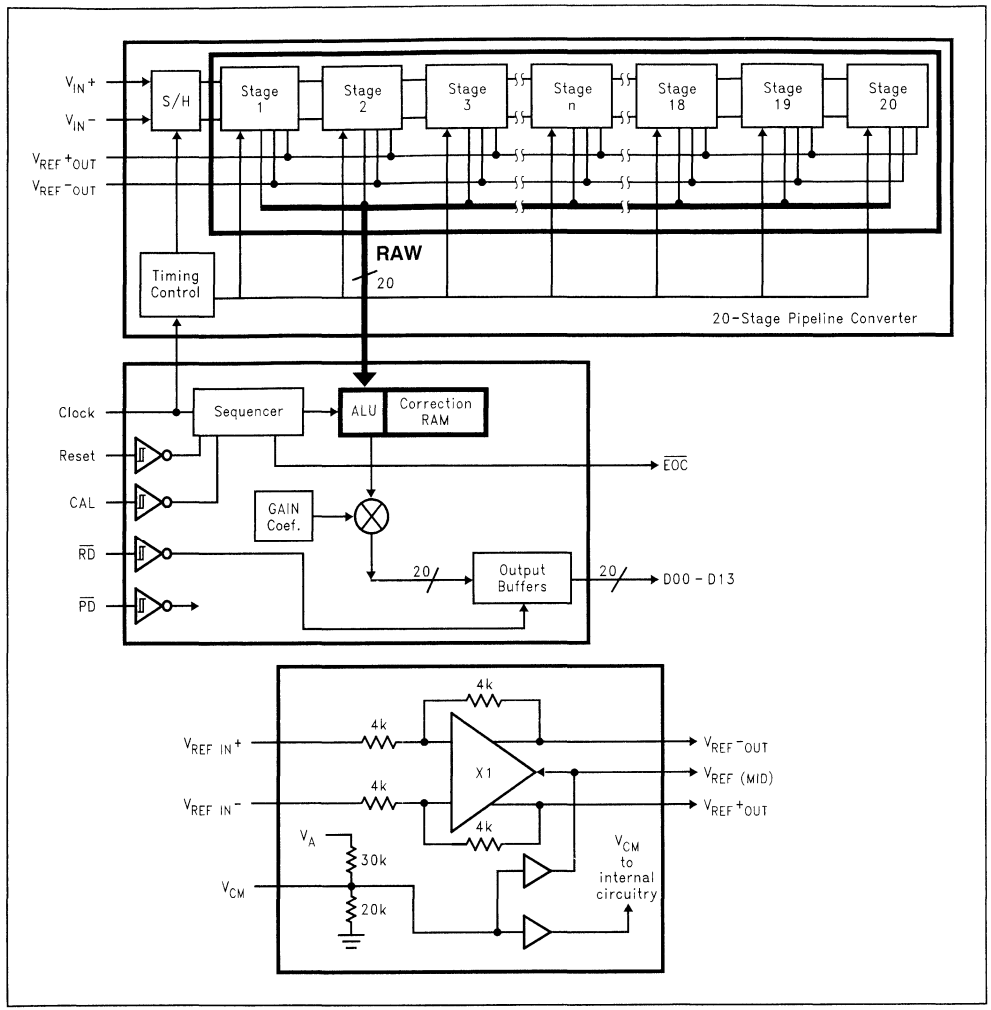


10010301

Ordering Information

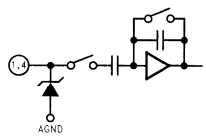
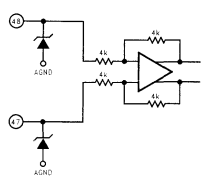
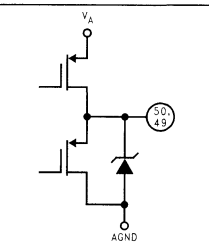
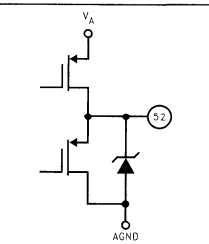
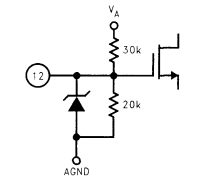
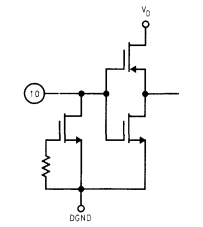
Commercial (0°C ≤ TA ≤ +70°C)	Package
ADC14061CCVT	VEG52A 52 Pin Thin Quad Flat Pack
ADC14061EVAL	Evaluation Board

Block Diagram

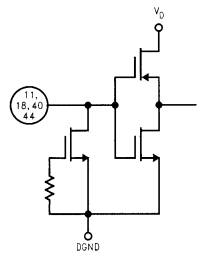
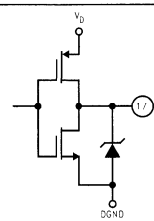
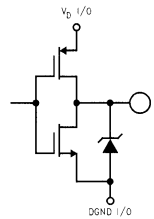


10010302

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
1	$V_{IN}+$		Non-Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 volt to 3.0 Volts.
4	$V_{IN}-$		Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 Volt to 3.0 Volts. The input signal should be balanced for best performance.
48	$V_{REF}+$ IN		Positive reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ minus V_{REF-} IN should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+$ IN minus $V_{REF}-$ IN.
47	$V_{REF}-$ IN		Negative reference input. In most applications this pin should be connected to AGND and the full reference voltage applied to $V_{REF}+$ IN. If the application requires that $V_{REF}-$IN be offset from AGND, this pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ IN minus V_{REF-} IN should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+$ IN minus $V_{REF}-$ IN .
50	$V_{REF}+$ OUT		Output of the high impedance positive reference buffer. With a 2.0V reference input, and with a V_{CM} of 2.0V, this pin will have a 3.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
49	REF− OUT		The output of the negative reference buffer. With a 2.0V reference and a V_{CM} of 2.0V, this pin will have a 1.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
52	V_{REF} (MID)		Output of the reference mid-point, nominally equal to 0.4 V_A (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. This voltage is derived from V_{CM}.
51	V_{CM}		Input to the common mode buffer, nominally equal to 40% of the supply voltage (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. Best performance is obtained if this pin is driven with a low impedance source of 2.0V.
Digital I/O			
10	Clock		Digital clock input. The input voltage is captured t_{AD} after the fall of the clock signal. The range of frequencies for this input is 300 kHz to 2.5 MHz. The clock frequency should not be changed or interrupted during conversion or while reading data output.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
11	CAL		CAL is a level-sensitive digital input that, when pulsed high for at least two clock cycles, puts the ADC into the CALIBRATE mode. Calibration should be performed upon ADC power-up (after asserting a reset) and each time the temperature changes by more than 50°C since the ADC14061 was last calibrated. See Section 2.3 for more information.
40	RESET		RESET is a level-sensitive digital input that, when pulsed high for at least 2 CLOCK cycles, results in the resetting of the ADC. This reset pulse must be applied after ADC power-up, before calibration.
18	$\overline{RD}$		$\overline{RD}$ is the (READ) digital input that, when low, enables the output data buffers. When this input pin is high, the output data bus is in a high impedance state.
44	$\overline{PD}$		$\overline{PD}$ is the Power Down input that, when low, puts the converter into the power down mode. When this pin is high, the converter is in the active mode.
17	$\overline{EOC}$		$\overline{EOC}$ is a digital output that, when low, indicates the availability of new conversion results at the data output pins.
23-32 35-38	D00-13		Digital data outputs that make up the 14-bit TRI-STATE conversion results. D00 is the LSB, while D13 is the MSB (SIGN bit) of the two's complement output word.
Analog Power			
6, 7, 45	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet +5V source and bypassed to AGND with 0.1 µF monolithic capacitors in parallel with 10 µF capacitors, both located within 1 cm of these power pins.
5, 8, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC14061 package. See Section 5 (Layout and grounding) for more details).
Digital Power			
20	V_D		Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10µF capacitor, both located within 1 cm of the power pin.
12,13 14,19, 41,42, 43	DGND		The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC14061 package. See Section 5 (Layout and Grounding) for more details.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
34	V_D I/O		Positive digital supply pin for the ADC14061's output drivers. This pin should be connected to a +3V to +5V source and bypassed to DGND I/O with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. All bypass capacitors should be located within 1 cm of the supply pin.
33	DGND I/O		The ground return for the digital supply for the ADC14061's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC14061's DGND or AGND pins. See Section 5.0 (Layout and Grounding) for more details.
NC			
2, 3, 9, 15, 16, 21, 22, 39	NC		All pins marked NC (no connect) should be left floating. Do not connect the NC pins to ground, power supplies, or any other potential or signal. These pins are used for test in the manufacturing process.

National Semiconductor

ADC14071
14-Bit, 7 MSPS, 380 mW A/D Converter

General Description

The ADC14071 is a 14-bit, monotholic analog to digital converter capable of conversion rates up to 8 Megasamples per second. This CMOS converter uses a differential, piperlined architecture with digital error correction and an on-chip track-and-hold circuit to maintain superb dynamic performance with input frequencies up to 20MHz. Tested and guaranteed dynamic performance specifications provide the designer with known performance. The ADC14071 operates on a +5V single supply consuming just 380mW (typical). The Power Down feature reduces power consumption to 20mW, typical.

The differential inputs provide a full scale input swing of $\pm V_{REF}$ with the possibility of a single input. Full use of the differential input is recommended for optimum perfomance. For ease of use, the reference input is single ended. This single-ended reference input is converted on-chip to a differential reference configuration for use by the processing circuitry. Output data format is 14-bit straight binary.

The ADC14071 may be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC14071 comes in a 48-pin TQFP and is specified to operate over the industrial temperature range of −40°C to +85°C.

Features

- Single +5V Operation
- Power Down Mode
- TTL/CMOS Input/Output Compatible

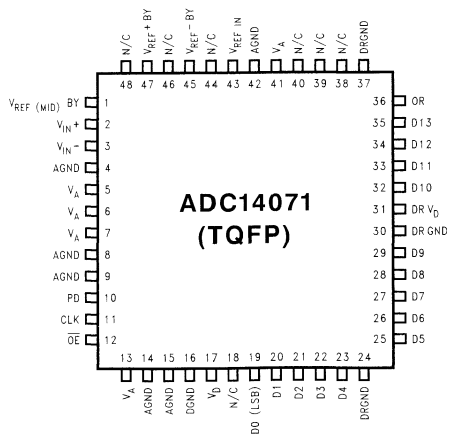
Key Specifications

■ Resolution	14 Bits
■ Max Conversion Rate	7 Msps (min)
■ DNL	±0.6 LSB (typ)
■ SNR (f_{IN} = 500 kHz)	80 dB (typ)
■ ENOB (f_W = 500 kHz)	12.6 Bits (typ)
■ Supply Voltage	+5V ±5%
■ Power Consumption	380 mW (typ)

Applications

- Document Scanners
- Imaging
- Instrumentation
- PC-Based Data Acquisition
- Spectrum Analyzers
- Sonar/Radar
- xDSL
- Wireless Local Loop
- Data Acquisition Systems
- DSP Front End

Connection Diagram

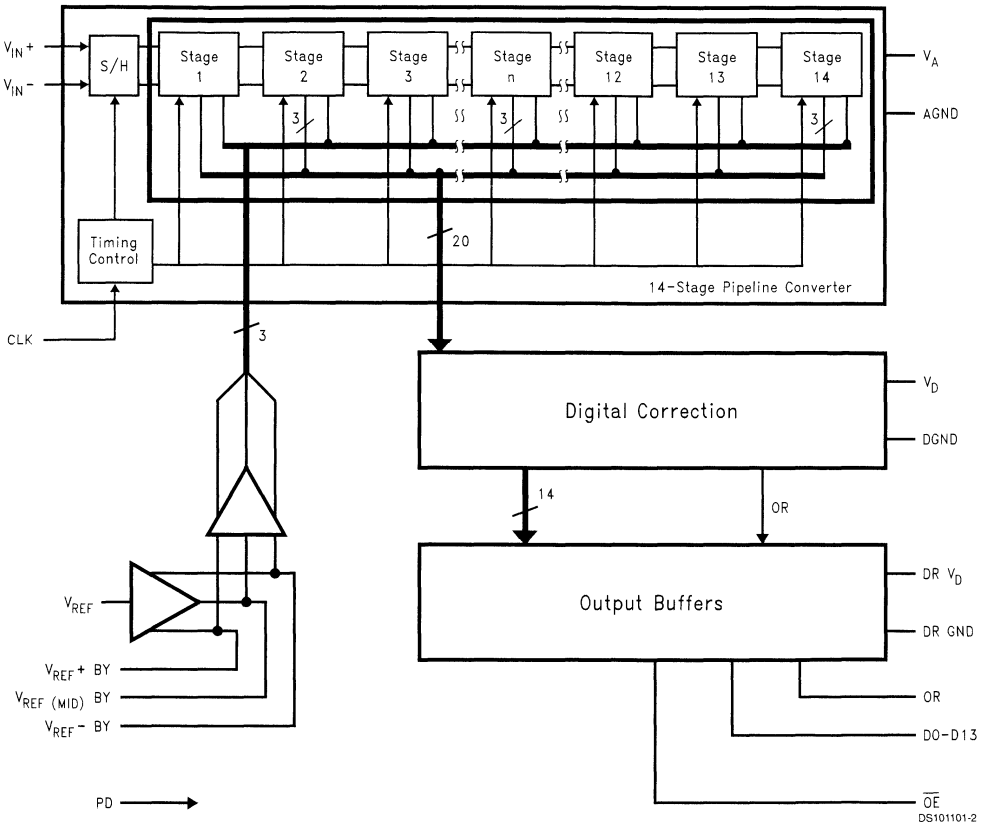


DS101101-1

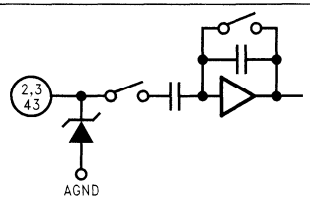
Ordering Information

Industrial Temperature Range ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)	NS Package
ADC14071CIVBH	VBH48A 48-Pin Thin Quad Flatpak
ADC14071EVAL	Evaluation System

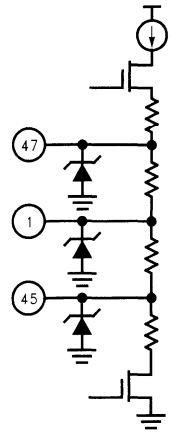
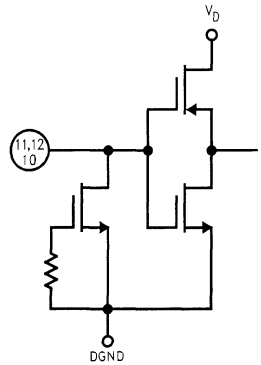
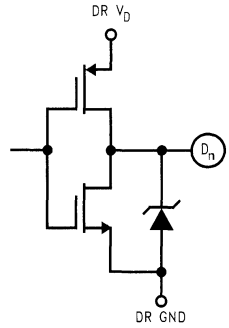
Block Diagram



Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
2	$V_{IN}+$		Non-Inverting analog signal input. With a 2.0V reference voltage the input signal voltage range is from 0V to 2.0V.
3	$V_{IN}-$		Inverting analog signal input. With a 2.0V reference voltage the input signal voltage range is from 0V to 2.0V. This pin may be connected to a voltage of ½ the reference voltage for single-ended operation, but a balanced input signal is required for best performance.
43	$V_{REF\ IN}$		Positive reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. V_{REF} is 2.0V nominal and should be in the range of 1.0V to 2.7V.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
ANALOG I/O			
47	V_{REF}+ BY		These pins are high impedance reference bypass pins only. Connect a 0.1µF capacitor from each of these pins the AGND. DO NOT connect anything else to these pins.
1	$V_{REF\ (MID)}$ BY		
45	V_{REF}− BY		
DIGITAL I/O			
11	CLOCK		Digital clock input. The range of frequencies for this input is 25 kHz to 8 MHz (typical) with guaranteed performance at 7 MHz. The input is sampled on the rising edge of this input.
12	$\overline{OE}$		$\overline{OE}$ is the output enable pin that, when low, enables the TRI-STATE® data output pins. When this pin is high, the outputs are in a high impedance state.
10	PD		PD is the Power Down input pin. When high, this input puts the converter into the power down mode. When this pin is low, the converter is in the active mode.
36	OR		Out of Range pin. A high at this output pin indicates that the input voltage is either above the reference voltage or is below ground. When this pin is high, the digital output pins will indicate a full scale for input voltages above the reference voltage, or will indicate a zero scale for input voltages below zero scale.
19-23, 25-29, 32-35	D0–D13		Digital data output pins that make up the 14-bit conversion results. D0 is the LSB, while D13 is the MSB of the straight binary output word.
ANALOG POWER			
5, 6, 7, 13, 41	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet +5V voltage source and bypassed to AGND with 0.1 µF monolithic capacitors located within 1 cm of these power pins, and by a 10 µF capacitor.
4, 8, 9, 14, 15, 42	AGND		The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC14071 package. See Section 5 (Layout and Grounding) for more details.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
DIGITAL POWER			
17	V_D		Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor, both located within 1 cm of the power pin.
16	DGND		The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC14071 package. See Section 5 (Layout and Grounding) for more details.
31	DR V_D		Positive digital supply pin for the ADC14071's output drivers. This pin should be connected to a voltage source of +3 to +5V and bypassed to DR GND with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF tantalum capacitor and never exceed the voltage on V_D. All bypass capacitors should be located within 1 cm of the supply pin.
24, 30, 37	DR GND		The ground return for the digital supply for the ADC14071's output drivers. These pins should be connected to the system digital ground, but not be connected in close proximity to the ADC14071's DGND or AGND pins. See Section 5 (Layout and Grounding) for more details.
NC			
18, 38, 39, 40, 44, 46, 48	NC		All pins marked NC (no connect) should not be connected to any potential (or to ground). Allow these pins to float.

National Semiconductor

ADC14161
Low-Distortion, Self-Calibrating 14-Bit, 2.5 MSPS, 390 mW A/D Converter

General Description

The ADC14161 is a self-calibrating 14-bit, 2.5 Megasample per second analog to digital converter. It operates on a single +5V supply, consuming just 390mW (typical).

The ADC14161 provides an easy and affordable upgrade from 12 bit converters. The ADC14161 may also be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC14161 operates with input frequencies up to ½ the clock frequency. The calibration feature of the ADC14161 can be used to get more consistent and repeatable results over the entire operating temperature range. On-command self-calibration reduces many of the effects of temperature-induced drift, resulting in more repeatable conversions.

Tested and guaranteed dynamic performance specifications provide the designer with known performance.

The Power Down feature reduces power consumption to less than 2mW.

The ADC14161 comes in a TQFP and is designed to operate over the industrial temperature range of −40°C to +85°C.

Features

- Single +5V Operation
- Auto-Calibration
- Power Down Mode
- TTL/CMOS Input/Output compatible

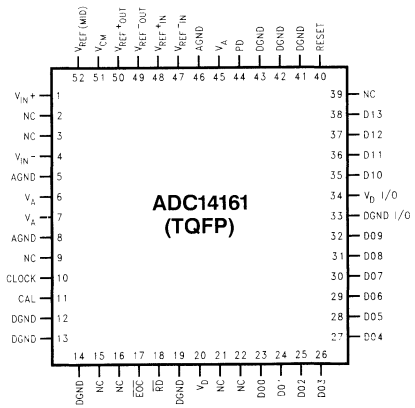
Key Specifications

■ Resolution	14 Bits
■ Conversion Rate	2.5 Msps (min)
■ DNL	0.3 LSB (typ)
■ SNR (f_{IN} = 500 kHz)	80 dB (typ)
■ ENOB	12.8 Bits (typ)
■ Supply Voltage	+5V ±5%
■ Power Consumption	390mW (typ)

Applications

- Instrumentation
- PC-Based Data Acquisition
- Data Communications
- Blood Analyzers
- Sonar/Radar

Connection Diagram

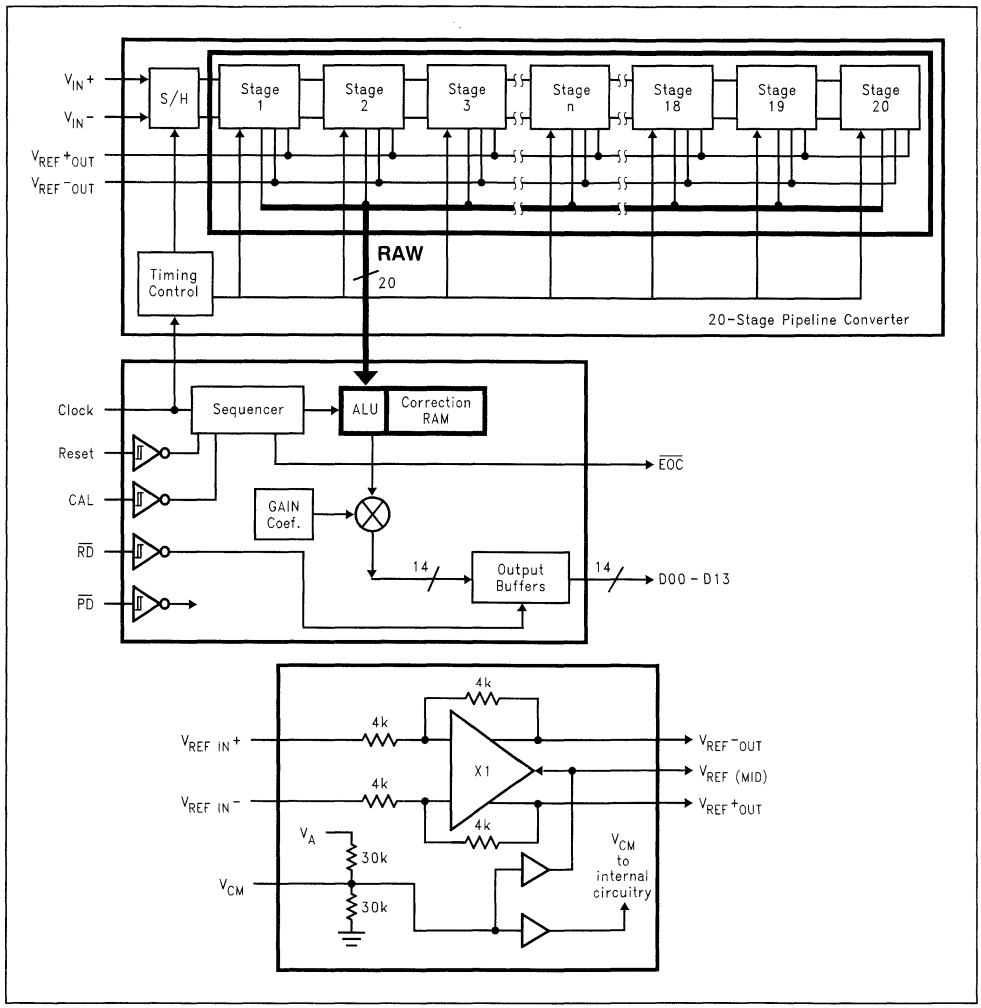


10015401

Ordering Information

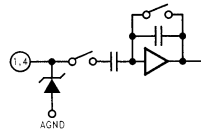
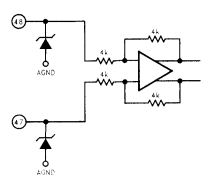
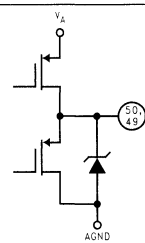
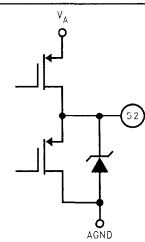
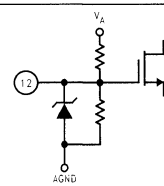
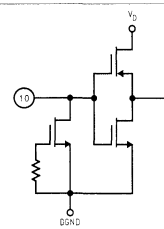
Industrial ($-40^{\circ}C \leq TA \leq +85^{\circ}C$)	Package
ADC14161CIVT	VEG52A 52 Pin Thin Quad Flat Pack
ADC14161EVAL	Evaluation Board

Block Diagram

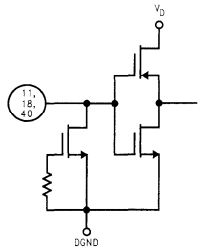
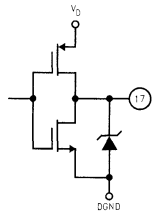
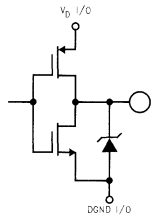


10015402

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
1	$V_{IN}+$		Non-Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 volt to 3.0 Volts.
4	$V_{IN}-$		Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 Volt to 3.0 Volts. The input signal should be balanced for best performance.
48	$V_{REF}+$ IN		Positive reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ minus V_{REF-} IN should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+$ IN minus $V_{REF}-$ IN.
47	$V_{REF}-$ IN		Negative reference input. In most applications this pin should be connected to AGND and the full reference voltage applied to $V_{REF}+$ IN. If the application requires that $V_{REF}-$IN be offset from AGND, this pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ IN minus V_{REF-} IN should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+$ IN minus $V_{REF}-$ IN .
50	$V_{REF}+$ OUT		Output of the high impedance positive reference buffer. With a 2.0V reference input, and with a V_{CM} of 2.0V, this pin will have a 3.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
49	REF− OUT		The output of the negative reference buffer. With a 2.0V reference and a V_{CM} of 2.0V, this pin will have a 1.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
52	V_{REF} (MID)		Output of the reference mid-point, nominally equal to 0.4 V_A (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. This voltage is derived from V_{CM}.
51	V_{CM}		Input to the common mode buffer, nominally equal to 40% of the supply voltage (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. Best performance is obtained if this pin is driven with a low impedance source of 2.0V.
Digital I/O			
10	Clock		Digital clock input. The input voltage is captured t_{AD} after the fall of the clock signal. The range of frequencies for this input is 300 kHz to 2.5 MHz. The clock frequency should not be changed or interrupted during conversion or while reading data output.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
11	CAL		CAL is a level-sensitive digital input that, when pulsed high for at least two clock cycles, puts the ADC into the CALIBRATE mode. Calibration should be performed upon ADC power-up (after asserting a reset) and each time the temperature changes by more than 50°C since the ADC14161 was last calibrated. See Section 2.3 for more information.
40	RESET		RESET is a level-sensitive digital input that, when pulsed high for at least 2 CLOCK cycles, results in the resetting of the ADC. This reset pulse must be applied after ADC power-up, before calibration.
18	$\overline{RD}$		$\overline{RD}$ is the (READ) digital input that, when low, enables the output data buffers. When this input pin is high, the output data bus is in a high impedance state.
44	$\overline{PD}$		$\overline{PD}$ is the Power Down input that, when low, puts the converter into the power down mode. When this pin is high, the converter is in the active mode.
17	$\overline{EOC}$		$\overline{EOC}$ is a digital output that, when low, indicates the availability of new conversion results at the data output pins.
23-32 35-38	D00-13		Digital data outputs that make up the 14-bit TRI-STATE conversion results. D00 is the LSB, while D13 is the MSB (SIGN bit) of the two's complement output word.
Analog Power			
6, 7, 45	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet +5V source and bypassed to AGND with 0.1 µF monolithic capacitors in parallel with 10 µF capacitors, both located within 1 cm of these power pins.
5, 8, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC14161 package. See Section 5 (Layout and grounding) for more details).
Digital Power			
20	V_D		Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source of as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10µF capacitor, both located within 1 cm of the power pin.
12,13 14,19 41,42 43	DGND		The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC14161 package. See Section 5 (Layout and Grounding) for more details.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
34	V_D I/O		Positive digital supply pin for the ADC14161's output drivers. This pin should be connected to a +3V to +5V source and bypassed to DGND I/O with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. All bypass capacitors should be located within 1 cm of the supply pin.
33	DGND I/O		The ground return for the digital supply for the ADC14161's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC14161's DGND or AGND pins. See Section 5.0 (Layout and Grounding) for more details.
NC			
2, 3, 9,15, 16,21 22,39	NC		All pins marked NC (no connect) should be left floating. Do not connect the NC pins to ground, power supplies, or any other potential or signal. These pins are used for test in the manufacturing process.

National Semiconductor

ADC16061
Self-Calibrating 16-Bit, 2.5 MSPS, 390 mW A/D Converter

General Description

The ADC16061 is a self-calibrating 16-bit, 2.5 Megasample per second analog to digital converter. It operates on a single +5V supply, consuming just 390mW (typical).

The ADC16061 provides an easy and affordable upgrade from 12 bit and 14 bit converters. The ADC16061 may also be used to replace many hybrid converters with a resultant saving of space, power and cost.

The ADC16061 operates with excellent dynamic performance at input frequencies up to ½ the clock frequency. The calibration feature of the ADC16061 can be used to get more consistent and repeatable results over the entire operating temperature range. On-command self-calibration reduces many of the effects of temperature-induced drift, resulting in more repeatable conversions.

The Power Down feature reduces power consumption to less than 2mW.

The ADC16061 comes in a TQFP and is designed to operate over the commercial temperature range of 0°C to +70°C.

Features

- Single +5V Operation
- Self Calibration
- Power Down Mode

Key Specifications

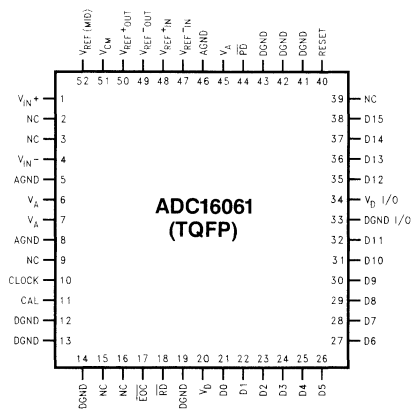
■ Resolution	16 Bits
■ Conversion Rate	2.5 Msps (min)
■ DNL	1.0 LSB (typ)
■ SNR (f_{IN} = 500 kHz)	80 dB (typ)
■ Supply Voltage	+5V ±5%
■ Power Consumption	390mW (typ)

Applications

- PC-Based Data Acquisition
- Document Scanners
- Digital Copiers
- Film Scanners
- Blood Analyzers
- Sonar/Radar

6

Connection Diagram

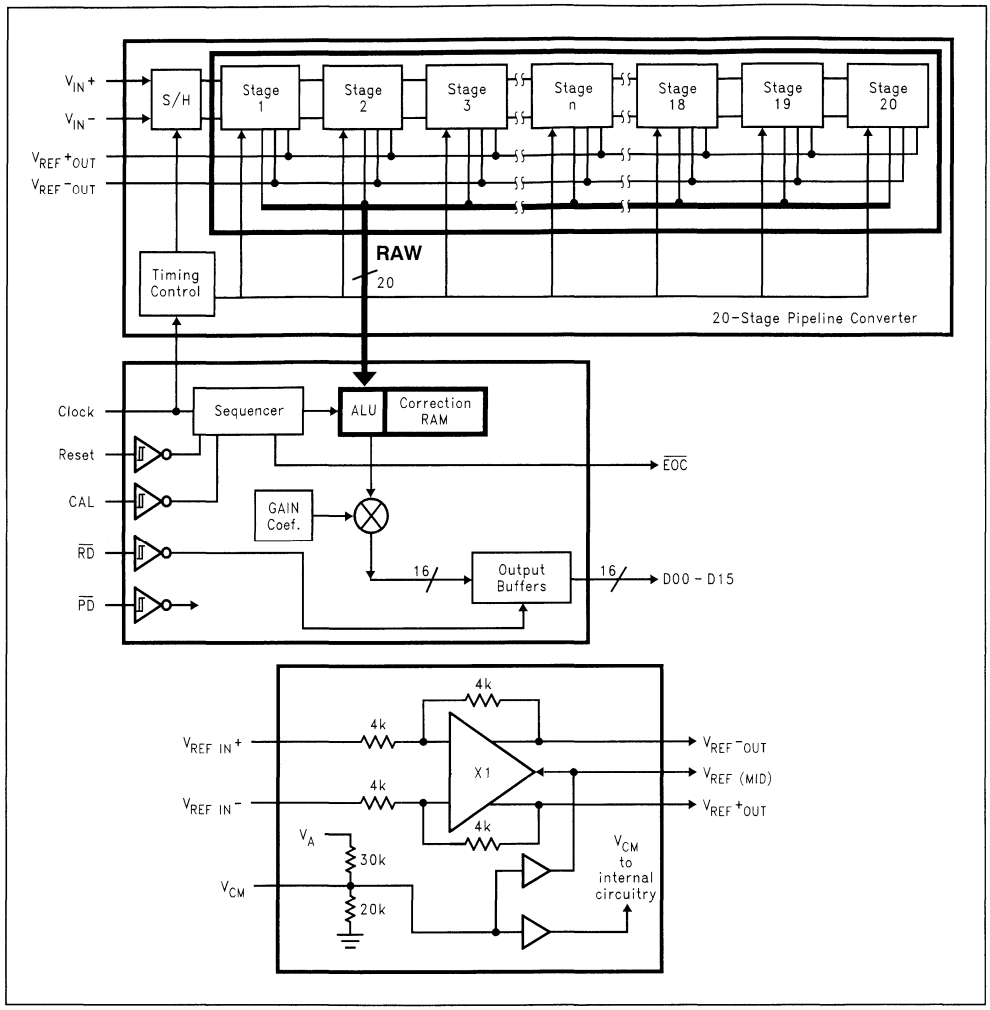


10088901

Ordering Information

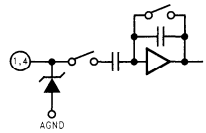
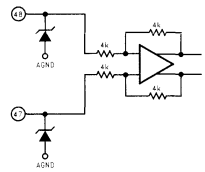
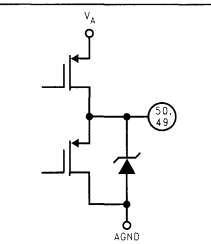
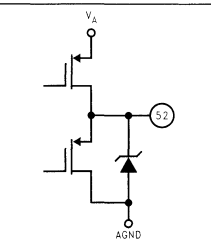
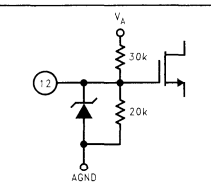
Commercial (0°C ≤ TA ≤ +70°C)	Package
ADC16061CCVT	VEG52A 52 Pin Thin Quad Flat Pack
ADC16061EVAL	Evaluation Board

Block Diagram

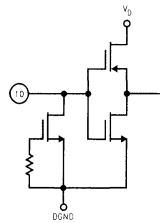
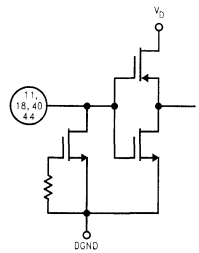
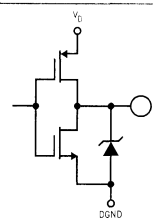
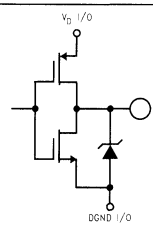


10088902

Pin Descriptions and Equivalent Circuits

Pin No.	Symbol	Equivalent Circuit	Description
Analog I/O			
1	$V_{IN}+$		Non-Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 volt to 3.0 Volts.
4	$V_{IN}-$		Inverting analog signal Input. With a 2.0V reference voltage and a 2.0V common mode voltage, V_{CM}, the input signal voltage range is from 1.0 Volt to 3.0 Volts. The input signal should be balanced for best performance.
48	$V_{REF}+_{IN}$		Positive reference input. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+$ minus $V_{REF-\ IN}$ should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+_{IN}$ minus $V_{REF}-_{IN}$.
47	$V_{REF}-_{IN}$		Negative reference input. In most applications this pin should be connected to AGND and the full reference voltage applied to $V_{REF}+_{IN}$. If the application requires that $V_{REF}-_{IN}$ be offset from AGND, this pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. $V_{REF}+_{IN}$ minus $V_{REF-\ IN}$ should be a minimum of 1.8V and a maximum of 2.2V. The full-scale input voltage is equal to $V_{REF}+_{IN}$ minus $V_{REF}-_{IN}$.
50	$V_{REF}+_{OUT}$		Output of the high impedance positive reference buffer. With a 2.0V reference input, and with a V_{CM} of 2.0V, this pin will have a 3.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
49	$V_{REF}-_{OUT}$		The output of the negative reference buffer. With a 2.0V reference and a V_{CM} of 2.0V, this pin will have a 1.0V output voltage. This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor in parallel with a 10 µF capacitor.
52	$V_{REF\ (MID)}$		Output of the reference mid-point, nominally equal to 0.4 V_A (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. This voltage is derived from V_{CM}.
51	V_{CM}		Input to the common mode buffer, nominally equal to 40% of the supply voltage (2.0V). This pin should be bypassed to AGND with a 0.1 µF monolithic capacitor. Best performance is obtained if this pin is driven with a low impedance source of 2.0V.

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
Digital I/O			
10	CLOCK		Digital clock input. The input voltage is captured t_{AD} after the fall of the clock signal. The range of frequencies for this input is 300 kHz to 2.5 MHz. The clock frequency should not be changed or interrupted during conversion or while reading data output.
11	CAL		CAL is a level-sensitive digital input that, when pulsed high for at least two clock cycles, puts the ADC into the CALIBRATE mode. Calibration should be performed upon ADC power-up (after asserting a reset) and each time the temperature changes by more than 50°C since the ADC16061 was last calibrated. See Section 2.3 for more information.
40	RESET		RESET is a level-sensitive digital input that, when pulsed high for at least 2 CLOCK cycles, results in the resetting of the ADC. This reset pulse must be applied after ADC power-up, before calibration.
18	$\overline{RD}$		$\overline{RD}$ is the (READ) digital input that, when low, enables the output data buffers. When this input pin is high, the output data bus is in a high impedance state.
44	$\overline{PD}$		$\overline{PD}$ is the Power Down input that, when low, puts the converter into the power down mode. When this pin is high, the converter is in the active mode.
17	$\overline{EOC}$		$\overline{EOC}$ is a digital output that, when low, indicates the availability of new conversion results at the data output pins.
21-32 35-38	D00-15		Digital data outputs that make up the 16-bit TRI-STATE conversion results. D00 is the LSB, while D15 is the MSB (SIGN bit) of the two's complement output word.
Analog Power			
6, 7, 45	V_A		Positive analog supply pins. These pins should be connected to a clean, quiet +5V source and bypassed to AGND with 0.1 µF monolithic capacitors in parallel with 10 µF capacitors, both located within 1 cm of these power pins.
5, 8, 46	AGND		The ground return for the analog supply. AGND and DGND should be connected together directly beneath the ADC16061 package. See Section 5 (Layout and grounding) for more details).

Pin Descriptions and Equivalent Circuits (Continued)

Pin No.	Symbol	Equivalent Circuit	Description
Digital Power			
20	V_D		Positive digital supply pin. This pin should be connected to the same clean, quiet +5V source as is V_A and bypassed to DGND with a 0.1 µF monolithic capacitor in parallel with a 10µF capacitor, both located within 1 cm of the power pin.
12, 13, 14, 19, 41, 42, 43	DGND		The ground return for the digital supply. AGND and DGND should be connected together directly beneath the ADC16061 package. See Section 5 (Layout and Grounding) for more details.
34	V_D I/O		Positive digital supply pin for the ADC16061's output drivers. This pin should be connected to a +3V to +5V source and bypassed to DGND I/O with a 0.1 µF monolithic capacitor. If the supply for this pin is different from the supply used for V_A and V_D, it should also be bypassed with a 10 µF capacitor. All bypass capacitors should be located within 1 cm of the supply pin.
33	DGND I/O		The ground return for the digital supply for the ADC16061's output drivers. This pin should be connected to the system digital ground, but not be connected in close proximity to the ADC16061's DGND or AGND pins. See Section 5.0 (Layout and Grounding) for more details.
NC			
2, 3, 9, 15, 16, 39	NC		All pins marked NC (no connect) should be left floating. Do not connect the NC pins to ground, power supplies, or any other potential or signal. These pins are used for test in the manufacturing process.

National Semiconductor

ADCV0831
8 Bit Serial I/O Low Voltage Low Power ADC with Auto Shutdown in a SOT Package

General Description

The ADCV0831 is a low voltage 8-bit successive approximation A/D converter with serial I/O. The I/O is a 3-wire serial interface compatible with NSC's MICROWIRE™ & Motorola's SPI standards. It easily interfaces with standard shift registers or microprocessors.

Low voltage and auto shutdown features make the ADCV0831 ideal for portable battery operated electronic devices. The main benefits are most apparent in small portable electronic devices. The tiny A/D converter can be placed anywhere on the board.

Applications

- Digitizing automotive sensors
- Process control monitoring
- Remote sensing in noisy environments
- Instrumentation
- Test systems
- Embedded diagnostics

Features

- Tiny 6-pin SOT 23 package
- Serial digital data link requires few I/O pins
- Auto Shutdown
- 0V to 3V analog input range with single 3V power supply
- TTL/CMOS input/output compatible

Key Specifications

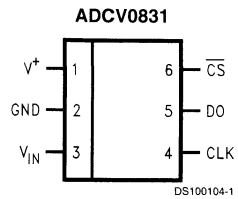
(For 3V supply, typical, unless otherwise noted.)

- Resolution: 8 bits
- Conversion time (f_C = 700 kHz): 16µs
- Low power dissipation: 720µW
- Single supply: 2.7V to $5V_{DC}$
- Linearity error: ±1.5LSB over temperature
- No missing codes over temperature
- Shutdown supply current 10nA

Ordering Information

Temperature Range ($0^\circ C \le T_j \le +70^\circ C$)	Package	Supplied As
ADCV0831M6	MA06A	1k Units Tape and Reel
ADCV0831M6X	MA06A	3k Units Tape and Reel

Connection Diagram



National Semiconductor

CLC5956
12-Bit, 65 MSPS Broadband Monolithic A/D Converter

General Description

The CLC5956 is a monolithic 12-bit, 65 MSPS analog-to-digital converter subsystem. The device has been optimized for use in cellular base stations and other applications where high resolution, high sampling rate, wide dynamic range, low power dissipation, and compact size are required. The CLC5956 features differential analog inputs, low jitter differential PECL clock inputs, a low distortion track-and-hold with DC to 300 MHz input bandwidth, a bandgap voltage reference, TTL compatible CMOS output logic, and a proprietary 12-bit multi-stage quantizer. The CLC5956 is fabricated on the ABIC-IV 0.8 micron BiCMOS process. The part features a 73 dB spurious free dynamic range (SFDR) and 67 dB SNR. The wideband track-and-hold allows sampling of IF signals to greater than 250 MHz. The part produces two-tone, dithered, spurious-free dynamic range of 83 dBFS at 75 MHz input frequency. The differential analog input provides excellent common-mode rejection, while the differential PECL clock inputs permit the use of balanced transmission to minimize jitter in distributed systems. The 48-pin TSSOP package provides an extremely small footprint for applications where space is a critical consideration. The CLC5956 operates from a single +5V power supply over the industrial temperature range of −40°C to +85°C. National thoroughly tests each part to verify full compliance with the guaranteed specifications.

Features

- Wide dynamic range
- IF sampling capability
- 300 MHz input bandwidth
- Small 48-pin TSSOP
- Single +5V supply
- Low cost

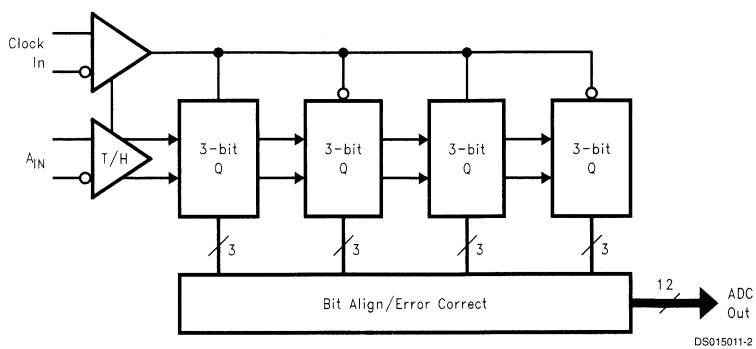
Key Specifications

Sample Rate	65 MSPS
SFDR	73 dBc
SFDR with dither	85 dBFS
SNR	67 dB
Low power consumption	615 mW

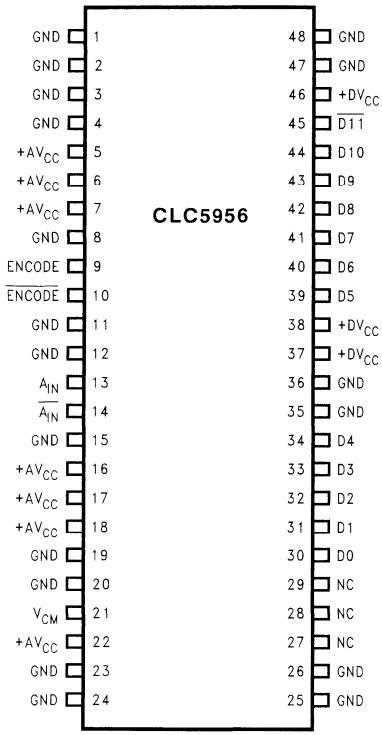
Applications

- Cellular base-stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video

Block Diagram



Pin Configuration



DS015011-1

Ordering Information

CLC5956IMTD	48-Pin TSSOP
CLC5956IMTDX	48-Pin TSSOP (Taped Reel)
CLC5956PCASM	Evaluation Board

Pin Descriptions

Pin Name	Pin No.	Description
A_{IN} / $\overline{A_{IN}}$	13, 14	Differential input with a common mode voltage of +2.4V. The ADC full scale input is 1.024 V_{PP} on each of the complimentary input signals.
ENCODE / $\overline{\text{ENCODE}}$	9, 10	Differential clock where ENCODE initiates a new data conversion cycle on each rising edge. Logic for these inputs are a 50% duty cycle differential PECL signal.
V_{CM}	21	Internal common mode voltage reference. Nominally +2.4V. Can be used for the input common mode voltage. This voltage is derived from an internal bandgap reference. V_{CM} should be buffered when driving any additional load beyond the input transformer. Failure to buffer this signal can cause errors in the internal bias currents.
D0–$\overline{\text{D11}}$	30–34, 39–45	Digital data outputs are CMOS and TTL compatible. D0 is the LSB and $\overline{\text{D11}}$ is the MSB. MSB is inverted. Output coding is two's complement.
GND	1–4, 8, 11, 12, 15, 19, 20, 23–26, 35, 36, 47, 48	Circuit ground.
+AV_{CC}	5–7, 16–18, 22	+5V power supply for the analog section. Bypass to ground with a 0.1 µF capacitor.
+DV_{CC}	37, 38, 46	+5V power supply for the digital section. Bypass to ground with a 0.1 µF capacitor.
NC	27, 28, 29	No connect. May be left open or grounded.

National Semiconductor

CLC5958
14-Bit, 52 MSPS A/D Converter

General Description

The CLC5958 is a monolithic 14-bit, 52 MSPS analog-to-digital converter. The ultra-wide dynamic range and high sample rate of the device make it an excellent choice for wideband receivers found in multi-channel base-stations. The CLC5958 integrates a low distortion track-and-hold amplifier and a 14-bit multi-stage quantizer on a single die. Other features include differential analog inputs, low jitter differential clock inputs, an internal bandgap voltage reference, and CMOS/TTL compatible outputs. The CLC5958 is fabricated on the National ABIC-V 0.8 micron BiCMOS process.

The CLC5958 features a 90 dB spurious free dynamic range (SFDR) and 70 dB signal-to-noise ratio (SNR). The balanced differential analog inputs ensure low even-order distortion, while the differential clock inputs permit the use of balanced clock signals to minimize clock jitter. The 48-pin CSP package provides an extremely small footprint for applications where space is a critical consideration. The package also provides a very low thermal resistance to ambient. The CLC5958 may be operated with a single +5V power supply. Alternatively, an additional supply may be used to program the digital output levels over the range of +3.3V to +5V. Operation over the industrial temperature range of –40°C to +85°C is guaranteed. National Semiconductor tests each part to verify compliance with the guaranteed specifications.

Features

- Ultra-wide dynamic range
- Excellent performance to Nyquist
- IF sampling capability
- Very small package: 48-pin CSP
- Programmable Output Levels: 3.3V to 5V

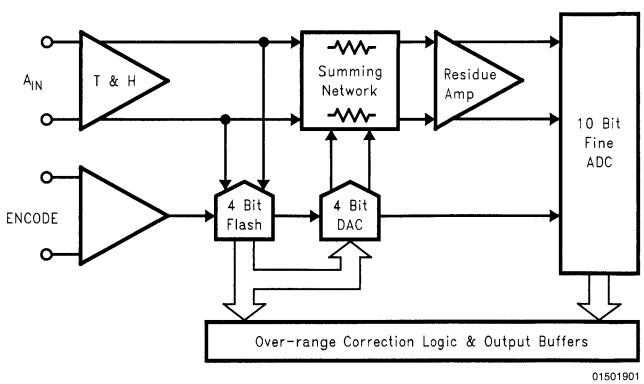
Key Specifications

■ Sample Rate	52 MSPS
■ SFDR	90 dB
■ Noise floor	–72 dBFS

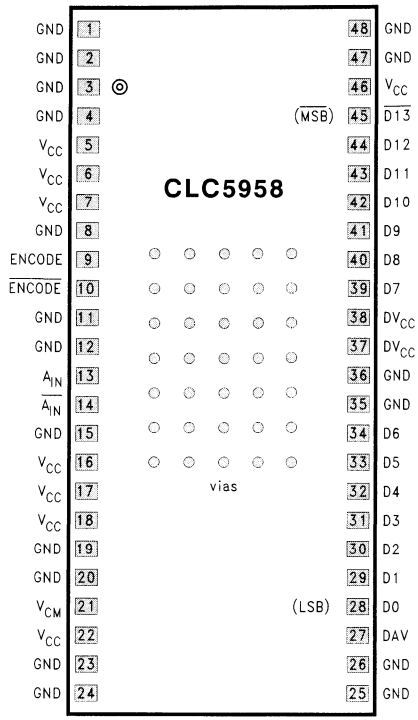
Applications

- Multi-channel basestations
- Multi-standard basestations: GSM, WCDMA, DAMPS, etc.
- Smart antenna systems
- Wireless local loop
- Wideband digital communications

Block Diagram



Pin Configuration



01501902

Ordering Information

CLC5958SLB	48-Pin CSP
CLC5958PCASM	Evaluation Board

Pin Descriptions

Pin Name	Pin No.	Description
A_{IN}, $\overline{A_{IN}}$	13, 14	Differential inputs. Self biased at a common mode voltage of +3.25V. The ADC full scale input is 2.048 V_{PP} differential.
ENCODE, $\overline{ENCODE}$	9, 10	Differential clock inputs. ENCODE initiates a new data conversion cycle on each rising edge. Clock signals may be sinusoidal or square waves with PECL encode levels. The falling edge of ENCODE clocks internal pipeline stages.
D0–$\overline{D13}$	28–34, 39–45	Digital data outputs. CMOS and TTL compatible. D0 is the LSB and $\overline{D13}$ is the inverted MSB. Output coding is two's complement.
DAV	27	Data valid. The rising edge of this signal occurs when output data is valid and may be used to latch data into following circuitry.
V_{CM}	21	Internal analog input common mode voltage reference. Nominally +3.25V. Can be used to establish the analog input common mode voltage for DC coupled applications (DC coupling not recommended, see applications section).
GND	1–4, 8, 11, 12, 15, 19, 20, 23–26, 35, 36, 47, 48 and vias	Circuit ground.
V_{CC}	5–7, 16–18, 22, 46	+5V power supply. Bypass each group of supply pins to ground with a 0.01 µF capacitor.
DV_{CC}	37, 38	+3.3V to +5V power supply for the digital outputs. Establishes the high output level for the digital outputs. Bypass to ground with a 0.1 µF capacitor.

National Semiconductor

DAC0800/DAC0802
8-Bit Digital-to-Analog Converters

General Description

The DAC0800 series are monolithic 8-bit high-speed current-output digital-to-analog converters (DAC) featuring typical settling times of 100 ns. When used as a multiplying DAC, monotonic performance over a 40 to 1 reference current range is possible. The DAC0800 series also features high compliance complementary current outputs to allow differential output voltages of 20 Vp-p with simple resistor loads as shown in *Figure 1*. The reference-to-full-scale current matching of better than ±1 LSB eliminates the need for full-scale trims in most applications while the nonlinearities of better than ±0.1% over temperature minimizes system error accumulations.

The noise immune inputs of the DAC0800 series will accept TTL levels with the logic threshold pin, V_{LC}, grounded. Changing the V_{LC} potential will allow direct interface to other logic families. The performance and characteristics of the device are essentially unchanged over the full ±4.5V to ±18V power supply range; power dissipation is only 33 mW with ±5V supplies and is independent of the logic input states.

The DAC0800, DAC0802, DAC0800C and DAC0802C are a direct replacement for the DAC-08, DAC-08A, DAC-08C, and DAC-08H, respectively.

Features

- Fast settling output current: 100 ns
- Full scale error: ±1 LSB
- Nonlinearity over temperature: ±0.1%
- Full scale current drift: ±10 ppm/°C
- High output compliance: −10V to +18V
- Complementary current outputs
- Interface directly with TTL, CMOS, PMOS and others
- 2 quadrant wide range multiplying capability
- Wide power supply range: ±4.5V to ±18V
- Low power consumption: 33 mW at ±5V
- Low cost

6

Typical Applications

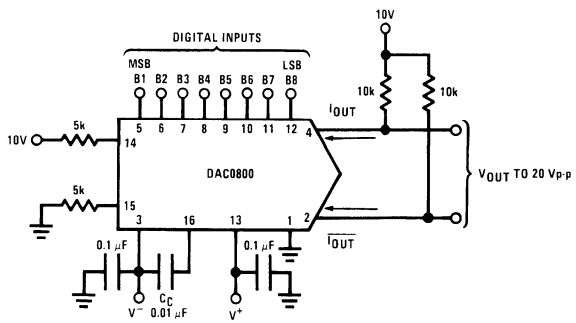


FIGURE 1. ±20 V_{P-P} Output Digital-to-Analog Converter (Note 5)

Ordering Information

Non-Linearity	Temperature Range	Order Numbers				
		J Package (J16A) (Note 1)		**N Package (N16E)** (Note 1)		**SO Package (M16A)**
±0.1% FS	0°C ≤ T_A ≤ +70°C	DAC0802LCJ	DAC-08HQ	DAC0802LCN	DAC-08HP	DAC0802LCM
±0.19% FS	−55°C ≤ T_A ≤ +125°C	DAC0800LJ	DAC-08Q			
±0.19% FS	0°C ≤ T_A ≤ +70°C	DAC0800LCJ	DAC-08EQ	DAC0800LCN	DAC-08EP	DAC0800LCM

Note 1: Devices may be ordered by using either order number.

National Semiconductor

DAC0808
8-Bit D/A Converter

General Description

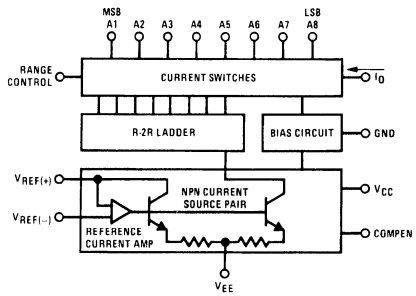
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Block and Connection Diagrams



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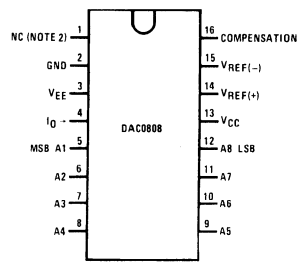
Dual-In-Line Package



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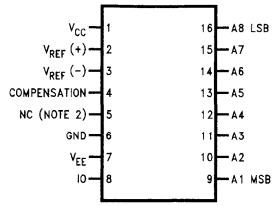
Top View
Order Number DAC0808
See NS Package M16A or N16A

Block and Connection Diagrams (Continued)

Small-Outline Package



DS005687-13

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	N PACKAGE (N16A) (Note 1)		SO PACKAGE (M16A)
8-bit	0°C≤T_A≤+75°C	DAC0808LCN	MC1408P8	DAC0808LCM

Note 1: Devices may be ordered by using either order number.

6

National Semiconductor

DAC0830/DAC0832
8-Bit µP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™).

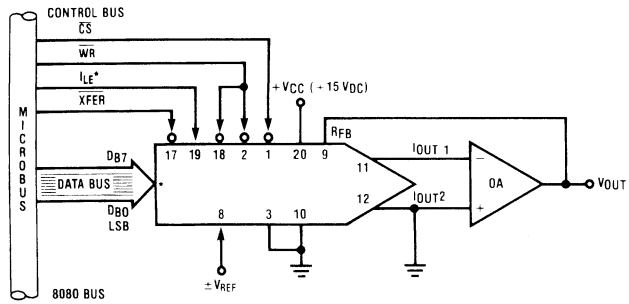
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only—NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without µP) if desired
- Available in 20-pin small-outline or molded chip carrier package

Key Specifications

- Current settling time: 1 µs
- Resolution: 8 bits
- Linearity: 8, 9, or 10 bits (guaranteed over temp.)
- Gain Tempco: 0.0002% FS/°C
- Low power dissipation: 20 mW
- Single power supply: 5 to 15 V_{DC}

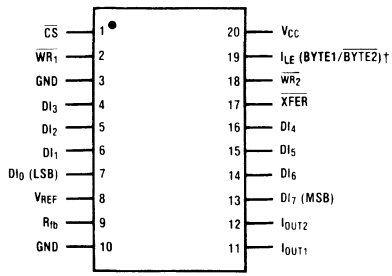
Typical Application



DS005608-1

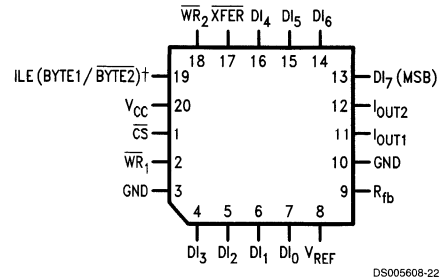
Connection Diagrams (Top Views)

Dual-In-Line and Small-Outline Packages



DS005608-21

Molded Chip Carrier Package



DS005608-22

National Semiconductor

LM12454/LM12458/LM12H458
12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12454, LM12458, and LM12H458 are highly integrated Data Acquisition Systems. Operating on just 5V, they combine a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12(H)458's eight-input multiplexer. The LM12454 has a four-channel multiplexer, a differential multiplexer output, and a differential S/H input. The LM12454 and LM12(H)458 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits.

Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers. The reference voltage input can be externally generated for absolute or ratiometric operation or can be derived using the internal 2.5V bandgap reference.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit databus. The LM12454 and LM12(H)458 include a direct memory access (DMA) interface for high-speed conversion data transfer.

An evaluation/interface board is available. Order number LM12458EVAL.

Additional applications information can be found in applications notes AN-906, AN-947 and AN-949.

Key Specifications

(f_{CLK} = 5 MHz; 8 MHz, H)

■ Resolution	12-bit + sign or 8-bit + sign
■ 13-bit conversion time	8.8 µs, 5.5 µs (H) (max)
■ 9-bit conversion time	4.2 µs, 2.6 µs (H) (max)
■ 13-bit Through-put rate	88k samples/s (min), 140k samples/s (H) (min)
■ Comparison time ("watchdog" mode)	2.2 µs (max), 1.4 µs (H) (max)
■ ILE	±1 LSB (max)
■ V_{IN} range	GND to V_A^+
■ Power dissipation	30 mW, 34 mW (H) (max)
■ Stand-by mode	50 µW (typ)
■ Single supply	3V to 5.5V

Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog"
- Single-ended or differential inputs
- Built-in Sample-and-Hold and 2.5V bandgap reference
- Instruction RAM and event sequencer
- 8-channel (LM12(H)458), 4-channel (LM12454) multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide databus dmicroprocessor or DSP interface

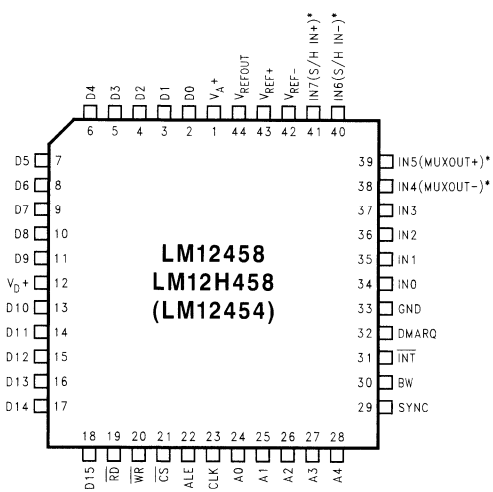
Applications

- Data Logging
- Instrumentation
- Process Control
- Energy Management
- Inertial Guidance

Ordering Information

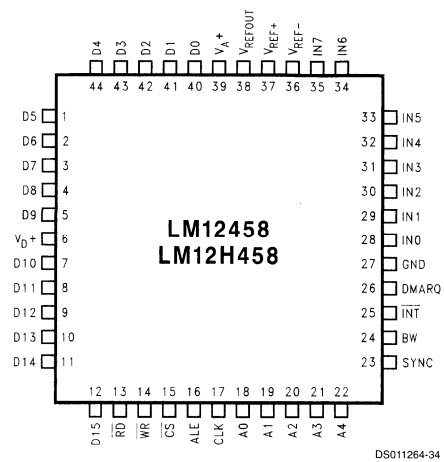
Guaranteed Clock Freq (min)	Guaranteed Linearity Error (max)	Order Part Number	See NS Package Number
8 MHz	±1.0 LSB	LM12H458CIV LM12H458CIVF LM12H458MEL/883 or 5962-9319502MYA	V44A VGZ44A EL44A
5 MHz	±1.0 LSB	LM12454CIV LM12458CIV LM12458CIVF	V44A V44A VGZ44A

Connection Diagrams



* Pin names in ( ) apply to the LM12454 and LM12H454.

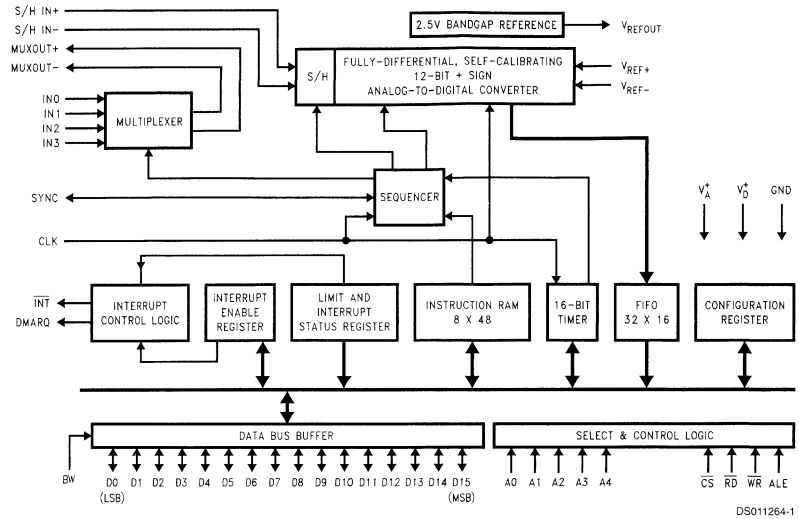
Order Number LM12454CIV,
LM12458CIV or LM12H458CIV
See NS Package Number V44A
Order Number LM12H458MEL/883 or 5962-9319502MYA
See NS Package Number EL44A



Order Number LM12458CIVF or LM12H458CIVF
See NS Package Number VGZ44A

Functional Diagrams

LM12454



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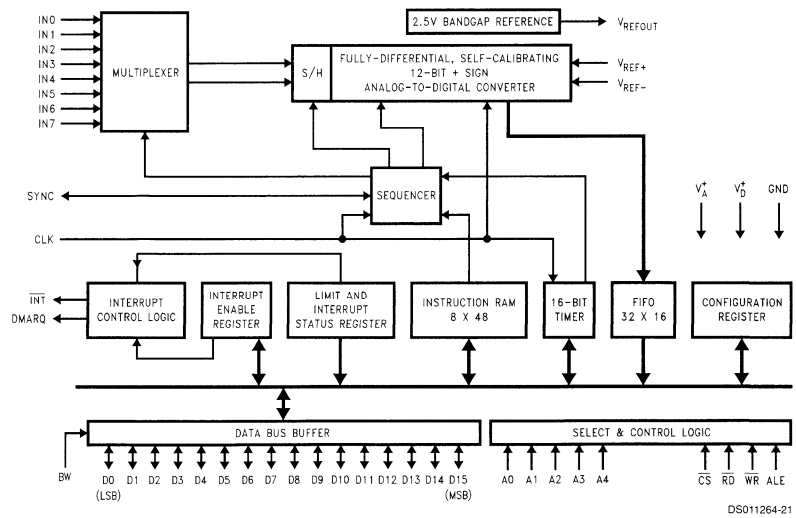
LM12(H)458



DS011264-21

National Semiconductor

LM12L458
12-Bit + Sign Data Acquisition System with Self-Calibration

General Description

The LM12L458 is a highly integrated 3.3V Data Acquisition System. It combines a fully-differential self-calibrating (correcting linearity and zero errors) 13-bit (12-bit + sign) analog-to-digital converter (ADC) and sample-and-hold (S/H) with extensive analog functions and digital functionality. Up to 32 consecutive conversions, using two's complement format, can be stored in an internal 32-word (16-bit wide) FIFO data buffer. An internal 8-word RAM can store the conversion sequence for up to eight acquisitions through the LM12L458's eight-input multiplexer. The LM12L458 can also operate with 8-bit + sign resolution and in a supervisory "watchdog" mode that compares an input signal against two programmable limits. Programmable acquisition times and conversion rates are possible through the use of internal clock-driven timers.

All registers, RAM, and FIFO are directly addressable through the high speed microprocessor interface to either an 8-bit or 16-bit databus. The LM12L458 includes a direct memory access (DMA) interface for high-speed conversion data transfer.

Applications

- Data Logging
- Process Control
- Energy Management
- Medical Instrumentation

Key Specifications

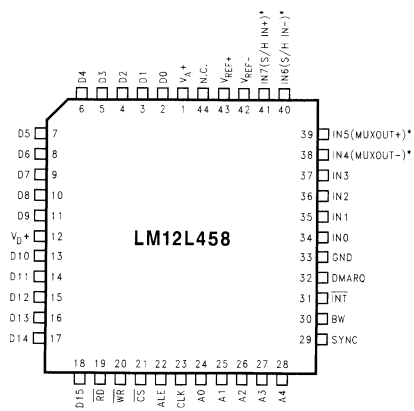
(f_{CLK} = 6 MHz)

■ Resolution	12-bit + sign or 8-bit + sign
■ 13-bit conversion time	7.3 µs
■ 9-bit conversion time	3.5 µs
■ 13-bit Through-put rate	106k samples/s (min)
■ Comparison time ("watchdog" mode)	1.8 µs (max)
■ ILE	±1 LSB (max)
■ V_{IN} range	GND to V_A^+
■ Power dissipation	15 mW (max)
■ Stand-by mode	5 µW (typ)
■ Single supply	3V to 5.5V

Features

- Three operating modes: 12-bit + sign, 8-bit + sign, and "watchdog"
- Single-ended or differential inputs
- Built-in Sample-and-Hold
- Instruction RAM and event sequencer
- 8-channel multiplexer
- 32-word conversion FIFO
- Programmable acquisition times and conversion rates
- Self-calibration and diagnostic mode
- 8- or 16-bit wide databus microprocessor or DSP interface
- CMOS compatible I/O

Connection Diagram



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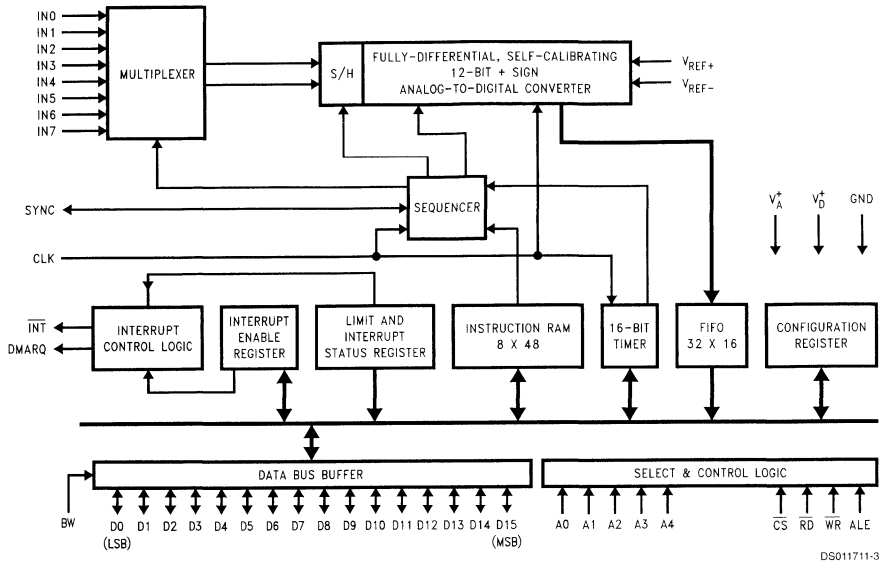
*Pin names in ( ) apply to the LM12L454.

Order Number LM12L458CIV
See NS Package Number V44A

Functional Diagram

LM12L458



DS011711-3

Ordering Information

Guaranteed Clock Freq (min)	Guaranteed Linearity Error (max)	Order Part Number	See NS Package Number
6 MHz	±1.0 LSB	LM12L458CIV	V44A

Section 7
Enhanced Solutions

Section 7 Contents

National Semiconductor

Enhanced Solutions Division

Enhanced Solutions is a well established division of National Semiconductor which has developed a core competency in taking National's standard products and 'enhancing' them for use in other applications such as Hi-Rel, industrial and now automotive.

The division, formerly known as the Military and Aerospace, has developed rapidly in the last few years and now incorporates 4 business areas including both mature and new dynamic businesses.

Military/Aerospace

A leader in the supply of a broad portfolio of products to the military, avionics and space markets. As a fully certified supplier we offer products to the industry standards such as QML-Q and QML-V as well as providing radiation tested and guaranteed products.

System Test Access

The demand for testability in new complex 'High Availability' electronic systems has increased in recent years. Based upon IEEE 1149.1 Boundary SCAN technology, the new digital and mixed-signal test access products from the System Test Access (STA) group enable remote embedded test and re-configuration of CPLDs.

Automotive

National has been a long-term supplier of products to the automotive market. With custom designs used in systems such as ABS and Airbags, the new focus is on providing standard building blocks tailored to the environment and needs found in new electronic intensive automobiles.

Die Products (see Appendices Section 20)

The 'information age' is creating a demand for new portable equipment with ever-increasing requirements for getting 'more out of less'. This has resulted in a huge growth in the demand for die. The Die Product Business Unit is a central, dedicated group with responsibility for all die and wafer sales.

http://www.national.com/appinfo/milaero/

National Semiconductor

Military-Aerospace Product Services

National Semiconductor is one of the largest suppliers of IC products for high reliability applications. We've provided analog and mixed-signal engineering for the military, aerospace and space markets for more than 30 years and our future commitment is equally firm.

Our expertise in system design and integration is creating innovative solutions for space, radar, communications, and other applications. For fast, effective product design, development, and delivery, National provides knowledge in systems integration and design, as well as organizational and partnership strategies—whether the product you need comes off-the-shelf or is customized for your environment and application.

National continually evaluates and develops new products for high reliability applications including expanding our space and RHA portfolio, introducing low-voltage analog, interface, and logic components and qualifying PLLs for the wireless market.

Processing Capabilities

Process Flow	Description
SPACE-LEVEL SYSTEMS	
QMLV	QML (DSCC Qualified Manufacturers List) product processed to MIL-PRF-38535 for space-level applications.
QMLV"R"	QML (DSCC Qualified Manufacturers List) product processed to MIL-PRF-38535 with guaranteed RHA radiation assurance testing.
JAN Class S	QPL (DSCC Qualified Products List) products processed to MIL-PRF-38535 Appendix B for space-level applications.
JAN Class S "R"	QPL (DSCC Qualified Products List) products processed to MIL-PRF-38535 Appendix B Level S with guaranteed RHA radiation assurance.
NAVAL/AIR/GROUND SYSTEMS	
QMLQ	QML (DSCC Qualified Manufacturers List) product processed to MIL-PRF-38535 for ground applications.
JAN Class B	QPL (DSCC Qualified Product List) products processed to MIL-PRF-38535 Appendix A Level B.
JAN Class B "R" **QMLQ"R"**	QPL (DSCC Qualified Product List) products processed to MIL-PRF-38535 Appendix A Level B, using space qualified die. Guaranteed RHA radiation assurance testing.
SMD	Standard Microcircuit Drawing tactical-level products processed to QML Level Q with electrical specifications controlled by DSCC. (National's SMD products that include an M or Q in the SMD part number are controlled by and fully compliant with MIL-PRF-38535 QML Q.)
/883	Products processed to MIL-STD-883 Level B for military with electrical specifications controlled by manufacturer.
COMMERCIAL GRADE SYSTEMS	
DC, HC	Hermetic commercially processed product.
OTHER SERVICES	
Radiation Testing	National Semiconductor has a large radiation-tested product offering, High Reliability devices, which are not currently offered as radiation-tolerant product, may be procured with Total Dose Testing performed as an add-on option. Reports of radiation test, performed by National, are available on many device types upon request.

National Semiconductor

Radiation Test Results

Analog Rad Tolerant Product Portfolio (Section 21-4 Inputs)

NSID	SMD	Source of Electricals	RAD Level	PKG	Radiation Limits	
					PRE	POST
CLC402AJFQML	5962F9203301MPA	5962-92033	300k	DIP	SAME>>>	SAME
CLC420AJFQML	5962F9175801PA	5962-91758	300k	DIP		
CLC420AWGFQML	5962F9175801XA	5962-91758	300k	SOIC		
DS16F95JFQML	5962F8961501QPA	5962-89615	300k	DIP	SAME>>>	SAME
DS16F95JFQMLV	5962F8961501VPA	5962-89615	300k	DIP		
DS16F95WFQML	5962F8961501QHA	5962-89615	300k	FLAT		
DS16F95WFQMLV	5962F8961501VHA	5962-89615	300k	FLAT		
DS16F95WGFQML	5962F8961501QXA	5962-89615	300k	SOIC		
DS16F95WGFQMLV	5962F8961501VXA	5962-89615	300k	SOIC		
DS26F31MJFQMLV	5962F7802302VEA	5962-78023	300k	DIP	SAME>>>	SAME
DS26F31MWFQMLV	5962F7802302VFA	5962-78023	300k	FLAT		
DS26F31MWGFQMLV	5962F7802302VZA	5962-78023	300k	SOIC		
DS26F32MERQML	5962R7802005Q2A	5962-78020	100k	LCC	SAME>>>	SAME
DS26F32MJRQML	5962R7802005QEA	5962-78020	100k	DIP		
DS26F32MJRQMLV	5962R7802005VEA	5962-78020	100k	DIP		
DS26F32MWGRQMLV	5962R7802005VZA	5962-78020	100k	SOIC		
DS26F32MWRQML	5962R7802005QFA	5962-78020	100k	FLAT		
DS26F32MWRQMLV	5962R7802005VFA	5962-78020	100k	FLAT		
DS26LS31MEFQML	5962F7802301Q2A	5962-78023	300k	LCC	SAME>>>	SAME
DS26LS31MJFQML	5962F7802301MEA	5962-78023	300k	DIP		
DS26LS31MJFQMLV	5962F7802301VEA	5962-78023	300k	DIP		
DS26LS31MWFQML	5962F7802301MFA	5962-78023	300k	FLAT		
DS26LS31MWFQMLV	5962F7802301VFA	5962-78023	300k	FLAT		
DS90C031WRQMLV	5962R9583301VFA	5962-95833	100k	FLAT	I_{CC} 25 mA	30 mA
DS90C032WLQMLV	5962L9583401VFA	5962-95834	50k	FLAT	I_{CC} 11 mA	20 mA
LM101AHRQMLV	5962R9951501VGA	38510/10103	100k	CAN	SAME>>>	SAME
LM108AHRQML	5962R9863702QGA	38510/10104	100k	CAN	+IIB 2 nA	5 nA
LM108AHRQMLV	5962R9863702VGA	38510/10104	100k	CAN	−IIB 2 nA	5 nA
LM108AJ-8RQML	5962R9863702QPA	38510/10104	100k	DIP	IIO 0.2 nA	0.5 nA
LM108AJ-8RQMLV	5962R9863702VPA	38510/10104	100k	DIP		
LM108AJRQML	5962R9863702QCA	38510/10104	100k	DIP		
LM108AWGRQML	5962R9863702QZA	38510/10104	100k	SOIC		
LM108AWGRQMLV	5962R9863702VZA	38510/10104	100k	SOIC		
LM111J-8PQMLV	5962P0052401VPA	38510/10304	30k	DIP		
LM111WGPQMLV	5962P0052401VZA	38510/10304	30k	SOIC		
LM117HRQMLV	5962R9951703VXA	38510/11703	100k	CAN	V_{OUT} 1.2V–1.3V	1.2V–1.325V
LM117KRQMLV	5962R9951704VYA	38510/11704	100k	CAN K	V_{OUT} 1.2V–1.3V	1.2V–1.325V
LM118HPQMLV	5962P9853901VGA	38510/10107	30k	CAN	SAME>>>	SAME
LM118J-8PQMLV	5962P9853901VPA	38510/10107	30k	DIP		
LM118WGPQMLV	5962P9853901VZA	38510/10107	30k	SOIC		
LM136AH-2.5RQML	5962R0050101QXA	5962-00501	100k	CAN	SAME>>>	SAME
LM136AH-2.5RQV	5962R0050101VXA	5962-00501	100k	CAN		

Analog Rad Tolerant Product Portfolio (Section 21-4 Inputs) (Continued)

NSID	SMD	Source of Electricals	RAD Level	PKG	Radiation Limits	
					PRE	POST
LM137KPQMLV	5962P9951702VYA	38510/11804	30k	CAN K	ΔI_{ADJ} +5 µA	+10 µA
LM158AHLQMLV	5962L8771002VGA	5962-87710	50k	CAN	VIO ±2 mV	±4 mV
LM158AJLQMLV	5962L8771002VPA	5962-87710	50k	DIP	+IIB 50 nA	60 nA
LM158AWGLQMLV	5962L8771002VXA	5962-87710	50k	SOIC	−IIB 50 nA	60 nA
LM6172AMJFQML	5962F9560401QPA	5962-95604	300k	DIP	SAME>>>	SAME
LM6172AMJFQMLV	5962F9560401VPA	5962-95604	300k	DIP		
LM6172AMWGFQML	5962F9560401QXA	5962-95604	300k	SOIC		
LM6172AMWGFQMLV	5962F9560401VXA	5962-95604	300k	SOIC		
LM7171AMJFQML	5962F9553601QPA	5962-95536	300k	DIP	SAME>>>	SAME
LM7171AMJFQMLV	5962F9553601VPA	5962-95536	300k	DIP		
LM7171AMWGFQML	5962F9553601QXA	5962-95536	300k	SOIC		
LM7171AMWGFQMLV	5962F9553601VXA	5962-95536	300k	SOIC		
DEVICES BEING PURSUED						
DS90LV031AW-QML	5962-9865101QFA	5962-98651	300k	FLAT		
DS90LV031AWGMLS	N/A		300k	SOIC		
DS90LV031AWGQML	5962-9865101QX	5962-98651	300k	SOIC		
DS90LV032AW-QML	5962-9865201QFA	5962-98652	100k	FLAT		
DS90LV032AWGMLS	N/A		100k	SOIC		
DS90LV032AWGQML	5962-9865201QXA	5962-98652	100k	SOIC		
TEMPORARILY WITHDRAWN						
LM117HRQML	5962R9951703QXA	38510/11703	100k	CAN	V_{OUT} 1.2V−1.3V	1.2V−1.325V
LM117HRQMLV	5962R9951703VXA	38510/11703	100k	CAN	VRLINE ±9 mV	±25 mV
LM101AWRQMLV	5962R9951501VHA	38510/11703	100k	FLAT		
LM101AJRQMLV	5962R9951501VPA	38510/11703	100k	DIP		
LM111HPQMLV	5962P0052401VGA	38510/10304	30k	CAN	SAME>>>	SAME
LM119JRQML	5962R9679801QCA	5962-96798	100k	DIP	IIB 0.475 µA	1000 nA
LM119WRQML	5962R9679801QHA	5962-96798	100k	FLAT	V_{OS} +3.8 mV	+4.0 mV
LM119HRQML	5962R9679801QIA	5962-96798	100k	CAN	I_{OS} +75 nA	+150 nA
LM119WGRQML	5962R9679801QXA	5962-96798	100k	SOIC		
LM119JRQMLV	5962R9679801VCA	5962-96798	100k	DIP		
LM119WRQMLV	5962R9679801VHA	5962-96798	100k	FLAT		
LM119HRQMLV	5962R9679801VIA	5962-96798	100k	CAN		
LM119WGRQMLV	5962R9679801VXA	5962-96798	100k	SOIC		
LM124AJRQML	5962R9950401QCA	38510/11006	100k	DIP	VIO ±2 mV	±2.2 mV
LM124AJRQMLV	5962R9950401VCA	38510/11006	100k	DIP	IIO ±10 nA	±15 nA
LM124AWGRQML	5962R9950401QZA	38510/11006	100k	SOIC	+IIB 50 nA	75 nA
LM124AWGRQMLV	5962R9950401VZA	38510/11006	100k	SOIC	−IIB 50 nA	75 nA
LM124AWRQML	5962R9950401QDA	38510/11006	100k	FLAT	AVS 50V/mV	40V/mV
LM124AWRQMLV	5962R9950401VDA	38510/11006	100k	FLAT		
LM137HPQML	5962P9951701QXA	38510/11803	30k	CAN	ΔI_{ADJ} + 5 µA	+10 µA
LM137HPQMLV	5962P9951701VXA	38510/11803	30k	CAN		
LM139AJRQML	5962R9673801QCA	5962-96738	100k	DIP	VIO ±2 mV	±2.5 mV
LM139AJRQMLV	5962R9673801VCA	5962-96738	100k	DIP	+IIB 100 nA	110 nA
LM139AWGRQML	5962R9673801QXA	5962-96738	100k	SOIC	−IIB 100 nA	110 nA
LM139AWGRQMLV	5962R9673801VXA	5962-96738	100k	SOIC	trLH 0.8 ns	0.9 ns
LM139AWRQML	5962R9673801QDA	5962-96738	100k	FLAT		
LM139AWRQMLV	5962R9673801VDA	5962-96738	100k	FLAT		

Note 1: Linear products have been irradiated to High Dose rates as required by MIL-STD-883, Method 1019. "Worst-case" conditions for Linear products are derived through Low Dose Rate testing.

Note 2: Using pre-radiation limits provides small additional margin for Linear products that are used in space environments tested at high dose rate.

Note 3: Parts qualified to a specific RHA Level R are guaranteed to meet their post rad specifications after the guaranteed krads(Si) total dose. Rad levels for all other products are typical and are not guaranteed.

Note 4: Radiation Hardness Assurance (RHA) Categories (Designates guaranteed limits up to):

P = 30 krad(Si)

R = 100 krad(Si)

F = 300 krad(Si)

National Semiconductor

SMD/JAN Drawing Cross-Reference

NSID	PBID	Part Description
AR629AU9/883	5962-9958101QXC	ARINC 629 Terminal Controller
CLC110AJ-QML	5962-8997501PA	Wideband Closed Loop Buffer Amp
CLC114AE-QML	5962-9233901M2A	Quad Low Power Video Buffer
CLC114AJ-QML	5962-9233901MCA	Quad Low Power Video Buffer
CLC400AE-QML	5962-89970012A	Fast Set Wideband Low Gain Amp
CLC400AJ-QML	5962-8997001PA	Fast Set Wideband Low Gain Amp
CLC401AJ-QML	5962-8997301PA	Fast Set Wideband High Gain Amp
CLC402AJFQML	5962F9203301MPA	Low Gain Amp w/Fast 14-Bit Set
CLC402AJ-QML	5962-9203301MPA	Low Gain Amp w/Fast 14-Bit Set
CLC404AJ-QML	5962-9099401MPA	Wideband High Slew Rate Op Amp
CLC406AJ-QML	5962-9200401MPA	Wideband Low Power Op Amp
CLC409AE-QML	5962-9203401M2A	Very Wideband Low Distortion Op Amp
CLC409AJ-QML	5962-9203401MPA	Wideband Low Power Op Amp
CLC410AJ-QML	5962-9060001PA	Fast Settle Vid Amp w/Disable
CLC411AJ-QML	5962-9456601MPA	Hi Speed Video Op Amp w/Disable
CLC412AE-QML	5962-9471901M2A	Dual Wideband Video Op Amp
CLC412AJ-QML	5962-9471901MPA	Dual Wideband Video Op Amp
CLC414AE-QML	5962-9169301M2A	Quad Low Power Op Amp
CLC414AJ-QML	5962-9169301MCA	Quad Low Power Op Amp
CLC415AJ-QML	5962-9305501MCA	Quad Wideband Op Amp
CLC420AE-QML	5962-9175801M2A	High Speed Voltage Feedbk Op Amp
CLC420AJFQML	5962F9175801MPA	Rad Tested B Lvl CLC420AJ
CLC420AJ-QML	5962-9175801MPA	Hi Speed Voltage Feedbk Op Amp
CLC420AWGFQML	5962F9175801MXA	Rad Tested B Lvl CLC420AJ
CLC420BJ-QML	5962-9175802MPA	High Speed Voltage Feedbk Op Amp
CLC425AJ-QML	5962-9325901MPA	Ultra Low Noise Wideband Op Amp
CLC428AJ-QML	5962-9470801MPA	Dual Wideband Low Noise Voltage Feedbk Amp
CLC430AE-QML	5962-9203001M2A	General Purpose 100 MHz Op Amp
CLC430AJ-QML	5962-9203001MPA	General Purpose 100 MHz Op Amp
CLC430AWG-QML	5962-9203001MXA	General Purpose 100 MHz Op Amp
CLC431AE-QML	5962-9472501M2A	Dual Wideband Op Amp
CLC431AJ-QML	5962-9472501MCA	Dual Wideband Op Amp
CLC432AJ-QML	5962-9472502MPA	Dual Wideband Op Amp
CLC440AJ-QML	5962-9751801MPA	High Bandwidth, Low Power Amp
CLC449AJ-QML	5962-9752001MPA	1.2 GHz Ultra Wideband Op Amp
CLC452AJ-QML	5962-9752101MPA	Low Power Line Driver
CLC501AJ-QML	5962-8997401PA	High Speed Output Clamping Op Amp
CLC502AE-QML	5962-9174301M2A	Clamp Low Gain Amp w/14-Bit Set
CLC502AJ-QML	5962-9174301MPA	Clamp Low Gain Amp w/14-Bit Set
CLC505AJ-QML	5962-9099301MPA	High Speed Prgm Supply Crnt Op Amp
CLC520AJ-QML	5962-9169401MCA	Amp w/Volt Cntrl Gain, AGC + Amp
CLC522AE-QML	5962-9451701M2A	Wideband Variable Gain Op Amp
CLC522AJ-QML	5962-9451701MCA	Wideband Variable Gain Op Amp
CLC532AE-QML	5962-9203501M2A	High Speed 2:1 Analog Multiplexer
CLC532AJ-QML	5962-9203501MCA	High Speed 2:1 Analog Multiplexer

NSID	PBID	Part Description
DS1691AJ-SMD	5962-8672101EA	EIA/TIA-485/422 Diff Bus Trans
DS16F95E/883	5962-89615012A	EIA/TIA-485/422 Diff Bus Trans
DS16F95J/883	5962-8961501PA	EIA/TIA-485/422 Diff Bus Trans
DS16F95JFQML	5962F8961501QPA	EIA/TIA-485/422 Diff Bus Trans
DS16F95JFQMLV	5962F8961501VPA	EIA/TIA-485/422 Diff Bus Trans
DS16F95J-QMLV	5962-8961501VPA	EIA/TIA-485/422 Diff Bus Trans
DS16F95WFQML	5962F8961501QHA	EIA/TIA-485/422 Diff Bus Trans
DS16F95WFQMLV	5962F8961501VHA	EIA/TIA-485/422 Diff Bus Trans
DS16F95WG/883	5962-8961501QXA	EIA/TIA-485/422 Diff Bus Trans
DS16F95WGFQML	5962F8961501QXA	EIA/TIA-485/422 Diff Bus Trans
DS16F95WGFQMLV	5962F8961501VXA	EIA/TIA-485/422 Diff Bus Trans
DS16F95WG-QMLV	59628961501VXA	EIA/TIA-485/422 Diff Bus Trans
DS16F95W-QMLV	59628961501VHA	EIA/TIA-485/422 Diff Bus Trans
DS16F95W-SMD	5962-8961501HA	EIA/TIA-485/422 Diff Bus Trans
DS1776E/883	5962-9231701M3A	Pi Bus Transceiver
DS26C31ME/883	5962-9163901M2A	EIA/TIA-422/423 Quad Diff Driver
DS26C31MJ/883	5962-9163901MEA	EIA/TIA-422/423 Quad Diff Driver
DS26C31MW/883	5962-9163901MFA	EIA/TIA-422/423 Quad Diff Driver
DS26C31MWG/883	5962-9163901MXA	EIA/TIA-422/423 Quad Diff Driver
DS26C32AME/883	5962-9164001M2A	Quad Differential Line Driver
DS26C32AMJ/883	5962-9164001MEA	Quad Differential Line Driver
DS26C32AMW/883	5962-9164001MFA	Quad Differential Line Driver
DS26C32AMWG/883	5962-9164001MXA	Quad Differential Line Driver
DS26F31ME/883	5962-7802302M2A	EIA/TIA-422/423 Quad Diff Driver
DS26F31MJ/883	5962-7802302MEA	EIA/TIA-422/423 Quad Diff Driver
DS26F31MJ-QMLV	5962-7802302VEA	EIA/TIA-422/423 Quad Diff Driver
DS26F31MW/883	5962-7802302MFA	EIA/TIA-422/423 Quad Diff Driver
DS26F31MW-QMLV	5962-7802302VFA	EIA/TIA-422/423 Quad Diff Driver
DS26F32ME/883	5962-7802005M2A	Quad Differential Line Driver
DS26F32MJ/883	5962-7802005MEA	Quad Differential Line Driver
DS26F32MJ-QMLV	5962-7802005VEA	Quad Differential Line Driver
DS26F32MW/883	5962-7802005MFA	Quad Differential Line Driver
DS26F32MW-QMLV	5962-7802005VFA	Quad Differential Line Driver
DS26LS31ME-SMD	5962-7802301Q2A	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MJFQML	5962F7802301MEA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MJFQMLV	5962F7802301VEA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MJ-QMLV	5962-7802301VEA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MJ-SMD	5962-7802301MEA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MWFQML	5962F7802301MFA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MWFQMLV	5962F7802301VFA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MW-QMLV	5962-7802301VFA	EIA/TIA-422/423 Quad Diff Driver
DS26LS31MW-SMD	5962-7802301MFA	EIA/TIA-422/423 Quad Diff Driver
DS26LS32ME/883	5962-7802006Q2A	Quad Differential Line Driver
DS26LS32MJ/883	5962-7802006QEA	EIA/TIA-422/423 Quad Diff Receiver
DS26LS32MW/883	5962-7802006QFA	EIA/TIA-422/423 Quad Diff Receiver
DS26LV31W-QML	5962-9858401QFA	EIA/TIA-422/423 Quad Diff Driver - Low Voltage
DS26LV32AW-QML	5962-9858501QFA	EIA/TIA-422/423 Quad Diff Receiver - Low Voltage
DS7831J-SMD	8004101EA	Dual Differential Line Driver
DS78C120J/883	5962-8963001EA	EIA/TIA-422/423 Dual Line Receiver
DS78C20J/883	5962-9321101MCA	EIA/TIA-422/423 Dual Line Receiver

NSID	PBID	Part Description
DS90C031E-QML	5962-9583301Q2A	LVDS Quad CMOS Diff Driver
DS90C031W-QML	5962-9583301QFA	LVDS Quad CMOS Diff Driver
DS90C031W-QMLV	5962-9583301VFA	LVDS Quad CMOS Diff Driver
DS90C032E-QML	5962-9583401Q2A	LVDS Quad CMOS Diff - Receiver
DS90C032W-QML	5962-9583401QFA	LVDS Quad CMOS Diff - Receiver
DS90LV031AW-QML	5962-9865101QFA	LVDS Quad 3V CMOS Diff Driver
DS90LV032AW-QML	5962-9865201QFA	LVDS Quad 3V CMOS Diff - Receiver
DS9622ME/883	5962-87522012A	Dual Line Receiver
DS9622MJ/883	5962-8752201CA	Dual Line Receiver
DS9627MJ/883	5962-8978701MEA	Dual Line Receiver
DS9636AJ/883	5962-8752301PA	EIA/TIA-422 Dual Line Driver
DS9637AMJ/883	5962-8752401PA	EIA/TIA-422 Dual Diff Line Receiver
DS9638J/883	5962-8754601PA	EIA/TIA-422 Dual Diff Line Driver
DS96F172ME/883	5962-9076501M2A	Quad Line Driver
DS96F172MJ/883	5962-9076501MEA	Quad Line Driver
DS96F173ME/883	5962-9076602M2A	Quad Line Receiver
DS96F173MJ/883	5962-9076602MEA	Quad Line Receiver
DS96F173MW/883	5962-9076602MFA	Quad Line Receiver
DS96F174ME/883	5962-9076502M2A	Quad Line Driver
DS96F174MJ/883	5962-9076502MEA	Quad Line Driver
DS96F174MJ-QMLV	5962-9076502VEA	Quad Line Driver
DS96F174MW/883	5962-9076502MFA	Quad Line Driver
DS96F175ME/883	5962-9076601M2A	Quad Line Receiver
DS96F175MJ/883	5962-9076601MEA	Quad Line Receiver
DS96F175MJ-QMLV	5962-9076601VEA	Quad Line Receiver
DS96F175MW/883	5962-9076601MFA	Quad Line Receiver
HPC003U20/883	5962-9054401MYC	High Performance Ucontroller
JL101ABCA	JM38510/10103BCA	General Purpose Op Amp
JL101ABGA	JM38510/10103BGA	General Purpose Op Amp
JL101ABHA	JM38510/10103BHA	General Purpose Op Amp
JL101ABPA	JM38510/10103BPA	General Purpose Op Amp
JL101ASGA	JM38510/10103SGA	General Purpose Op Amp
JL101ASPA	JM38510/10103SPA	General Purpose Op Amp
JL108ABCA	JM38510/10104BCA	Super Gain Op Amp
JL108ABGA	JM38510/10104BGA	Super Gain Op Amp
JL108ABHA	JM38510/10104BHA	Super Gain Op Amp
JL108ABPA	JM38510/10104BPA	Super Gain Op Amp
JL108ABZA	JM38510/10104BZA	Super Gain Op Amp
JL108ASCA	JM38510/10104SCA	Super Gain Op Amp
JL108ASGA	JM38510/10104SGA	Super Gain Op Amp
JL108ASHA	JM38510/10104SHA	Super Gain Op Amp
JL108ASPA	JM38510/10104SPA	Super Gain Op Amp
JL109BXA	JM38510/10701BXA	Voltage Regulator
JL109BYA	JM38510/10701BYA	Voltage Regulator
JL111BCA	JM38510/10304BCA	Voltage Comparator
JL111BGA	JM38510/10304BGA	Voltage Comparator
JL111BHA	JM38510/10304BHA	Voltage Comparator
JL111BPA	JM38510/10304BPA	Voltage Comparator
JL111SGA	JM38510/10304SGA	Voltage Comparator
JL111SHA	JM38510/10304SHA	Voltage Comparator

NSID	PBID	Part Description
JL111SPA	JM38510/10304SPA	Voltage Comparator
JL117BXA	JM38510/11703BXA	Adjustable Regulator
JL117BYA	JM38510/11704BYA	Adjustable Regulator
JL117SXA	JM38510/11703SXA	Adjustable Regulator
JL117SYA	JM38510/11704SYA	Adjustable Regulator
JL118BCA	JM38510/10107BCA	Fast Op Amp
JL118BGA	JM38510/10107BGA	Fast Op Amp
JL118BHA	JM38510/10107BHA	Fast Op Amp
JL118BPA	JM38510/10107BPA	Fast Op Amp
JL118SGA	JM38510/10107SGA	Fast Op Amp
JL118SHA	JM38510/10107SHA	Fast Op Amp
JL118SPA	JM38510/10107SPA	Fast Op Amp
JL119BCA	JM38510/10306BCA	High Speed Dual Comparator
JL119BIA	JM38510/10306BIA	High Speed Dual Comparator
JL120-12BXA	JM38510/11502BXA	Voltage Regulator
JL120-12BYA	JM38510/11506BYA	Voltage Regulator
JL120-15BXA	JM38510/11503BXA	Voltage Regulator
JL120-15BYA	JM38510/11507BYA	Voltage Regulator
JL120-15SXA	JM38510/11503SXA	Voltage Regulator
JL120-5BXA	JM38510/11501BXA	Voltage Regulator
JL120-5BYA	JM38510/11505BYA	Voltage Regulator
JL124ABCA	JM38510/11006BCA	Low Power Quad Op Amplifier
JL124ABDA	JM38510/11006BDA	Low Power Quad Op Amplifier
JL124ASCA	JM38510/11006SCA	Low Power Quad Op Amplifier
JL124ASDA	JM38510/11006SDA	Low Power Quad Op Amplifier
JL124BCA	JM38510/11005BCA	Low Power Quad Op Amplifier
JL124BDA	JM38510/11005BDA	Low Power Quad Op Amplifier
JL124SCA	JM38510/11005SCA	Low Power Quad Op Amplifier
JL124SDA	JM38510/11005SDA	Low Power Quad Op Amplifier
JL137BXA	JM38510/11803BXA	Adjustable Regulator
JL137BYA	JM38510/11804BYA	Adjustable Regulator
JL137SXA	JM38510/11803SXA	Adjustable Regulator
JL137SYA	JM38510/11804SYA	Adjustable Regulator
JL139BCA	JM38510/11201BCA	Quad Comparator
JL139BDA	JM38510/11201BDA	Quad Comparator
JL139SCA	JM38510/11201SCA	Quad Comparator
JL139SDA	JM38510/11201SDA	Quad Comparator
JL140-12BXA	JM38510/10703BXA	Voltage Regulator
JL140-12BYA	JM38510/10707BYA	Voltage Regulator
JL140-12SXA	JM38510/10703SXA	Voltage Regulator
JL140-12SYA	JM38510/10707SYA	Voltage Regulator
JL140-15BXA	JM38510/10704BXA	Voltage Regulator
JL140-15BYA	JM38510/10708BYA	Voltage Regulator
JL140-24BYA	JM38510/10709BYA	Voltage Regulator
JL140-5BXA	JM38510/10702BXA	Voltage Regulator
JL140-5BYA	JM38510/10706BYA	Voltage Regulator
JL140-5SXA	JM38510/10702SXA	Voltage Regulator
JL140-5SYA	JM38510/10706SYA	Voltage Regulator
JL147BCA	JM38510/11906BCA	Wide BW Quad JFET Op Amp
JL148BCA	JM38510/11001BCA	Quad 741 Op Amp

NSID	PBID	Part Description
JL148BDA	JM38510/11001BDA	Quad 741 Op Amp
JL148BZA	JM38510/11001BZA	Quad 741 Op Amp
JL148SCA	JM38510/11001SCA	Quad 741 Op Amp
JL148SDA	JM38510/11001SDA	Quad 741 Op Amp
JL1558BGA	JM38510/10108BGA	Dual Op Amp
JL155BGA	JM38510/11401BGA	JFET Input Op Amp
JL156BGA	JM38510/11402BGA	JFET Input Op Amp
JL156SGA	JM38510/11402SGA	JFET Input Op Amp
JL193BGA	JM38510/11202BGA	Dual Comparator
JL193BPA	JM38510/11202BPA	Dual Comparator
JL198BGA	JM38510/12501BGA	Monolithic Sample and Hold
JL198SGA	JM38510/12501SGA	Monolithic Sample and Hold
JL2951BPA	5962-3870501BPA	LDO Regulator
JL2951S2A	5962-3870501S2A	LDO Regulator
JL2951SPA	5962-3870501SPA	LDO Regulator
JL411BPA	JM38510/11904BPA	JFET Input Op Amp
JL412BGA	JM38510/11905BGA	JFET Input Dual Op Amp
JL412BPA	JM38510/11905BPA	JFET Input Dual Op Amp
JL555BGA	JM38510/10901BGA	Timer
JL555BPA	JM38510/10901BPA	Timer
JL555SGA	JM38510/10901SGA	Timer
JL555SPA	JM38510/10901SPA	Timer
JL723BIA	JM38510/10201BIA	Precision Voltage Regulator
JL723SCA	JM38510/10201SCA	Precision Voltage Regulator
JL723SIA	JM38510/10201SIA	Precision Voltage Regulator
JL741BCA	JM38510/10101BCA	Op Amp
JL741BGA	JM38510/10101BGA	Op Amp
JL741BHA	JM38510/10101BHA	Op Amp
JL741BPA	JM38510/10101BPA	Op Amp
JL741SGA	JM38510/10101SGA	Op Amp
JL741SPA	JM38510/10101SPA	Op Amp
JL747BCA	JM38510/10102BCA	Dual Op Amp
JL747BDA	JM38510/10102BDA	Dual Op Amp
JL747BIA	JM38510/10102BIA	Dual Op Amp
JL747SCA	JM38510/10102SCA	Dual Op Amp
JL747SIA	JM38510/10102SIA	Dual Op Amp
LF147J-SMD	8102306CA	Quad BIFET Op Amp
LM101AHRQML	5962R9951501QGA	General Purpose Op Amp
LM101AHRQMLV	5962R9951501VGA	General Purpose Op Amp
LM101AJRQML	5962R9951501QPA	General Purpose Op Amp
LM101AJRQMLV	5962R9951501VPA	General Purpose Op Amp
LM101AWRQML	5962R9951501QHA	General Purpose Op Amp
LM101AWRQMLV	5962R9951501VHA	General Purpose Op Amp
LM107H/883	5962-8958901GA	Operational Amplifier
LM108AHRQML	5962R9863702QGA	Super Gain Op Amp
LM108AHRQMLV	5962R9863702VGA	Super Gain Op Amp
LM108AJ-8RQML	5962R9863702QPA	Super Gain Op Amp
LM108AJ-8RQMLV	5962R9863702VPA	Super Gain Op Amp
LM108AJRQML	5962R9863702QCA	Super Gain Op Amp
LM108AJRQMLV	5962R9863702VCA	Super Gain Op Amp

NSID	PBID	Part Description
LM108AWGRQML	5962R9863702QZA	Super Gain Op Amp
LM108AWGRQMLV	5962R9863702VZA	Super Gain Op Amp
LM108AWRQML	5962R9863702QHA	Super Gain Op Amp
LM108AWRQMLV	5962R9863702VHA	Super Gain Op Amp
LM10H/883	5962-8760401GA	Op Amp and Voltage Reference
LM111E-SMD	5962-8687701Q2A	Voltage Comparator
LM111HPQML	5962P0052401QGA	Voltage Comparator
LM111HPQMLV	5962P0052401VGA	Voltage Comparator
LM111J-8PQML	5962P0052401QPA	Voltage Comparator
LM111J-8PQMLV	5962P0052401VPA	Voltage Comparator
LM111WGPQML	5962P0052401QZA	Voltage Comparator
LM111WGPQMLV	5962P0052401VZA	Voltage Comparator
LM113-1H-QMLV	5962-9684302VXA	Reference Diode (1% Tolerance)
LM113-1H-SMD	5962-8671102XA	Reference Diode (1% Tolerance)
LM113H-QMLV	5962-9684301VXA	Reference Diode (1% Tolerance)
LM113H-SMD	5962-8671101XA	Reference Diode (1% Tolerance)
LM113WG-QMLV	5962-9684301VZA	Reference Diode (1% Tolerance)
LM118HPQML	5962P9853901QGA	Fast Op Amp
LM118HPQMLV	5962P9853901VGA	Fast Op Amp
LM118J-8PQML	5962P9853901QPA	Fast Op Amp
LM118J-8PQMLV	5962P9853901VPA	Fast Op Amp
LM118WGPQML	5962P9853901QZA	Fast Op Amp
LM118WGPQMLV	5962P9853901VZA	Fast Op Amp
LM119E-SMD	86014012A	High Speed Dual Comparator
LM119H-QMLV	5962-9679801VIA	High Speed Dual Comparator
LM119H-SMD	8601401IA	High Speed Dual Comparator
LM119J-QMLV	5962-9679801VCA	High Speed Dual Comparator
LM119J-SMD	8601401CA	High Speed Dual Comparator
LM119WGRQML	5962R9679801QXA	High Speed Dual Comparator
LM119WGRQMLV	5962R9679801VXA	High Speed Dual Comparator
LM119W-QMLV	5962-9679801VHA	High Speed Dual Comparator
LM119W-SMD	8601401HA	High Speed Dual Comparator
LM124AE/883	77043022A	Hi Perc Low Power Quad Op Amp
LM124AJ/883	7704302CA	Hi Perc Low Power Quad Op Amp
LM124AWG/883	7704302XA	Hi Perc Low Power Quad Op Amp
LM124J/883	7704301CA	Hi Perc Low Power Quad Op Amp
LM129AH-SMD	5962-8992101XA	Prec Zener 10 PPM/DEG C 6.9V
LM136AH-5.0-SMD	8418002XA	5.0V Reference Diode (1%)
LM137H-SMD	7703403XA	Precision Adj Neg Regulator
LM137HVH-SMD	7703404XA	Prec Adj Neg Reg (High Volt)
LM137HVK-SMD	7703404YA	Prec Adj Neg Reg (High Volt)
LM137K-SMD	7703403YA	Precision Adj Neg Regulator
LM139AE-SMD	5962-87739012A	Low Power Low Offset Volt Quad Comp
LM139AJ-QMLV	5962-9673801VCA	Low Power Low Offset Volt Quad Comp
LM139AJRQML	5962R9673801QCA	Quad Comparator
LM139AJRQMLV	5962R9673801VCA	Quad Comparator
LM139AJ-SMD	5962-8773901CA	Low Power Low Offset Volt Quad Com
LM139AWG-QMLV	5962-9673801VXA	Low Power Low Offset Volt Quad Com
LM139AWGRQML	5962R9673801QXA	Quad Comparator
LM139AWGRQMLV	5962R9673801VXA	Quad Comparator

NSID	PBID	Part Description
LM139AWG-SMD	5962-8773901XA	Low Power Low Offset Volt Quad Com
LM139AW-QMLV	5962-9673801VDA	Low Power Low Offset Volt Quad Com
LM139AWRQML	5962R9673801QDA	Quad Comparator
LM139AWRQMLV	5962R9673801VDA	Quad Comparator
LM139AW-SMD	5962-8773901DA	Low Power Low Offset Volt Quad Comp
LM150K/883	5962-8767501XA	3-Amp Adj Regulator
LM1575HVK5-QML	5962-9167202QXA	1A Step Down Simple Switch Reg
LM1575J-12-QML	5962-9167301QEA	1A Step Down Simple Switch Reg
LM1575J-15-QML	5962-9167401QEA	1A Step Down Simple Switch Reg
LM1575J-5.0-QML	5962-9167201QEA	1A Step Down Simple Switch Reg
LM1575J-ADJ-QML	5962-9167101MEA	1A Step-Down Switch Regulator
LM1575K-5.0-QML	5962-9167201MXA	1A Step-Down Switch Regulator
LM1575K-ADJ-QML	5962-9167101MXA	1A Step-Down Switch Regulator
LM1575WG12-QML	5962-9167301QZA	1A Step Down Simple Switcher R
LM1575WG15-QML	5962-9167401QZA	1A Step Down Simple Switcher R
LM1575WG5.0-QML	5962-9167201QZA	1A Step Down Simple Switcher R
LM1575WGADJ-QML	5962-9167101QZA	1A Step Down Simple Switcher
LM1577K-ADJ/883	5962-9216601MXA	Step-Up Simple Switcher
LM158AHLQML	5962L8771002QGA	Low Power Dual Op Amplifier
LM158AHLQMLV	5962L8771002VGA	Low Power Dual Op Amplifier
LM158AH-QMLV	5962-8771002VGA	Low Power Dual Op Amplifier
LM158AH-SMD	5962-8771002GA	Low Power Dual Op Amplifier
LM158AJ/883	5962-8771002PA	Low Power Dual Op Amplifier
LM158AJLQML	5962L8771002QPA	Low Power Dual Op Amplifier
LM158AJLQMLV	5962L8771002VPA	Low Power Dual Op Amplifier
LM158AJ-QMLV	5962-8771002VPA	Low Power Dual Op Amplifier
LM158AWG/883	5962-8771002QXA	Low Power Dual Op Amplifier
LM158H-SMD	5962-8771001GA	Low Power Dual Op Amplifier
LM158J/883	5962-8771001PA	Low Power Dual Op Amplifier
LM160H/883	5962-8767401GA	High Speed Differential Comp
LM185BYH1.2-SMD	5962-8759405XA	Precision Volt Ref 50 PPM/Deg C
LM185BYH2.5-SMD	5962-8759406XA	Precision Volt Ref 50 PPM/Deg C
LM185BYH-SMD	5962-9091401MXA	Precision Volt Ref 50 PPM/Deg C
LM185E-1.2/883	5962-87594012A	1.2V UPower Voltage Ref Diode
LM185H-1.2-SMD	5962-8759401XA	Precision Voltage Reference
LM185H-2.5-SMD	5962-8759402XA	Precision Voltage Reference
LM193AH/883	5962-9452602MGA	Low Power Low Offset Volt Dual Comp
LM193AH-QMLV	5962-9452602VGA	Low Power Low Offset Volt Dual Comp
LM193AJ/883	5962-9452602MPA	Low Power Low Offset Volt Dual C
LM193AJ-QMLV	5962-9452602VPA	Low Power Low Offset Volt Dual C
LM194H/883	5962-8777701XA	Monolithic NPN Transistor
LM195H/883	5962-8777801XA	Ultrareliable Power Transistor
LM195K/883	5962-8777801YA	Ultrareliable Power Transistor
LM199AH-SMD	5962-8856101XA	Precision 6.9V Reference
LM2940J-12/883	5962-9088401QEA	1A, 12V Positive LDO VReg
LM2940J-15/883	5962-9088501QEA	1A, 15V Positive LDO VReg
LM2940J-5.0/883	5962-8958701EA	1A, 5V Positive LDO VReg
LM2940WG-12/883	5962-9088401QXA	1A, 12V Positive LDO Reg
LM2940WG-15/883	5962-9088501QXA	1A, 15V Positive LDO Reg
LM2940WG5.0/883	5962-898701XA	1A, 5V Positive LDO Reg

NSID	PBID	Part Description
LM2941J/883	5962-9166701QEA	1A, Adj Positive LDO VReg
LM2941WG/883	5962-9166701QYA	Pos Adj 1.0A Low Dropout Amp
LM2990J-12-QML	5962-9571001QEA	1A, 12V Negative LDO VReg
LM2990J-15-QML	5962-9570901QEA	1A, 15V Negative LDO VReg
LM2990J-5.0-QML	5962-9571101QEA	1A, 5V Negative LDO VReg
LM2990WG-12-QML	5962-9571001QXA	Negative Low Dropout Regulator
LM2990WG-15-QML	5962-9570901QXA	Negative Low Dropout Regulator
LM2990WG5.0-QML	5962-9571101QXA	Negative Low Dropout Regulator
LM2991J-QML	5962-9650501QEA	1A, Adj Negative LDO VReg
LM2991WG-QML	5962-9650501QXA	1A, Adj. Neg. LDO VReg
LM3940J-3.3-QML	5962-9688401QEA	1A, 5 to 3.3V Positive LDO VReg
LM3940WG3.3-QML	5962-9688401QXA	1A, 5 to 3.3V Positive LDO VReg
LM6118J/883	5962-9156501MPA	Fast Settling Dual Op Amp
LM6121H/883	5962-9081201MGA	High Speed VIP Buffer
LM6121J/883	5962-9081201MPA	High Speed Buffer
LM6125H/883	5962-9081501MGA	High Speed Buffer
LM613AMJ/883	5962-9300301MEA	Dual Op Amp/Dual Comp/Adj Ref
LM6142AMJ-QML	5962-9550301QPA	15 MHz Precision Op Amp
LM6161E/883	5962-89621012A	High Speed Operational Amp
LM6161J/883	5962-8962101PA	Unity Gain VIP Op Amp
LM6161W/883	5962-8962101HA	High Speed VIP Op Amplifier
LM6162J/883	5962-9216501MPA	High Speed VIP Op Amp
LM6164J/883	5962-8962401PA	VIP High Speed Op Amp (AV > 5)
LM6164WG/883	5962-8962401XA	High Speed VIP Op Amp
LM6165J/883	5962-8962501PA	High Speed VIP Op Amplifier
LM6172AMJ-QML	5962-9560401QPA	Dual High Speed, Low Power Op Amp
LM6172AMWG-QML	5962-9560401QXA	Dual High Speed, Low Power Op Amp
LM7171AMJ-QML	5962-9553601QPA	Very High Speed, High Current Amp
LM7171AMWG-QML	5962-9553601QXA	Very High Speed, High Current Op Amp
LM725H/883	5962-9552901MGA	Operational Amplifier
LM78S40J/883	5962-8876101EA	Switching Regulator
LMC555J/883	5962-8950305PA	CMOS Timer
LMC6061AMJ/883	5962-9460401MPA	Precision CMOS UPower Op Amp
LMC6062AMJ/883	5962-9209403MPA	Precision Dual CMOS UPower Op Amp
LMC6064AMJ/883	5962-9209303MCA	Precision Quad CMOS UPower Op Amp
LMC6462AMJ-QML	5962-9560301QPA	Dual UPower Rail-to-Rail Amp
LMC6464AMJ-QML	5962-9560302QCA	Quad UPower Rail-to-Rail Amp
LMC6464AMWG-QML	5962-9560302QXA	Quad UPower Rail-to-Rail Op Amp
LMC6482AMJ/883	5962-9453401MPA	CMOS Dual R/R I/O Op Amp
LMC6484AMJ/883	5962-9453402MCA	Quad Rail-to-Rail Input/Output
LMC6484AMWG/883	5962-9453402QXA	Quad Rail-to-Rail Input/Output
LMD18200-2D/883	5962-9232501MXA	H-Bridge Motor Driver
LMD18200-2D-QV	5962-9232501VXA	Space LVL H-Bridge Motor Drive
LMX2305WG-QML	5962-9855003QXA	Single PLL 550 MHz
LMX2315WG-QML	5962-9855001QXA	1.2 GHz Single PLL
LMX2325WG-QML	5962-9855002QXA	2.5 GHz PLL
LP2951E/883	5962-3870501M2A	Vos Adj 100 mA UPower LDO VReg
LP2951H/883	5962-3870501MGA	Pos Adj 100 mA UPower LDO VReg
LP2951J/883	5962-3870501MPA	Pos Adj 100 mA UPower LDO VReg
LP2951WG/883	5962-3870501MXA	Pos Adj 100 mA LDO VReg

NSID	PBID	Part Description
LP2953AMJ/883	5962-9233601MEA	Pos Adj 250 mA UPower LDO VReg
LP2953AMWG/883	5962-9233601QXA	Pos Adj 250 mA UPower LDO VReg
LP2953AMWG-QMLV	5962-9233601VXA	Pos Adj 250 mA UPower LDO VReg
SCAN18245	5962-9311501	Non-Inverting 5.0V 18-bit Transceiver w/JTAG
SCAN18373	5962-9311801	5.0V 18-bit Transparent Latch w/JTAG
SCAN18374	5962-9320701	5.0V 18-bit D Flip-Flop w/JTAG
SCAN18540	5962-9312701	Inverting 18-bit 5.0V Line Driver w/JTAG
SCAN18541	5962-9311601	Non-Inverting 18-bit 5.0V Line Driver w/JTAG

National Semiconductor

System Test Access Solutions

National Semiconductor is a major supporter of Design-For-Test (DFT) for the electronic industry. Design-For-Test is a proven technique that reduces time-to-market and minimizes manufacturing costs and scrap. One of the major standards of DFT for Digital circuits is the JTAG IEEE 1149.1. The IEEE 1149.1 Standard for Boundary Scan Test is the foundation of any test strategy in complex electronic systems. The use of IEEE 1149.1 for board level test is growing in popularity as a method to provide high availability and to reduce design, manufacturing, and support costs. The IEEE 1149.1 infrastructure is not only being used to provide embedded test access, but also as a delivery medium for configuration and programming of complex PLD's and Flash Memory. National Semiconductor Corporation's System Test Access products support the IEEE 1149.1 standard and enable testability as a standard feature to differentiate new designs.

The following table is a list of National's System Test Access devices and the databook section where the datasheets are located. Please visit our website for updates on this exciting and growing technology.

http://www.national.com/appinfo/scan/

Part	Description	SMD	Section	Availability
SCAN18245T	Non-Inverting 5.0V 18-bit Transceiver w/ JTAG	5962-9311501	7 (ES)	Military
SCAN18373T	5.0V 18-bit Transparent Latch w/ JTAG	5962-9311801	7 (ES)	Military
SCAN18374T	5.0V 18-bit D Flip-Flop w/ JTAG	5962-9320701	7 (ES)	Military
SCAN18540T	Inverting 18-bit 5.0V Line Driver w/ JTAG	5962-9312701	7 (ES)	Military
SCAN18541T	Non-Inverting 18-bit 5.0V Line Driver w/ JTAG	5962-9311601	7 (ES)	Military
SCANPSC100F	5.0V Embedded Boundary Scan Controller		7 (ES)	Military
SCANPSC110F	5.0V Multidrop Addressable JTAG Port		7 (ES)	Military
SCAN921023	20–66 MHz 10-Bit LVDS Serializer w/ IEEE 1149.1 Test Access and BIST		9 (LVDS)	Industrial
SCAN921025	30–80 MHz 10-Bit LVDS Serializer w/ IEEE 1149.1 Test Access and BIST		9 (LVDS)	Industrial
SCAN921224	20–66 MHz 10-Bit LVDS Deserializer w/ IEEE 1149.1 Test Access and BIST		9 (LVDS)	Industrial
SCAN921226	30–80 MHz 10-Bit LVDS Deserializer w/ IEEE 1149.1 Test Access and BIST		9 (LVDS)	Industrial
SCAN921260	X6 1:10 Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST		9 (LVDS)	Industrial
SCAN92LV090	9 Channel Bus LVDS Transceiver w/ IEEE 1149.1 Test Access		9 (LVDS)	Industrial
SCANH16512	Universal 16-bit Bus Transceiver w/ IEEE 1149.1 Test Access		9 (LVDS)	Industrial
SCANSTA111	3.0V Multidrop Addressable JTAG Multiplexer		9 (LVDS)	Industrial

National Semiconductor

SCAN18245T
Non-Inverting Transceiver with TRI-STATE® Outputs

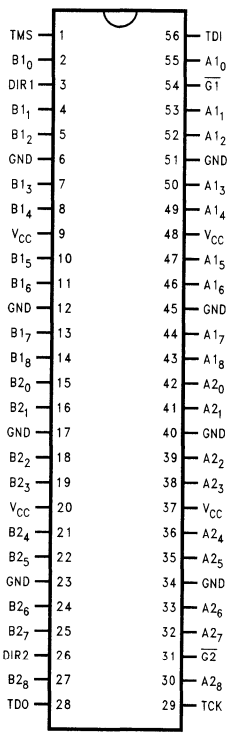
General Description

The SCAN18245T is a high speed, low-power bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Dual output enable control signals
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 24 mA/sink 48 mA
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch Cerpack package
- Includes CLAMP and HIGHZ instructions
- Available as Known Good Die
- Standard Microcircuit Drawing (SMD) 5962-9311501

Connection Diagram



10032001

Pin Names	Description
$A1_{(0-8)}$	Side A1 Inputs or TRI-STATE Outputs
$B1_{(0-8)}$	Side B1 Inputs or TRI-STATE Outputs
$A2_{(0-8)}$	Side A2 Inputs or TRI-STATE Outputs
$B2_{(0-8)}$	Side B2 Inputs or TRI-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins
DIR1, DIR2	Direction of Data Flow Pins

Truth Tables

Inputs		A1 (0–8)		B1 (0–8)
$\overline{G1}$	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

Inputs		A2 (0–8)		B2 (0–8)
$\overline{G2}$	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance

National Semiconductor

SCAN18373T
Transparent Latch with TRI-STATE® Outputs

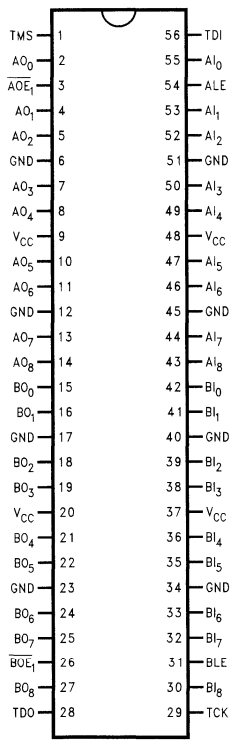
General Description

The SCAN18373T is a high speed, low-power transparent latch featuring separate data inputs organized into dual 9-bit bytes with byte-oriented latch enable and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Buffered active-low latch enable
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 24 mA/sink 48 mA
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch Cerpack packaging
- Includes CLAMP and HIGHZ instructions
- Standard Microcircuit Drawing (SMD) 5962-9311801

Connection Diagram



10032101

Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ALE, BLE	Latch Enable Inputs
$\overline{AOE_1}$, $\overline{BOE_1}$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Latch Outputs

Truth Tables

Inputs			AO (0–8)
ALE	$\overline{AOE_1}$	AI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	AO_0

Inputs			BO (0–8)
BLE	$\overline{BOE_1}$	BI (0–8)	
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	BO_0

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance
AO_0 = Previous AO before H-to-L transition of ALE
BO_0 = Previous BO before H-to-L transition of BLE

National Semiconductor

SCAN18374T
D Flip-Flop with TRI-STATE® Outputs

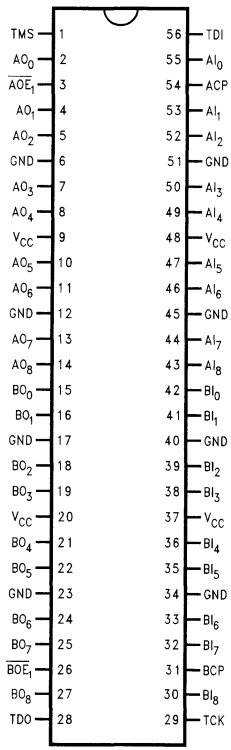
General Description

The SCAN18374T is a high speed, low-power D-type flip-flop featuring separate D-type inputs organized into dual 9-bit bytes with byte-oriented clock and output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and BOUNDARY-SCAN Architecture with the incorporation of the defined BOUNDARY-SCAN test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch Cerpack packaging
- Includes CLAMP and HIGHZ instructions
- Standard Microcircuit Drawing (SMD) 5962-9320701

Connection Diagram



10032201

Truth Tables

Pin Names	Description
$AI_{(0-8)}$, $BI_{(0-8)}$	Data Inputs
ACP, BCP	Clock Pulse Inputs
$\overline{AOE}_1$, $\overline{BOE}_1$	TRI-STATE Output Enable Inputs
$AO_{(0-8)}$, $BO_{(0-8)}$	TRI-STATE Outputs

Inputs			$AO_{(0-8)}$
ACP	$\overline{AOE}_1$	$AI_{(0-8)}$	
X	H	X	Z
N	L	L	L
N	L	H	H

Inputs			$BO_{(0-8)}$
BCP	$\overline{BOE}_1$	$BI_{(0-8)}$	
X	H	X	Z
N	L	L	L
N	L	H	H

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance
N= L-to-H Transition

National Semiconductor

SCAN18540T
Inverting Line Driver with TRI-STATE® Outputs

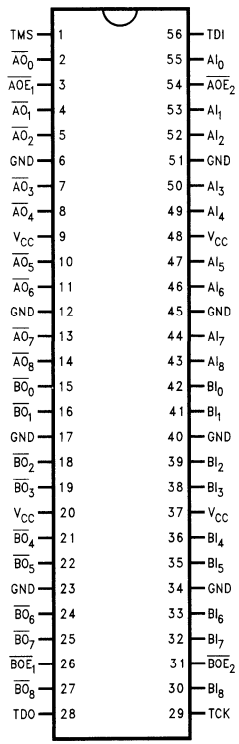
General Description

The SCAN18540T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) compliant
- Dual output enable signals per byte
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch Cerpack packaging
- Includes CLAMP and HIGHZ instructions
- Standard Microcircuit Drawing (SMD) 5962-9312701

Connection Diagram



10032301

Pin Names	Description
$AI_{(0-8)}$	Input pins, A side
$BI_{(0-8)}$	Input pins, B side
$\overline{AOE}_1$, $\overline{AOE}_2$	TRI-STATE Output Enable Input pins, A side
$\overline{BOE}_1$, $\overline{BOE}_2$	TRI-STATE Output Enable Input pins, B side
$\overline{AO}_{(0-8)}$	Output pins, A side
$\overline{BO}_{(0-8)}$	Output pins, B side

Truth Tables

Inputs			$\overline{AO}$ (0–8)
$\overline{AOE}_1$	$\overline{AOE}_2$	AI (0–8)	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

Inputs			$\overline{BO}$ (0–8)
$\overline{BOE}_1$	$\overline{BOE}_2$	BI (0–8)	
L	L	H	L
H	X	X	Z
X	H	X	Z
L	L	L	H

H= HIGH Voltage Level
X= Immaterial
L = LOW Voltage Level
Z = High Impedance

National Semiconductor

SCAN18541T
Non-Inverting Line Driver with TRI-STATE® Outputs

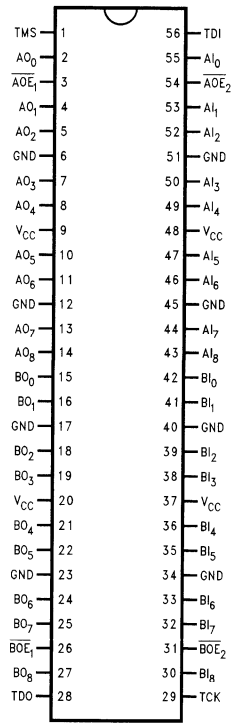
General Description

The SCAN18541T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- IEEE 1149.1 (JTAG) Compliant
- Dual output enable signals per byte
- TRI-STATE outputs for bus-oriented applications
- 9-bit data busses for parity applications
- Reduced-swing outputs source 24 mA/sink 48 mA (Mil)
- Guaranteed to drive 50Ω transmission line to TTL input levels of 0.8V and 2.0V
- TTL compatible inputs
- 25 mil pitch Cerpack packaging
- Includes CLAMP and HIGHZ instructions
- Standard Microcircuit Drawing (SMD) 5962-9311601

Connection Diagram



10032401

Pin Names

Pin Names	Description
$AI_{(0-8)}$	Input Pins, A Side
$BI_{(0-8)}$	Input Pins, B Side
$\overline{AOE}_1$, $\overline{AOE}_2$	TRI-STATE Output Enable Input Pins, A Side
$\overline{BOE}_1$, $\overline{BOE}_2$	TRI-STATE Output Enable Input Pins, B Side
$AO_{(0-8)}$	Output Pins, A Side
$AO_{(0-8)}$	Output Pins, B Side

Truth Tables

Inputs			AO (0–8)
$\overline{AOE}_1$	$\overline{AOE}_2$	AI (0–8)	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

Inputs			BO (0–8)
$\overline{BOE}_1$	$\overline{BOE}_2$	BI (0–8)	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H= HIGH Voltage Level
L= LOW Voltage Level
X= Immaterial
Z= High Impedance

National Semiconductor

SCANPSC100F
Embedded Boundary Scan Controller (IEEE 1149.1 Support)

General Description

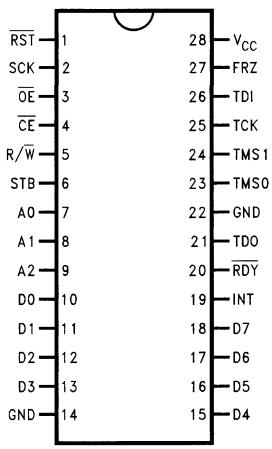
The SCANPSC100F is designed to interface a generic parallel processor bus to a serial scan test bus. It is useful in improving scan throughput when applying serial vectors to system test circuitry and reduces the software overhead that is associated with applying serial patterns with a parallel processor. The 'PSC100F operates by serializing data from the parallel bus for shifting through the chain of 1149.1 compliant components (i.e., scan chain). Scan data returning from the scan chain is placed on the parallel port to be read by the host processor. Up to two scan chains can be directly controlled with the 'PSC100F via two independent TMS pins. Scan control is supplied with user specific patterns which makes the 'PSC100F protocol-independent. Overflow and underflow conditions are prevented by stopping the test clock. A 32-bit counter is used to program the number of TCK cycles required to complete a scan operation within the boundary scan chain or to complete a 'PSC100F Built-In Self Test (BIST) operation. SCANPSC100F device drivers and 1149.1 embedded test application code are available with National's SCANEase software tools.

Features

- Compatible with IEEE Std. 1149.1 (JTAG) Test Access Port and Boundary Scan Architecture
- Supported by National's SCAN Ease (Embedded Application Software Enabler) Software
- Uses generic, asynchronous processor interface; compatible with a wide range of processors and PCLK frequencies
- Directly supports up to two 1149.1 scan chains
- 16-bit Serial Signature Compaction (SSC) at the Test Data In (TDI) port
- Automatically produces pseudo-random patterns at the Test Data Out (TDO) port
- Fabricated on FACT™ 1.5 µm CMOS process
- Supports 1149.1 test clock (TCK) frequencies up to 25 MHz
- TTL-compatible inputs; full-swing CMOS outputs with 24 mA source/sink capability
- Standard Microcircuit Drawing (SMD) 5962-9475001

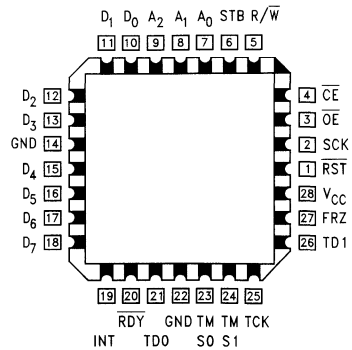
Connection Diagrams

28-Pin DIP and Flatpak



10032501

Pin Assignment for LCC



10032518

National Semiconductor

SCANPSC110F
SCAN Bridge Hierarchical and Multidrop Addressable JTAG Port (IEEE1149.1 System Test Support)

General Description

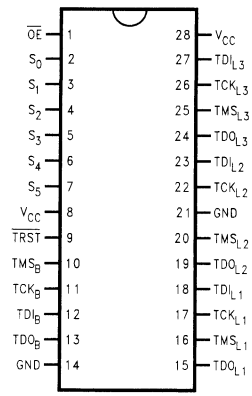
The SCANPSC110F Bridge extends the IEEE Std. 1149.1 test bus into a multidrop test bus environment. The advantage of a hierarchical approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules. Each SCANPSC110F Bridge supports up to 3 local scan rings which can be accessed individually or combined serially. Addressing is accomplished by loading the instruction register with a value matching that of the Slot inputs. Backplane and inter-board testing can easily be accomplished by parking the local TAP Controllers in one of the stable TAP Controller states via a Park instruction. The 32-bit TCK counter enables built in self test operations to be performed on one port while other scan chains are simultaneously tested.

Features

- True IEEE1149.1 hierarchical and multidrop addressable capability
- The 6 slot inputs support up to 59 unique addresses, a Broadcast Address, and 4 Multi-cast Group Addresses
- 3 IEEE 1149.1-compatible configurable local scan ports
- Mode Register allows local TAPs to be bypassed, selected for insertion into the scan chain individually, or serially in groups of two or three
- 32-bit TCK counter
- 16-bit LFSR Signature Compactor
- Local TAPs can be tri-stated via the $\overline{OE}$ input to allow an alternate test master to take control of the local TAPs
- The IP version of this device supports features not described in this datasheet such as 8 slot inputs for enhanced address capability and additional instructions. For a completed description of the additional instructions supported, refer to the SCANPSC110 supplemental datasheet.

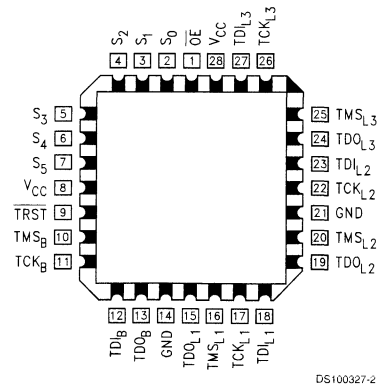
Connection Diagrams

28-Pin
CDIP and Flatpak



DS100327-1

Pin Assignment for LCC



DS100327-2

Connection Diagrams (Continued)

Order Number	Description
SCANPSC110FFMQB	Military Flatpak
SCANPSC110FDMQB	Military DIP
SCANPSC110FLMQB	Military Leadless Chip Carrier

Pin Names	Description
TCK_B	Backplane Test Clock Input
TMS_B	Backplane Test Mode Select Input
TDI_B	Backplane Test Data Input
TDO_B	Backplane Test Data Output
$\overline{TRST}$	Asynchronous Test Reset Input (Active low)
$S_{(0,5)}$	Address Select Port
$\overline{OE}$	Local Scan Port Output Enable (Active low)
$TCK_{L(1-3)}$	Local Port Test Clock Output
$TMS_{L(1-3)}$	Local Port Test Mode Select Output
$TDI_{L(1-3)}$	Local Port Test Data Input
$TDO_{L(1-3)}$	Local Port Test Data Output

National Semiconductor

Automotive Products and Services

National Semiconductor remains a major supplier to the automotive market which it has served for more than 30 years. The Enhanced Solutions Division, adapts select products and designs from National's broad portfolio to the automotive-market place.

Some examples of products which have been characterized to meet the stringent demands of Automotive applications are as follows with the datasheets located in the sections specified.

Special Functions (Section 11)

LM1815; Adaptive Variable Reluctance Sensor Amplifier
LM1949; Injector Drive Controller
LM2907/LM2917; Frequency to Voltage Converter
LM9061; Power MOSFET Driver with Loss less Protection

Automotive Engine Control

LM9011; Electronic Ignition Interface
LM9040; Dual Lambda Sensor Interface Amplifier
LM9044; Lambda Sensor Interface Amplifier

Liquid Crystal Display Drivers

MM5452/MM5453; Liquid Crystal Display Drivers
MM5483; Liquid Crystal Display Driver
MM145453; Liquid Crystal Display Driver

Motion Control

LMD18400; Quad High Side Driver

Peripheral Drivers

DP8310/DP8311; Octal Latched Peripheral Drivers
DS0026; Dual High-Speed MOS Driver
DS2003; High Current/Voltage Darlington Drivers
DS3658; Quad High Current Peripheral Driver
DS3668; Quad Fault Protected Peripheral Driver
DS3680; Quad Negative Voltage Relay Driver
DS75451/2/3; Series Dual Peripheral Drivers

Vacuum Florescent Display Drivers

LM9022; Vacuum Fluorescent Display Filament Driver
MM58342; High Voltage Display Driver

Voltage Regulators - Linear (Section 15)

LM9074; System Voltage Regulator with Keep-Alive ON/OFF Control

Low Dropout Regulators (Section 16)

LM2936-3.0; Ultra-Low Quiescent Current 3.0V Regulator
LM2936-3.3; Ultra-Low Quiescent Current 3.3V Regulator
LM2936-5.0; Ultra-Low Quiescent Current 5.0V Regulator
LM2984; Microprocessor Power Supply System
LM9070; Low-Dropout System Voltage Regulator with Keep-Alive ON/OFF Control
LM9071; Low-Dropout System Voltage Regulator with Delayed Reset
LM9072; Dual Tracking Low-Dropout System Regulator
LM9073; Dual High Current Low-Dropout System Regulator

Section 8
Interface - Data Transmission Circuits

Section 8 Contents

BACKPLANE TRANSCEIVER LOGIC (BTL)

GENERAL PURPOSE DRIVERS/RECEIVERS

TIA/EIA-485 (RS-485)

National Semiconductor

Interface-Data Transmission Circuits

TIA/EIA-485 (RS-485)

Tx	Rx	Temp Range	Base Part Number	Page No.
0	4	Com	DS96173C	8-97
0	4	Com	DS96175C	8-97
0	4	Mil-883	DS96F173M	8-101
0	4	Com	DS96F175C	8-101
0	4	Mil-883	DS96F175M	8-101
1	1	Com	DS1487	8-82
1	1	Mil	DS16F95	8-83
1	1	Mil-883	DS16F95	8-83
1	1	Com	DS36276	8-84
1	1	Ind	DS36277T	8-85
1	1	Com	DS3695	8-86
1	1	Com	DS3695A	8-89
1	1	Ind	DS3695AT	8-89
1	1	Ind	DS3695T	8-86
1	1	Com	DS3696	8-86
1	1	Com	DS3696A	8-89
1	1	Com	DS3697	8-86
1	1	Com	DS36C278	8-90
1	1	Ind	DS36C278T	8-90
1	1	Com	DS36C279	8-91
1	1	Ind	DS36C279T	8-91
1	1	Com	DS36C280	8-92
1	1	Ind	DS36C280T	8-92
1	1	Com	DS36F95	8-83
1	1	Ind	DS481T	8-93
1	1	Com	DS485	8-94
1	1	Ind	DS485T	8-94
1	1	Com	DS75176B	8-95
1	1	Ind	DS75176BT	8-95
1	1	Com	DS96176C	8-98
1	1	Com	DS96177C	8-99
4	0	Com	DS96172C	8-96
4	0	Com	DS96174C	8-96
4	0	Mil-883	DS96F172M	8-100
4	0	Com	DS96F174C	8-100
4	0	Mil-883	DS96F174M	8-100
4	4	Com	DS36950	8-87
4	4	Com	DS36954	8-88

TIA/EIA-422 Drivers (RS-422)
TIA/EIA-422/423 Receivers (RS-422/423)

Tx	Rx	Temp Range	Base Part Number	Page No.
0	2	Mil-883	DS78C120	8-42
0	2	Mil-883	DS78C20	8-41
0	2	Mil-883	DS78LS120	8-43
0	2	Com	DS88C120	
0	2	Com	DS88C20	8-41
0	2	Com	DS9637AC	8-52
0	2	Mil-883	DS9637AM	8-52
0	4	Mil-883	DS26C32AM	8-30
0	4	Ind	DS26C32AT	8-30
0	4	Mil-883	DS26F32M	8-32
0	4	Com	DS26LS32AC	8-33
0	4	Com	DS26LS32C	8-33
0	4	Mil-883	DS26LS32M	8-33
0	4	Com	DS26LS33AC	8-33
0	4	Mil-883	DS26LS33M	8-33
0	4	Ind	DS26LV32AT	8-31
0	4	Mil	DS26LV32AW	8-31
0	4	Com	DS3486	8-37
0	4	Ind	DS34C86T	8-35
0	4	Ind	DS34LV86T	8-36
0	12	Ind	DS89C386T	8-49
1	1	Com	DS8921	8-44
1	1	Com	DS8921A	8-44
1	1	Ind	DS8921AT	8-44
1	1	Ind	DS89C21T	8-45
2	0	Mil-883	DS1691A	8-25
2	0	Com	DS3691	8-25
2	0	Com	DS9638C	8-53
2	0	Mil-883	DS9638M	8-53
2	2	Com	DS8922	8-46
2	2	Com	DS8922A	8-46
2	2	Com	DS8923A	8-46
2	3	Com	DS8925	8-48
2	3	Com	DS8935	
4	0	Mil-883	DS26C31M	8-26
4	0	Ind	DS26C31T	8-26
4	0	Mil-883	DS26F31M	8-28
4	0	Com	DS26LS31C	8-29
4	0	Mil-883	DS26LS31M	8-29
4	0	Ind	DS26LV31T	8-27
4	0	Mil	DS26LV31W	8-27
4	0	Com	DS3487	8-40
4	0	Ind	DS34C87T	8-38
4	0	Ind	DS34LV87T	8-39
12	0	Ind	DS89C387T	8-50

TIA/EIA-423 (RS-423)

Tx	Rx	Temp Range	Base Part Number	Page No.
2	0	Mil-883	DS9636A	8-51
2	0	Com	DS9636AC	8-51
4	0	Mil-883	DS1691A	8-25
4	0	Com	DS3691	8-25

TIA/EIA-232 (RS-232)

Tx	Rx	Temp Range	Base Part Number	Page No.
0	2	Mil-883	DS9627M	8-16
0	4	Com	DS1489	8-11
0	4	Com	DS1489A	8-11
0	4	Com	DS14C89A	8-13
0	4	Com	DS75154	8-15
2	0	Com	DS75150	8-14
2	2	Mil-883	DS14C232	8-17
2	2	Com	DS14C232C	8-17
2	2	Ind	DS14C232T	8-17
3	5	Com	DS14185	8-22
3	5	Com	DS14C335	8-20
3	5	Com	DS14C535	8-21
4	0	Com	DS1488	8-9
4	0	Com	DS14C88	8-10
4	4	Com	DS14C238	8-18
4	5	Com	DS14C241	8-19
5	3	Com	DS14196	8-23
5	3	Com	DSV14196	8-24

General Purpose Line Drivers and Receivers

Tx	Rx	Temp Range	Base Part Number	Page No.
0	2	Mil-883	DS1603	8-68
0	2	Com	DS75107	8-70
0	2	Com	DS75107A	8-70
0	2	Mil-883	DS7820	8-71
0	2	Mil-883	DS7820A	8-71
0	2	Com	DS8820A	8-71
0	2	Mil-883	DS9622M	8-72
0	4	Com	DS3650	8-69
0	4	Com	DS3651	
2	0	Mil	DS1692	
2	0	Com	DS75110A	8-64
2	0	Mil-883	DS7830	8-65
2	0	Mil-883	DS7831	8-65
2	0	Mil	DS7831	8-65
2	0	Mil-883	DS7832	8-66
2	0	Com	DS8832	8-66
4	4	Com	DS26S10	8-81
4	4	Com	DS3662	8-73
4	4	Com	DS8641	8-76
4	4	Com	DS8838	8-78

General Purpose Line Drivers and Receivers (Continued)

Tx	Rx	Temp Range	Base Part Number	Page No.
8	8	Mil-883	DS1776	8-80
8	8	Com	DS3862	8-74
8	8	Com	DS75160A	8-75
8	8	Com	DS75161A	8-75

BTL

Tx	Rx	Temp Range	Base Part Number	Page No.
4	4	Com	DS3893A	8-62
4	4	Com	DS3897	8-63
6	6	Com	DS3884A	8-56
8	8	Com	DS3896	8-63
9	9	Com	DS3883A	8-54
9	9	Com	DS3886A	8-58
9	9	Com	DS38C86A	8-60

Temperature ranges:

Com = Commercial 0˚C to +70˚C

Ind = Industrial −40˚C to +85˚C

Mil = Military −55˚C to +125˚C

Mil-883 = Military 883 Qual −55˚C to +125˚C

National Semiconductor

DS1488
Quad Line Driver

General Description

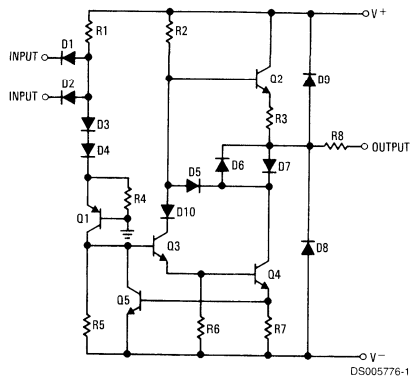
The DS1488 is a quad line driver which converts standard TTL input logic levels through one stage of inversion to output levels which meet EIA Standard RS-232D and CCITT Recommendation V.24.

Features

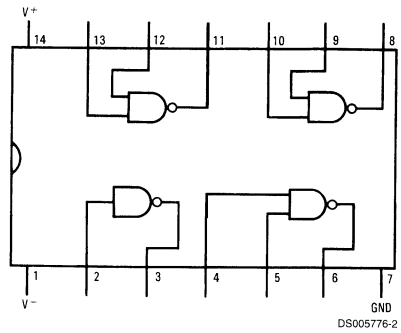
- Current limited output: ±10 mA typ
- Power-off source impedance: 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are TTL/LS compatible

Schematic and Connection Diagrams

1/4 Circuit



Dual-In-Line Package



Top View
Order Number DS1488M or DS1488N
See NS Package Number M14A or N14A

National Semiconductor

DS14C88
Quad CMOS Line Driver

General Description

The DS14C88, pin-for-pin compatible to the DS1488/ MC1488, is a quad line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). This device translates standard TTL/ CMOS logic levels to levels conforming to EIA-232-D and CCITT V.28 standards.

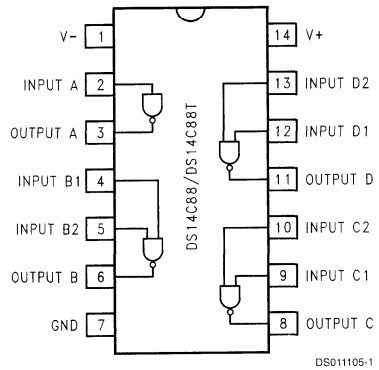
The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to its bipolar equivalents: 500 µA (DS14C88) versus 25 mA (DS1488).

The DS14C88 simplifies designs by eliminating the need for external slew rate control capacitors. Slew rate control in accordance with EIA-232D is provided on-chip, eliminating the output capacitors.

Features

- Meets EIA-232D and CCITT V.28 standards
- LOW power consumption
- Wide power supply range: ±5V to ±12V
- Available in SOIC package

Connection Diagram



Order Number DS14C88N, or DS14C88M
See NS Package Number N14A or M14A

National Semiconductor

DS1489/DS1489A
Quad Line Receiver

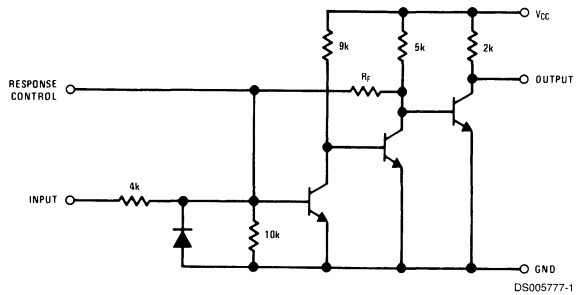
General Description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA Standard RS-232D. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements.

Features

- Four separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode: high output for open inputs
- Inputs withstand ±30V

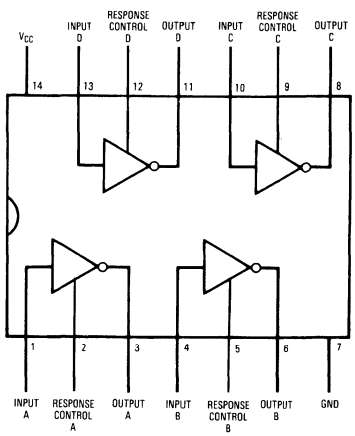
Schematic and Connection Diagrams



DS005777-1

(¼ of unit shown)
DS1489: R_F = 10k
DS1489A: R_F = 2k

Dual-In-Line Package



DS005777-2

Top View
Order Number DS1489M, DS1489N
DS1489AM or DS1489AN
See NS Package Number M14A or N14A

AC Test Circuit and Voltage Waveforms

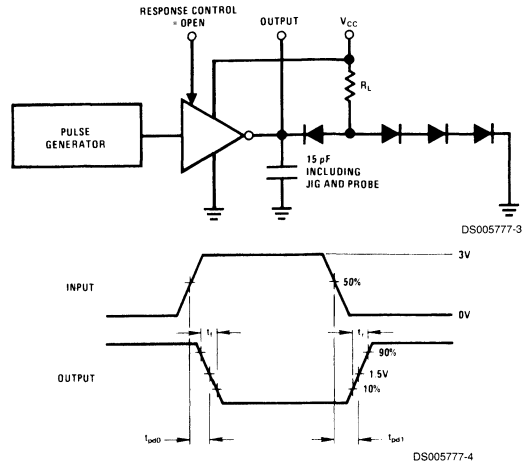


FIGURE 1.

National Semiconductor

DS14C89A
Quad CMOS Receiver

General Description

The DS14C89A, pin-for-pin compatible to the DS1489A/MC1489A, ia a quad receiver designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). These devices translate levels conforming to EIA-232E and CCITT V.28 standards to TTL/CMOS logic levels.

The device is fabricated in low threshold CMOS metal gate technology. The device provides very low power consumption compared to their bipolar equivalents: 900 µA (DS14C89A) versus 26 mA (DS1489A).

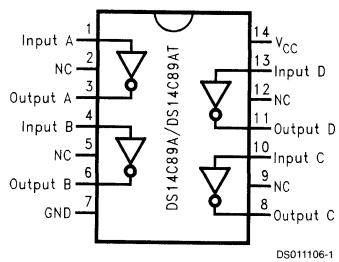
The DS14C89A provides on chip noise filtering which eliminates the need for external response control filter capacitors.

When replacing the DS1489A with the DS14C89A, the response control filter pins can be tied high, low, or not connected.

Features

- Meets EIA/TIA-232-E and CCITT V.28 Standards
- Failsafe - Output High for Open Input
- LOW Power consumption
- On chip noise filter
- Available in SOIC Package

Connection Diagram



DS011106-1

Order Number DS14C89AN, DS14C89AM,
See NS Package Number M14A, N14A

National Semiconductor

DS75150
Dual Line Driver

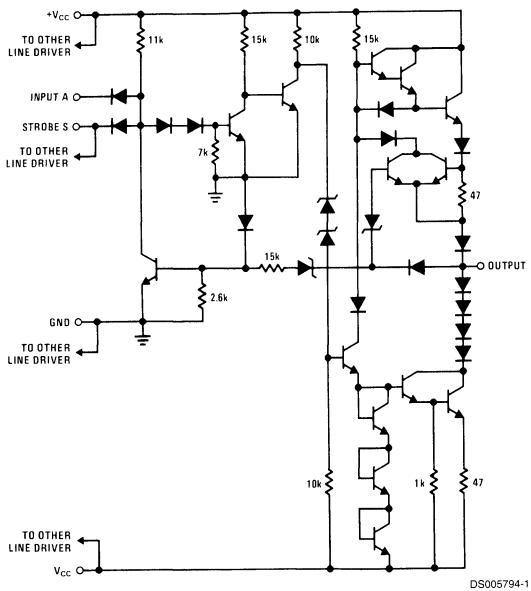
General Description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and LS families. Operation is from −12V and +12V power supplies.

Features

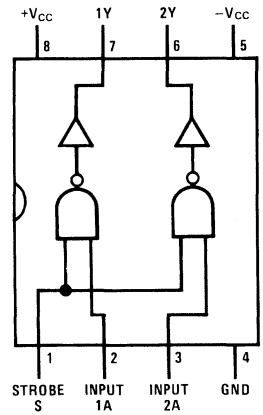
- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2 μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and LS families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages: ±12V

Schematic and Connection Diagrams



Component values shown are nominal.
1/2 of circuit shown

Dual-In-Line Package



Positive Logic C = $\overline{AS}$

Top View
Order Number DS75150M
See NS Package Number M08A

National Semiconductor

DS75154
Quad Line Receiver

General Description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and LS circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

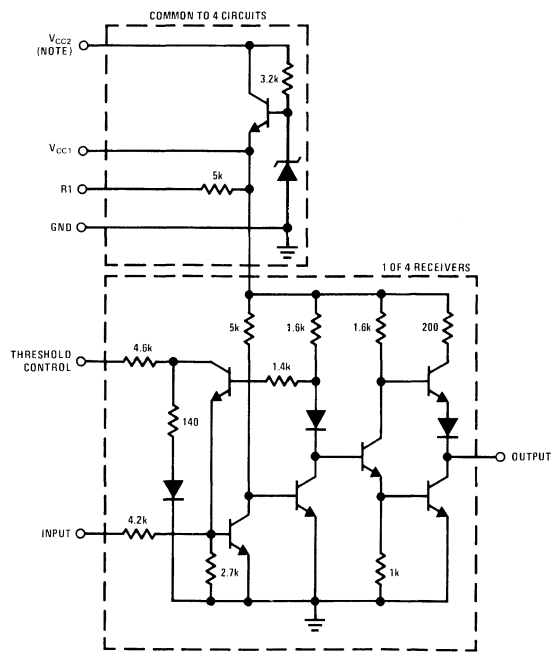
For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

Features

- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with TTL or LS
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

8

Schematic Diagram



DS005795-1

Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

National Semiconductor

DS9627
Dual Line Receiver

General Description

The DS9627 is a dual-line receiver which meets the electrical interface specifications of EIA RS-232C and MIL-STD-188C. The input circuitry accommodates ±25V input signals and the differential inputs allow user selection of either inverting or non-inverting logic for the receiver operation. The DS9627 provides both a selectable hysteresis range and selectable receiver input resistance. When pin 1 is tied to V^-, the typical switching points are at 2.6V and −2.6V, thus meeting RS-232-C requirements. When pin 1 is open, the typical switching points are at 50 µA and −50 µA, thus satisfying the requirements of MIL-STD-188C LOW level interface. Connecting the RA and/or RB pins to the (−) input yields an input impedance in the range of 3 kΩ to 7 kΩ and satisfies RS-232-C requirements; leaving RA and/or RB pins unconnected, the input resistance will be greater than 6 kΩ to satisfy MIL-STD-188C.

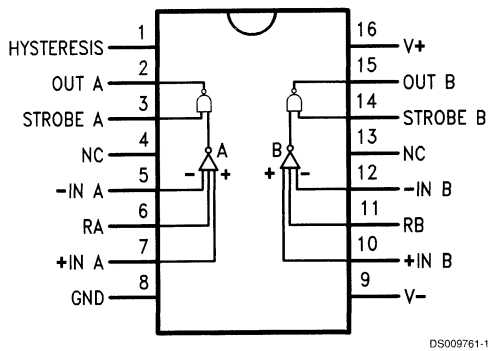
The output circuitry is TTL/DTL compatible and will allow "collector-dotting" to generate the wired-OR function. A TTL/DTL strobe is also provided for each receiver.

Features

- EIA RS-232-C input standards
- MIL-STD-188C input standards
- Variable hysteresis control
- High common mode rejection
- R control (5 kΩ or 10 kΩ)
- Wired-OR capability
- Choice of inverting and non-inverting inputs
- Outputs and strobe TTL compatible

Connection Diagram

16-Lead DIP



Top View
Order Number DS9627MJ/883
See NS Package Number J16A
For Complete Military 883 Specifications, see RETS Data Sheet.

National Semiconductor

DS14C232
Low Power +5V Powered TIA/EIA-232 Dual Driver/Receiver

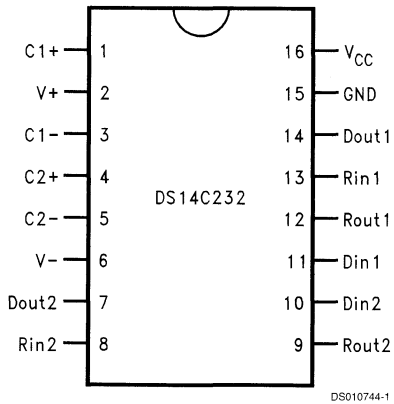
General Description

The DS14C232 is a low power dual driver/receiver featuring an onboard DC to DC converter, eliminating the need for ±12V power supplies. The device only requires a +5V power supply. I_{CC} is specified at 3.0 mA maximum, making the device ideal for battery and power conscious applications. The drivers' slew rate is set internally and the receivers feature internal noise filtering, eliminating the need for external slew rate and filter capacitors. The device is designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE). The driver inputs and receiver outputs are TTL and CMOS compatible. DS14C232C driver outputs and receiver inputs meet TIA/EIA-232-E (RS-232) and CCITT V.28 standards.

Features

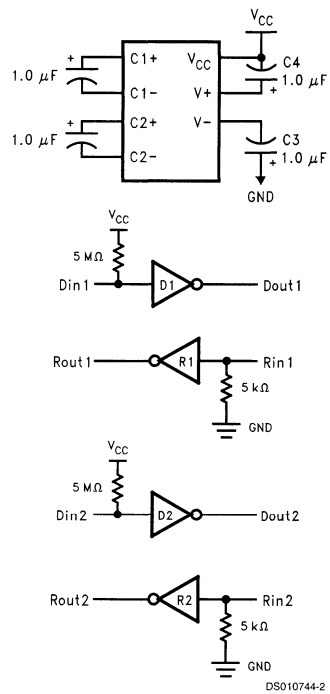
- Pin compatible with industry standard MAX232, LT1081, ICL232 and TSC232
- Single +5V power supply
- Low power—I_{CC} 3.0 mA maximum
- DS14C232C meets TIA/EIA-232-E (RS-232) and CCITT V.28 standards
- CMOS technology
- Receiver Noise Filter
- Package efficiency—2 drivers and 2 receivers
- Available in Plastic DIP, Narrow and Wide SOIC packages
- TIA/EIA-232 compatible extended temperature range option:
  DS14C232T −40°C to +85°C
  DS14C232E/J: −55°C to +125°C

Connection Diagram



Order Number DS14C232CN, DS14C232CM, or DS14C232TM
See NS Package Number N16E, or M16A

Functional Diagram



National Semiconductor

DS14C238
Single Supply TIA/EIA-232 4 x 4 Driver/Receiver

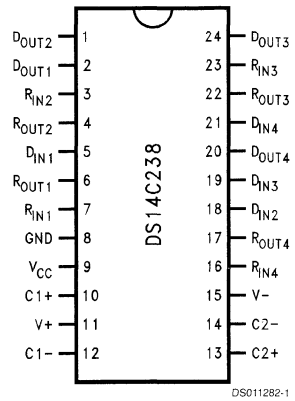
General Description

The DS14C238 is a four driver, four receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC-DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors.

Features

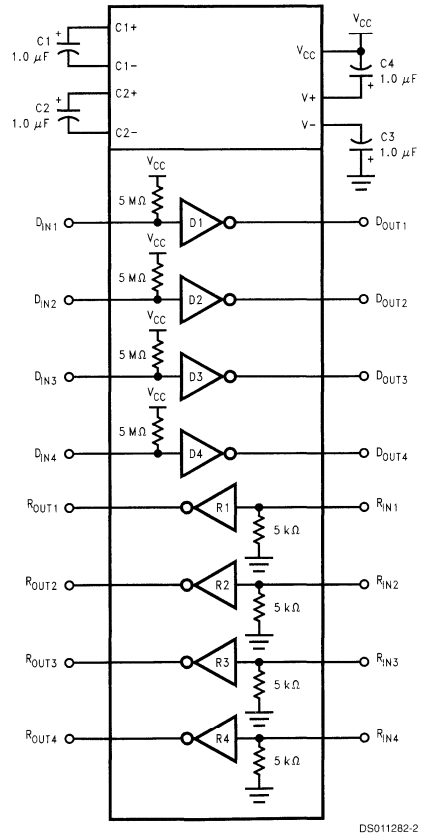
- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC-DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Internal driver slew rate control
- Receiver noise filtering
- Operates above 120 kbits/sec
- Direct replacement for MAX238

Connection Diagram



Order Number DS14C238WM
See NS Package Number M24B

Functional Diagram



National Semiconductor

DS14C241
Single Supply TIA/EIA-232 4 x 5 Driver/Receiver

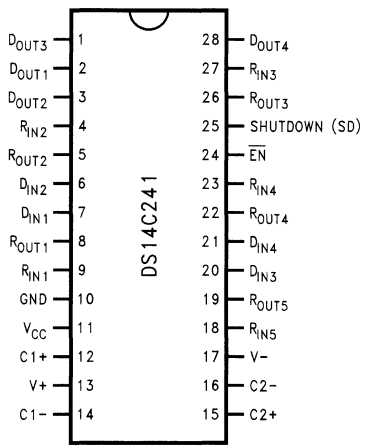
General Description

The DS14C241 is four driver, five receiver device which conforms to the TIA/EIA-232-E standard and CCITT V.28 recommendations. This device eliminates ±12V supplies by employing an internal DC–DC converter to generate the necessary output levels from a single +5V supply. Driver slew rate control and receiver noise filtering have also been internalized to eliminate the need for external slew rate control and noise filtering capacitors. With the addition of TRI-STATE®receiver outputs and a shutdown mode, device power consumption is kept to a minimum.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28
- Internal DC–DC converter
- Operates with single +5V supply
- Low power requirement—I_{CC} 10 mA max
- Shutdown mode—I_{CX} 10 µA max
- Internal driver slew rate control
- Receiver noise filtering
- Operates above 120 kbits/sec
- TRI-STATE receiver outputs
- Direct replacement for MAX241

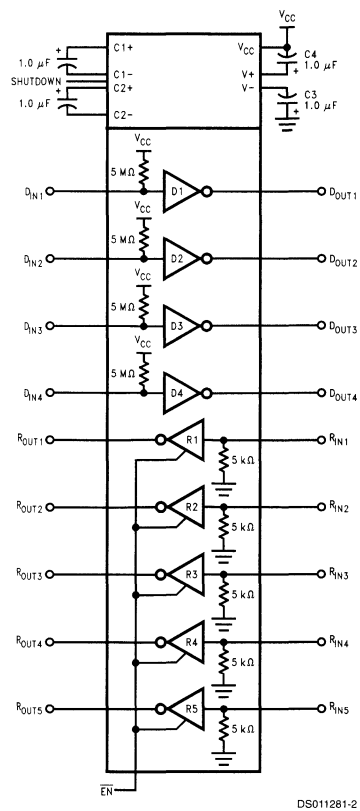
Connection Diagram



DS011281-1

Order Number DS14C241WM
See NS Package Number M28B

Functional Diagram



DS011281-2

National Semiconductor

DS14C335
+3.3V Supply TIA/EIA-232 3 x 5 Driver/Receiver

General Description

The DS14C335 is three driver, five receiver device which conforms to TIA/EIA-232-E and CCITT V.28 standard specifications. This device employs an internal DC-DC converter to generate the necessary output levels from a +3.3V power supply. A SHUTDOWN (SD) mode reduces the supply current to 10 µA maximum. In the SD mode, one receiver is active, allowing ring indicator (RI) to be monitored. PC Board space consumption is minimized by the availability of Shrink Small Outline Packaging (SSOP).

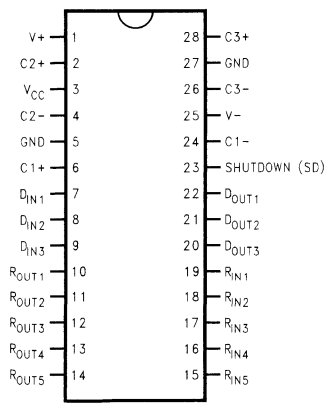
This device's low power requirement and small footprint makes it an ideal choice for Laptop and Notebook applications.

Features

- Conforms to TIA/EIA-232-E and CCITT V.28 specifications
- Operates with single +3.3V power supply
- Low power requirement—I_{CC} 20 mA maximum
- SHUTDOWN mode—I_{CX} 10 µA maximum
- One Receiver (R5) active during SHUTDOWN
- Operates up to 128 kbps—Lap-Link® Compatible
- Flow through pinout
- 4V/µs minimum Slew Rate guaranteed
- Inter-operates with +5V UARTs
- Available in 28-lead SSOP EIAJ Type II package

Connection Diagram

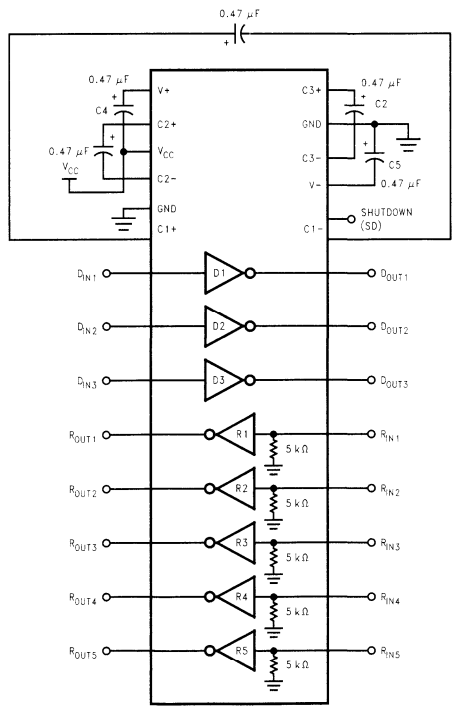
DS14C335



DS011734-1

Order Number DS14C335MSA
See NS Package Number MSA28

Functional Diagram



DS011734-2

National Semiconductor

DS14C535
+5V Supply EIA/TIA-232 3 x 5 Driver/Receiver

General Description

The DS14C535 is three driver, five receiver device which conforms to EIA/TIA-232-E and CCITT (ITU-T) V.28 standard specifications. This device employs an internal DC-DC converter to generate the necessary output levels from a +5V power supply. A SHUTDOWN (SD) mode reduces the supply current to 10 µA maximum. In the SD mode, one receiver is active, allowing ring indicator (RI) to be monitored. PC Board space consumption is minimized by the availability of Shrink Small Outline Packaging (SSOP).

The DS14C535 provides a one-chip solution for the common 9-pin serial RS-232 interface between data terminal and data circuit-terminating equipment.

This device allows an easy migration path to the 3.3V DS14C335. The packages are the same. The N/C pins on the DS14C535 are not physically connected to the chip. Board layout for the DS14C335 will accommodate both devices.

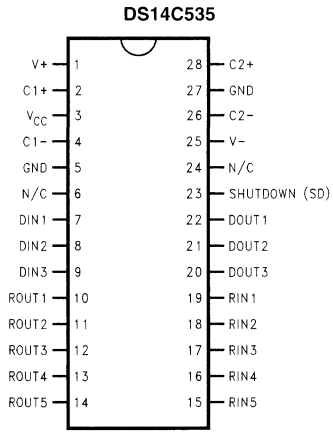
This device's low power requirement and small footprint makes it an ideal choice for Laptop and Notebook applications.

Features

- Pin compatible with DS14C335
- Conforms to EIA/TIA-232-E and CCITT (ITU-T) V.28 specifications
- Failsafe receiver outputs high when inputs open
- Operates with single +5V power supply
- Low power requirement—I_{CC} 12 mA maximum
- SHUTDOWN mode—I_{CX} 10 µA maximum
- One Receiver (R5) active during SHUTDOWN
- Operates up to 128 kbps—Lap-Link® Compatible
- 4V/µs minimum Slew Rate guaranteed
- ESD rating of 3 kV on all pins (H, B, M)
- Available in 28-lead SSOP EIAJ Type II package
- Only four 0.1 µF capacitors required for the DC-DC converter

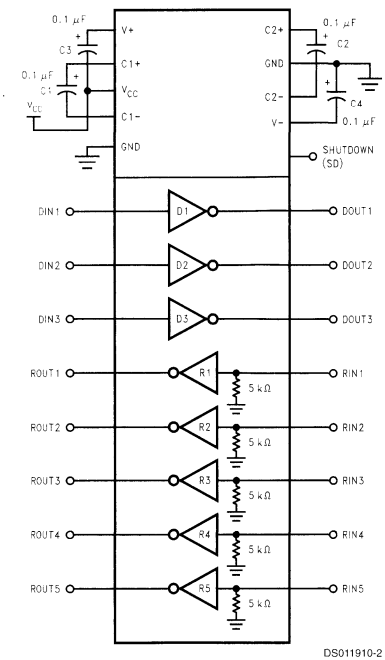
8

Connection Diagram



Order Number DS14C535MSA
See NS Package Number MSA28

Functional Diagram



National Semiconductor

DS14185
EIA/TIA-232 3 Driver x 5 Receiver

General Description

The DS14185 is a three driver, five receiver device which conforms to the EIA/TIA-232-E standard.

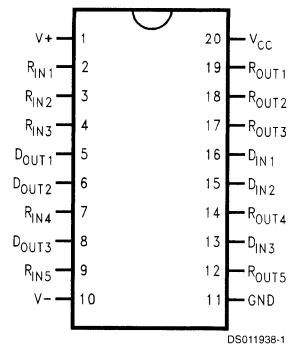
The flow-through pinout facilitates simple non-crossover board layout. The DS14185 provides a one-chip solution for the common 9-pin serial RS-232 interface between data terminal and data communications equipment.

Features

- Replaces one 1488 and two 1489s
- Conforms to EIA/TIA-232-E
- 3 drivers and 5 receivers
- Flow through pinout
- Failsafe receiver outputs
- 20-pin SOIC package
- LapLink® compatible −200 kbps data rate

Connection Diagram

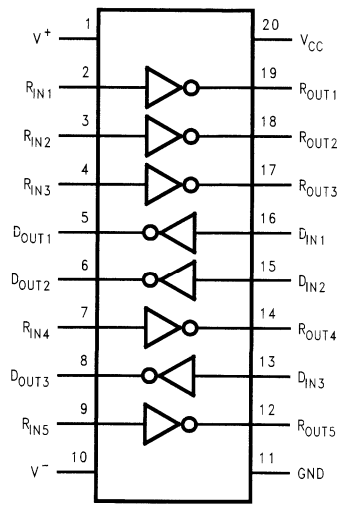
SOIC



DS011938-1

Order Number DS14185WM
See NS Package M20B

Functional Diagram



DS011938-2

National Semiconductor

DS14196
EIA/TIA-232 5 Driver x 3 Receiver

General Description

The DS14196 is a five driver, three receiver device which conforms to the EIA/TIA-232-E and the ITU-T V.28 standards.

The flow-through pinout facilitates simple non-crossover board layout. The DS14196 provides a peripheral side one-chip solution for the common 9-pin serial RS-232 interface between data terminals and data communications equipment.

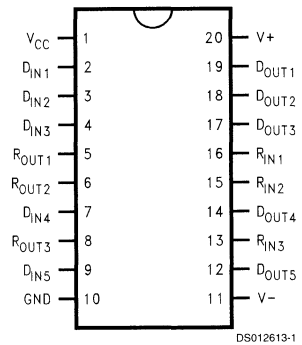
The DS14196 offers optimum performance when used with the DS14185 3 x 5 Driver/Receiver, a host side one-chip solution for the common 9-pin serial RS-232 interface between data terminals and data communications equipment.

Features

- Replaces two 1488s and one 1489
- Conforms to EIA/TIA-232-E and ITU-T V.28
- 5 drivers and 3 receivers
- Flow-through pinout
- Failsafe receiver outputs high when inputs open
- 20-pin wide SOIC package
- LapLink® compatible — 230.4 kbps data rate
- Pin compatible with: SN75196, GD75323

Connection Diagram

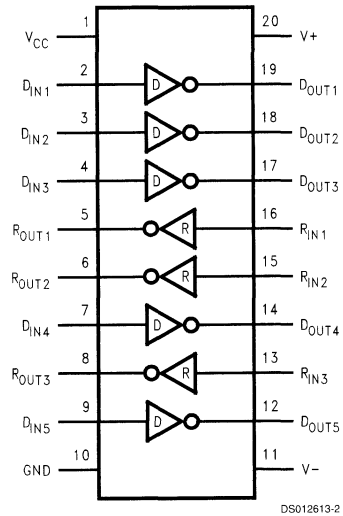
SOP



DS012613-1

Order Number DS14196WM
See NS Package Number M20B

Functional Diagram



DS012613-2

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National Semiconductor

DSV14196
+3.3V Supply EIA/TIA-232 5 Driver x 3 Receiver

General Description

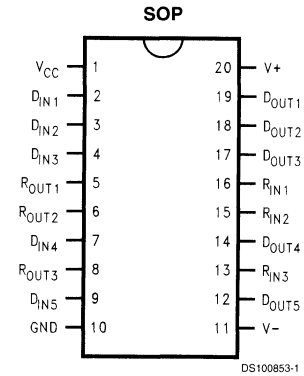
The DSV14196/DSV14196T is a five driver, three receiver device which conforms to the EIA/TIA-232-E and the ITU-T V.28 standards.

The flow-through pinout facilitates simple non-crossover board layout. The DSV14196/DSV14196T provides a peripheral side one-chip solution for the common 9-pin serial RS-232 interface between data terminals and data communications equipment.

Features

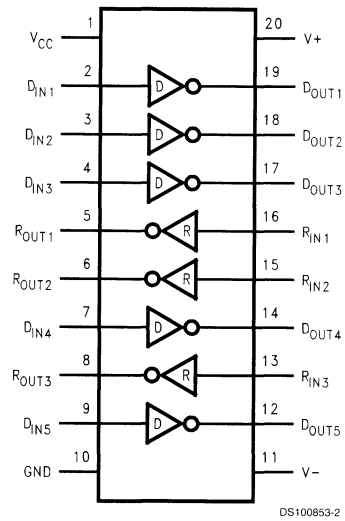
- Conforms to EIA/TIA-232-E and ITU-T V.28
- 5 drivers and 3 receivers
- Flow-through pinout
- Failsafe receiver outputs high when inputs open
- 20-pin wide SOIC package
- LapLink® compatible—230.4 kbps data rate
- +3.3V Logic Interface
- Commercial temperature range option DSV14196 (0°C to 70°C)
- Industrial temperature range option DSV14196T (−40°C to +85°C)

Connection Diagram



Order Number DSV14196WM,DSV14196TWM
See NS Package Number M20B

Functional Diagram



National Semiconductor

DS1691A/DS3691
(RS-422/RS-423) Line Drivers with TRI-STATE® Outputs

General Description

The DS1691A/DS3691 are low power Schottky TTL line drivers designed to meet the requirements of EIA standards RS-422 and RS-423. They feature 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 single-ended line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to slow the rise time for suppression of near end crosstalk to other receivers in the cable. Rise time capacitors are primarily intended for waveshaping output signals in the single-ended driver mode. Multipoint applications in differential mode with waveshaping capacitors is not allowed.

With the mode select pin low, the DS1691A/DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

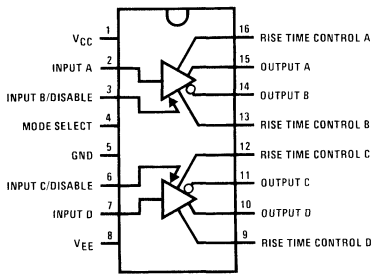
Features

- Dual RS-422 line driver with mode pin low, or quad RS-423 line driver with mode pin high
- TRI-STATE outputs in RS-422 mode
- Short circuit protection for both source and sink outputs
- Outputs will not clamp line with power off or in TRI-STATE
- 100Ω transmission line drive capability
- Low I_{CC} and I_{EE} power consumption
  RS-422: I_{CC} = 9 mA/driver typ
  RS-423: I_{CC} = 4.5 mA/driver typ:
  I_{EE} = 2.5 mA/driver typ
- Low current PNP inputs compatible with TTL, MOS and CMOS
- Pin compatible with AM26LS30

8

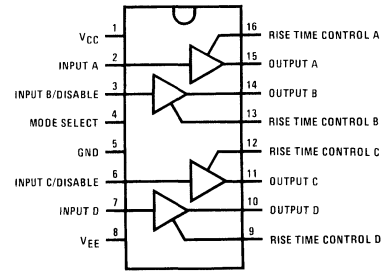
Connection Diagrams

With Mode Select LOW
(RS-422 Connection)



Top View

With Mode Select HIGH
(RS-423 Connection)



Top View

Ordering Information

Order Number	Package Type	NS Package Number
DS3691M	SO Package	M16A
DS3691N	Molded DIP	N16E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.		
DS1691AJ/883	Ceramic DIP	J16A

National Semiconductor

DS26C31T/DS26C31M
CMOS Quad TRI-STATE® Differential Line Driver

General Description

The DS26C31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken (Note 8). This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

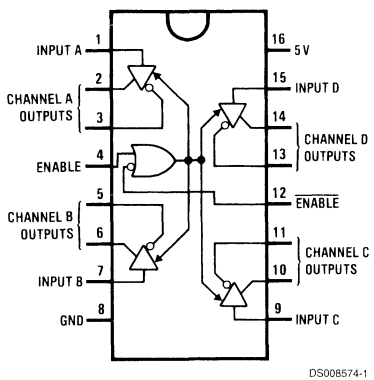
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs will not load line when V_{CC} = 0V
- DS26C31T meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount
- Mil-Std-883C compliant

Connection Diagrams

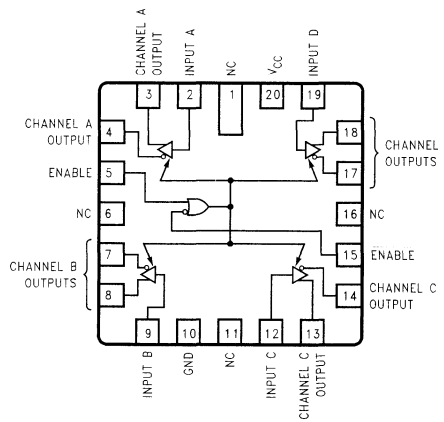
Dual-In-Line Package



DS008574-1

Top View
Order Number DS26C31TM or DS26C31TN
See NS Package Number M16A or N16E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26C31ME/883, DS26C31MJ/883 or DS26C31MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier (E)



DS008574-12

ENABLE	$\overline{\text{ENABLE}}$	Input	Non-Inverting Output	Inverting Output
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE (high impedance)

National Semiconductor

DS26LV31T
3V Enhanced CMOS Quad Differential Line Driver

General Description

The DS26LV31T is a high-speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV31T features low static I_{CC} of 100 µA MAX which makes it ideal for battery powered and power conscious applications.

Differential outputs have the same V_{OD} guarantee (≥2V) as the 5V version.

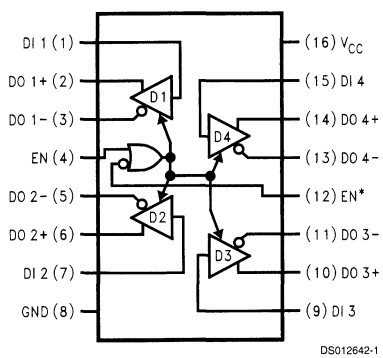
The EN and EN* inputs allow active Low or active High control of the TRI-STATE® outputs. The enables are common to all four drivers. Protection diodes protect all the driver inputs against electrostatic discharge. Outputs have enhanced ESD protection providing greater than 7 kV tolerance. The driver and enable inputs (DI, EN, EN*) are compatible with low voltage LVTTL and LVCMOS devices.

Features

- Industrial product meets TIA/EIA-422-B (RS-422) and ITU-T V.11 recommendation
- Military product conforms to TIA/EIA-422-B (RS-422)
- Interoperable with existing 5V RS-422 networks
- Industrial and Military temperature range
- Guaranteed V_{OD} of 2V min over operating conditions
- Balanced output crossover for low EMI (typical within 40 mV of 50% voltage level)
- Low power design (330 µW @ 3.3V static)
- ESD ≥ 7 kV on cable I/O pins (HBM)
- Guaranteed AC parameter:
  — Maximum driver skew: 2 ns
  — Maximum transition time: 10 ns
- Pin compatible with DS26C31
- Available in SOIC and Cerpack packaging
- Standard Microcircuit Drawing (SMD) 5962-98584

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS26LV31TM or DS26LV31W
See NS Package Number M16A or W16A

Enables		Input	Outputs	
EN	EN*	DI	DO+	DO−
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE

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National Semiconductor

DS26F31M
Quad High Speed Differential Line Drivers

General Description

The DS26F31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26F31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The DS26F31 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F31 features lower power, extended temperature range, and improved specifications.

The circuit provides an enable and disable function common to all four drivers. The DS26F31M features TRI-STATE® outputs and logical OR-ed complementary enable inputs. The inputs are all LS compatible and are all one unit load.

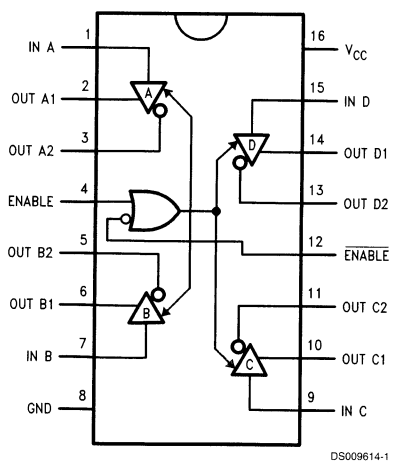
The DS26F31M offers optimum performance when used with the DS26F32 Quad Differential Line Receiver.

Features

- Military temperature range
- Output skew—2.0 ns typical
- Input to output delay—10 ns
- Operation from single +5.0V supply
- 16-lead ceramic DIP Package
- Outputs won't load line when V_{CC} = 0V
- Output short circuit protection
- Meets the requirements of EIA standard RS-422
- High output drive capability for 100Ω terminated transmission lines

Connection and Logic Diagrams

16-Lead Dual-In-Line Package



Top View
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26F31ME/883, DS26F31MJ/883, or DS26F31MW/883
See NS Package Numbers E20A, J16A, or W16A

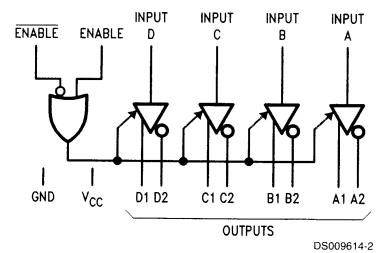
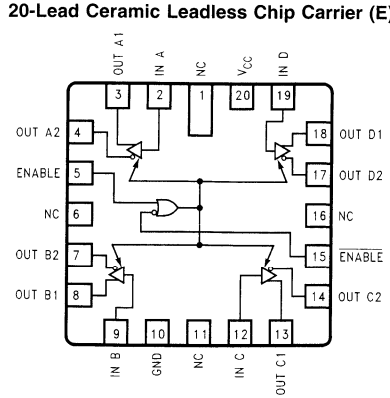


FIGURE 1. Logic Symbol

20-Lead Ceramic Leadless Chip Carrier (E)



National Semiconductor

DS26LS31C/DS26LS31M
Quad High Speed Differential Line Driver

General Description

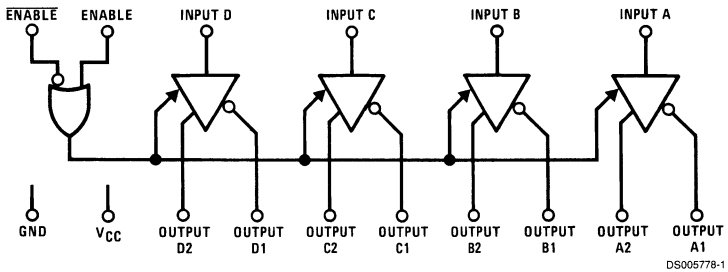
The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE ® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

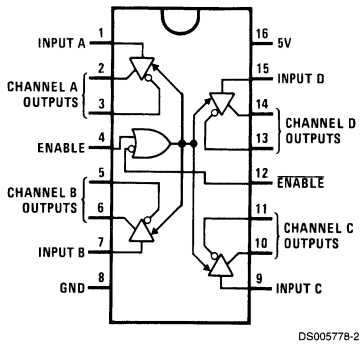
Features

- Output skew—2.0 ns typical
- Input to output delay—10 ns typical
- Operation from single 5V supply
- Outputs won't load line when V_{CC} = 0V
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range

Logic and Connection Diagrams



Dual-In-Line Package



Top View
Order Number DS26LS31CM, or DS26LS31CN
See NS Package M16A or N16E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26LS31MJ/883, DS26LS31ME/883 or DS26LS31MW/883
See NS Package E20A, J16A or W16A

National Semiconductor

DS26C32AT/DS26C32AM
Quad Differential Line Receiver

General Description

The DS26C32A is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

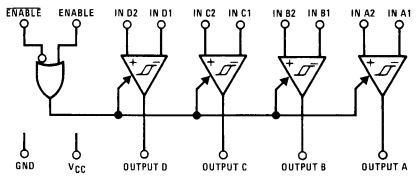
The DS26C32A has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. The DS26C32A features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

The DS26C32A provides an enable and disable function common to all four receivers, and features TRI-STATE ® outputs with 6 mA source and sink capability. This product is pin compatible with the DS26LS32A and the AM26LS32.

Features

- CMOS design for low power
- ±0.2V sensitivity over input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for connection to system buses
- Available in Surface Mount
- Mil-Std-883C compliant

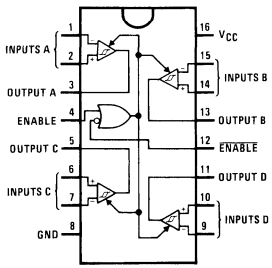
Logic Diagram



DS008764-1

Connection Diagrams

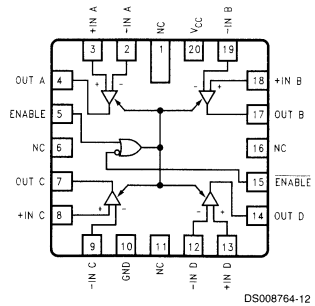
Dual-In-Line Package



DS008764-2

Top View
Order Number DS26C32ATM or DS26C32ATN
See NS Package M16A or N16E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26C32AME/883, DS26C32AMJ/883 or DS26C32AMW/883
See NS Package E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



DS008764-12

National Semiconductor

DS26LV32AT
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS26LV32A is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS26LV32AT features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The TRI-STATE® enables, EN and EN*, allow the device to be active High or active Low. The enables are common to all four receivers.

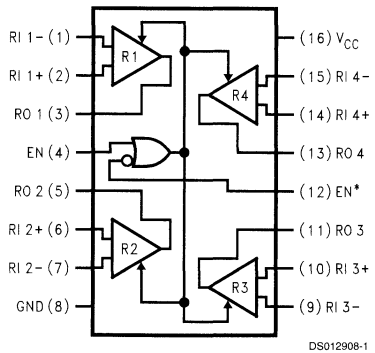
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±10V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Features

- Low Power CMOS design (30 mW typical)
- Interoperable with existing 5V RS-422 networks
- Industrial and Military Temperature Range
- Conforms to TIA/EIA-422-B (RS-422) and ITU-T V.11 Recommendation
- 3.3V Operation
- ±7V Common Mode Range @ V_{ID} = 3V
- ±10V Common Mode Range @ V_{ID} = 0.2V
- Receiver OPEN input failsafe feature
- Guaranteed AC Parameter:
  Maximum Receiver Skew: 4 ns
  Maximum Transition Time: 10 ns
- Pin compatible with DS26C32AT
- 32 MHz Toggle Frequency
- > 6.5k ESD Tolerance (HBM)
- Available in SOIC and Cerpack Packaging
- Standard Microcircuit Drawing (SMD) 5962-98585

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS26LV32ATM or DS26LV32AW
See NS Package Number M16A or W16A

Enables		Inputs	Output
EN	EN*	RI+−RI−	RO
L	H	X	Z
All Other Combinations of Enable Inputs		$V_{ID} \geq +0.2V$	H
		$V_{ID} \leq -0.2V$	L
		Open÷	H

÷ Open, not terminated
L = Logic Low
H = Logic High
X = Irrelevant
Z = TRI-STATE

National Semiconductor

DS26F32M
Quad Differential Line Receivers

General Description

The DS26F32 is a quad differential line receiver designed to meet the requirements of EIA Standards RS-422 and RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26F32 offers improved performance due to the use of state-of-the-art L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by utilizing extremely short gate delay times. Thus, the DS26F32 features lower power, extended temperature range, and improved specifications.

The device features an input sensitivity of 200 mV over the input common mode range of ±7.0V. The DS26F32 provides an enable function common to all four receivers and TRI-STATE ® outputs with 8.0 mA sink capability. Also, a fail-safe input/output relationship keeps the outputs high when the inputs are open.

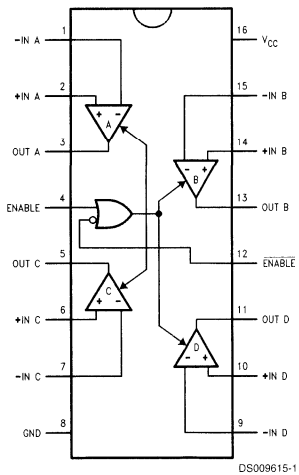
The DS26F32 offers optimum performance when used with the DS26F31 Quad Differential Line Driver.

Features

- Military temperature range
- Input voltage range of ±7.0V (differential or common mode) ±0.2V sensitivity over the input voltage range
- Meets all the requirements of EIA standards RS-422 and RS-423
- High input impedance (18k typical)
- 30 mV input hysteresis
- Operation from single +5.0V supply
- Input pull-down resistor prevents output oscillation on unused channels
- TRI-STATE outputs, with choice of complementary enables, for receiving directly onto a data bus
- Propagation delay 15 ns typical

Connection Diagrams

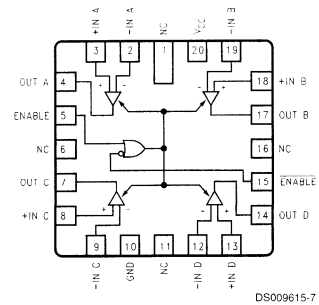
16-Lead DIP



DS009615-1

Top View
See NS Package Number J16A
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26F32ME/883, DS26F32MJ/883 or DS26F32MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



DS009615-7

Function Table

(Each Receiver)

Differential Inputs	Enables		Outputs
$V_{ID} = (V_{IN}+) - (V_{IN}-)$	E	$\overline{E}$	OUT
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	H	Z

H = High Level
L = Low Level
X = Immaterial

National Semiconductor

DS26LS32AC/DS26LS32C/DS26LS32M/DS26LS33M Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 have an input sensitivity of 500 mV over the input voltage range of ±15V.

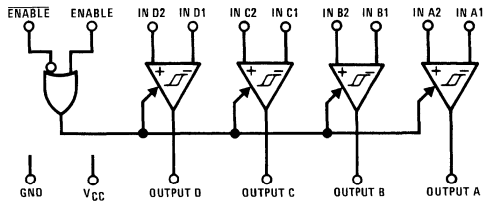
The DS26LS32A differ in function from the popular DS26LS32 and DS26LS33 in that input pull-up and pull-down resistors are included which prevent output oscillation on unused channels.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE ® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commerical operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ±7V on the DS26LS32 and DS26LS32A and ±15V on the DS26LS33
- ±0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ±0.5V sensitivity on the DS26LS33
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33
- Operation from a single 5V supply
- TRI-STATE outputs, with choice of complementary output enables for receiving directly onto a data bus

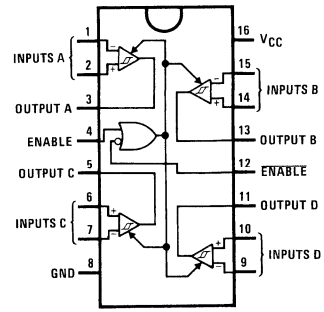
Logic Diagram



DS005255-1

Connection Diagrams

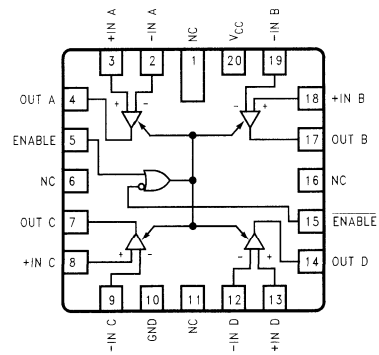
Dual-In-Line Package



DS005255-2

Top View
Order Number DS26LS32CM, DS26LS32CN, DS26LS32ACM, DS26LS32ACN, DS26LS33ACM or DS26LS33ACN
See NS Package Number M16A or N16E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS26LS32MJ/883, DS26LS32MW/883, DS26LS32ME/883, DS26LS33MW/883
See NS Package Number E20A, J16A or W16A

20-Lead Ceramic Leadless Chip Carrier



DS005255-12

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0

Hi-Z = TRI-STATE®
Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

National Semiconductor

DS34C86T
Quad CMOS Differential Line Receiver

General Description

The DS34C86T is a quad differential line receiver designed to meet the RS-422, RS-423, and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission, while retaining the low power characteristics of CMOS.

The DS34C86T has an input sensitivity of 200 mV over the common mode input voltage range of ±7V. Hysteresis is provided to improve noise margin and discourage output instability for slowly changing input waveforms.

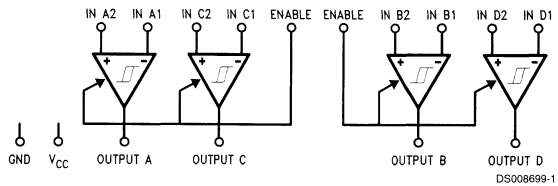
The DS34C86T features internal pull-up and pull-down resistors which prevent output oscillation on unused channels.

Separate enable pins allow independent control of receiver pairs. The TRI-STATE® outputs have 6 mA source and sink capability. The DS34C86T is pin compatible with the DS3486.

Features

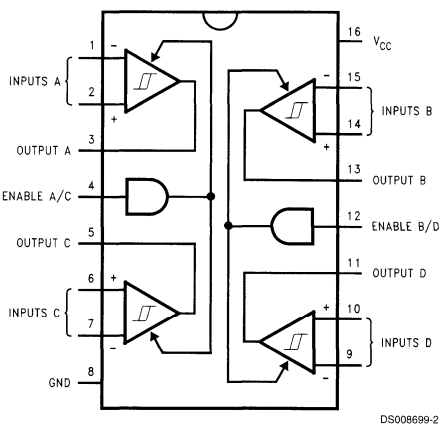
- CMOS design for low power
- ±0.2V sensitivity over the input common mode voltage range
- Typical propagation delays: 19 ns
- Typical input hysteresis: 60 mV
- Inputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- TRI-STATE outputs for system bus compatibility
- Available in surface mount
- Open input Failsafe feature, output high for open input

Logic Diagram



Connection Diagram

Dual-In-Line Package



Top View
Order Number DS34C86TM, and DS34C86TN
See NS Package Number M16A and N16E

Enable	Input	Output
L	X	Z
H	$V_{ID} \geq V_{TH}$ (Max)	H
H	$V_{ID} \leq V_{TH}$ (Min)	L
H	Open*	H

*Open, not terminated
Z = TRI-STATE

National Semiconductor

DS34LV86T
3V Enhanced CMOS Quad Differential Line Receiver

General Description

The DS34LV86T is a high speed quad differential CMOS receiver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV86T features typical low static I_{CC} of 9 mA which makes it ideal for battery powered and power conscious applications. The TRI-STATE® enables, EN, allow the device to be disabled when not in use to minimize power consumption. The dual enable scheme allows for flexibility in turning receivers on and off.

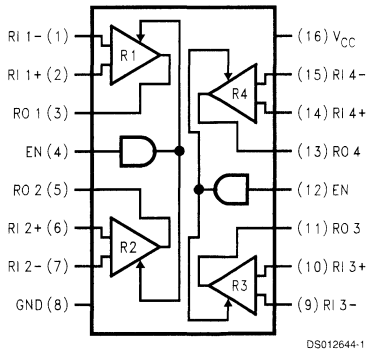
The receiver output (RO) is guaranteed to be High when the inputs are left open. The receiver can detect signals as low as ±200 mV over the common mode range of ±10V. The receiver outputs (RO) are compatible with TTL and LVCMOS levels.

Features

- Low power CMOS design (30 mW typical)
- Interoperable with existing 5V RS-422 networks
- Industrial temperature range
- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 recommendation
- 3.3V Operation
- ±7V common mode range @ V_{ID} = 3V
- ±10V common mode range @ V_{ID} = 0.2V
- Receiver OPEN input failsafe feature
- Guaranteed AC parameter:
  Maximum Receiver Skew: 4 ns
  Transition time: 10 ns
- Pin compatible with DS34C86T
- 32 MHz Toggle Frequency
- >6.5k ESD Tolerance (HBM)
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS34LV86TM
See NS Package Number M16A

Enable EN	Inputs RI+−RI−	Output RO
L	X	Z
H	$V_{ID} \geq +0.2V$	H
H	$V_{ID} \leq -0.2V$	L
H	Open[÷]	H

L = Logic Low
H = Logic High
X = Irrelevant
Z = TRI-STATE
÷ = Open, Not Terminated

National Semiconductor

DS3486
Quad RS-422, RS-423 Line Receiver

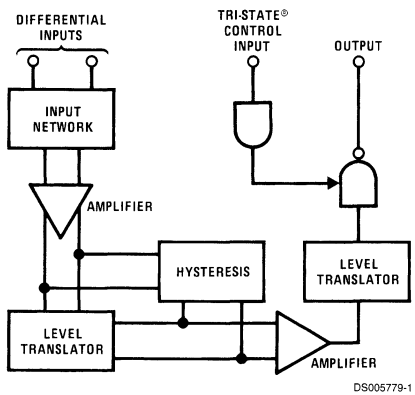
General Description

National's quad RS-422, RS-423 receiver features four independent receivers which comply with EIA Standards for the electrical characteristics of balanced/unbalanced voltage digital interface circuits. Receiver outputs are 74LS compatible, TRI-STATE® structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. A PNP device buffers each output control pin to assure minimum loading for either logic one or logic zero inputs. In addition, each receiver has internal hysteresis circuitry to improve noise margin and discourage output instability for slowly changing input waveforms.

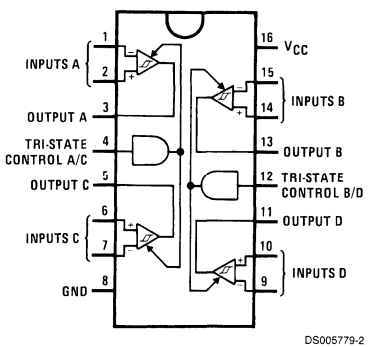
Features

- Four independent receivers
- TRI-STATE outputs
- Internal hysteresis −140 mV (typ)
- Fast propagation times −19 ns (typ)
- TTL compatible outputs
- 5V supply
- Pin compatible and interchangeable with MC3486

Block and Connection Diagrams



Dual-In-Line Package



Top View
Order Number DS3486M or DS3486N
See NS Package Number M16A or N16E

National Semiconductor

DS34C87T
CMOS Quad TRI-STATE Differential Line Driver

General Description

The DS34C87T is a quad differential line driver designed for digital data transmission over balanced lines. The DS34C87T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS34C87T accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the individual drivers to power down without loading down the bus. This device has separate enable circuitry for each pair of the four drivers. The DS34C87T is pin compatible to the DS3487T.

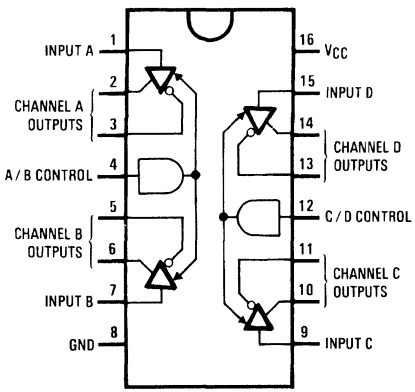
All inputs are protected against damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delays: 6 ns
- Typical output skew: 0.5 ns
- Outputs won't load line when V_{CC} = 0V
- Meets the requirements of EIA standard RS-422
- Operation from single 5V supply
- TRI-STATE outputs for connection to system buses
- Low quiescent current
- Available in surface mount

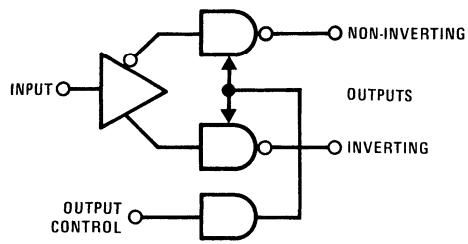
Connection and Logic Diagrams

Dual-In-Line Package



DS008576-1

Top View
Order Number DS34C87TM or DS34C87TN
See NS Package Number M16A or N16E



DS008576-2

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE (high performance)

National Semiconductor

DS34LV87T
Enhanced CMOS Quad Differential Line Driver

General Description

The DS34LV87T is a high speed quad differential CMOS driver that meets the requirements of both TIA/EIA-422-B and ITU-T V.11. The CMOS DS34LV87T features low static I_{CC} of 100 µA max which makes it ideal for battery powered and power conscious applications. The TRI-STATE® enable, EN, allows the device to be disabled when the device is not in use to minimize power. The dual enable scheme allows for flexibility in turning devices on or off.

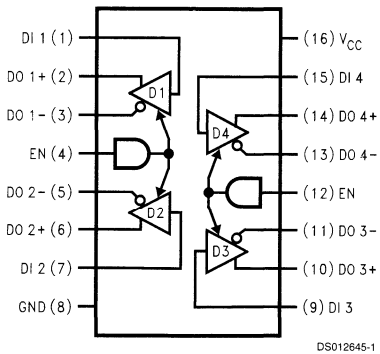
Protection diodes protect all the driver inputs against electrostatic discharge. The driver and enable inputs (DI and EN) are compatible with LVTTL and LVCMOS devices. Differential outputs have the same V_{OD} (≥2V) guarantee as the 5V version. The outputs have enhanced ESD Protection providing greater than 7 kV tolerance.

Features

- Meets TIA/EIA-422-B (RS-422) and ITU-T V.11 recommendation
- Interoperable with existing 5V RS-422 networks
- Guaranteed V_{OD} of 2V min over operating conditions
- Balanced output crossover for low EMI (typical within 40 mV of 50% voltage level)
- Low power design (330 µW @ 3.3V static)
- ESD ≥ 7 kV on cable I/O pins (HBM)
- Industrial temperature range
- Guaranteed AC parameter:
  — Maximum driver skew: 2 ns
  — Maximum transition time: 10 ns
- Pin compatible with DS26C31
- Available in SOIC packaging

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS34LV87TM
See NS Package Number M16A

Truth Table

Enables	Input	Outputs	
EN	DI	DO+	DO−
L	X	Z	Z
H	H	H	L
H	L	L	H

L = Low logic state
X = Irrelevant
H = High logic state
Z = TRI-STATE

8

National Semiconductor

DS3487
Quad TRI-STATE® Line Driver

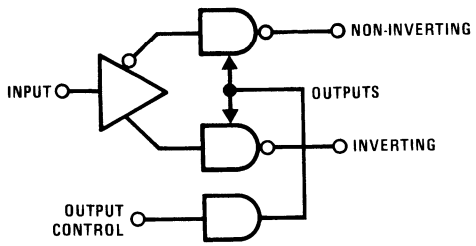
General Description

National's quad RS-422 driver features four independent drivers which comply with EIA Standards for the electrical characteristics of balanced voltage digital interface circuits. The outputs are TRI-STATE structures which are forced to a high impedance state when the appropriate output control pin reaches a logic zero condition. All input pins are PNP buffered to minimize input loading for either logic one or logic zero inputs.

Features

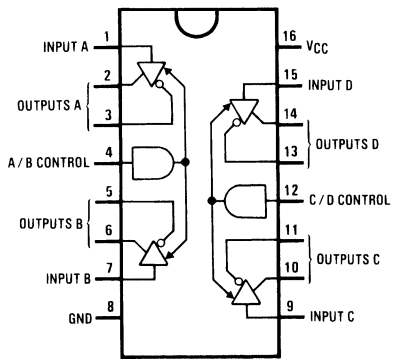
- Four independent drivers
- TRI-STATE ® outputs
- Fast propagation times (typ 10 ns)
- TTL compatible
- 5V supply
- Output rise and fall times less than 15 ns
- Pin compatible with DS8924 and MC3487

Block and Connection Diagrams



DS005780-1

Dual-In-Line Package



DS005780-2

Top View
Order Number DS3487M or DS3487N
See NS Package Number M16A or N16E

Input	Control Input	Non-Inverting Output	Inverting Output
H	H	H	L
L	H	L	H
X	L	Z	Z

L = Low logic state
H = High logic state
X = Irrelevant
Z = TRI-STATE(high impedance)

National Semiconductor

DS78C20/DS88C20
Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

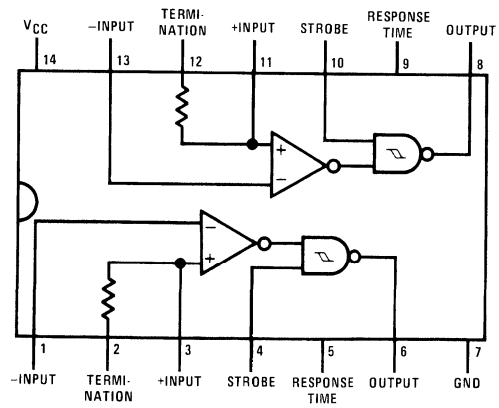
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

Features

- Meets requirements of EIA Standards RS-232-C RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- ½ V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- DS7830/DS8830 recommended driver

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS88C20N
See NS Package Numbers N14A
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS78C20J/883
See NS Package Number J14A

National Semiconductor

DS78C120
Dual CMOS Compatible Differential Line Receiver

General Description

The DS78C120 is a high performance, dual differential, CMOS compatible line receiver for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

Input specifications meet or exceed those of the popular DS7820 line receiver.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

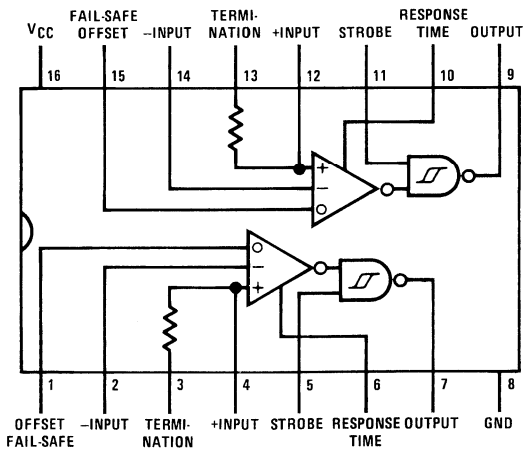
Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes a 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78C120 is specified over a −55°C to +125°C temperature range.

Features

- Full compatibility with EIA Standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k typical input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V
- Separate fail-safe mode

Connection Diagram

Dual-In-Line Package



Top View
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS78C120J/883
See NS Package Number J16A

National Semiconductor

DS78LS120
Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

General Description

The DS78LS120 is a high performance, dual differential, TTL compatible line receiver for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range.

Input specifications meet or exceed those of the popular DS7820 line receiver.

Features

- Meets EIA standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50mV input hysteresis
- 200mV input threshold
- Separate fail-safe mode

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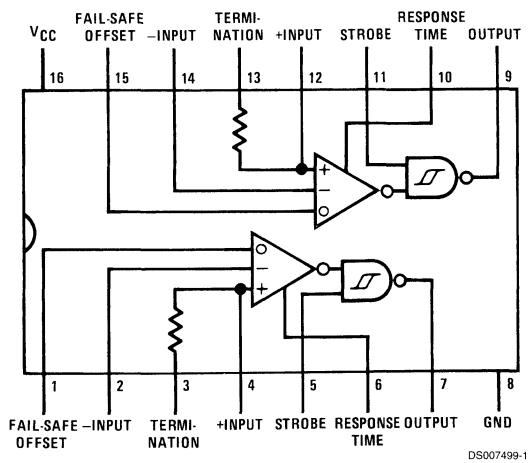
Connection Diagram

Dual-In-Line-Package



Top View
see RETS Data Sheet.
Order Number DS78LS120J/883 or DS78LS120W/883
See NS Package Number J16A or W16A

National Semiconductor

DS8921/DS8921A/DS8921AT
Differential Line Driver and Receiver Pair

General Description

The DS8921, DS8921A are Differential Line Driver and Receiver pairs designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, these devices meet the requirements of the EIA Standard RS-422.

The DS8921, DS8921A receivers offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms.

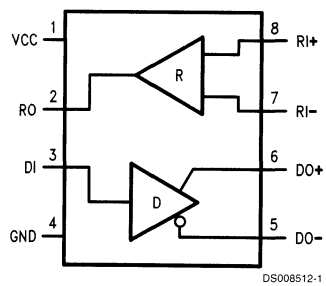
The DS8921, DS8921A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

The DS8921, DS8921A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew - 0.5 ns typical
- Meet the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input hysteresis-70 mV typical
- DS8921AT industrial temperature operation: (−40°C to +85°C)

Connection Diagram



DS008512-1

Order Number DS8921M, DS8921N, DS8921AM, DS8921AN, DS8921ATM, or DS8921ATN
See NS Package Number M08A or N08E

Receiver		Driver		
Input	V_{OUT}	Input	V_{OUT}	$\overline{V_{OUT}}$
$V_{ID} \geq V_{TH}$ (MAX)	1	1	1	0
$V_{ID} \leq V_{TH}$ (MIN)	0	0	0	1
Open	1			

National Semiconductor

DS89C21
Differential CMOS Line Driver and Receiver Pair

General Description

The DS89C21 is a differential CMOS line driver and receiver pair, designed to meet the requirements of TIA/EIA-422-A (RS-422) electrical characteristics interface standard. The DS89C21 provides one driver and one receiver in a minimum footprint. The device is offered in an 8-pin SOIC package.

The CMOS design minimizes the supply current to 6 mA, making the device ideal for use in battery powered or power conscious applications.

The driver features a fast transition time specified at 2.2 ns, and a maximum differential skew of 2 ns making the driver ideal for use in high speed applications operating above 10 MHz.

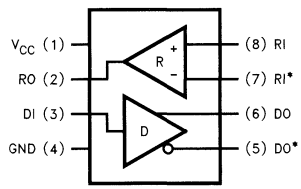
The receiver can detect signals as low as 200 mV, and also incorporates hysteresis for noise rejection. Skew is specified at 4 ns maximum.

The DS89C21 is compatible with TTL and CMOS levels (DI and RO).

Features

- Meets TIA/EIA-422-A (RS-422) and CCITT V.11 recommendation
- LOW POWER design—15 mW typical
- Guaranteed AC parameters:
  - —Maximum driver skew 2.0 ns
  - —Maximum receiver skew 4.0 ns
- Extended temperature range: −40°C to +85°C
- Available in SOIC packaging
- Operates over 20 Mbps
- Receiver OPEN input failsafe feature

Connection Diagram



DS011753-1

Order Number DS89C21TM
See NS Package Number M08A

Driver

Input	Outputs	
DI	**DO**	**DO***
H	H	L
L	L	H

Receiver

Inputs	Output
RI–RI*	**RO**
$V_{DIFF} \geq +200$ mV	H
$V_{DIFF} \leq -200$ mV	L
OPEN†	H

†Non-terminated

8

National Semiconductor

DS8922/DS8922A/DS8923A TRI-STATE® RS-422 Dual Differential Line Driver and Receiver Pairs

General Description

The DS8922/22A and DS8923A are Dual Differential Line Driver and Receiver pairs. These devices are designed specifically for applications meeting the ST506, ST412 and ESDI Disk Drive Standards. In addition, the devices meet the requirements of the EIA Standard RS-422.

These devices offer an input sensitivity of 200 mV over a ±7V common mode operating range. Hysteresis is incorporated (typically 70 mV) to improve noise margin for slowly changing input waveforms. An input fail-safe circuit is provided such that if the receiver inputs are open the output assumes the logical one state.

The DS8922A and DS8923A drivers are designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. Complementary outputs are logically ANDed and provide an output skew of 0.5 ns (typ.) with propagation delays of 12 ns.

Both devices feature TRI-STATE outputs. The DS8922/22A have independent control functions common to a driver and receiver pair. The DS8923A has separate driver and receiver control functions.

Power up/down circuitry is featured which will TRI-STATE the outputs and prevent erroneous glitches on the transmission lines during system power up or power down operation.

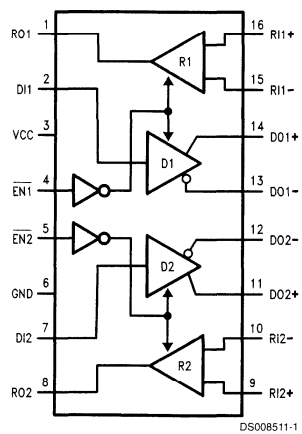
The DS8922/22A and DS8923A are designed to be compatible with TTL and CMOS.

Features

- 12 ns typical propagation delay
- Output skew—±0.5 ns typical
- Meets the requirements of EIA Standard RS-422
- Complementary Driver Outputs
- High differential or common-mode input voltage ranges of ±7V
- ±0.2V receiver sensitivity over the input voltage range
- Receiver input fail-safe circuitry
- Receiver input hysteresis—70 mV typical
- Glitch free power up/down
- TRI-STATE outputs

Connection Diagrams

DS8922A Dual-In-Line

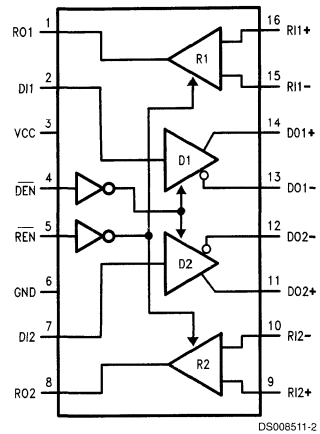


DS008511-1

Order Number DS8922M, DS8922N, DS8922AM or DS8922AN
See NS Package Number M16A or N16E

Connection Diagrams (Continued)

DS8923A Dual-In-Line



DS008511-2

Order Number DS8923AM, DS8923AN,
See NS Package Number M16A or N16E

DS8922/22A

$\overline{EN1}$	$\overline{EN2}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	HI-Z	ACTIVE	HI-Z	ACTIVE
0	1	ACTIVE	HI-Z	ACTIVE	HI-Z
1	1	HI-Z	HI-Z	HI-Z	HI-Z

DS8923A

$\overline{DEN}$	$\overline{REN}$	RO1	RO2	DO1	DO2
0	0	ACTIVE	ACTIVE	ACTIVE	ACTIVE
1	0	ACTIVE	ACTIVE	HI-Z	HI-Z
0	1	HI-Z	HI-Z	ACTIVE	ACTIVE
1	1	HI-Z	HI-Z	HI-Z	HI-Z

National Semiconductor

DS8925
LocalTalk™ Dual Driver/Triple Receiver

General Description

The DS8925 is a dual driver/triple receiver device optimized to provide a single chip solution for a LocalTalk Interface. The device provides one differential TIA/EIA-422 driver, one TIA/EIA-423 single ended driver, one TIA/EIA-422 receiver and two TIA/EIA-423 receivers, all in a surface mount 16 pin package. This device is electrically similar to the 26LS30 and 26LS32 devices.

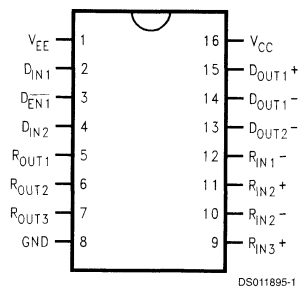
The drivers feature ±10V common mode range, and the differential driver provides TRI-STATEable outputs. The receivers offer ±200 mV thresholds over the ±10V common mode range.

Features

- Single chip solution for LocalTalk port
- Two driver/three receivers per package
- Wide common mode range: ±10V
- ±200 mV receiver sensitivity
- 70 mV typical receiver input hysteresis
- Available in SOIC packaging

Connection Diagram

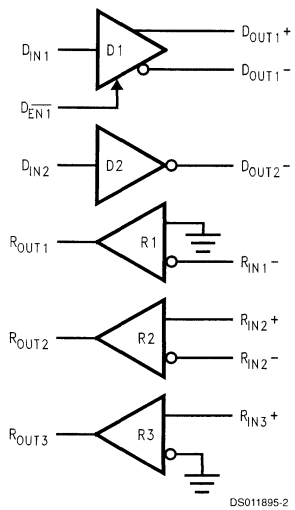
Dual-In-Line Package



DS011895-1

Order Number DS8925M
See NS Package Number M16A

Functional Diagram



DS011895-2

National Semiconductor

DS89C386
Twelve Channel CMOS Differential Line Receiver

General Description

The DS89C386 is a high speed twelve channel CMOS differential receiver that meets the requirements of TIA/EIA-422-B. The DS89C386 features low power dissipation of 240 mW typical.

Each TRI-STATE® enable, EN, allows the receiver output to be active or in a Hi-impedance off state. Each enable is common to only two receivers for flexibility and multiplexing of receiver outputs.

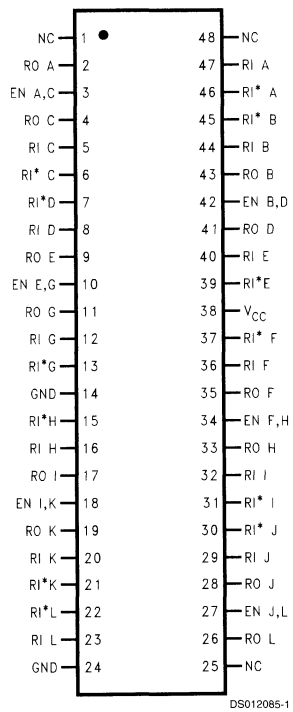
The receiver output (RO) is guaranteed to be High when the inputs are left open and unterminated. The receiver can detect signals as low and including ±200 mV over the common mode range of ±7V. The receiver outputs (RO) are compatible with both TTL and CMOS levels.

Features

- Low power design—240 mW typical
- Meets TIA/EIA-422-B (RS-422)
- Receiver OPEN input failsafe feature
- Guaranteed AC parameters:
  - — Maximum receiver skew –4 ns
  - — Maximum transition time –9 ns
- High Output Drive Capability: ±6 mA
- Available in SSOP packaging:
  - — Requires 30% less PCB space than 3 DS34C86TMs

Connection Diagram

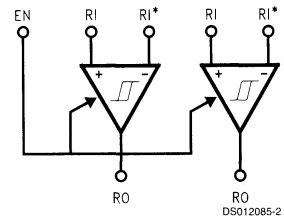
48L SSOP
DS89C386



DS012085-1

Order Number DS89C386TMEA
See NS Package Number MS48A

Function Diagram



DS012085-2

1/6 of package

Enable	Inputs	Output
EN	RI–RI*	RO
L	X	Z
H	≥200 mV or OPEN†	H
H	≤ –200 mV	L
H	+200 mV > and > –200 mV	X

†Not terminated.

National Semiconductor

DS89C387
Twelve Channel CMOS Differential Line Driver

General Description

The DS89C387 is a high speed twelve channel CMOS differential driver that meets the requirements of TIA/EIA-422-B. The DS89C387 features a low I_{CC} specification of 1.5 mA maximum, which makes it ideal for battery powered and power conscious applications. The device replaces three DS34C87s and offers a PC board space savings up to 30%. The twelve channel driver is available in a SSOP package. The device is ideal for wide parallel bus applications.

Each TRI-STATE® enable (EN) allows the driver outputs to be active or in a HI-impedance off state. Each enable is common to only two drivers for flexibility and control. The drivers may be disabled to turn off load current and to save power when data is not being transmitted.

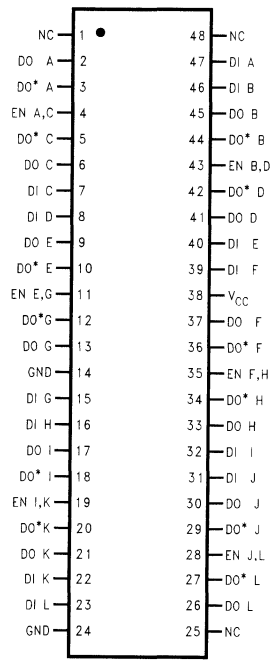
The driver's input (DI) is compatible with both TTL and CMOS signal levels.

Features

- Low power I_{CC}: 1.5 mA maximum
- Meets TIA/EIA-422-B (RS-422)
- Guaranteed AC parameters:
  - — Maximum driver skew −3 ns
  - — Maximum transition time −10 ns
- Available in SSOP packaging:
  - — Requires 30% less PCB space than 3 DS34C87TMs

Connection Diagram

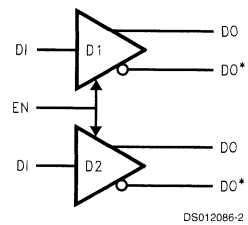
48L SSOP
DS89C387



DS012086-1

Order Number DS89C387TMEA
See NS Package Number MS48A

Functional Diagram



DS012086-2

1/6 of package

Enable	Input	Outputs	
EN	DI	DO	DO*
L	X	Z	Z
H	H	H	L
H	L	L	H

National Semiconductor

DS9636A
RS-423 Dual Programmable Slew Rate Line Driver

General Description

The DS9636A is a TTL/CMOS compatible, dual, single ended line driver which has been specifically designed to satisfy the requirements of EIA Standard RS-423.

The DS9636A is suitable for use in digital data transmission systems where signal wave shaping is desired. The output slew rates are jointly controlled by a single external resistor connected between the wave shaping control lead (WS) and ground. This eliminates any need for external filtering of the output signals. Output voltage levels and slew rates are independent of power supply variations. Current-limiting is provided in both output states. The DS9636A is designed for nominal power supplies of ±12V.

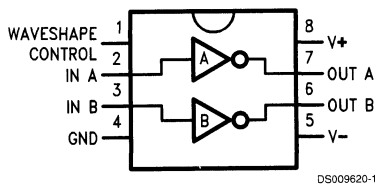
Inputs are TTL compatible with input current loading low enough (1/10 UL) to be also compatible with CMOS logic. Clamp diodes are provided on the inputs to limit transients below ground.

Features

- Programmable slew rate limiting
- Meets EIA Standard RS-423
- Commercial or extended temperature range
- Output short circuit protection
- TTL and CMOS compatible inputs

Connection Diagram

8-Lead DIP



DS009620-1

Top View
Order Number DS9636ACN,
See NS Package Number N08E
For Complete Military Product Specifications,
refer to the appropriate SMD or MDS.
Order Number DS9636AJ/883
See NS Package Number J08A

National Semiconductor

DS9637A
Dual Differential Line Receiver

General Description

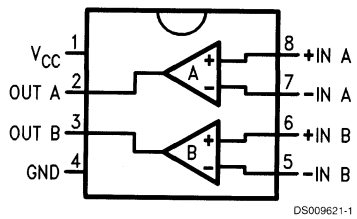
The DS9637A is a Schottky dual differential line receiver which has been specifically designed to satisfy the requirements of EIA Standards RS-422 and RS-423. In addition, the DS9637A satisfies the requirements of MIL-STD 188-114 and is compatible with the International Standard CCITT recommendations. The DS9637A is suitable for use as a line receiver in digital data systems, using either single ended or differential, unipolar or bipolar transmission. It requires a single 5V power supply and has Schottky TTL compatible outputs. The DS9637A has an operational input common mode range of ±7V either differentially or to ground.

Features

- Dual channel
- Single 5V supply
- Satisfies EIA standards RS-422 and RS423
- Built-in ±35 mV hysteresis
- High input common mode voltage range
- High input impedance
- TTL compatible outputs
- Schottky technology
- Extended temperature range

Connection Diagram

8–Lead DIP and SO-8 Package



Top View
Order Number DS9637ACM or DS9637ACN
See NS Package Number M08A or N08E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS9637AMJ/883
See NS Package Number J08A

National Semiconductor

DS9638
RS-422 Dual High Speed Differential Line Driver

General Description

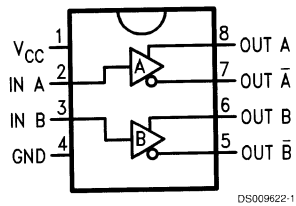
The DS9638 is a Schottky, TTL compatible, dual differential line driver designed specifically to meet the EIA Standard RS-422 specifications. It is designed to provide unipolar differential drive to twisted pair or parallel wire transmission lines. The inputs are TTL compatible. The outputs are similar to totem pole TTL outputs, with active pull-up and pull-down. The device features a short circuit protected active pull-up with low output impedance and is specified to drive 50Ω transmission lines at high speed. The mini-DIP provides high package density.

Features

- Single 5V supply
- Schottky technology
- TTL and CMOS compatible inputs
- Output short circuit protection
- Input clamp diodes
- Complementary outputs
- Minimum output skew (<1.0 ns typical)
- 50 mA output drive capability for 50Ω transmission lines
- Meets EIA RS-422 specifications
- Propagation delay of less than 10 ns
- "Glitchless" differential output
- Delay time stable with V_{CC} and temperature variations (<2.0 ns typical) (*Figure 3*)
- Extended temperature range

Connection Diagram

8-Lead DIP



Top View
Order Number DS9638CM or DS9638CN
See NS Package Number M08A or N08E
For Complete Military Product Specifications, refer to the appropriate SMD or MDS.
Order Number DS9638MJ/883
See NS Package Number J08A

National Semiconductor

DS3883A
BTL 9-Bit Data Transceiver

General Description

The DS3883A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3883A, is a BTL 9-bit Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. Utilization of the DS3883A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

The DS3883A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with its collector to isolate the transistor output capacitance from the bus thus reducing the bus loading in the inactive state. The combined output capacitance of the driver and receiver input is less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. BTL eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.The transceiver's control and driver inputs are designed with high impedance PNP input structures and are fully TTL compatible.

The receiver is a high speed comparator that utilizes a bandgap reference for precision threshold control allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The DS3883A supports live insertion as defined in 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported the LI pin must be tied to the V_{CC} pin. The DS3883A also provides glitch free power up/down protection during power sequencing.

The DS3883A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two logic V_{CC} pins on the DS3883 that provide the supply voltage for the logic and control circuitry. Multiple power pins reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

Additionally, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} + 0.5V.

There are three different types of ground pins on the DS3883A. They are the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

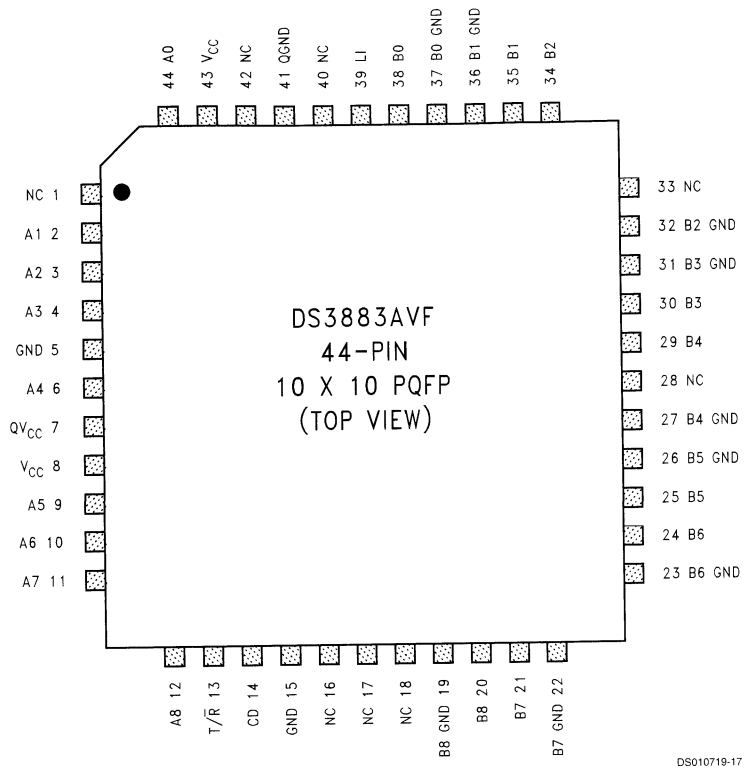
Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3883, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power-up/down sequencing.

When CD (Chip Disable) is high, An and Bn are in a high impedance state. To transmit data (An to Bn) the $T/\overline{R}$ signal is high. To receive data (Bn to An) the $T/\overline{R}$ signal is low.

Features

- 9-bit Inverting BTL transceiver meets IEEE 1194.1 standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low bus-port voltage swing (typically 1V) at 80 mA
- Open collector bus-port output allows Wired-OR
- Controlled rise and fall time to reduce noise coupling
- TTL compatible driver and control inputs
- Built in bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Exceeds 2 kV ESD (Human Body Model)
- Individual bus-port ground pins minimize ground bounce
- Tight skew (1 ns typical)

Connection Diagram



Order Number DS3883AVF
See NS Package Number VF44B

National Semiconductor

DS3884A
BTL Handshake Transceiver

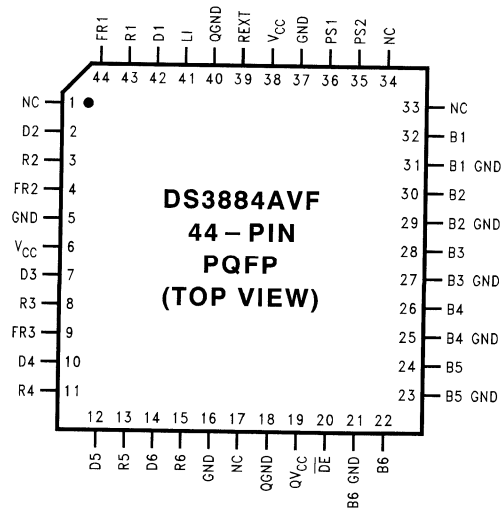
General Description

The DS3884A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3884A is a BTL 6-bit Handshake Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification.

Features

- Fast propagation delay (3 ns typ)
- 6-bit BTL transceiver
- Selective receiver glitch filtering (FR1–FR3)
- Meets 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports live insertion
- Glitch free power-up/down protection
- Typically less than 5 pF bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80 mA
- TTL compatible driver and control inputs
- Separate TTL I/O
- Open collector bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- Built in Bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Exceeds 2 kV ESD testing (Human Body Model)
- Individual Bus-port ground pins
- Product offered in PQFP package styles

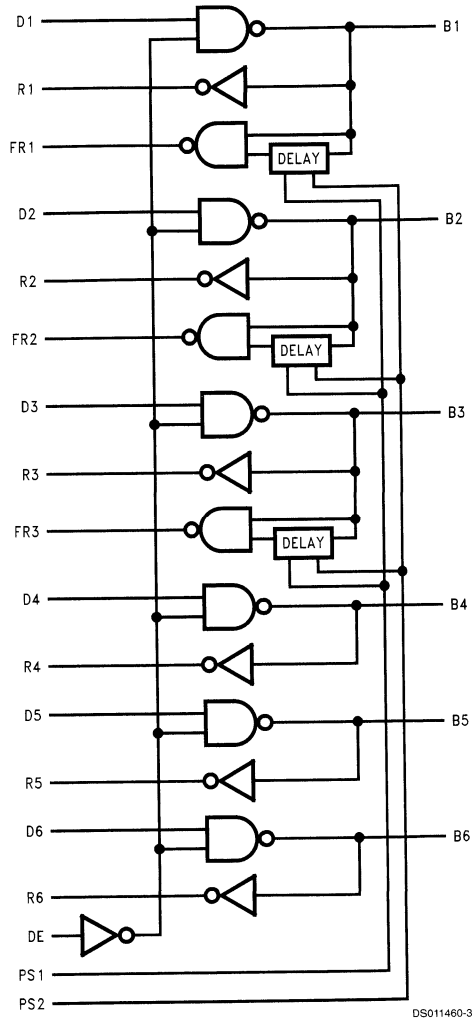
Connection Diagram



DS011460-1

Order Number DS3884AVF
See NS Package VF44B

Logic Diagram



National Semiconductor

DS3886A
BTL 9-Bit Latching Data Transceiver

General Description

The DS3886A is a higher speed, lower power, pin compatible version of the DS3886.

The DS3886A is one in a series of transceivers designed specifically for the implementation of high performance Futurebus+ and proprietary bus interfaces. The DS3886A is a BTL 9-Bit Latching Data Transceiver designed to conform to IEEE 1194.1 (Backplane Transceiver Logic—BTL) as specified in the IEEE 896.2 Futurebus+ specification. The DS3886A incorporates an edge-triggered latch in the driver path which can be bypassed during fall-through mode of operation and a transparent latch in the receiver path. Utilization of the DS3886A simplifies the implementation of byte wide address/data with parity lines and also may be used for the Futurebus+ status, tag and command lines.

The DS3886A driver output configuration is an NPN open collector which allows Wired-OR connection on the bus. Each driver output incorporates a Schottky diode in series with it's collector to isolate the transistor output capacitance from the bus, thus reducing the bus loading in the inactive state. The combined output capacitance of the driver output and receiver input is less than 5 pF. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 1194.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to 2.1V at both ends. The low voltage is typically 1V.

Separate ground pins are provided for each BTL output to minimize induced ground noise during simultaneous switching.

The unique driver circuitry meets the maximum slew rate of 0.5 V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control, allowing maximum noise immunity to the BTL 1V signaling level. Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The output is TRI-STATE® and fully TTL compatible.

The DS3886A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the V_{CC} pin. The DS3886A also provides glitch free power up/down protection during power sequencing.

The DS3886A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two Logic V_{CC} pins on the DS3886A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. As these pins are common to the V_{CC} bus internal to the device, a voltage delta should never exist between these pins and the voltage difference between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn) the $T/\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} +0.5V.

There are three different types of ground pins on the DS3886A; the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

Since many different grounding schemes could be implemented and ESD circuitry exists on the DS3886A, it is important to note that any voltage difference between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power up/down sequencing.

The DS3886A is offered in 44-pin PLCC, and 44-pin PQFP high density package styles.

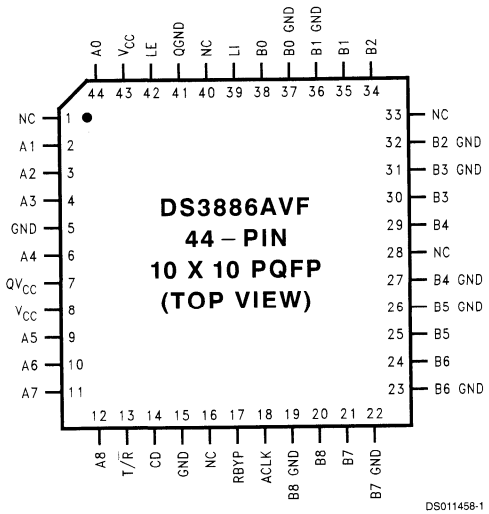
Features

- Fast propagation delay (3ns typ)
- 9-BIT BTL Latched Transceiver
- Driver incorporates edge triggered latches
- Receiver incorporates transparent latches
- Meets IEEE 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Supports Live Insertion
- Glitch free Power-up/down protection
- Typically less than 5 pF Bus-port capacitance
- Low Bus-port voltage swing (typically 1V) at 80 mA
- Exceeds 2 KV ESD testing (Human Body Model)
- Open collector Bus-port outputs allows Wired-OR connection

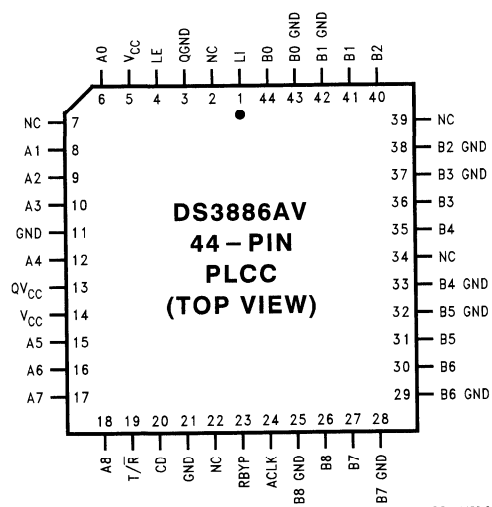
Features (Continued)

- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible Driver and Control inputs
- Built in Bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Individual Bus-port ground pins
- Product offered in PLCC and PQFP package styles
- Tight skew (0.5 ns typical)

Connection Diagrams



DS011458-1



DS011458-2

Order Number DS3886AV, or DS3886AVF
See NS Package Number V44A, or VF44B

National Semiconductor

DS38C86A
CMOS BTL 9-Bit Latching Data Transceiver

General Description

The DS38C86A is a 9-bit BTL Latching Data Transceiver designed specifically for proprietary bus interfaces. The device is implemented in CMOS technology, and delivers all of the performance of its Bi-CMOS counterparts while consuming less then half of the power supply current of the DS3886A. The DS38C86A conforms to the IEEE 11941.1 (Backplane Transceiver Logic - BTL) Standard.

The DS38C86A incorporates an edge-triggered latch in the driver path which can be bypassed during fall-through mode of operation and a transparent latch in the receiver path. The DS38C86A driver output configuration is an open drain which allows Wired-OR connection on the bus. A unique design reduces the bus loading to 3 pF typical. The driver also has high sink current capability to comply with the bus loading requirements defined within IEEE 11941.1 BTL specification.

Backplane Transceiver Logic (BTL) is a signaling standard that was invented and first introduced by National Semiconductor, then developed by the IEEE to enhance the performance of backplane buses. BTL transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. The BTL standard eliminates settling time delays that severely limit TTL bus performance, and thus provide significantly higher bus transfer rates. The backplane bus is intended to be operated with termination resistors (selected to match the bus impedance) connected to a 2.1V at both ends. The low voltage is typically 1V.

The DS38C86A provides an alternative to high power Bipolar and BiCMOS devices with the use of CMOS technology. The CMOS technology enables the DS38C86A to operate at 50% of the I_{CC} required by the Bi-CMOS DS3886A. This can have a major impact on system power consumption. For example, if a backplane is 128 bits wide, 16 devices (9 bits each) required per card. Also assume the backplane is one rack with 20 slots. Power dissipation savings for this application is calculated by the following equation:

$P = I_{CC}$-savings x Power supply voltage x number of devices

$$P = 32 \text{ mA} \times 5.5\text{V} \times 320 = 56 \text{ Watts}$$

The power dissipation savings may increase even more when; the system bus is wider than 128 bits, there are multiple racks in the system, or if the system includes a hot backup. This may double the power dissipation savings.

Separate ground pins are provided for each BTL output minimize induced ground noise during simultaneous switching.

The unique driver circuitry provides a maximum slew rate of 0.9V/ns which allows controlled rise and fall times to reduce noise coupling to adjacent lines.

The transceiver's high impedance control and driver inputs are fully TTL compatible.

The receiver is a high speed comparator that utilizes a Bandgap reference for precision threshold control allowing maximum immunity to the BTL 1V signaling level.

Separate QV_{CC} and QGND pins are provided to minimize the effects of high current switching noise. The receiver output is TRI-STATE® and fully TTL compatible.

The DS38C86A supports live insertion as defined in IEEE 896.2 through the LI (Live Insertion) pin. To implement live insertion the LI pin should be connected to the live insertion power connector. If this function is not supported, the LI pin must be tied to the V_{CC} pin. The DS38C86A also provides glitch free power up/down protection during power sequencing.

The DS38C86A has two types of power connections in addition to the LI pin. They are the Logic V_{CC} (V_{CC}) and the Quiet V_{CC} (QV_{CC}). There are two Logic V_{CC} pins on the DS38C86A that provide the supply voltage for the logic and control circuitry. Multiple connections are provided to reduce the effects of package inductance and thereby minimize switching noise. A voltage delta between V_{CC} and QV_{CC} should never exceed ±0.5V because of ESD circuitry.

When CD (Chip Disable) is high, An is in high impedance state and Bn is high. To transmit data (An to Bn), the $T/\overline{R}$ signal is high.

When RBYP is high, the positive edge triggered flip-flop is in the transparent mode. When RBYP is low, the positive edge of the ACLK signal clocks the data.

In addition, the ESD circuitry between the V_{CC} pins and all other pins except for BTL I/O's and LI pins requires that any voltage on these pins should not exceed the voltage on V_{CC} +0.5V.

There are three different types of ground pins on the DS38C86A; the logic ground (GND), BTL grounds (B0GND–B8GND) and the Bandgap reference ground (QGND). All of these ground reference pins are isolated within the chip to minimize the effects of high current switching transients. For optimum performance the QGND should be returned to the connector through a quiet channel that does not carry transient switching current. The GND and B0GND–B8GND should be connected to the nearest backplane ground pin with the shortest possible path.

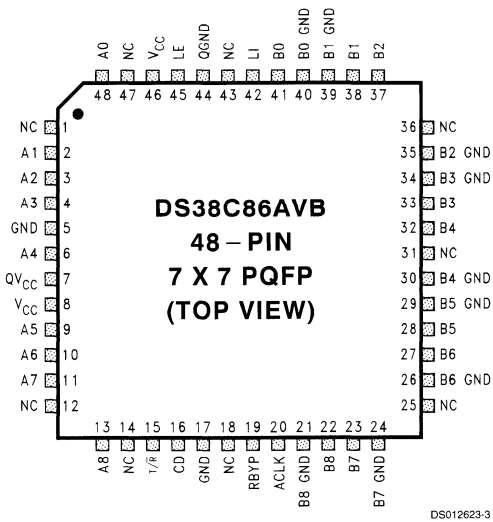
Since many different grounding schemes could be implemented and ESD circuitry exists on the DS38C86A, it is important to note that any voltage between ground pins, QGND, GND or B0GND–B8GND should not exceed ±0.5V including power up/down sequencing.

The DS38C86A is offered in a 48-pin 7 x 7 space saving PQFP package.

Features

- >50% Less I_{CC} then Bi-CMOS DS3886A
- 9-Bit inverting BTL latching transceiver
- Meets IEEE 1194.1 Standard on Backplane Transceiver Logic (BTL)
- Very low bus-port capacitance—3 pF typical
- Supports live insertion
- Glitch free power-up/down protection
- Fast propagation delays
  - — An to Bn (Fall-Thru Mode) 6.0 ns max
  - — Bn to An (Bypass Mode) 7.0 ns max
- 1V Signal swings with 80 mA sink capability
- Open drain bus-port outputs allow Wired-OR connection
- Controlled rise and fall time to reduce noise coupling to adjacent lines
- TTL compatible Driver and Control inputs
- Built in Bandgap reference with separate QV_{CC} and QGND pins for precise receiver thresholds
- Individual bus-port ground pins
- Tight skew—
  - — Driver 2.0 ns max
  - — Receiver 2.5 ns max

Connection Diagram



DS012623-3

Ordering Information

NSID	Package	NS Package Number
DS38C86AVB	PQFP (7x7)	VBH48A

National Semiconductor

DS3893A
BTL TURBOTRANSCEIVER™

General Description

The TURBOTRANSCEIVER is designed for use in very high speed bus systems. The bus terminal characteristics of the TURBOTRANSCEIVER are referred to as "Backplane Transceiver Logic" (BTL). BTL is a new logic signaling standard that has been developed to enhance the performance of backplane buses. BTL compatible transceivers feature low output capacitance drivers to minimize bus loading, a 1V nominal signal swing for reduced power consumption and receivers with precision thresholds for maximum noise immunity. This new standard eliminates the settling time delays, that severely limit the TTL bus performance, to provide significantly higher bus transfer rates.

The TURBOTRANSCEIVER is compatible with the requirements of the proposed IEEE 896 Futurebus draft standard. It is similar to the DS3896/97 BTL TRAPEZOIDAL™ Transceivers but the trapezoidal feature has been removed to improve the propagation delay. A stripline backplane is therefore required to reduce the crosstalk induced by the faster rise and fall times. This device can drive a 10Ω load with a typical propagation delay of 3.5 ns for the driver and 5 ns for the receiver.

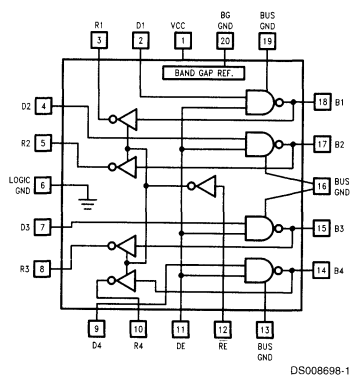
When multiple devices are used to drive a parallel bus, the driver enables can be tied together and used as a common control line to get on and off the bus. The driver enable delay is designed to be the same as the driver propagation delay in order to provide maximum speed in this configuration. The low input current on the enable pin eases the drive required for the common control line.

The bus driver is an open collector NPN with a Schottky diode in series to isolate the transistor output capacitance from the bus when the driver is in the inactive state. The active output low voltage is typically 1V. The bus is intended to be operated with termination resistors (selected to match the bus impedance) to 2.1V at both ends. Each of the resistors can be as low as 20Ω.

Features

- Fast single ended transceiver (typical driver enable and receiver propagation delays are 3.5 ns and 5 ns)
- Backplane Transceiver Logic (BTL) levels (1V logic swing)
- Less than 5 pF bus-port capacitance
- Drives densely loaded backplanes with equivalent load impedances down to 10Ω
- 4 transceivers in 20 pin PCC package
- Specially designed for stripline backplanes
- Separate bus ground returns for each driver to minimize ground noise
- High impedance, MOS and TTL compatible inputs
- TRI-STATE™ control for receiver outputs
- Built-in bandgap reference provides accurate receiver threshold
- Glitch free power up/down protection on all outputs
- Oxide isolated bipolar technology

Connection and Logic Diagram



Order Number DS3893AV
See NS Package Number V20A

National Semiconductor

DS3896/DS3897
BTL Trapezoidal™ Transceivers

General Description

These advanced transceivers are specifically designed to overcome problems associated with driving a densely populated backplane, and thus provide significant improvement in both speed and data integrity. Their low output capacitance, low output signal swing and noise immunity features make them ideal for driving low impedance buses with minimum power consumption.

The DS3896 is an octal high speed schottky bus transceiver with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. The separate driver disable pins (En) feature internal pull ups and may be left open if not required. On the other hand, the DS3896 provides high package density for data/address lines.

The open collector drivers generate precise trapezoidal waveforms, which are relatively independent of capacitive loading conditions on the outputs. This significantly reduces noise coupling to adjacent lines. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity and provide equal rejection to both negative and positive going noise pulses on the bus.

To minimize bus loading, these devices also feature a schottky diode in series with the open collector output that isolates the driver output capacitance in the disabled state. The output low voltage is typically "1V" and the output high level is intended to be 2V. This is achieved by terminating the bus with a pull up resistor to 2V at both ends. The device can drive an equivalent DC load of 18.5Ω (or greater) in the above configuration.

These signalling requirements, including a 1 volt signal swing, low output capacitance and precise receiver thresholds are referred to as Bus Transceiver Logic (BTL).

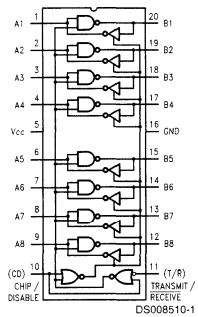
Features

- 8 bit DS3896 transceiver provides high package density
- 4 bit DS3897 transceiver provides separate driver input and receiver output pins
- BTL compatible
- Less than 5 pF output capacitance for minimal bus loading
- 1 Volt bus signal swing reduces power consumption
- Trapezoidal driver waveforms (t_r, $t_f \cong 6$ ns typical) reduce noise coupling to adjacent lines
- Temperature insensitive receiver thresholds track the bus logic high level to maximize noise immunity in both high and low states
- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs and receiver outputs

8

Logic Diagrams

DS3896N, M



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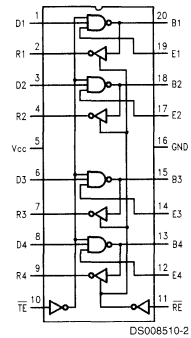
DS3897N, M



DS008510-2

Order Numbers DS3896M, DS3896N, DS3897M or DS3897N
See NS Package Number M20B or N20A

National Semiconductor

DS75110A
Dual Line Drivers

General Description

The DS75110A is a dual line driver with independent channels, common supply and ground terminals featuring constant current outputs. These drivers are designed for optimum performance when used with the DS75107, DS75108 line receivers.

The output current of the DS75110A is nominally 12 mA and may be switched to either of two output terminals with the appropriate logic levels at the driver input.

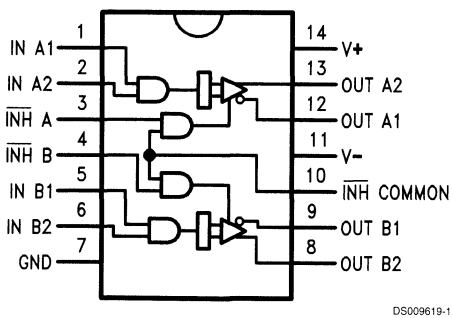
Separate or common control inputs are provided for increased logic versatility. These control or inhibit inputs allow the output current to be switched off (inhibited) by applying low logic levels to the control inputs. The output current in the inhibit mode, $I_{O(Off)}$, is specified so that minimum line loading is induced. This is highly desirable in system applications using party line data communications.

Features

- Improved stability over supply voltage and temperature ranges
- Constant current, high impedance outputs
- High speed: 15 ns max propagation delay
- Standard supply voltages
- Inhibitor available for driver selection
- High common mode output voltage range (−3.0V to 10V)
- TTL input compatibility

Connection Diagram

14–Lead Dual-In-Line Package and SO-14 Package



DS009619-1

Top View
Order Number DS75110AM or DS75110AN
See NS Package Number M14A or N14A

Function Table

Inputs				Outputs	
Logic		Inhibitor			
1	2	A/B	$\overline{INH}$	A1/B1	A2/B2
X	X	L	X	Off	Off
X	X	X	L	Off	Off
L	X	H	H	Off	On
X	L	H	H	Off	On
H	H	H	H	On	Off

H = High
L = Low
X = Don't Care

National Semiconductor

DS7830
Dual Differential Line Driver

General Description

The DS7830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

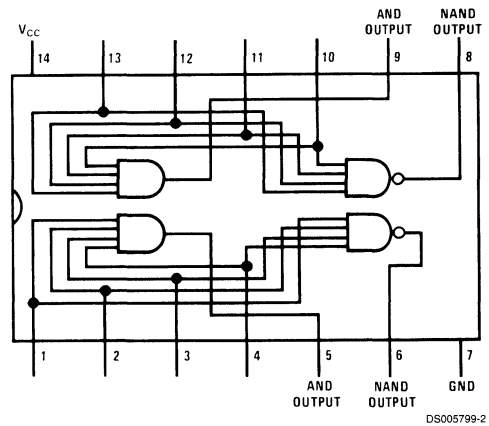
TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

Features

- Single 5V power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High speed
- Short circuit protection

Connection Diagram

Dual-In-Line and Flat Package



Top View
For Complete Military 883 Specificatons, See RETS Data Sheet.
Order Number DS7830J/883 or DS7830W/883
See NS Package Number J14A

National Semiconductor

DS7831/DS8832
Dual TRI-STATE® Line Driver

General Description

Through simple logic control, the DS7831/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS8832 does not have the V_{CC} clamp diodes found on the DS7831.

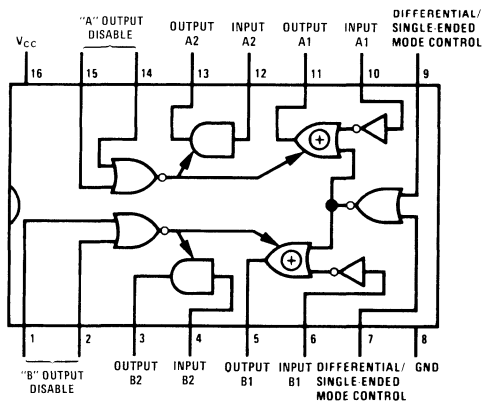
The DS7831 is specified for operation over the −55°C to +125°C military temperature range. The DS8832 is specified for operation over the 0°C to +70°C temperature range.

Features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line

Connection and Logic Diagram

Dual-In-Line Package



DS005800-1

Top View
Order Number DS8832J or DS8832N
See NS Package Number J16A or N16A
For Complete Military 883 Specificatons,
See RETS Data Sheet.
Order Number DS7831J/883, DS7831W/883,
See NS Package Number J16A or W16A

Truth Table

(Shown for A Channels Only)

"A" Output Disable		Differential/ Single-Ended Mode Control		Input A1	Output A1	Input A2	Output A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X 1	1 X	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
1 X	X 1	X	X	X	High Impedance State	X	High Impedance State

X = Don't Care

National Semiconductor

DS1603
TRI-STATE® Dual Receiver

General Description

The DS16033 is a dual differential TRI-STATE line receiver designed for a broad range of system applications. It features a high input impedance and low input current which reduces the loading effects on a digital transmission line, making it ideal for use in party line systems and general purpose applications like transducer preamplifiers, level translators and comparators.

The receivers feature a ±25 mV input sensitivity specified over a ±3V common mode range. Input protection diodes are incorporated in series with the collectors of the differential stage. These diodes are useful in applications that have multiple V_{CC}+ supplies or V_{CC}+ supplies that are turned off thus avoiding signal clamping. In addition, TTL compatible strobe and control lines are provide for flexibility in the application.

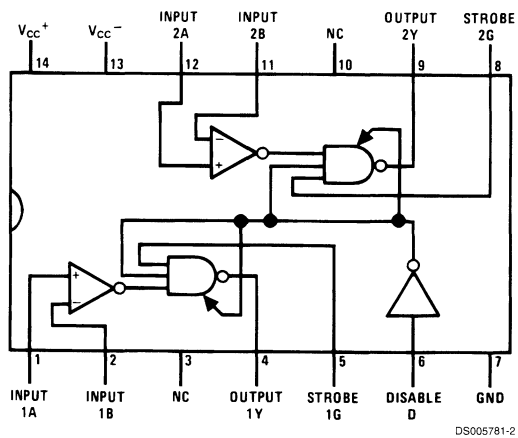
The DS1603 is pin compatible with the DS75107 dual line receiver.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±25 mV input sensitivity
- ±3V input common-mode range
- High-input inpedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- TRI-STATE outputs for high speed buses

Connection Diagram

Dual-In-Line Package



Top View
For Complete Military 883 Specifications, See RETS Data Sheet.
Order Number: DS1603J/883 or DS1603W/883
See NS Package Number J14A

National Semiconductor

DS3650
Quad Differential Line Receivers

General Description

The DS3650 is TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bussed organizations.

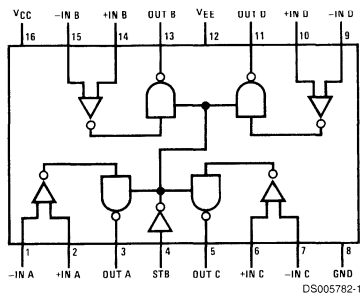
The DS3650 has active pull-up outputs and offers a TRI-STATE strobe.

Features

- High speed
- TTL compatible
- Input sensitivity: ±25 mV
- TRI-STATE outputs for high speed busses
- Standard supply voltages: ±5V
- Pin and function compatible with MC3450

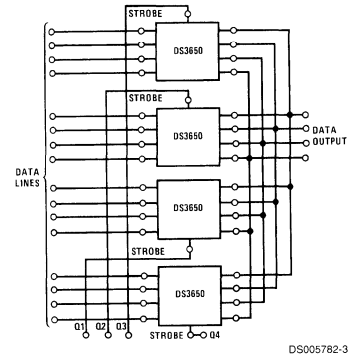
Connection Diagrams

Dual-In-Line Package



Top View
Order Number DS3650M or DS3650N
See NS Package Number M16A or N16A
For Complete Military 883 Specifications, see RETS Data Sheet.

Wired "OR" Data Selecting Using TRI-STATE Logic



Input	Strobe	Output
		DS3650
$V_D \geq 25$ mV	L	H
	H	Open
-25 mV $\leq V_{ID} \leq 25$ mV	L	X
	H	Open
$V_{ID} \leq -25$ mV	L	L
	H	Open

L = Low Logic State Open = TRI-STATE
H = High Logic State X = Indeterminate State

National Semiconductor

DS75107
Dual Line Receiver

General Description

The product described herein is a TTL compatible dual high speed circuit intended for sensing in a broad range of system applications. While the primary usage will be for line receivers of MOS sensing, the product may effectively be used as a voltage comparator, level translator, window detector, transducer preamplifier, and in other sensing applications. As a digital line receiver the product is applicable with the SN55109/SN75109 and μA75110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems.

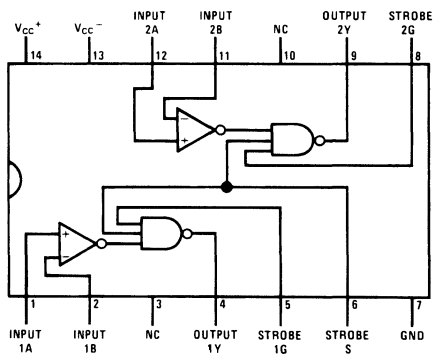
Input protection diodes are incorporated in series with the collectors of the differential input stage. These diodes are useful in certain applications that have multiple V_{CC}+ supplies or V_{CC}+ supplies that are turned off.

Features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or V_{CC} = 0V
- Strobes for channel selection
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS75107M, DS75107N
See NS Package Number M14A or N14A
For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS55107AJ/883
See NS Package Number J14A

Selection Guide

Temperature→	$0°C \leq T_A \leq +70°C$	
Package→	Cavity or Molded Dip	
Input Sensitivity→	±25 mV	±10 mV
Output Logic↓		
TTL Active Pull-Up	DS75107	
TTL Open Collector		

National Semiconductor

DS7820A/DS8820A
Dual Line Receiver

General Description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with TTL or LS integrated circuits.

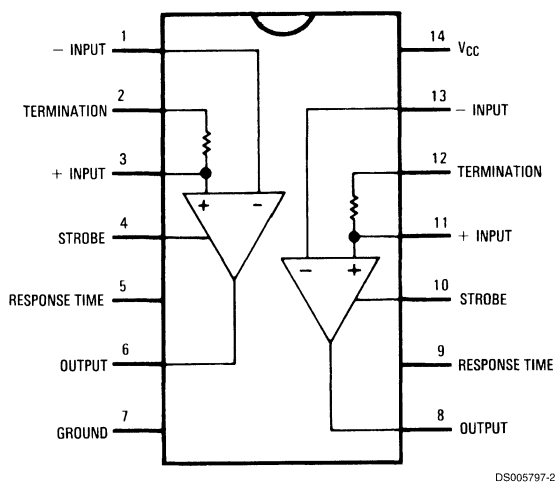
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to +125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

Features

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

Connection Diagram

Dual-in-Line Package



DS005797-2

Note 1: Pin 7 connected to bottom of cavity package.

Top View
Order Number DS7820AJ or DS8820AN See NS Package Number J14A or N14A
For Complete Military 883 Specificatons, See RETS Data Sheet.
Order Number DS7820AJ/883
See NS Package Number J14A or W14B

National Semiconductor

DS9622
Dual Line Receiver

General Description

The DS9622 is a dual line receiver designed to discriminate a worst case logic swing of 2V from a ±10V common mode noise signal or ground shift. A 1.5V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors.

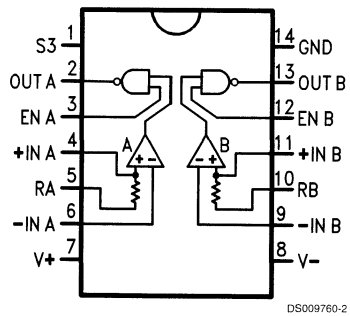
The DS9622 allows the choice of output states with the input open, without affecting circuit performance by use of S3. A 130Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to 12V by tying it to a positive supply through a resistor. The output circuits allow wired-OR operation.

Features

- TTL compatible threshold voltage
- Input terminating resistors
- Choice of output state with inputs open
- TTL compatible output
- High common mode
- Wired-OR capability
- Enable inputs
- Logic compatible supply voltages

Connection Diagram

14–Lead DIP



Top View
For Complete Military 883 Specifications, see RETS Datasheet.
Order Number DS9622ME/883,
DS9622MJ/883 or DS9622MW/883
See NS Package Number E20A, J14A or W14B

National Semiconductor

DS3662
Quad High Speed Trapezoidal™ Bus Transceiver

General Description

The DS3662 is a quad high speed Schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 15 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. A two input NOR gate is provided to disable all drivers in a package simultaneously.

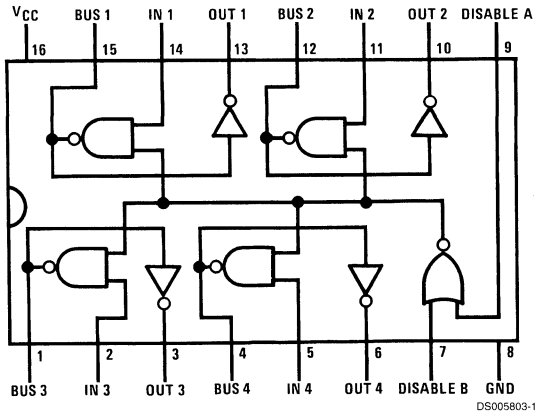
Features

- Pin to pin functional replacement for DS8641
- Guaranteed AC specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Precision receiver thresholds provide maximum noise immunity and symmetrical response to positive and negative going pulses
- Open collector driver output allows wire-OR connection
- High speed Schottky technology
- 15 μA typical bus termination current with normal V_{CC} or with V_{CC} = 0V
- Glitch free power up/down protection on the driver output
- TTL compatible driver and disable inputs, and receiver outputs

8

Block and Connection Diagram

Dual-In-Line Package



Top View
Order Number DS3662J, DS3662N or DS3662WM
See NS Package Number J16A, N16A or M16B

National Semiconductor

DS3862
Octal High Speed Trapezoidal Bus Transceiver

General Description

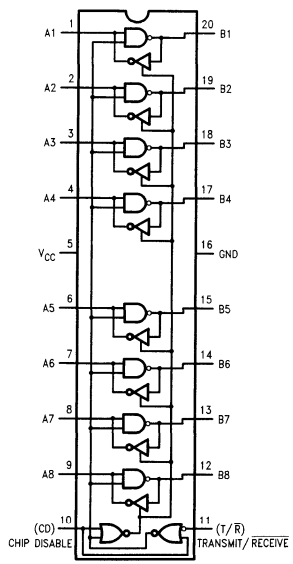
The DS3862 is an octal high speed schottky bus transceiver intended for use with terminated 120Ω impedance lines. It is specifically designed to reduce noise in unbalanced transmission systems. The open collector drivers generate precise trapezoidal waveforms with rise and fall times of 9 ns (typical), which are relatively independent of capacitive loading conditions on the outputs. This reduces noise coupling to the adjacent lines without any appreciable impact on the maximum data rate obtainable with high speed bus transceivers. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity. Tightly controlled threshold levels on the receiver provide equal rejection to both negative and positive going noise pulses on the bus.

The external termination is intended to be a 180Ω resistor from the bus to 5V logic supply, together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends.

Features

- Guaranteed A.C. specifications on noise immunity and propagation delay over the specified temperature and supply voltage range
- Temperature insensitive receiver thresholds track bus logic level and respond symmetrically to positive and negative going pulses
- Trapezoidal bus waveforms reduce noise coupling to adjacent lines
- Open collector driver output allows wire-or connection
- Advanced low power schottky technology
- Glitch free power up/down protection on driver and receiver outputs
- TTL compatible driver and control inputs, and receiver outputs
- Control logic is the same as the DS3896

Logic and Connection Diagram



DS008539-1

Order Number DS3862J, DS3862N or DS3862WM
See NS Package Number J20A, N20A or M20B

National Semiconductor

DS75160A/DS75161A
IEEE-488 GPIB Transceivers

General Description

This family of high-speed-Schottky 8-channel bi-directional transceivers is designed to interface TTL/MOS logic to the IEEE Standard 488-1978 General Purpose Interface Bus (GPIB). PNP inputs are used at all driver inputs for minimum loading, and hysteresis is provided at all receiver inputs for added noise margin. The IEEE-488 required bus termination is provided internally with an active turn-off feature which disconnects the termination from the bus when V_{CC} is removed.

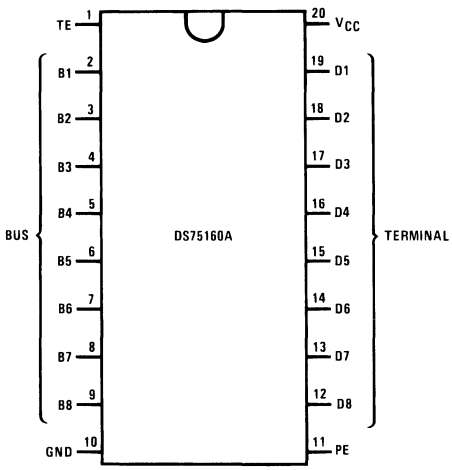
The General Purpose Interface Bus is comprised of 16 signal lines — 8 for data and 8 for interface management. The data lines are always implemented with DS75160A, and the management lines are either implemented with DS75161A in a single-controller system.

Features

- 8-channel bi-directional non-inverting transceivers
- Bi-directional control implemented with TRI-STATE® output design
- Meets IEEE Standard 488-1978
- High-speed Schottky design
- Low power consumption
- High impedance PNP inputs (drivers)
- 500 mV (typ) input hysteresis (receivers)
- On-chip bus terminators
- No bus loading when V_{CC} is removed
- Pin selectable open collector mode on DS75160A driver outputs
- Accommodates multi-controller systems

Connection Diagrams

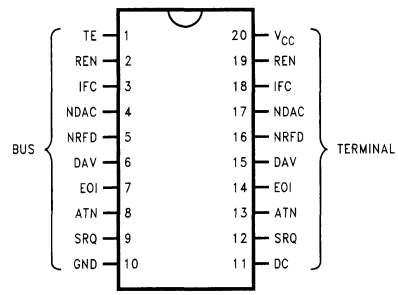
Dual-In-Line Package



DS005804-1

Top View
Order Number DS75160AN or DS75160AWM
See NS Package Number M20B or N20A

Dual-In-Line Package



DS005804-16

Order Number DS75161AN or DS75161AWM
See NS Package Number M20B or N20B

8

National Semiconductor

DS8641
Quad Unified Bus Transceiver

General Description

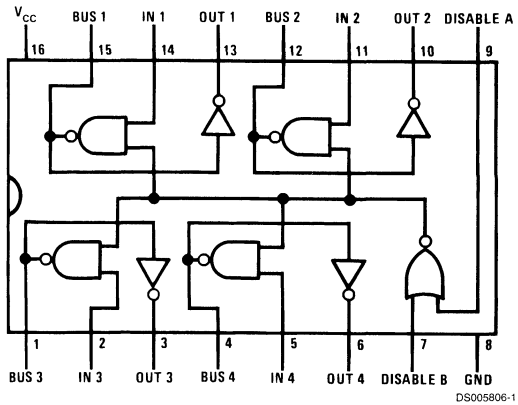
The DS8641 is a quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

Features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30 µA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

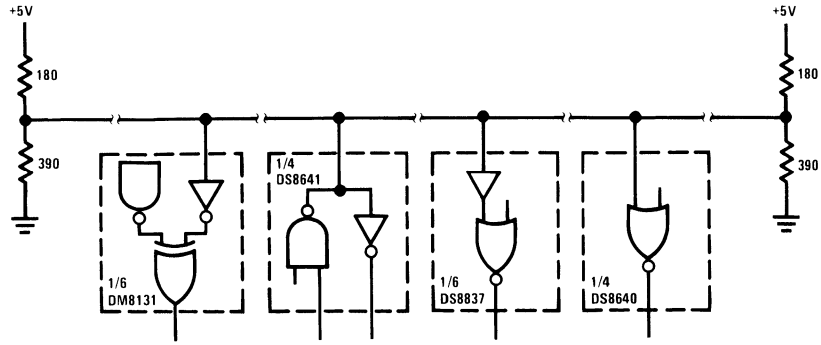
Connection Diagram

Dual-In-Line Package



Top View
Order Number DS8641N
See NS Package Number N16A

Typical Application



DS005806-2

National Semiconductor

DS8838
Quad Unified Bus Transceiver

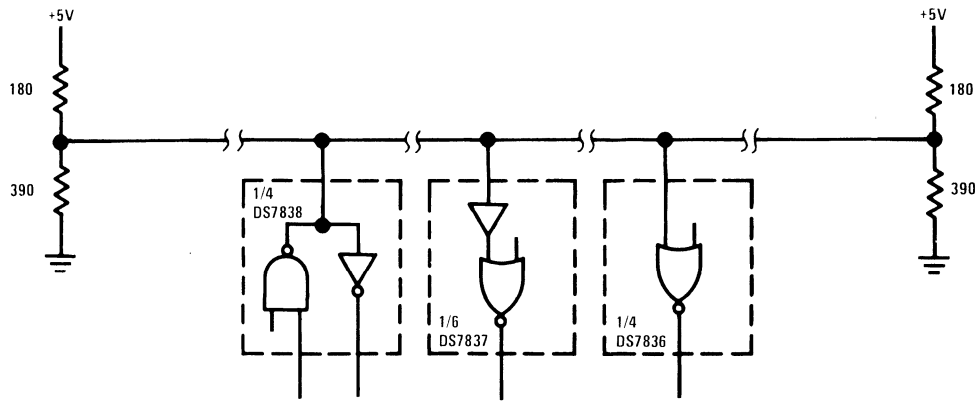
General Description

The DS8838 is a quad high speed driver/receiver designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times ≤ 1.0 µs/V.

Features

- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20 µA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

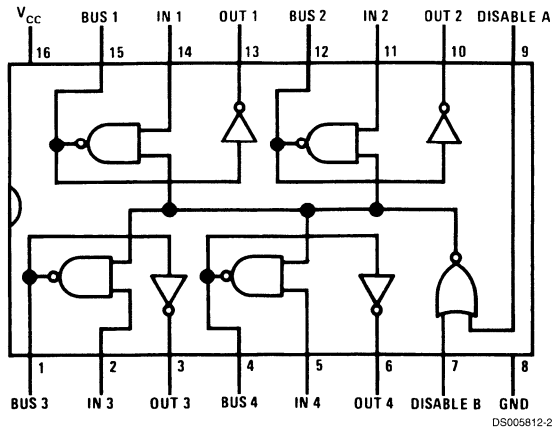
Typical Application



DS005812-1

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS7838J, DS8838M or DS8838N
See NS Package Number J16A, M16A or N16A

National Semiconductor

DS1776
PI-Bus Transceiver

General Description

The DS1776 is an octal PI-bus Transceiver. The A to B path is latched. B outputs are open collector with series Schottky diode, ensuring minimum B output loading. B outputs also have ramped rise and fall times (2.5 ns typical), ensuring minimum PI-bus ringing. B inputs have glitch rejection circuitry, 4 ns typical.

Designed using National's Bi-CMOS process for both low operating and disabled power. AC performance is optimized for the PI-Bus inter-operability requirements.

The DS1776 is an octal latched transceiver and is intended to provide the electrical interface to a high performance wired-or bus. This bus has a loaded characteristic impedance range of 20Ω to 50Ω and is terminated on each end with a 30Ω to 40Ω resistor.

The DS1776 is an octal bidirectional transceiver with open collector B and TRI-STATE® A port output drivers. A latch function is provided for the A port signals. The B port output driver is designed to sink 100 mA from 2V and features a controlled linear ramp to minimize crosstalk and ringing on the bus.

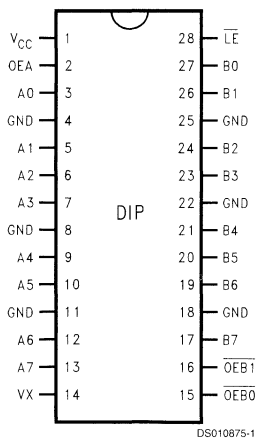
A separate high level control voltage (V_X) is provided to prevent the A side output high level from exceeding future high density processor supply voltage levels. For 5V systems, V_X is tied to V_{CC}.

Features

- Mil-Std-883C qualified
- Similar to BTL
- Low power I_{CCL} = 41 mA max
- B output controlled ramp rate
- B input noise immunity, typically 4 ns
- Available in 28-pin DIP, Flatpak and CLCC
- Pin and function compatible with Signetics 54F776

Pin Configurations

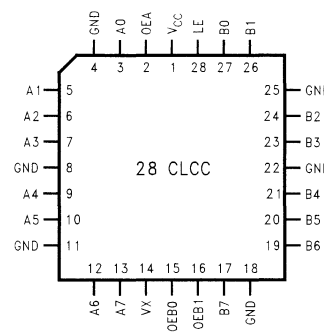
Pin Configuration



DS010875-1

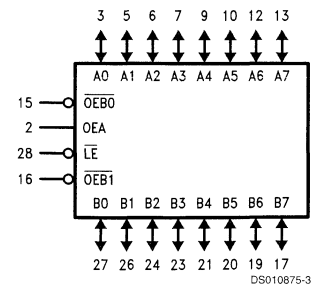
Order Number DS1776E/883 or DS1776J/883
See NS Package E28A or J28B

Pin Configuration



DS010875-2

Logic Symbol



DS010875-3

National Semiconductor

DS26S10
Quad Bus Transceiver

General Description

The DS26S10 is a quad Bus Transceiver consisting of 4 high speed bus drivers with open-collector outputs capable of sinking 100 mA at 0.8V and 4 high speed bus receivers. Each driver output is connected internally to the high speed bus receiver in addition to being connected to the package pin. The receiver has a Schottky TTL output capable of driving 10 Schottky TTL unit loads.

An active low enable gate controls the 4 drivers so that outputs of different device drivers can be connected together for party-line operation.

The bus output high-drive capability in the low state allows party-line operation with a line impedance as low as 100Ω. The line can be terminated at both ends, and still give considerable noise margin at the receiver. The receiver typical switching point is 2V.

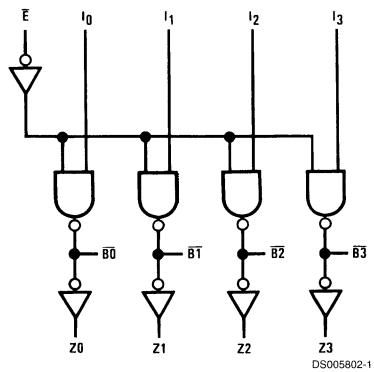
The DS26S10 features advanced Schottky processing to minimize propagation delay. The device package also has 2 ground pins to improve ground current handling and allow close decoupling between V_{CC} and ground at the package. Both GND 1 and GND 2 should be tied to the ground bus external to the device package.

Features

- Input to bus is inverting on DS26S10
- Quad high speed open-collector bus transceivers
- Driver outputs can sink 100 mA at 0.8V maximum
- Advanced Schottky processing
- PNP inputs to reduce input loading

Logic Diagram

DS26S10



DS005802-1

National Semiconductor

DS1487
Low Power RS-485 ¼ Unit Load Multipoint Transceiver

General Description

The DS1487 is a low-power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The drivers slew rate allows for operation up to 2.0 Mbps (see Applications Information section). The transceiver presents ¼ unit loading to the RS-485 bus allowing up to 128 nodes to be connected together without the use of repeaters.

The transceiver draws 200 µA of supply current when unloaded or fully loaded with the driver disabled and operates from a single +5V supply.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE® (High Impedance state) under fault conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

The receiver has a failsafe feature that guarantees a logic-high output if the input is open circuit.

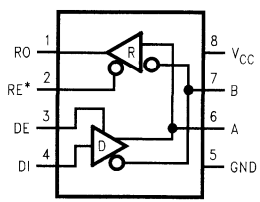
The DS1487 is available in surface mount and DIP packages.

Features

- Meets TIA/EIA RS-485 multipoint standard
- Allows up to 128 transceivers on the bus (¼ U.L.)
- Guaranteed full load output voltage (V_{OD3})
- Low quiescent current: 200 µA typ
- −7V to +12V common-mode input voltage range
- TRI-STATE outputs on driver and receiver
- AC performance:
  - — Driver transition time: 25 ns typ
  - — Driver propagation delay: 40 ns typ
  - — Driver skew: 1 ns typ
  - — Receiver propagation delay: 200 ns typ
  - — Receiver skew: 20 ns typ
- Half-duplex flow through pinout
- Operates from a single 5V supply
- Current-limiting and thermal shutdown for driver overload protection
- Pin and functional compatible with MAX1487

Connection and Logic Diagram

DIP and SOIC



DS012920-1

*Note: Non Terminated, Open Input only

Order Number	Temp. Range	Package/###
DS1487N	0°C to +70°C	DIP/N08E
DS1487M	0°C to +70°C	SOP/M08A

Truth Table

DRIVER SECTION				
RE (Note 1)	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE (Note 1)	**DE**	**A-B**		**RO**
L	L	≥+0.2V		H
L	L	≤−0.2V		L
H	X	X		Z
L	L	OPEN (Note 1)		H

X = indeterminate

Z = TRI-STATE

Note 1: Non Terminated, Open Input only

National Semiconductor

DS16F95, DS36F95
EIA-485/EIA-422A Differential Bus Transceiver

General Description

The DS16F95/DS36F95 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets both EIA-485 and EIA-422A standards.

The DS16F95/DS36F95 offers improved performance due to the use of L-FAST bipolar technology. The L-FAST technology allows for higher speeds and lower currents by minimizing gate delay times. Thus, the DS16F95 and DS36F95 consume less power, and feature an extended temperature range as well as improved specifications.

The DS16F95/DS36F95 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to accommodate loads of up to 60 mA of sink or source current and features positive and negative current limiting in addition to thermal shutdown for protection from line fault conditions.

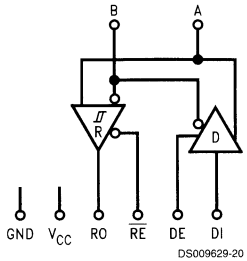
The DS16F95/DS36F95 can be used in transmission line applications employing the DS96F172 and the DS96F174 quad differential line drivers and the DS96F173 and DS96F175 quad differential line receivers.

Features

- Meets EIA-485 and EIA-422A
- Meets SCSI-1 (5 MHZ) specifications
- Designed for multipoint transmission
- Wide positive and negative input/output bus voltage ranges
- Thermal shutdown protection
- Driver positive and negative current-limiting
- High impedance receiver input
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Reduced power consumption
- Pin compatible with DS3695 and SN75176A
- Military temperature range available
- Qualified for MIL-STD 883C
- Standard Military Drawings (SMD) available
- Available in DIP (J), SOIC (M), LCC (E), and Flatpak (W) packages

8

Logic Diagram



Function Tables

Driver

Driver Input	Enable	Outputs	
DI	**DE**	**A**	**B**
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A–B	**$\overline{RE}$**	**RO**
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (Off)

National Semiconductor

DS36276
FAILSAFE Multipoint Transceiver

General Description

The DS36276 FAILSAFE Multipoint Transceiver is designed for use on bi-directional differential busses. It is compatible with existing TIA/EIA-485 transceivers, however, it offers an additional feature not supported by standard transceivers.

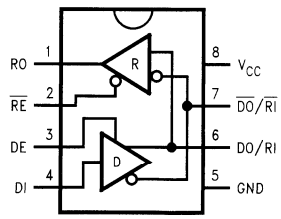
The FAILSAFE feature guarantees the receiver output to a known state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault conditions (open or short). The receiver output is in a HIGH state for the following conditions: OPEN Inputs, Terminated Inputs (50Ω), and SHORTED Inputs.

FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Compatible with popular interface standards:
  - — TIA/EIA-485 (RS-485)
  - — TIA/EIA-422-A (RS-422-A)
  - — CCITT Recommendation V.11
- Bi-Directional Transceiver
  - — Designed for multipoint transmission
- Separate driver input, driver enable, receiver enable, and receiver output for maximum flexibility
- Wide bus common mode range
  - — (−7V to +12V)
- Pin compatible with: DS75176B, DS96176, DS3695 and SN75176A and B
- Available in SOIC package

Connection and Logic Diagram



DS011383-1

Order Number DS36276M
See NS Package Number M08A

Driver

Inputs			Outputs	
$\overline{RE}$	DE	DI	DO/RI	$\overline{DO}$ /$\overline{RI}$
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

Receiver

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	≥0V	H
L	L	≤−500 mV	L
H	X	X	Z

Receiver FAILSAFE

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	SHORTED	H
L	L	OPEN	H
H	X	X	Z

National Semiconductor

DS36277
Dominant Mode Multipoint Transceiver

General Description

The DS36277 Dominant Mode Multipoint Transceiver is designed for use on bi-directional differential busses. It is optimal for use on Interfaces that utilize Society of Automotive Engineers (SAE) J1708 Electrical Standard.

The device is similar to standard TIA/EIA-485 transceivers, but differs in enabling scheme. The Driver's Input is normally externally tied LOW, thus providing only two states: Active (LOW), or Disabled (OFF). When the driver is active, the dominant mode is LOW, conversely, when the driver is disabled, the bus is pulled HIGH by external bias resistors.

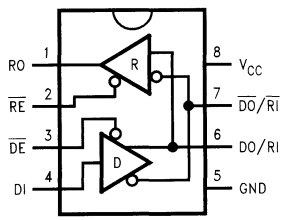
The receiver provides a FAILSAFE feature that guarantees a known output state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault Conditions (open or short). The receiver output is HIGH for the following conditions: Open Inputs, Terminated Inputs (50Ω), or Shorted Inputs. FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Optimal for use in SAE J1708 Interfaces
- Compatible with popular interface standards:
  - — TIA/EIA-485 and TIA/EIA-422-A
  - — CCITT recommendation V.11
- Bi-directional transceiver
  - — Designed for multipoint transmission
- Wide bus common mode range
  - — (−7V to +12V)
- Available in plastic DIP and SOIC packages

8

Connection and Logic Diagram



DS011384-1

Order Number DS36277TM or DS36277TN
See NS Package Number M08A or N08E

Driver

Inputs		Outputs	
$\overline{DE}$	DI	DO/RI	$\overline{DO}$ /$\overline{RI}$
L	L	L	H
L	H	H	L
H	X	Z	Z

Receiver

Inputs		Output
$\overline{RE}$	DO/RI–$\overline{DO}$ /$\overline{RI}$	RO
L	≥ 0 mV	H
L	≤ −500 mV	L
L	SHORTED	H
L	OPEN	H
H	X	Z

National Semiconductor

DS3695/DS3695T/DS3696/DS3697
Multipoint RS485/RS422 Transceivers/Repeaters

General Description

The DS3695, DS3696, and DS3697 are high speed differential TRI-STATE® bus/line transceivers/repeaters designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission.

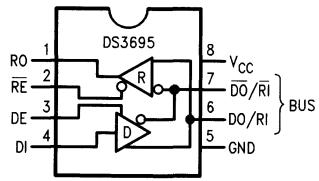
The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696 provides an output pin TS (thermal shutdown) which reports the occurrence of the thermal shutdown of the device. This is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the line fault outputs of several devices to be wire OR-ed.

Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

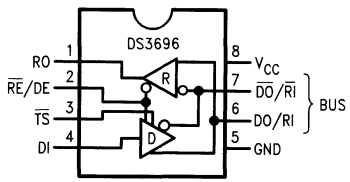
Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422
- 15 ns driver propagation delays with 2 ns skew (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis

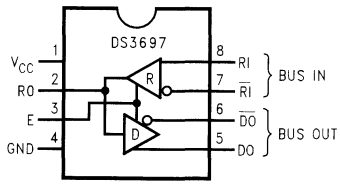
Connection and Logic Diagrams



Top View



Top View



Top View

Order Number DS3695N, DS3695TN, DS3696N, or DS3697N
See NS Package Number N08E

Note 1: $\overline{TS}$ pin was $\overline{LF}$ (Line Fault) in previous datasheets and reports the occurrence of a thermal shutdown of the device.

National Semiconductor

DS36950
Quad Differential Bus Transceiver

General Description

The DS36950 is a low power, space-saving quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, computer I/O bus applications. A compact 20-pin surface mount PLCC package provides high transceiver integration and a very small PC board footprint.

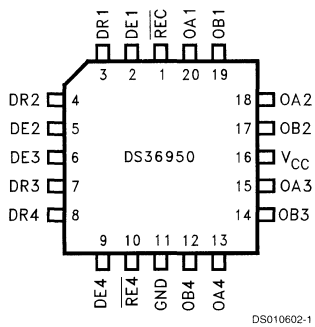
Timing uncertainty across an interface using multiple devices, a typical problem in a parallel interface, is specified—minimum and maximum propagation delay times are guaranteed.

Six devices can implement a complete IPI master or slave interface. Three transceivers in a package are pinned out for connection to a parallel databus. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

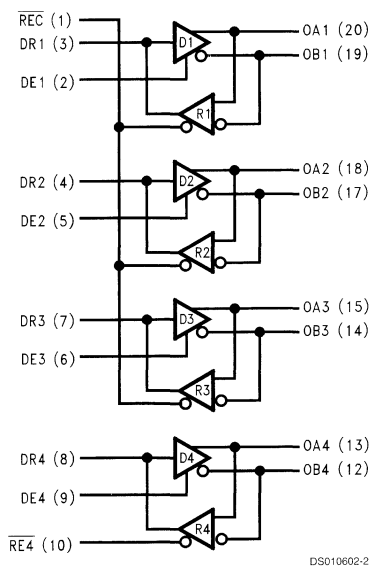
Features

- Pinout for IPI interface
- Compact 20-pin PLCC package
- Meets EIA-485 standard for multipoint bus transmission
- Greater than 60 mA source/sink
- Thermal Shutdown Protection

Pinout and Logic Diagrams



Order Number DS36950
See NS Package Number V20A



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National Semiconductor

DS36954
Quad Differential Bus Transceiver

General Description

The DS36954 is a low power, quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, I/O bus applications. A compact 20-pin surface mount PLCC or SOIC package provides high transceiver integration and a very small PC board footprint.

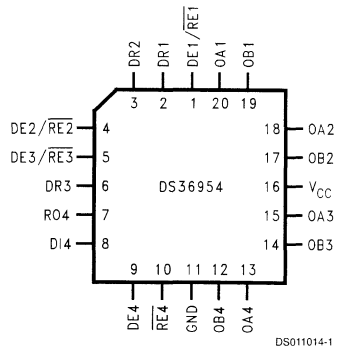
Propagation delay skew between devices is specified to aid in parallel interface designs—limits on maximum and minimum delay times are guaranteed.

Five devices can implement a complete SCSI initiator or target interface. Three transceivers in a package are pinned out for data bus connections. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

Features

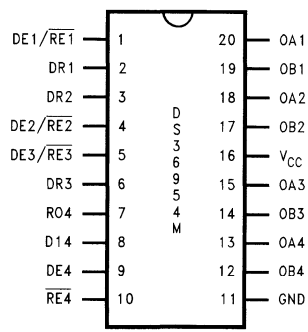
- Pinout for SCSI interface
- Compact 20-pin PLCC or SOIC package
- Meets EIA-485 standard for multipoint bus transmission
- Greater than 60 mA source/sink currents
- Thermal shutdown protection
- Glitch-free driver outputs on power up and down

Connection Diagrams



DS011014-1

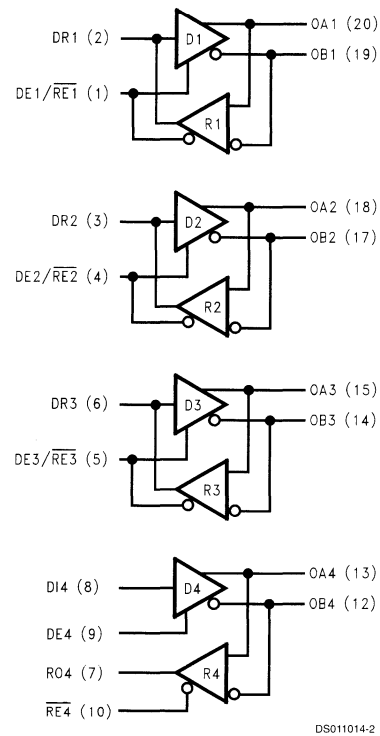
Order Number DS36954V
See NS Package Number V20A



DS011014-19

Order Number DS36954M
See NS Package Number M20B

Logic Diagrams



DS011014-2

National Semiconductor

DS3695A/DS3695AT/DS3696A Multipoint RS485/RS422 Transceivers

General Description

The DS3695A and DS3696A are high speed differential TRI-STATE® bus/line transceivers designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition they are compatible with requirements of RS-422.

The driver and receiver outputs feature TRI-STATE capability. The driver outputs remain in TRI-STATE over the entire common mode range of +12V to −7V. Bus faults that cause excessive power dissipation within the device trigger a thermal shutdown circuit, which forces the driver outputs into the high impedance state. The DS3696A provides an output pin (TS) which reports the thermal shutdown of the device. TS is an "open collector" pin with an internal 10 kΩ pull-up resistor. This allows the TS outputs of several devices to be wire OR-ed.

Both AC and DC specifications are guaranteed over the 0°C to 70°C temperature and 4.75V to 5.25V supply voltage range.

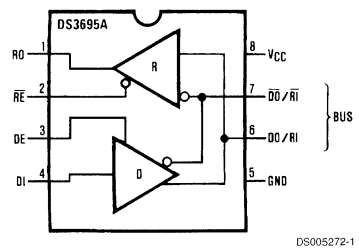
Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422
- 10 ns driver propagation delays (typical)
- Single +5V supply
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus
- Thermal shutdown protection
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus
- 70 mV typical receiver hysteresis
- Available in SOIC packaging

8

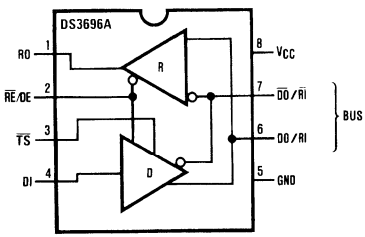
Connection and Logic Diagrams

Molded Package, Small Outline (M)



DS005272-1

Top View



DS005272-2

$\overline{TS}$ was $\overline{LF}$ (Line Fault) on previous datasheets, $\overline{TS}$ goes low upon thermal shutdown.

Top View
Order Number DS3695AM, DS3695ATM or DS3696AM
See NS Package Number M08A

National Semiconductor

DS36C278
Low Power Multipoint EIA-RS-485 Transceiver

General Description

The DS36C278 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 standard for multipoint data transmission. In addition it is compatible with TIA/EIA-422-B.

The CMOS design offers significant power savings over its bipolar and ALS counterparts without sacrificing ruggedness against ESD damage. The device is ideal for use in battery powered or power conscious applications. I_{CC} is specified at 500 µA maximum.

The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

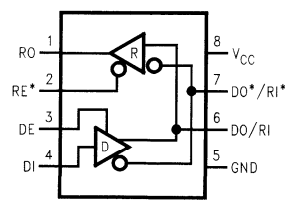
The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open. (Note 1)

The DS36C278T is fully specified over the industrial temperature range (−40°C to +85°C).

Features

- 100% RS-485 compliant
  — Guaranteed RS-485 device interoperation
- Low power CMOS design: I_{CC} 500 µA max
- Built-in power up/down glitch-free circuitry
  — Permits live transceiver insertion/displacement
- DIP and SOIC packages available
- Industrial temperature range: −40°C to +85°C
- On-board thermal shutdown circuitry
  — Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range: −7V to +12V
- Receiver open input fail-safe (Note 1)
- ¼ unit load (DS36C278): ≥128 nodes
- ½ unit load (DS36C278T): ≥64 nodes
- ESD (human body model): ≥2 kV
- Drop in replacement for:
  — LTC485, MAX485, DS75176, DS3695

Connection and Logic Diagram



DS012040-1

Order Number DS36C278TM, DS36C278TN, DS36C278M, DS36C278N
See NS Package Number M08A or N08E

DRIVER SECTION				
RE*	**DE**	**DI**	**DO/RI**	**DO*/RI***
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

RECEIVER SECTION			
RE*	**DE**	**RI-RI***	**RO**
L	L	≥+0.2V	H
L	L	≤−0.2V	L
H	L	X	Z
L	L	OPEN (Note 1)	H

Note 1: Non-terminated, open input only

National Semiconductor

DS36C279
Low Power EIA-RS-485 Transceiver with Sleep Mode

General Description

The DS36C279 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition it is compatible with TIA/EIA-422-B.

The sleep mode feature automatically puts the device in a power saving mode when both the driver and receiver are disabled.†† The device is ideal for use in power conscious applications where the device may be disabled for extended periods of time.

The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into a high impedance state.

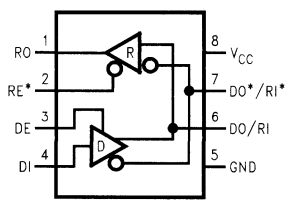
The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open.†

The DS36C279T is fully specified over the industrial temperature range (−40°C to +85°C).

Features

- 100% RS-485 compliant
  — Guaranteed RS-485 device interoperation
- Low power CMOS design: I_{CC} 500 µA max
- Automatic sensing sleep mode
  — Reduces I_{CC} to 10 µA maximum
- Built-in power up/down glitch-free circuitry
  — Permits live transceiver intersection/displacement
- SOIC packages
- Industrial temperature range: −40°C to +85°C
- On-board thermal shutdown circuitry
  — Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range: −7V to +12V
- Receive open input fail-safe (Note 1)
- ¼ unit load (DS36C279): ≥ 128 nodes
- ½ unit load (DS36C279T): ≥ 64 nodes
- ESD (Human Body Model): ≥ 2 kV
- Drop-in replacement for:
  — LTC485 MAX485 DS75176 DS3695

Connection and Logic Diagram



DS012053-1

Order Number DS36C279M, DS36C279TM
See NS Package Number M08A

DRIVER SECTION				
RE*	**DE**	**DI**	**DO/RI**	**DO*/RI***
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

RECEIVER SECTION			
RE*	**DE**	**RI-RI***	**RO**
L	L	≥+0.2V	H
L	L	≤−0.2V	L
H	L	X	Z (Note 2)
L	L	OPEN (Note 1)	H

Note 1: Non-terminated, open input only

Note 2: Device enters sleep mode if enable conditions are held > 600 ns

National Semiconductor

DS36C280
Slew Rate Controlled CMOS EIA-RS-485 Transceiver

General Description

The DS36C280 is a low power differential bus/line transceiver designed to meet the requirements of RS-485 Standard for multipoint data transmission. In addition, it is compatible with TIA/EIA-422-B.

The slew rate control feature allows the user to set the driver rise and fall times by using an external resistor. Controlled edge rates can reduce switching EMI.

The CMOS design offers significant power savings over its bipolar and ALS counterparts without sacrificing ruggedness against ESD damage. The device is ideal for use in battery powered or power conscious applications. I_{CC} is specified at 500 µA maximum.

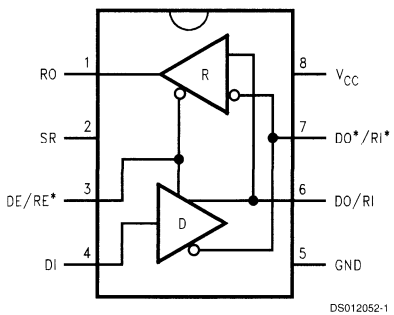
The driver and receiver outputs feature TRI-STATE® capability. The driver outputs operate over the entire common mode range of −7V to +12V. Bus contention or fault situations are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

The receiver incorporates a fail safe circuit which guarantees a high output state when the inputs are left open (Note 1) .

Features

- 100% RS-485 compliant
  — Guaranteed RS-485 device interoperation
- Low power CMOS design: I_{CC} 500 µA max
- Adjustable slew rate control
  — Minimizes EMI affects
- Built-in power up/down glitch-free circuitry
  — Permits live transceiver insertion/displacement
- SOIC packages
- Industrial temperature range: −40°C to +85°C
- On-board thermal shutdown circuitry
  — Prevents damage to the device in the event of excessive power dissipation
- Wide common mode range: −7V to +12V
- Receiver open input fail-safe (Note 1)
- ¼ unit load (DS36C280): ≥128 nodes
- ½ unit load (DS36C280T): ≥64 nodes
- ESD (human body model): ≥2 kV

Connection and Logic Diagram



DS012052-1

Order Number DS36C280M, DS36C280TM
See NS Package Number M08A

DRIVER SECTION			
DE/RE*	**DI**	**DO/RI**	**DO*/RI***
H	H	H	L
H	L	L	H
L	X	Z	Z

RECEIVER SECTION		
DE/RE*	**RI-RI***	**RO**
L	≥+0.2V	H
L	≤−0.2V	L
H	X	Z
L	OPEN (Note 1)	H

Note 1: Non-terminated, Open Inputs only

National Semiconductor

DS481
Low Power RS-485/RS-422 Multipoint Transceiver with Sleep Mode

General Description

The DS481 is a low-power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The drivers slew rate allows for operation up to 2.0 Mbps (see Applications Information section).

The transceiver draws 200 µA of supply current when unloaded or 0.2 µA when in the automatic sleep mode. Sleep mode is activated by inactivity on the enables (DE and RE (Note 1)). Holding DE =L and RE (Note 1)=H for greater than 600 ns will enable the sleep mode. The DS481 operates from a single +5V supply.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE® (High Impedance state) under fault conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

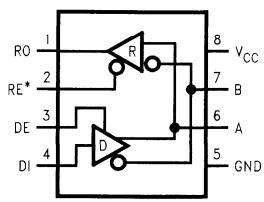
The receiver has a failsafe feature that guarantees a logic-high output if the input is open circuit.

The DS481 is available in a surface mount package and is characterized for Industrial temperature range operation.

Features

- Meets TIA/EIA RS-485 multipoint standard
- Sleep mode reduces I_{CC} to 0.2 µA
- Guaranteed full load output voltage (V_{OD3})
- Low quiescent current: 200 µA typ
- −7V to +12V common-mode input voltage range
- TRI-STATE outputs on driver and receiver
- AC performance:
  - — Driver transition time: 25 ns typ
  - — Driver propagation delay: 40 ns typ
  - — Driver skew: 1 ns typ
  - — Receiver propagation delay: 200 ns typ
  - — Receiver skew: 20 ns typ
- Half-duplex flow through pinout
- Operates from a single 5V supply
- Allows up to 64 tranceivers on the bus
- Current-limiting and thermal shutdown for driver overload protection
- Industrial temperature range operation
- Pin and functional compatible with MAX481C and MAX481E

Connection and Logic Diagram



DS012919-1

*Note: Non Terminated, Open Input only

Order Number	Temp. Range	Package/###
DS481TM	−40˚C to +85˚C	SOP/M08A

Truth Table

DRIVER SECTION				
RE (Note 1)	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z (Note 2)

RECEIVER SECTION			
RE (Note 1)	**DE**	**A-B**	**RO**
L	L	≥+0.2V	H
L	L	≤−0.2V	L
H	X	X	Z (Note 2)
L	L	OPEN (Note 1)	H

X = indeterminate

Z = TRI-STATE

Note 1: Non Terminated, Open Input only

Note 2: Device enters sleep mode if enable conditions are held > 600 ns, DE = L and RE (Note 1) = H.

National Semiconductor

DS485
Low Power RS-485/RS-422 Multipoint Transceiver

General Description

The DS485 is a low-power transceiver for RS-485 and RS-422 communication. The device contains one driver and one receiver. The drivers slew rate allows for operation up to 2.5 Mbps (see Applications Information section).

The transceiver draws 200 µA of supply current when unloaded or fully loaded with the driver disabled and operates from a single +5V supply.

The driver is short-circuit current limited and is protected against excessive power dissipation by thermal shutdown circuitry that places the driver outputs into TRI-STATE® (High Impedance state) under fault conditions. The driver guarantees a minimum of 1.5V differential output voltage with maximum loading across the common mode range (V_{OD3}).

The receiver has a failsafe feature that guarantees a logic-high output if the input is open circuit.

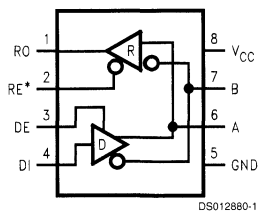
The DS485 is available in surface mount and DIP packages and is characterized for Industrial and Commercial temperature range operation.

Features

- Meets TIA/EIA RS-485 multipoint standard
- Guaranteed full load output voltage (V_{OD3})
- Low quiescent current: 200 µA typ
- −7V to +12V common-mode input voltage range
- TRI-STATE outputs on driver and receiver
- AC performance:
  - — Driver transition time: 25 ns typ
  - — Driver propagation delay: 40 ns typ
  - — Driver skew: 1 ns typ
  - — Receiver propagation delay: 200 ns typ
  - — Receiver skew: 20 ns typ
- Half-duplex flow through pinout
- Operates from a single 5V supply
- Allows up to 32 transceivers on the bus
- Current-limiting and thermal shutdown for driver overload protection
- Industrial temperature range operation
- Pin and functional compatible with MAX485 and LTC485

Connection and Logic Diagram

DIP and SOIC



DS012880-1

Order Number	Temp. Range	Package/###
DS485N	0°C to +70°C	DIP/N08E
DS485M	0°C to +70°C	SOP/M08A
DS485TN	−40°C to +85°C	DIP/N08E
DS485TM	−40°C to +85°C	SOP/M08A

DRIVER SECTION				
RE*	**DE**	**DI**	**A**	**B**
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z
RECEIVER SECTION				
RE*	**DE**	**A-B**		**RO**
L	L	≥+0.2V		H
L	L	≤−0.2V		L
H	X	X		Z
L	L	OPEN*		H

*Note: Non Terminated, Open Input only
X = indeterminate
Z = TRI-STATE

National Semiconductor

DS75176B/DS75176BT
Multipoint RS-485/RS-422 Transceivers

General Description

The DS75176B is a high speed differential TRI-STATE® bus/line transceiver designed to meet the requirements of EIA standard RS485 with extended common mode range (+12V to −7V), for multipoint data transmission. In addition, it is compatible with RS-422.

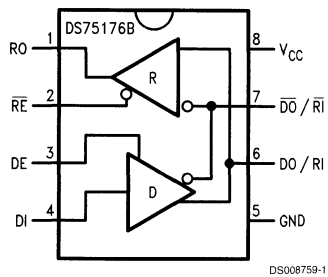
The driver and receiver outputs feature TRI-STATE capability, for the driver outputs over the entire common mode range of +12V to −7V. Bus contention or fault situations that cause excessive power dissipation within the device are handled by a thermal shutdown circuit, which forces the driver outputs into the high impedance state.

DC specifications are guaranteed over the 0 to 70°C temperature and 4.75V to 5.25V supply voltage range.

Features

- Meets EIA standard RS485 for multipoint bus transmission and is compatible with RS-422.
- Small Outline (SO) Package option available for minimum board space.
- 22 ns driver propagation delays.
- Single +5V supply.
- −7V to +12V bus common mode range permits ±7V ground difference between devices on the bus.
- Thermal shutdown protection.
- High impedance to bus with driver in TRI-STATE or with power off, over the entire common mode range allows the unused devices on the bus to be powered down.
- Pin out compatible with DS3695/A and SN75176A/B.
- Combined impedance of a driver output and receiver input is less than one RS485 unit load, allowing up to 32 transceivers on the bus.
- 70 mV typical receiver hysteresis.

Connection and Logic Diagram



Top View
Order Number DS75176BN, DS75176BTN, DS75176BM or DS75176BTM
See NS Package Number N08E or M08A

National Semiconductor

DS96172/DS96174
RS-485/RS-422 Quad Differential Line Drivers

General Description

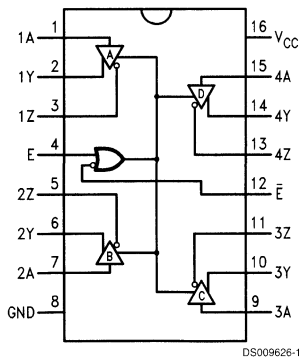
The DS96172 and DS96174 are high speed quad differential line drivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided and occurs at junction temperature of approximately 160°C. The DS96172 features an active high and active low Enable, common to all four drivers. The DS96174 features separate active high Enables for each driver pair. Compatible RS-485 receivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96173, DS96175, DS96176 AND DS96177.

Features

- Meets EIA Standard RS-485 and RS-422A
- Monotonic differential output switching
- Transmission rate to 10 Mbs
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7V to +12V
- Operates from single +5V supply
- Thermal shutdown protection
- DS96172/DS96174 are lead and function compatible with the SN75172/75174 or the AM26LS31/MC3487 respectively

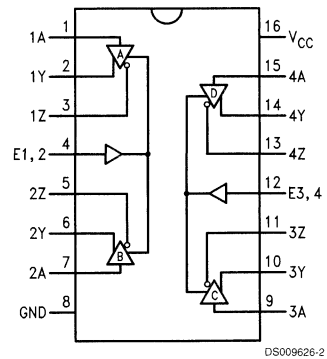
Connection Diagrams

16-Lead DIP
DS96172



Top View

16-Lead DIP
DS96174



Top View

Order Number DS96172CN or DS96174CN
See NS Package Number N16E

National Semiconductor

DS96173/DS96175
RS-485/RS-422 Quad Differential Line Receivers

General Description

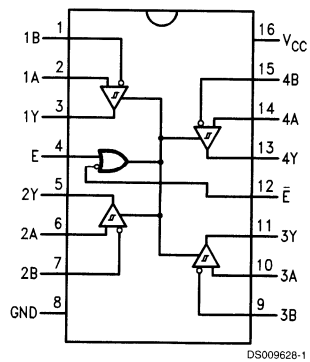
The DS96173 and DS96175 are high speed quad differential line receivers designed to meet EIA Standard RS-485. The devices have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 10 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96173 features an active high and active low Enable, common to all four receivers. The DS96175 features separate active high Enables for each receiver pair. Compatible RS-485 drivers, transceivers, and repeaters are also offered to provide optimum bus performance. The respective device types are DS96172, DS96174, DS96176 and DS96177.

Features

- Meets EIA Standard RS-485, RS-422A, RS-423A
- Designed for multipoint bus applications
- TRI-STATE Outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5V supply
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- DS96173/DS96175 are lead and function compatible with SN75173/75175 or the AM26LS32/MC3486 respectively

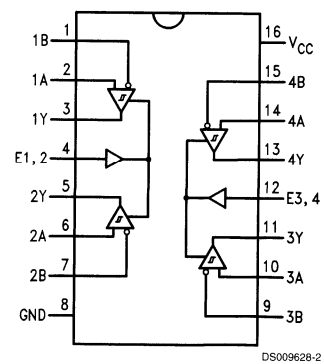
Connection Diagrams

16-Lead DIP
DS96173



DS009628-1

16-Lead DIP
DS96175



DS009628-2

Order Number DS96173CN or DS96175CN
See NS Package Number N16E

National Semiconductor

DS96176
RS-485/RS-422 Differential Bus Transceiver

General Description

The DS96176 Differential Bus Transceiver is a monolithic integrated circuit designed for bidirectional data communication on balanced multipoint bus transmission lines. The transceiver meets EIA Standard RS-485 as well as RS-422A.

The DS96176 combines a TRI-STATE® differential line driver and a differential input line receiver, both of which operate from a single 5.0V power supply. The driver and receiver have an active Enable that can be externally connected to function as a direction control. The driver differential outputs and the receiver differential inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or when V_{CC} = 0V. These ports feature wide positive and negative common mode voltage ranges, making the device suitable for multipoint applications in noisy environments.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive and negative current-limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at junction temperature of approximately 160°C. The receiver features a typical input impedance of 15 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

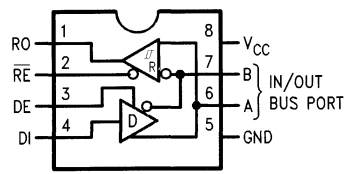
The DS96176 can be used in transmission line applications employing the DS96172 and the DS96174 quad differential line drivers and the DS96173 and DS96175 quad differential line receivers.

Features

- Bidirectional transceiver
- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission
- TRI-STATE driver and receiver enables
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- Driver output capability ±60 mA Maximum
- Thermal shutdown protection
- Driver positive and Negative current-limiting
- High impedance receiver input
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

Connection Diagram

8-Lead DIP



DS009630-1

Top View
Order Number DS96176CN
See NS Package Number N08E

Function Table

Driver

Input	Enable	Outputs	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

Receiver

Differential Inputs	Enable	Output
A-B	$\overline{RE}$	R
$V_{ID} \geq 0.2V$	L	H
$V_{ID} \leq -0.2V$	L	L
X	H	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

National Semiconductor

DS96177
RS-485/RS-422 Differential Bus Repeater

General Description

The DS96177 Differential Bus Repeater is a monolithic integrated device designed for one-way data communication on multipoint bus transmission lines. This device is designed for balanced transmission bus line applications and meets EIA Standard RS-485 and RS-422A. The device is designed to improve the performance of the data communication over long bus lines. The DS96177 has an active high Enable.

The DS96177 features positive and negative current limiting and TRI-STATE® outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −12V to +12V. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 160°C. The driver is designed to drive current loads up to 60 mA maximum.

The DS96177 is designed for optimum performance when used on transmission buses employing the DS96172 and DS96174 differential line drivers, DS96173 and DS96175 differential line receivers, or DS96176 differential bus transceivers.

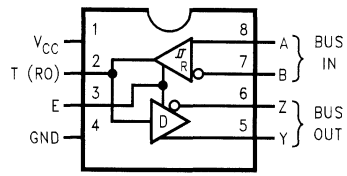
Features

- Meets EIA Standard RS-422A and RS-485
- Designed for multipoint transmission on long bus lines in noisy environments
- TRI-STATE outputs
- Bus voltage range −7.0V to +12V
- Positive and negative current limiting
- Driver output capability ±60 mA max
- Driver thermal shutdown protection
- Receiver input high impedance
- Receiver input sensitivity of ±200 mV
- Receiver input hysteresis of 50 mV typical
- Operates from single 5.0V supply
- Low power requirements

8

Connection Diagram

8-Lead Dual-In-Line Package



DS009644-1

Top View
Order Number DS96177CN
See NS Package Number N08E

Function Table

Differential Inputs	Enable	Outputs		
A−B	E	T	Y	Z
$V_{ID} \geq 0.2V$	H	H	H	L
$V_{ID} \leq -0.2V$	H	L	L	H
X	L	Z	Z	Z

Note: T is an output pin only, monitoring the BUS (RO).
H = High Level
L = Low Level
X = Immaterial
Z = High Impedance (off)

National Semiconductor

DS96F172M/DS96F174C/DS96F174M
EIA-485/EIA-422 Quad Differential Drivers

General Description

The DS96F172 and the DS96F174 are high speed quad differential line drivers designed to meet EIA-485 Standards. The DS96F172 and the DS96F174 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F172 and DS96F174 to operate at higher speeds while minimizing power consumption.

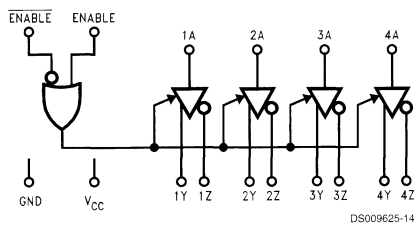
The DS96F172 and the DS96F174 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The drivers have wide positive and negative common mode range for multipoint applications in noisy environments. Positive and negative current-limiting is provided which protects the drivers from line fault conditions over a +12V to −7.0V common mode range. A thermal shutdown feature is also provided. The DS96F172 features an active high and active low Enable, common to all four drivers. The DS96F174 features separate active high Enables for each driver pair.

Features

- Meets EIA-485 and EIA-422 standards
- Monotonic differential output switching
- TRI-STATE outputs
- Designed for multipoint bus transmission
- Common mode output voltage range: −7.0V to +12V
- Operates from single +5.0V supply
- Reduced power consumption
- Thermal shutdown protection
- DS96F172 and DS96F174 are lead and function compatible with the SN75172/174 or the AM26LS31/MC3487
- Military temperature range available
- Qualified for MIL-STD-883C
- Standard military drawings available (SMD)
- Available in DIP (J), LCC (E), and Flatpak (W) packages

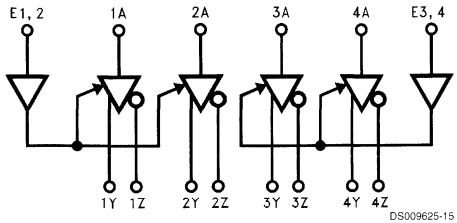
Logic Diagrams

DS96F172



DS009625-14

DS96F174



DS009625-15

Function Tables (Each Driver)

DS96F172

Input	Enable		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

DS96F174

Input	Enable	Outputs	
A	E	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High Level
L = Low Level
X = Don't Care
Z = High Impedance (Off)

National Semiconductor

DS96F173M/DS96F175C/DS96F175M
EIA-485/EIA-422 Quad Differential Receivers

General Description

The DS96F173 and the DS96F175 are high speed quad differential line receivers designed to meet the EIA-485 standard. The DS96F173 and the DS96F175 offer improved performance due to the use of L-FAST bipolar technology. The use of LFAST technology allows the DS96F173 and DS96F175 to operate at higher speeds while minimizing power consumption.

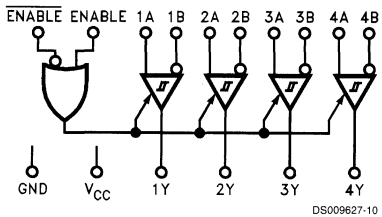
The DS96F173 and the DS96F175 have TRI-STATE® outputs and are optimized for balanced multipoint data bus transmission at rates up to 15 Mbps. The receivers feature high input impedance, input hysteresis for increased noise immunity, and input sensitivity of 200 mV over a common mode input voltage range of −7V to +12V. The receivers are therefore suitable for multipoint applications in noisy environments. The DS96F173 features an active high and active low Enable, common to all four receivers. The DS96F175 features separate active high Enables for each receiver pair.

Features

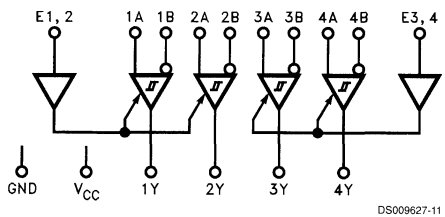
- Meets EIA-485, EIA-422A, EIA-423A standards
- Designed for multipoint bus applications
- TRI-STATE outputs
- Common mode input voltage range: −7V to +12V
- Operates from single +5.0V supply
- Reduced power consumption (I_{CC} = 50 mA max)
- Input sensitivity of ±200 mV over common mode range
- Input hysteresis of 50 mV typical
- High input impedance
- Military temperature range available
- Qualified for MIL STD 883C
- Available to standard military drawings (SMD)
- Available in DIP(J), LCC(E), and FlatPak (W) packages
- DS96F173 and DS96F175 are lead and function compatible with SN75173/175 or the AM26LS32/MC3486

8

Logic Diagrams



DS96F175



Function Tables

(Each Receiver) DS96F173

Differential Inputs A–B	Enable E	Enable $\overline{E}$	Output Y
$V_{ID} \geq 0.2V$	H	X	H
	X	L	H
$V_{ID} \leq -0.2V$	H	X	L
	X	L	L
X	L	X	Z
X	X	H	Z

H = High Level
L = Low Level
Z = High Impedance (off)
X = Don't Care

(Each Receiver) DS96F175

Differential Inputs A–B	Enable E	Output Y
$V_{ID} \geq 0.2V$	H	H
$V_{ID} \leq -0.2V$	H	L
X	L	Z

Section 9

Interface - LVDS Circuits

Section 9 Contents

National Semiconductor

Interface-LVDS Line Drivers and Receivers Selection Guide

Tx	Rx	Temp Range	Base Part Number	Page No.
0	1	Ind	DS90LV018A	9-11
0	2	Ind	DS90C402	9-35
0	2	Ind	DS90LV028A	9-16
0	4	Ind	DS90C032	9-26
0	4	Mil-883	DS90C032E	9-26
0	4	Ind	DS90C032B	9-24
0	4	Ind	DS90LV032A	9-28
0	4	Ind	DS90LV048A	9-32
1	0	Com	DS90LV017	9-9
1	0	Ind	DS90LV017A	9-10
2	0	Ind	DS90C401	9-34
2	0	Com	DS90LV027	9-14
2	0	Ind	DS90LV027A	9-15
4	0	Ind	DS90C031	9-18
4	0	Mil-883	DS90C031E	9-18
4	0	Ind	DS90C031B	9-17
4	0	Ind	DS90LV031A	9-20
4	0	Ind	DS90LV031B	9-22
4	0	Ind	DS90LV047A	9-30
1	1	Ind	DS90LV019	9-12
1	1	Ind	DS90LV001	9-8
2	2	Ind	DS90CP22	9-13
2	2	Com	DS36C200	9-36
10	1	Ind	DS90LV110	9-33

Temperature ranges:

Com = Commercial 0°C to +70°C

Ind = Industrial −40°C to +85°C

Mil-883 = Military 883 Qual −55°C to +125°C

Check WEB Site availability and options

National Semiconductor

Channel Link Selection Guide

Datasheets

Part Number	Transmitter/ Receiver	Max Data Throughout	Number of Bits	Page Number
+3.3V/112 MHz Family				
DS90CR481	Transmitter	5.37 Gbps	48	9-58
DS90CR483	Transmitter	5.37 Gbps	48	9-59
DS90CR484	Receiver	5.37 Gbps	48	9-59
+3.3V/85 MHz Family				
DS90CR287	Transmitter	2.38 Gbps	28	9-54
DS90CR288A	Receiver	2.38 Gbps	28	9-56
DS90CR217	Transmitter	1.78 Gbps	21	9-43
DS90CR218A	Receiver	1.78 Gbps	21	9-45
+3.3V/75 MHz Family				
DS90CR287	Transmitter	2.10 Gbps	28	9-54
DS90CR288	Receiver	2.10 Gbps	28	9-54
DS90CR217	Transmitter	1.57 Gbps	21	9-43
DS90CR218	Receiver	1.57 Gbps	21	9-43
+3.3V/66 MHz Family				
DS90CR285	Transmitter	1.84 Gbps	28	9-51
DS90CR286	Receiver	1.84 Gbps	28	9-51
DS90CR286A	Receiver	1.84 Gbps	28	9-53
DS90CR215	Transmitter	1.38 Gbps	21	9-41
DS90CR216	Receiver	1.38 Gbps	21	9-41
DS90CR216A	Receiver	1.38 Gbps	21	9-53
+5V/66 MHz Family				
DS90CR283	Transmitter	1.84 Gbps	28	9-49
DS90CR284	Receiver	1.84 Gbps	28	9-49
DS90CR213	Transmitter	1.38 Gbps	21	9-39
DS90CR214	Receiver	1.38 Gbps	21	9-39
+5V/40 MHz Family				
DS90CR281	Transmitter	1.12 Gbps	28	9-47
DS90CR282	Receiver	1.12 Gbps	28	9-47
DS90CR211	Transmitter	840 Mbps	21	9-37
DS90CR212	Receiver	840 Mbps	21	9-37

Application Notes

AN-XXXX	Title
AN-971	An Overview of LVDS Technology
AN-1035	PCB Design Guidelines for LVDS Technology
AN-1041	Channel Link Introduction
AN-1059	High Speed Transmission with LVDS Devices
AN-1084	Parallel Application of High Speed Link

Channel-Link Evaluation Boards

Evaluation boards are available for a nominal charge that demonstrate the basic operation of the Channel-Link chipsets. The evaluation boards can be ordered through National's distributors and come assembled with a transmitter board, receiver board, ribbon cable, and instructions.

ORDER NUMBERS	DESCRIPTION
CLINK5V21BT-66	5V, 21 bit device, 20-66MHz operation
CLINK3V21BT-66	3.3V, 21 bit device, 20-66MHz operation
CLINK5V28BT-66	5V, 28 bit device, 20-66MHz operation
CLINK3V28BT-66	3.3V, 28 bit device, 20-66MHz operation

National Semiconductor

Bus LVDS Selection Guide

Bus LVDS Transceiver and Repeater Products

Part No.	Function	Data Rate (Mbps)	# of Drivers	# of RECs	Power Supply (V_{CC})	Page No.
DS92LV010A	Transceiver	155	1	1	5V or 3.3V	9-61
DS92LV222A	2 CH MUXed Repeater	200	2	2	3.3V	9-71
DS92LV040A	4 CH Transceiver	155	4	4	3.3V	9-65
DS92LV090A	9 CH Transceiver	200	9	9	3.3V	9-66
SCAN92LV090	1149.1 (JTAG) Compliant DS92LV090	200	9	9	3.3V	9-68
DS92CK16	1:6 Clock Distribution	125	1	6	3.3V	9-62

All devices Industrial Temperature Range (−40°C to +85°C)

Bus LVDS Serializer/Deserializer Products

Part No.	Function	Data Rate (Mbps)	# of Data Bits	Clock Freq. (MHz)	Power Supply (V_{CC})	Page No.
DS92LV1021	Serializer	400	10	16–40	3.3V	9-72
DS92LV1210	Deserializer	400	10	16–40	3.3V	9-72
DS92LV1212A	Deserializer (Random Lock)	400	10	16–40	3.3V	9-75
DS92LV1023	Serializer	660	10	40–66	3.3V	9-87
DS92LV1224	Deserializer (Random Lock)	660	10	40–66	3.3V	9-87
SCAN921023	1149.1 (JTAG) Compliant DS92LV1023	660	10	40–66	3.3V	9-79
SCAN921224	1149.1 (JTAG) Compliant DS92LV1224	660	10	40–66	3.3V	9-79
SCAN921025	Serializer with 1149.1 (JTAG) and at-speed BIST	800	10	80	3.3V	9-83
SCAN921226	Deserializer with 1149.1 (JTAG) and at-speed BIST	800	10	80	3.3V	9-83
DS92LV1260	6 CH Integrated DS92LV1224 Deserializer	2400	6 x 10	20–40	3.3V	9-91
SCAN921260	Deserializer with 1149.1 (JTAG) and at-speed BIST	2400	6 x 10	20–40	3.3V	9-92
DS92LV8028	8 CH Integrated DS92LV1023 Serializer	5280	8 x 10	25–66	3.3V	9-93
DS92LV16	Serializer/Deserializer	2560	16	35–80	3.3V	9-64

All devices Industrial Temperature Range (−40°C to +85°C)

National Semiconductor

DS90LV001
3.3V LVDS-LVDS Buffer

General Description

The DS90LV001 LVDS-LVDS Buffer takes an LVDS input signal and provides an LVDS output signal. In many large systems, signals are distributed across backplanes, and one of the limiting factors for system speed is the 'stub length' or the distance between the transmission line and the unterminated receivers on individual cards. Although it is generally recognized that this distance should be as short as possible to maximize system performance, real-world packaging concerns often make it difficult to make the stubs as short as the designer would like.

The DS90LV001, available in the LLP (Leadless Leadframe Package) package, will allow the receiver to be placed very close to the main transmission line, thus improving system performance.

A wide input dynamic range will allow the DS90LV001 to receive differential signals from LVPECL as well as LVDS sources. This will allow the device to also fill the role of an LVPECL-LVDS translator.

An output enable pin is provided, which allows the user to place the LVDS output in TRI-STATE.

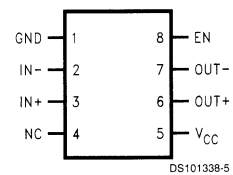
The DS90LV001 is offered in two package options, an 8 pin LLP and SOIC.

Features

- Single +3.3 V Supply
- LVDS receiver inputs accept LVPECL signals
- TRI-STATE outputs
- Receiver input threshold < ±100 mV
- Fast propagation delay of 1.4 ns (typ)
- Low jitter 800 Mbps fully differential data path
- 100 ps (typ) of pk-pk jitter with PRBS = $2^{23}-1$ data pattern at 800 Mbps
- Compatible with ANSI/TIA/EIA-644-A LVDS standard
- 8 pin SOIC and space saving (70%) LLP package
- Industrial Temperature Range

Connection Diagram

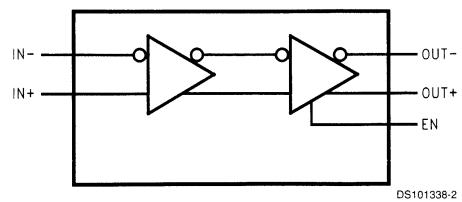
Top View



DS101338-5

Order Number DS90LV001TM, DS90LV001TLD
See NS Package Number M08A, LDA08A

Block Diagram



DS101338-2

National Semiconductor

DS90LV017
LVDS Single High Speed Differential Driver

General Description

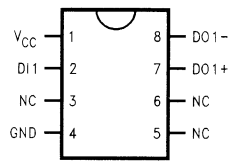
The DS90LV017 is a single LVDS driver device optimized for high data rate and low power applications. The DS90LV017 is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is in a 8-lead small Outline Package. The DS90LV017 has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its low output swings typically 340 mV.

Features

- Ultra Low Power Dissipation
- Operating Range above 155 Mbps
- Flow-through pinout simplifies PCB layout
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC Package Saves Space
- V_{CM} ±1V center around 1.2V
- Low Differential Output Swing Typical 340 mV
- Power Off Protection (outputs in high impedance)

Connection Diagram

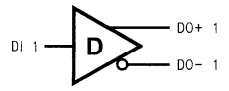
Dual-In-Line



DS012900-1

Order Number DS90LV017M
See NS Package Number M08A

Functional Diagram



DS012900-2

National Semiconductor

DS90LV017A
LVDS Single High Speed Differential Driver

General Description

The DS90LV017A is a single LVDS driver device optimized for high data rate and low power applications. The DS90LV017A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

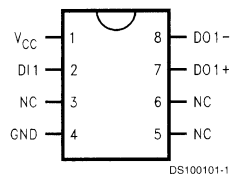
The device is in a 8-lead small outline package. The DS90LV017A has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 355 mV. The DS90LV017A can be paired with its companion single line receiver, the DS90LV018A, or with any of National's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Features

- >600 Mbps (300 MHz) switching rates
- 0.3 ns typical differential skew
- 0.7 ns maximum differential skew
- 1.5 ns maximum propagation delay
- 3.3V power supply design
- ±355 mV differential signaling
- Low power dissipation (23 mW @ 3.3V static)
- Flow-through design simplifies PCB layout
- Interoperable with existing 5V LVDS devices
- Power Off Protection (outputs in high impedance)
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC package saves space
- Industrial temperature operating range (−40°C to +85°C)

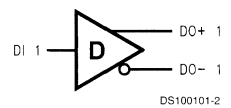
Connection Diagram

Dual-In-Line



Order Number DS90LV017ATM
See NS Package Number M08A

Functional Diagram



National Semiconductor

DS90LV018A
3V LVDS Single CMOS Differential Line Receiver

General Description

The DS90LV018A is a single CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV018A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver also supports open, shorted and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV018A has a flow-through design for easy PCB layout.

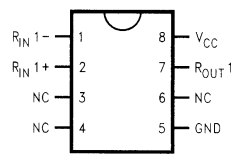
The DS90LV018A and companion LVDS line driver provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 50 ps differential skew (typical)
- 2.5 ns maximum propagation delay
- 3.3V power supply design
- Flow-through pinout
- Power down high impedance on LVDS inputs
- Low Power design (18mW @ 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) differential signal levels
- Supports open, short and terminated input fail-safe
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial temperature operating range (−40°C to +85°C)
- Available in SOIC package

Connection Diagram

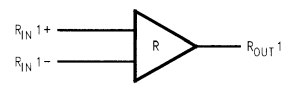
Dual-in-Line



DS100078-1

Order Number DS90LV018ATM
See NS Package Number M08A

Functional Diagram



DS100078-2

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L
Full Fail-safe OPEN/SHORT or Terminated	H

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National Semiconductor

DS90LV019
3.3V or 5V LVDS Driver/Receiver

General Description

The DS90LV019 is a Driver/Receiver designed specifically for the high speed low power point-to-point interconnect applications. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. The DS90LV019 features an independent driver and receiver with TTL/CMOS compatibility (D_{IN} and R_{OUT}). The logic interface provides maximum flexibility as 4 separate lines are provided (D_{IN}, DE, $\overline{RE}$, and R_{OUT}). The device also features a flow-through pin out which allows easy PCB routing for short stubs between its pins and the connector. The driver has 3.5 mA output loop current.

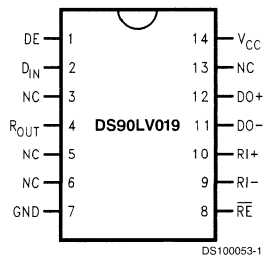
The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common-mode noise rejection.

The receiver threshold is ±100 mV over a ±1V common-mode range and translates the low swing differential levels to standard (TTL/CMOS) levels.

Features

- LVDS Signaling
- 3.3V or 5.0V operation
- Low power CMOS design
- Balanced Output Impedance
- Glitch free power up/down (Driver disabled)
- High Signaling Rate Capacity (above 100 Mbps)
- Ultra Low Power Dissipation
- ±1V Common-Mode Range
- ±100 mV Receiver Sensitivity
- Product offered in SOIC and TSSOP packages
- Flow-Through Pin Out
- Industrial Temperature Range Operation

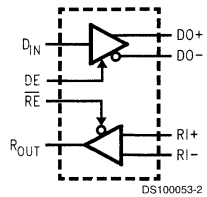
Connection Diagram



DS100053-1

Order Number DS90LV019TM or DS90LV019TMTC
See NS Package Number M14A or MTC14

Block Diagram



DS100053-2

National Semiconductor

DS90CP22
2X2 800 Mbps LVDS Crosspoint Switch

General Description

DS90CP22 is a 2x2 crosspoint switch utilizing LVDS (Low Voltage Differential Signaling) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The non-blocking design allows connection of any input to any output or outputs. LVDS I/O enable high speed data transmission for point-to-point interconnects. This device can be used as a high speed differential crosspoint, 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter. The mux and demux functions are useful for switching between primary and backup circuits in fault tolerant systems. The 1:2 signal splitter and 2:1 mux functions are useful for distribution of serial bus across several rack-mounted backplanes.

The DS90CP22 accepts LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

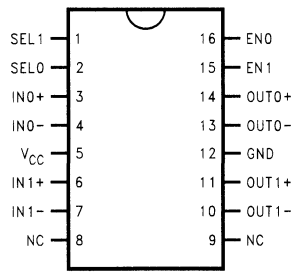
The individual LVDS outputs can be put into TRI-STATE by use of the enable pins.

For more details, please refer to the Application Information section of this datasheet.

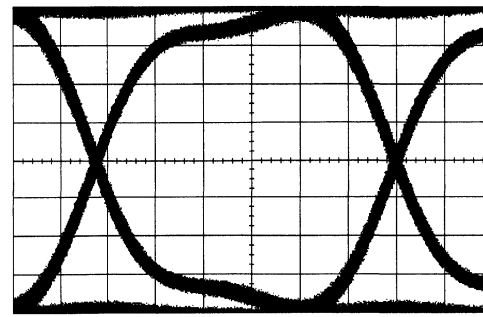
Features

- Low jitter 800 Mbps fully differential data path
- 75 ps (typ) of pk-pk jitter with PRBS = 2^{23}–1 data pattern at 800 Mbps
- Single +3.3 V Supply
- Less than 330 mW (typ) total power dissipation
- Non-blocking "Switch Architecture"
- Balanced output impedance
- Output channel-to-channel skew is 35 ps (typ)
- Configurable as 2:1 mux, 1:2 demux, repeater or 1:2 signal splitter
- LVDS receiver inputs accept LVPECL signals
- Fast switch time of 1.2ns (typ)
- Fast propagation delay of 1.3ns (typ)
- Receiver input threshold < ±100 mV
- 16 lead SOIC package
- Inter-operates with ANSI/TIA/EIA-644-1995 LVDS standard
- Operating Temperature: −40˚C to +85˚C

Connection Diagram



Order Number DS90CP22M-8
See NS Package Number M16A



DS101053-10

Diff. Output Eye-Pattern in 1:2 split mode @ 800 Mbps
Conditions: 3.3 V, PRBS = 2^{23}–1 data pattern,
V_{ID} = 300mV, V_{CM} = +1.2 V, 200 ps/div, 100 mV/div

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National Semiconductor

DS90LV027
LVDS Dual High Speed Differential Driver

General Description

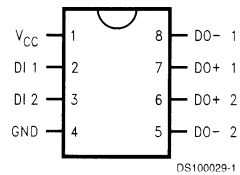
The DS90LV027 is a dual LVDS driver device optimized for high data rate and low power applications. The DS90LV027 is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is in a 8-lead small Outline Package. The DS90LV027 has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its low output swings typically 340 mV. Perfect for high speed transfer of clock and data. Pair with any of National's LVDS receivers.

Features

- Ultra Low Power Dissipation
- Operating Range above 155 Mbps
- Flow-through pinout simplifies PCB layout
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC Package Saves Space
- V_{CM} ±1V center around 1.2V
- Low Differential Output Swing Typical 340 mV
- Power Off Protection (outputs in high impedance)

Connection Diagram

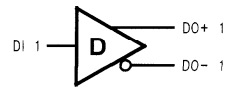
Dual-In-Line



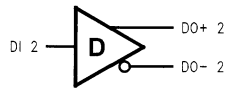
DS100029-1

Order Number DS90LV027M
See NS Package Number M08A

Functional Diagram



DS100029-2



DS100029-3

National Semiconductor

DS90LV027A
LVDS Dual High Speed Differential Driver

General Description

The DS90LV027A is a dual LVDS driver device optimized for high data rate and low power applications. The device is designed to support data rates in excess of 600Mbps (300MHz) utilizing Low Voltage Differential Signaling (LVDS) technology. The DS90LV027A is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized.

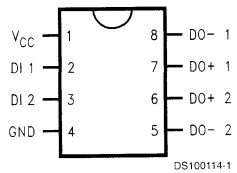
The device is in a 8-lead small outline package. The DS90LV027A has a flow-through design for easy PCB layout. The differential driver outputs provides low EMI with its typical low output swing of 360 mV. It is perfect for high speed transfer of clock and data. The DS90LV027A can be paired with its companion dual line receiver, the DS90LV028A, or with any of National's LVDS receivers, to provide a high-speed point-to-point LVDS interface.

Features

- >600 Mbps (300MHz) switching rates
- 0.3 ns typical differential skew
- 0.7 ns maximum differential skew
- 1.5 ns maximum propagation delay
- 3.3V power supply design
- ±360 mV differential signaling
- Low power dissipation (46 mW @ 3.3V static)
- Flow-through design simplifies PCB layout
- Interoperable with existing 5V LVDS devices
- Power Off Protection (outputs in high impedance)
- Conforms to TIA/EIA-644 Standard
- 8-Lead SOIC package saves space
- Industrial temperature operating range (−40°C to +85°C)

Connection Diagram

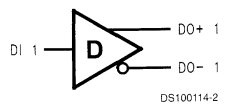
Dual-In-Line



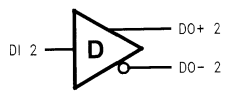
DS100114-1

Order Number DS90LV027ATM
See NS Package Number M08A

Functional Diagram



DS100114-2



DS100114-3

National Semiconductor

DS90LV028A
3V LVDS Dual CMOS Differential Line Receiver

General Description

The DS90LV028A is a dual CMOS differential line receiver designed for applications requiring ultra low power dissipation, low noise and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV028A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver also supports open, shorted and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV028Ahas a flow-through design for easy PCB layout.

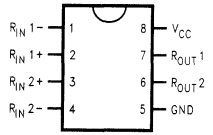
The DS90LV028A and companion LVDS line driver provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 50 ps differential skew (typical)
- 0.1 ns channel-to-channel skew (typical)
- 2.5 ns maximum propagation delay
- 3.3V power supply design
- Flow-through pinout
- Power down high impedance on LVDS inputs
- Low Power design (18mW @ 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) differential signal levels
- Supports open, short and terminated input fail-safe
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial temperature operating range (−40°C to +85°C)
- Available in SOIC package

Connection Diagram

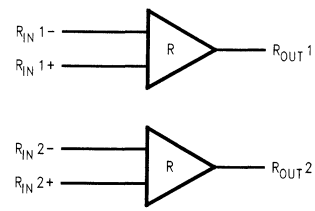
Dual-in-Line



DS100077-1

Order Number DS90LV028ATM
See NS Package Number M08A

Functional Diagram



DS100077-2

INPUTS	OUTPUT
$[R_{IN}+] - [R_{IN}-]$	R_{OUT}
$V_{ID} \geq 0.1V$	H
$V_{ID} \leq -0.1V$	L
Full Fail-safe OPEN/SHORT or Terminated	H

National Semiconductor

DS90C031B
LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031B is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031B accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11 mW typical.

In addition, the DS90C031B provides power-off high impedance LVDS outputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present.

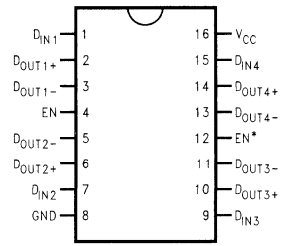
The DS90C031B and companion line receiver (DS90C032B) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- High impedance LVDS outputs with power-off
- ±350 mV differential signaling
- Ultra low power dissipation
- 400 ps maximum differential skew (5V, 25˚C)
- 3.5 ns maximum propagation delay
- Industrial operating temperature range
- Pin compatible with DS26C31, MB571 (PECL) and 41LG (PECL)
- Conforms to ANSI/TIA/EIA-644 LVDS standard
- Offered in narrow body SOIC package
- Fail-safe logic for floating inputs

Connection Diagram

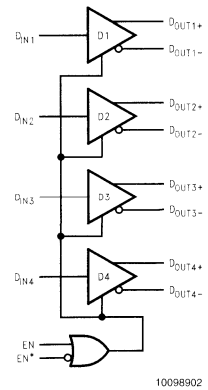
Dual-In-Line



10098901

Order Number DS90C031BTM
See NS Package Number M16A

Functional Diagram



10098902

Driver Truth Table

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

National Semiconductor

DS90C031
LVDS Quad CMOS Differential Line Driver

General Description

The DS90C031 is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C031 accepts TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 11 mW typical.

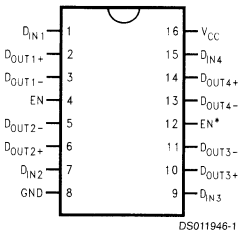
The DS90C031 and companion line receiver (DS90C032) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- ±350 mV differential signaling
- Ultra low power dissipation
- 400 ps maximum differential skew (5V, 25˚C)
- 3.5 ns maximum propagation delay
- Industrial operating temperature range
- Military operating temperature range option
- Available in surface mount packaging (SOIC) and (LCC)
- Pin compatible with DS26C31, MB571 (PECL) and 41LG (PECL)
- Compatible with IEEE 1596.3 SCI LVDS standard
- Conforms to ANSI/TIA/EIA-644 LVDS standard
- Available to Standard Microcircuit Drawing (SMD) 5962-95833

Connection Diagrams

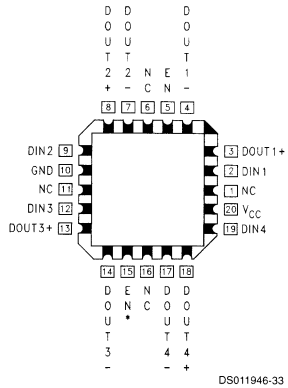
Dual-In-Line



DS011946-1

Order Number DS90C031TM
See NS Package Number M16A

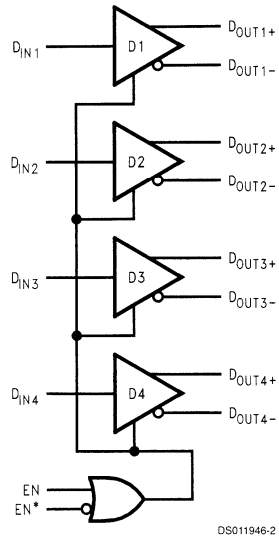
LCC Package



DS011946-33

Order Number DS90C031E-QML
See NS Package Number E20A
For Complete Military Specifications, refer to appropriate SMD or MDS.

Functional Diagram



DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

National Semiconductor

DS90LV031A
3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV031A is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical.

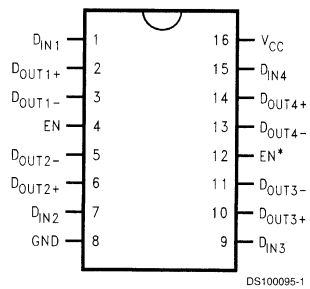
The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031A and companion line receiver (DS90LV032A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 0.1 ns typical differential skew
- 0.4 ns maximum differential skew
- 2.0 ns maximum propagation delay
- 3.3V power supply design
- ±350 mV differential signaling
- Low power dissipation (13mW at 3.3V static)
- Interoperable with existing 5V LVDS devices
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with TIA/EIA-644 LVDS standard
- Industrial and Military operating temperature range
- Available in SOIC, TSSOP and Cerpack surface mount packaging
- Standard Microcircuit Drawing (SMD) 5962-9865201

Connection Diagram

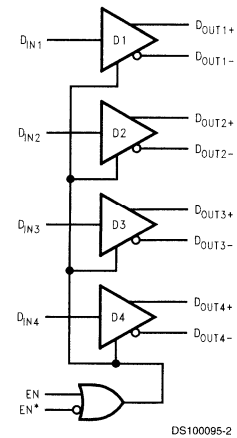
Dual-In-Line



DS100095-1

Order Number DS90LV031ATM
or DS90LV031ATMTC
or DS90LV031AW
See NS Package Number M16A or MTC16 or W16A

Functional Diagram



DS100095-2

Truth Table

DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

National Semiconductor

DS90LV031B
3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV031B is a quad CMOS differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV031B accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical. The DS90LV031B is enhanced over the DS90LV031A in that the inputs are further ruggedized for excessive undershoot.

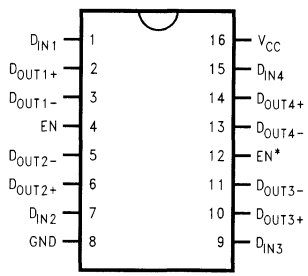
The EN and EN* inputs allow active Low or active High control of the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV031B and companion line receiver (DS90LV032A) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 0.1 ns typical differential skew
- 0.4 ns maximum differential skew
- 2.0 ns maximum propagation delay
- Ruggedized inputs that can withstand excessive undershoot
- 3.3V power supply design
- ±350 mV differential signaling
- Low power dissipation (13mW at 3.3V static)
- Interoperable with existing 5V LVDS devices
- Compatible with IEEE 1596.3 SCI LVDS standard
- Compatible with TIA/EIA-644 LVDS standard
- Industrial temperature operating range
- Available in SOIC and TSSOP surface mount packaging

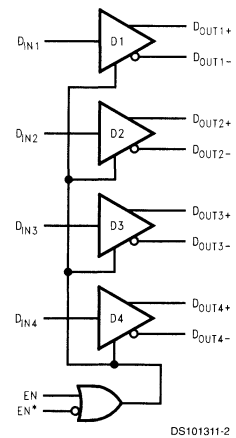
Connection Diagram

Dual-In-Line



Order Number DS90LV031BTM
or DS90LV031BTMTC
See NS Package Number M16A or MTC16

Functional Diagram



Truth Table

DRIVER

Enables		Input	Outputs	
EN	**EN***	**D_{IN}**	**D_{OUT+}**	**D_{OUT-}**
L	H	X	Z	Z
All other combinations of ENABLE inputs		L	L	H
		H	H	L

National Semiconductor

DS90C032B
LVDS Quad CMOS Differential Line Receiver

General Description

The DS90C032B is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C032B accepts low voltage (350 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN and terminated (100Ω) input Fail-safe. Receiver output will be HIGH for both Fail-safe conditions.

The DS90C032B provides power-off high impedance LVDS inputs. This feature assures minimal loading effect on the LVDS bus lines when V_{CC} is not present.

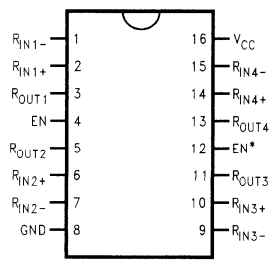
The DS90C032B and companion line driver (DS90C031B) provide a new alternative to high power pseudo-ECL devices for high speed point-to-point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- Accepts small swing (350 mV) differential signal levels
- High Impedance LVDS inputs with power down
- Ultra low power dissipation
- 600 ps maximum differential skew (5V, 25˚C)
- 6.0 ns maximum propagation delay
- Industrial operating temperature range
- Available in surface mount packaging (SOIC)
- Pin compatible with DS26C32A, MB570 (PECL) and 41LF (PECL)
- Supports OPEN and terminated input fail-safe
- Conforms to ANSI/TIA/EIA-644 LVDS standard

Connection Diagram

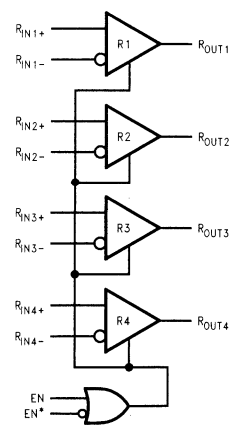
Dual-In-Line



DS100990-1

Order Number DS90C032BTM See NS Package Number M16A

Functional Diagram



DS100990-2

Receiver Truth Table

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Fail-safe OPEN or Terminated	H

National Semiconductor

DS90C032
LVDS Quad CMOS Differential Line Receiver

General Description

The DS90C032 is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 155.5 Mbps (77.7 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90C032 accepts low voltage (350 mV) differential input signals and translates them to CMOS (TTL compatible) output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports OPEN, shorted and terminated (100Ω) input Fail-safe. Receiver output will be HIGH for all fail-safe conditions.

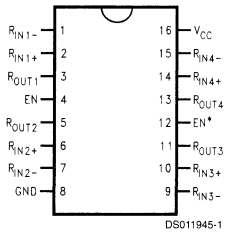
The DS90C032 and companion line driver (DS90C031) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- >155.5 Mbps (77.7 MHz) switching rates
- Accepts small swing (350 mV) differential signal levels
- Ultra low power dissipation
- 600 ps maximum differential skew (5V, 25°C)
- 6.0 ns maximum propagation delay
- Industrial operating temperature range
- Military operating temperature range option
- Available in surface mount packaging (SOIC) and (LCC)
- Pin compatible with DS26C32A, MB570 (PECL) and 41LF (PECL)
- Supports OPEN, short and terminated input fail-safe
- Compatible with IEEE 1596.3 SCI LVDS standard
- Conforms to ANSI/TIA/EIA-644 LVDS standard
- Available to Standard Microcircuit Drawing (SMD) 5962-95834

Connection Diagrams

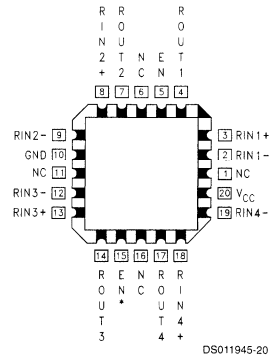
Dual-In-Line



DS011945-1

Order Number
DS90C032TM
See NS Package Number M16A

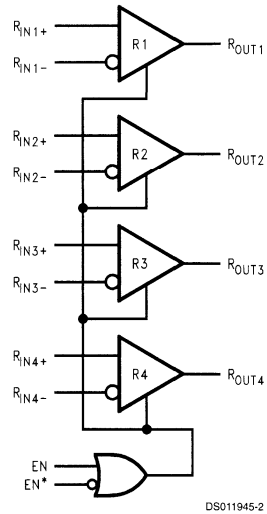
LCC Package



DS011945-20

Order Number
DS90C032E-QML
See NS Package Number E20A
For complete Military Specifications, refer to appropriate SMD or MDS.

Functional Diagram and Truth Tables



RECEIVER

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

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National Semiconductor

DS90LV032A
3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV032A is a quad CMOS differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV032A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input Fail-safe. The receiver output will be HIGH for all fail-safe conditions.

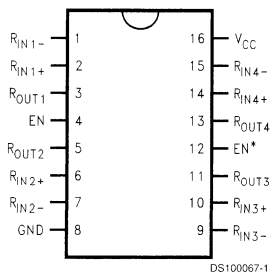
The DS90LV032A and companion LVDS line driver (eg. DS90LV031A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- 0.1 ns channel-to-channel skew (typical)
- 0.1 ns differential skew (typical)
- 3.3 ns maximum propagation delay
- 3.3V power supply design
- Power down high impedance on LVDS inputs
- Low Power design (40mW @ 3.3V static)
- Interoperable with existing 5V LVDS networks
- Accepts small swing (350 mV typical) VID
- Supports open, short and terminated input fail-safe
- Compatible with ANSI/TIA/EIA-644
- Industrial temp. operating range (-40°C to +85°C)
- Available in SOIC and TSSOP Packaging

Connection Diagram

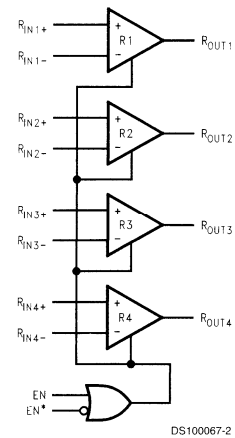
Dual-in-Line



DS100067-1

Order Number DS90LV032ATM
or DS90LV032ATMTC
See NS Package Number M16A or MTC16

Functional Diagram



DS100067-2

Truth Table

ENABLES		INPUTS	OUTPUT
EN	EN*	$R_{IN+} - R_{IN-}$	R_{OUT}
L	H	X	Z
All other combinations of ENABLE inputs		$V_{ID} \geq 0.1V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H

National Semiconductor

DS90LV047A
3V LVDS Quad CMOS Differential Line Driver

General Description

The DS90LV047A is a quad CMOS flow-through differential line driver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV047A accepts low voltage TTL/CMOS input levels and translates them to low voltage (350 mV) differential output signals. In addition, the driver supports a TRI-STATE® function that may be used to disable the output stage, disabling the load current, and thus dropping the device to an ultra low idle power state of 13 mW typical. The DS90LV047A has a flow-through pinout for easy PCB layout.

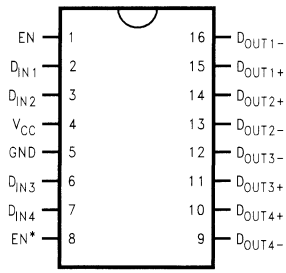
The EN and EN* inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four drivers. The DS90LV047A and companion line receiver (DS90LV048A) provide a new alternative to high power psuedo-ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- 300 ps typical differential skew
- 400 ps maximum differential skew
- 1.7 ns maximum propagation delay
- 3.3V power supply design
- ±350 mV differential signaling
- Low power dissipation (13mW at 3.3V static)
- Interoperable with existing 5V LVDS receivers
- High impedance on LVDS outputs on power down
- Conforms to TIA/EIA-644 LVDS Standard
- Industrial operating temperature range (−40°C to +85°C)
- Available in surface mount (SOIC) and low profile TSSOP package

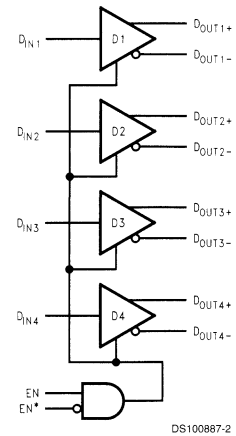
Connection Diagram

Dual-In-Line



Order Number DS90LV047ATM, DS90LV047ATMTC
See NS Package Number M16A, MTC16

Functional Diagram



Truth Table

ENABLES		INPUT	OUTPUTS	
EN	EN*	D_{IN}	D_{OUT+}	D_{OUT-}
H	L or Open	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z

National Semiconductor

DS90LV048A
3V LVDS Quad CMOS Differential Line Receiver

General Description

The DS90LV048A is a quad CMOS flow-through differential line receiver designed for applications requiring ultra low power dissipation and high data rates. The device is designed to support data rates in excess of 400 Mbps (200 MHz) utilizing Low Voltage Differential Signaling (LVDS) technology.

The DS90LV048A accepts low voltage (350 mV typical) differential input signals and translates them to 3V CMOS output levels. The receiver supports a TRI-STATE® function that may be used to multiplex outputs. The receiver also supports open, shorted and terminated (100Ω) input fail-safe. The receiver output will be HIGH for all fail-safe conditions. The DS90LV048A has a flow-through pinout for easy PCB layout.

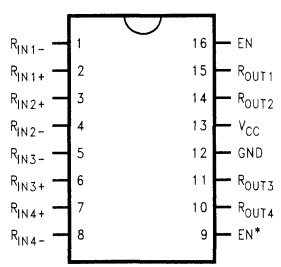
The EN and EN* inputs are ANDed together and control the TRI-STATE outputs. The enables are common to all four receivers. The DS90LV048A and companion LVDS line driver (eg. DS90LV047A) provide a new alternative to high power PECL/ECL devices for high speed point-to-point interface applications.

Features

- >400 Mbps (200 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- 150 ps channel-to-channel skew (typical)
- 100 ps differential skew (typical)
- 2.7 ns maximum propagation delay
- 3.3V power supply design
- High impedance LVDS inputs on power down
- Low Power design (40mW @ 3.3V static)
- Interoperable with existing 5V LVDS drivers
- Accepts small swing (350 mV typical) differential signal levels
- Supports open, short and terminated input fail-safe
- 0V to −100mV threshold region
- Conforms to ANSI/TIA/EIA-644 Standard
- Industrial temperature operating range (-40°C to +85°C)
- Available in SOIC and TSSOP package

Connection Diagram

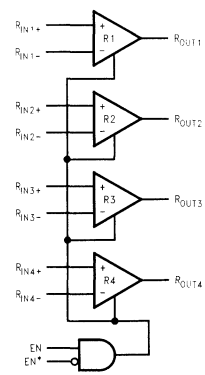
Dual-in-Line



10088801

Order Number DS90LV048ATM, DS90LV048ATMTC
See NS Package Number M16A, MTC16

Functional Diagram



10088802

Truth Table

ENABLES		INPUTS	OUTPUT
EN	**EN***	**$R_{IN+} - R_{IN-}$**	**R_{OUT}**
H	L or Open	$V_{ID} \geq 0V$	H
		$V_{ID} \leq -0.1V$	L
		Full Fail-safe OPEN/SHORT or Terminated	H
All other combinations of ENABLE inputs		X	Z

National Semiconductor

DS90LV110T
1 to 10 LVDS Data/Clock Distributor

General Description

DS90LV110 is a 1 to 10 data/clock distributor utilizing LVDS (Low Voltage Differential Signaling) technology for low power, high speed operation. Data paths are fully differential from input to output for low noise generation and low pulse width distortion. The design allows connection of 1 input to all 10 outputs. LVDS I/O enable high speed data transmission for point-to-point interconnects. This device can be used as a high speed differential 1 to 10 signal distribution / fanout replacing multi-drop bus applications for higher speed links with improved signal quality. It can also be used for clock distribution up to 400MHz.

The DS90LV110 accepts LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

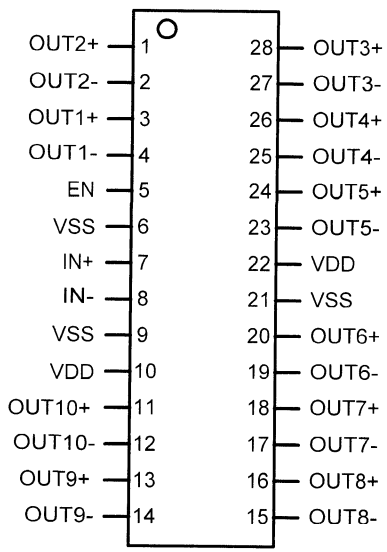
The LVDS outputs can be put into TRI-STATE by use of the enable pin.

For more details, please refer to the Application Information section of this datasheet.

Features

- Low jitter 800 Mbps fully differential data path
- 145 ps (typ) of pk-pk jitter with PRBS = 2^{23}–1 data pattern at 800 Mbps
- Single +3.3 V Supply
- Less than 413 mW (typ) total power dissipation
- Balanced output impedance
- Output channel-to-channel skew is 35ps (typ)
- Differential output voltage (V_{OD}) is 320mV (typ) with 100Ω termination load.
- LVDS receiver inputs accept LVPECL signals
- Fast propagation delay of 2.8 ns (typ)
- Receiver input threshold < ±100 mV
- 28 lead TSSOP package
- Conforms to ANSI/TIA/EIA-644 LVDS standard

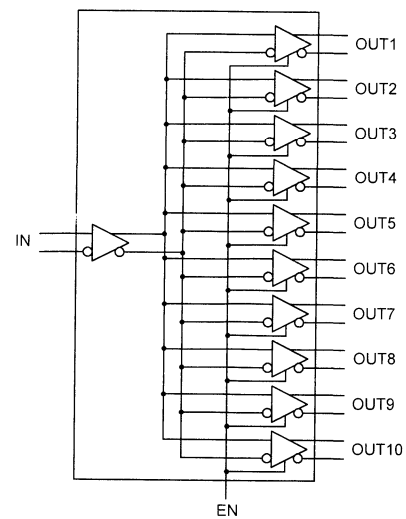
Connection Diagram



10133705

Order Number DS90LV110TMTC
See NS Package Number MTC28

Block Diagram



10133701

9

National Semiconductor

DS90C401
Dual Low Voltage Differential Signaling (LVDS) Driver

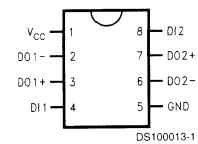
1.0 General Description

The DS90C401 is a dual driver device optimized for high data rate and low power applications. This device along with the DS90C402 provides a pair chip solution for a dual high speed point-to-point interface. The DS90C401 is a current mode driver allowing power dissipation to remain low even at high frequency. In addition, the short circuit fault current is also minimized. The device is in a 8 lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 340 mV.

2.0 Features

- Ultra low power dissipation
- Operates above 155.5 Mbps
- Standard TIA/EIA-644
- 8 Lead SOIC Package saves space
- Low Differential Output Swing typical 340 mV

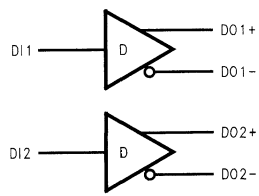
3.0 Connection Diagram



DS100013-1

Order Number DS90C401M
See NS Package Number M08A

4.0 Functional Diagram



DS100013-2

National Semiconductor

DS90C402
Dual Low Voltage Differential Signaling (LVDS) Receiver

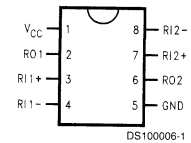
1.0 General Description

The DS90C402 is a dual receiver device optimized for high data rate and low power applications. This device along with the DS90C401 provides a pair chip solution for a dual high speed point-to-point interface. The device is in a PCB space saving 8 lead small outline package. The receiver offers ±100 mV threshold sensitivity, in addition to common-mode noise protection.

2.0 Features

- Ultra Low Power Dissipation
- Operates above 155.5 Mbps
- Standard TIA/EIA-644
- 8 Lead SOIC Package saves PCB space
- V_{CM} ±1V center around 1.2V
- ±100 mV Receiver Sensitivity

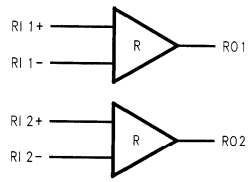
3.0 Connection Diagram



DS100006-1

Order Number DS90C402M
See NS Package Number M08A

4.0 Functional Diagram



DS100006-2

National Semiconductor

DS36C200
Dual High Speed Bi-Directional Differential Transceiver

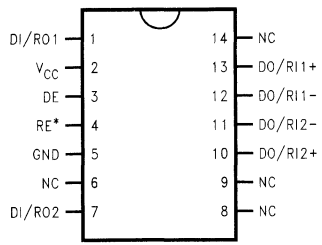
General Description

The DS36C200 is a dual transceiver device optimized for high data rate and low power applications. This device provides a single chip solution for a dual high speed bi-directional interface. Also, both control pins may be routed together for single bit control of datastreams. Both control pins are adjacent to each other for ease of routing them together. The DS36C200 is compatible with IEEE 1394 physical layer and may be used as an economical solution with some considerations. Please reference the application information on 1394 for more information. The device is in a 14-lead small outline package. The differential driver outputs provides low EMI with its low output swings typically 210 mV. The receiver offers ±100 mV threshold sensitivity, in addition to common-mode noise protection.

Features

- Optimized for DSS to DVHS interface link
- Compatible IEEE 1394 signaling voltage levels
- Operates above 100 Mbps
- Bi-directional transceivers
- 14-lead SOIC package
- Ultra low power dissipation
- ±100 mV receiver sensitivity
- Low differential output swing typical 210 mV
- High impedance during power off

Connection Diagram

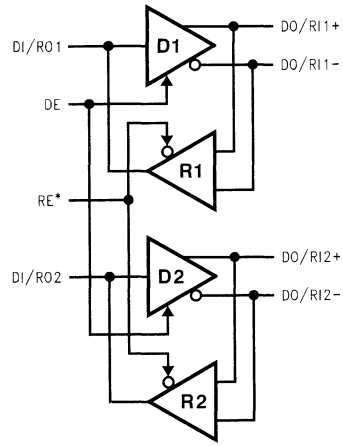


01262101

Order Number DS36C200M
See NS Package Number M14A

Note: * denotes active LOW pin

Functional Diagram



01262102

National Semiconductor

DS90CR211/DS90CR212
21-Bit Channel Link

General Description

The DS90CR211 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR212 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 21 bits of TTL data are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 840 Mbit/s(105 Mbyte/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data bus and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, providing a system cost savings, reduces connector physical size, and reduces shielding requirements due to the cables smaller form factor.

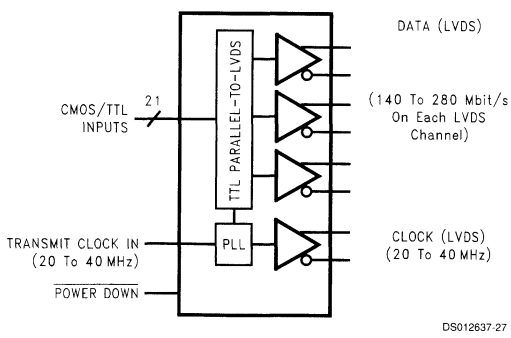
The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, 5 4-bit nibbles plus 1 control, or 2 9-bit (byte + parity) and 3 control.

Features

- Narrow bus reduces cable size and cost
- ±1V Common mode range (ground shifting)
- 290 mV swing LVDS data transmission
- 840 Mbit/s data throughput
- Low swing differential current mode drivers reduce EMI
- Rising edge data strobe
- Power down mode
- Offered in low profile 48-lead TSSOP package

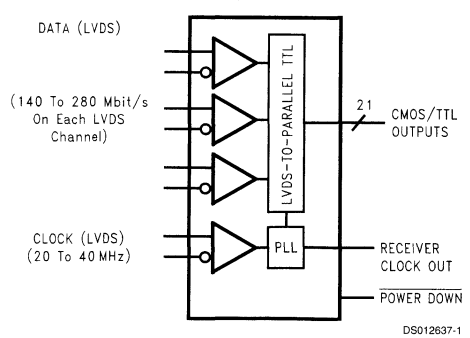
Block Diagrams

DS90CR211



Order Number DS90CR211MTD
See NS Package Number MTD48

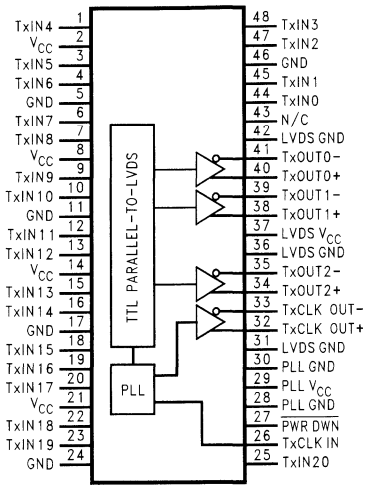
DS90CR212



Order Number DS90CR212MTD
See NS Package Number MTD48

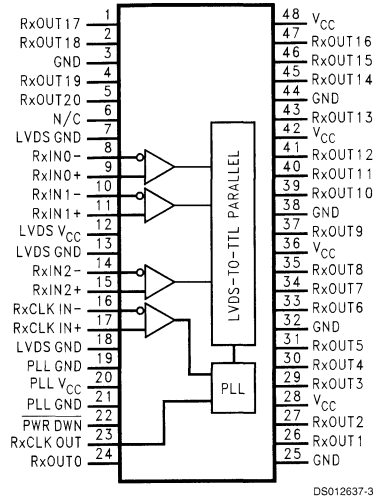
Connection Diagrams

DS90CR211



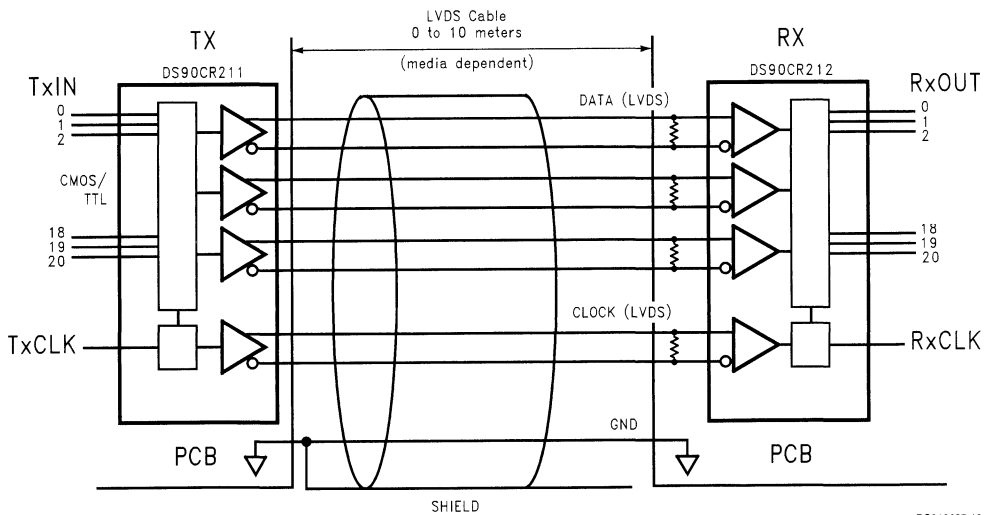
DS012637-2

DS90CR212



DS012637-3

Typical Application



DS012637-19

National Semiconductor

DS90CR213/DS90CR214
21-Bit Channel Link—66 MHz

General Description

The DS90CR213 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR214 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 21 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.386 Gbit/s (173 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cable's smaller form factor.

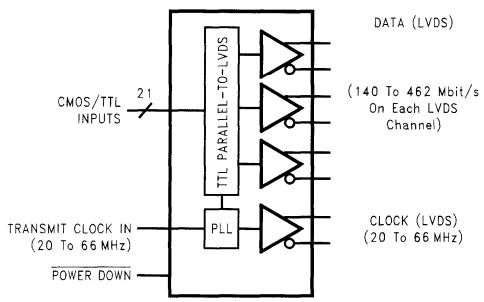
The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, 5 4-bit nibbles (byte + parity) or 2 9-bit (byte + 3 parity) and 1 control.

Features

- 66 MHz Clock Support
- Up to 173 Mbytes/s bandwidth
- Low power CMOS design (<610 mW)
- Power-down mode (<0.5 mW total)
- Up to 1.386 Gbit/s data throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS Standard

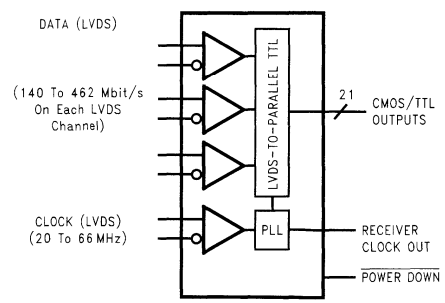
Block Diagrams

DS90CR213



Order Number DS90CR213MTD
See NS Package Number MTD48

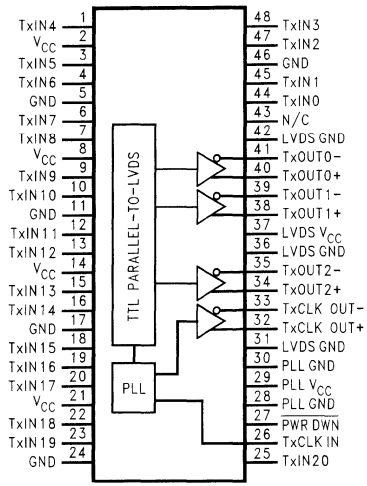
DS90CR214



Order Number DS90CR214MTD
See NS Package Number MTD48

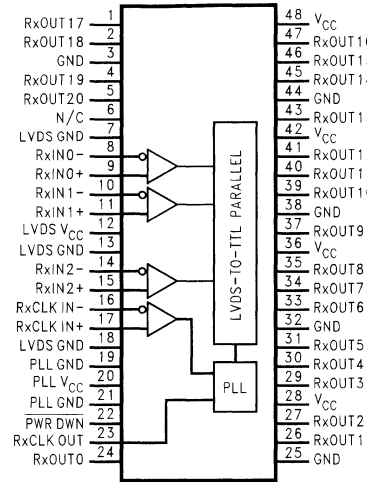
Pin Diagrams

DS90CR213



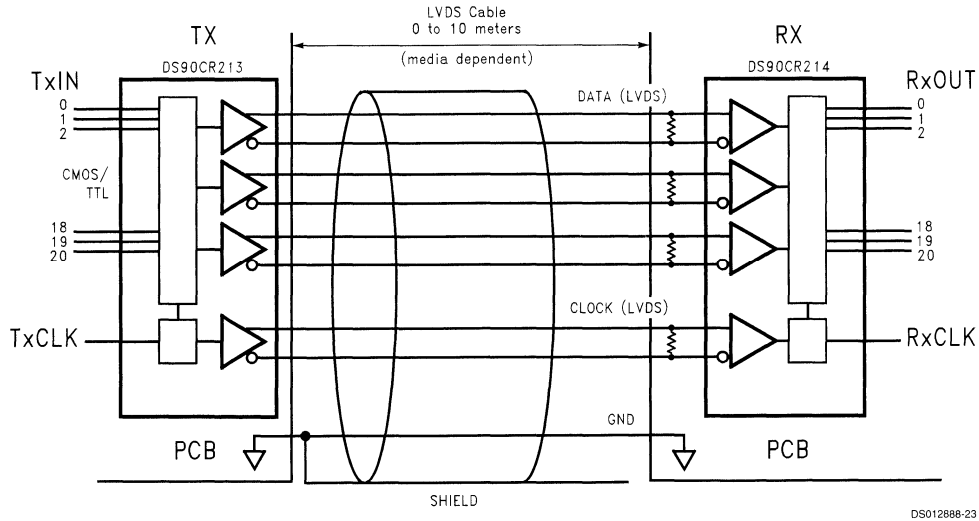
DS012888-21

DS90CR214



DS012888-22

Typical Application



DS012888-23

National Semiconductor

DS90CR215/DS90CR216
+3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link - 66 MHz

General Description

The DS90CR215 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR216 receiver converts the LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 21 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.386 Gbit/s (173 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 21-bit wide data and one clock, up to 44 conductors are required. With the Channel Link chipset as few as 9 conductors (3 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 21 CMOS/TTL inputs can support a variety of signal combinations. For example, five 4-bit nibbles plus 1 control, or two 9-bit (byte + parity) and 3 control.

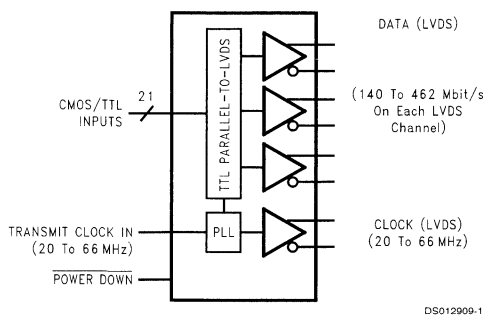
Features

- Single +3.3V supply
- Chipset (Tx + Rx) power consumption <250 mW (typ)
- Power-down mode (<0.5 mW total)
- Up to 173 Megabytes/sec bandwidth
- Up to 1.386 Gbps data throughput
- Narrow bus reduces cable size
- 290 mV swing LVDS devices for low EMI
- +1V common mode range (around +1.2V)
- PLL requires no external components
- Low profile 48-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- ESD Rating > 7 kV
- Operating Temperature: −40°C to +85°C

9

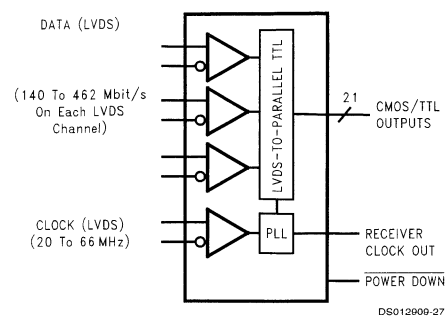
Block Diagrams

DS90CR215



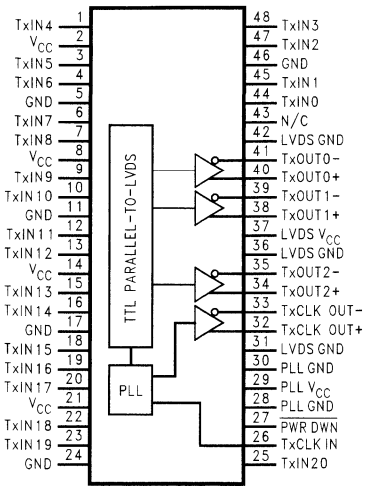
Order Number DS90CR215MTD
See NS Package Number MTD48

DS90CR216

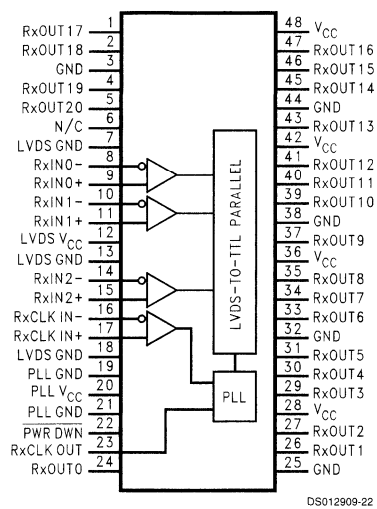


Order Number DS90CR216MTD
See NS Package Number MTD48

Pin Diagrams

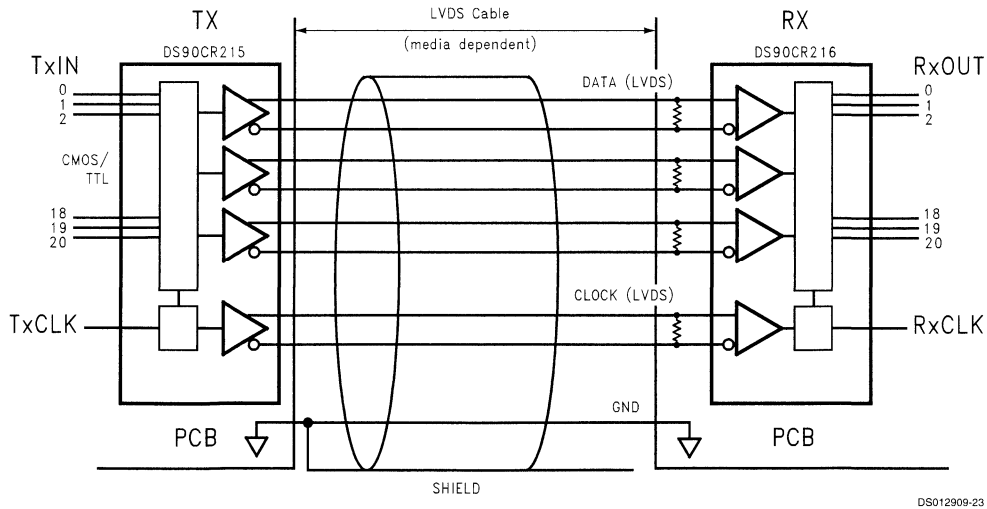


DS90CR215



DS90CR216

Typical Application



National Semiconductor

DS90CR217/DS90CR218
+3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link - 75 MHz

General Description

The DS90CR217 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR218 receiver converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 75 MHz, 21 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75 MHz clock, the data throughput is 1.575 Gbit/s (197 Mbytes/sec).

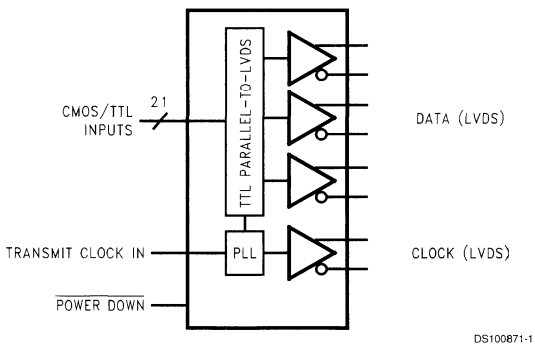
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 75 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best-in-Class Set & Hold Times on TxINPUTs and RxOUTPUTs
- Low power consumption
- Tx + Rx Powerdown mode <400µW (max)
- ±1V common-mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 1.575 Gbps throughput
- Up to 197 Mbytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 48-lead TSSOP package

Block Diagrams

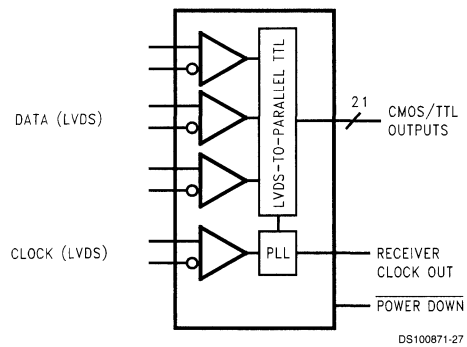
DS90CR217



DS100871-1

Order Number DS90CR217MTD
See NS Package Number MTD48

DS90CR218

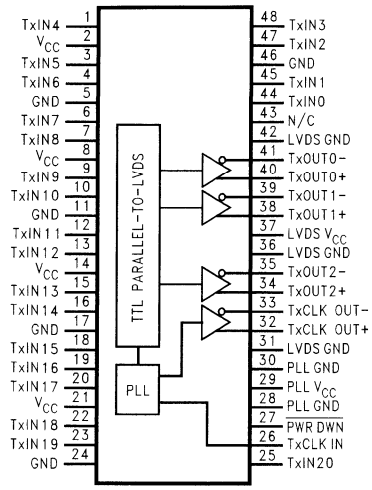


DS100871-27

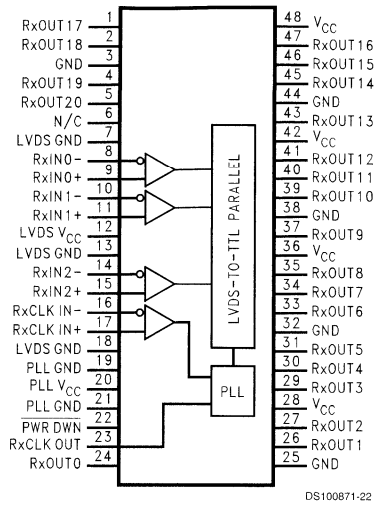
Order Number DS90CR218MTD
See NS Package Number MTD48

9

Pin Diagrams

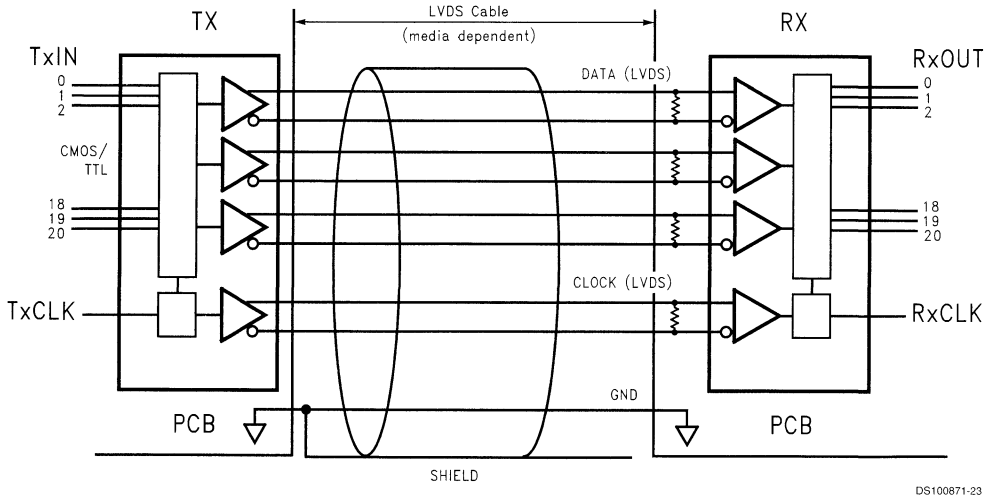


DS90CR217



DS90CR218

Typical Application



National Semiconductor

DS90CR217/DS90CR218A
+3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link - 85 MHz

General Description

The DS90CR217 transmitter converts 21 bits of CMOS/TTL data into three LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fourth LVDS link. Every cycle of the transmit clock 21 bits of input data are sampled and transmitted. The DS90CR218A receiver converts the three LVDS data streams back into 21 bits of CMOS/TTL data. At a transmit clock frequency of 85 MHz, 21 bits of TTL data are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 1.785 Gbit/s (223 Mbytes/sec).

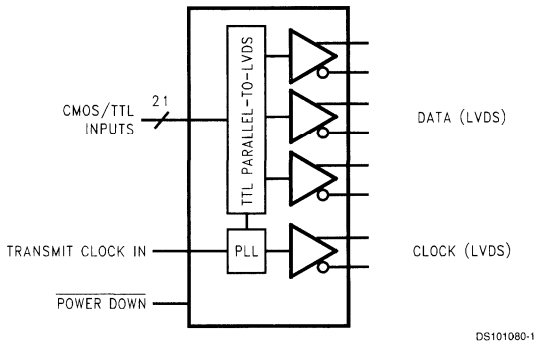
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 85 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best-in-Class Set & Hold Times on TxINPUTs
- Low power consumption
- ±1V common-mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 1.785 Gbps throughput
- Up to 223 Mbytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 48-lead TSSOP package

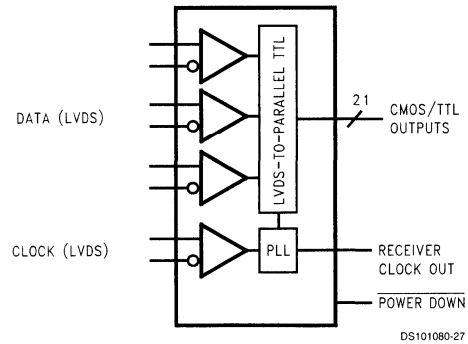
Block Diagrams

DS90CR217



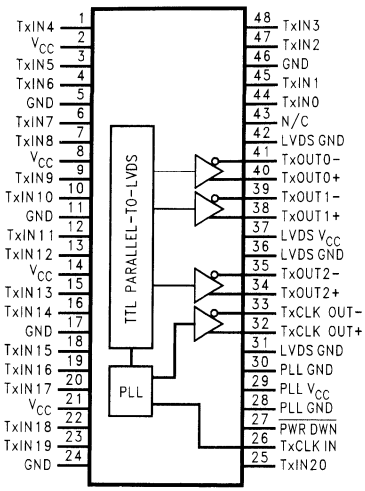
Order Number DS90CR217MTD
See NS Package Number MTD48

DS90CR218A

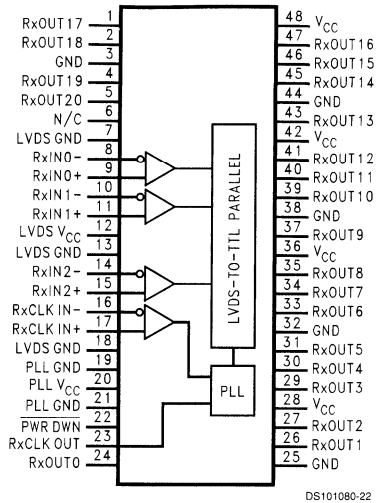


Order Number DS90CR218AMTD
See NS Package Number MTD48

Pin Diagrams

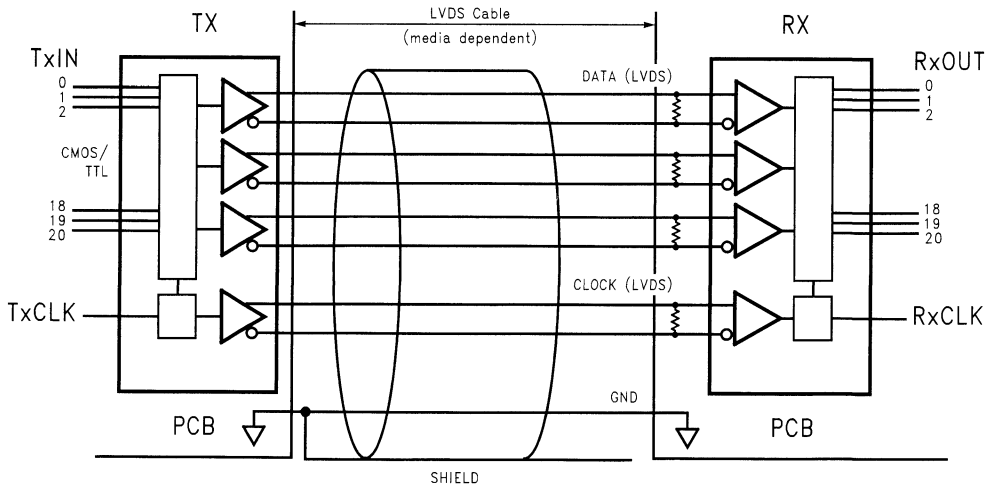


DS90CR217



DS90CR218A

Typical Application



National Semiconductor

DS90CR281/DS90CR282
28-Bit Channel Link

General Description

The DS90CR281 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR282 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 40 MHz, 28 bits of TTL data are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 1.12 Gbit/s (140 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 28-bit wide data bus and one clock, up to 58 conductors are required. With the Channel Link chipset as few as 11 conductors (4 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

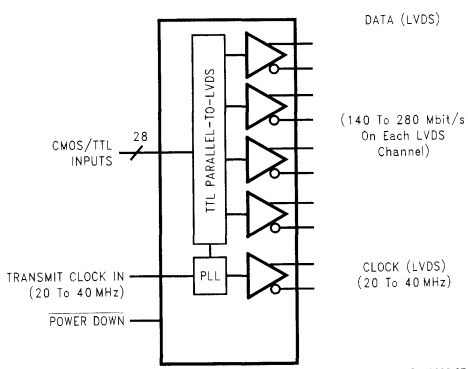
The 28 CMOS/TTL inputs can support a variety of signal combinations. For example, 7 4-bit nibbles or 3 9-bit (byte + parity) and 1 control.

Features

- Narrow bus reduces cable size and cost
- ±1V common mode range (ground shifting)
- 290 mV swing LVDS data transmission
- 1.12 Gbit/s data throughput
- Low swing differential current mode drivers reduce EMI
- Rising edge data strobe
- Power down mode
- Offered in low profile 56-lead TSSOP package

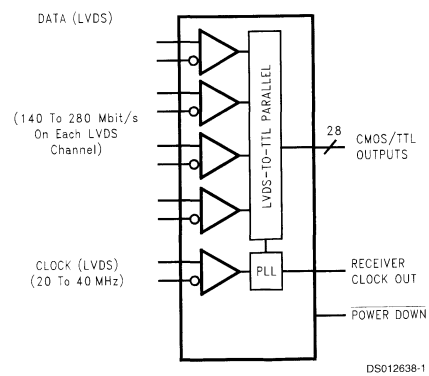
Block Diagrams

DS90CR281



Order Number DS90CR281MTD
See NS Package Number MTD56

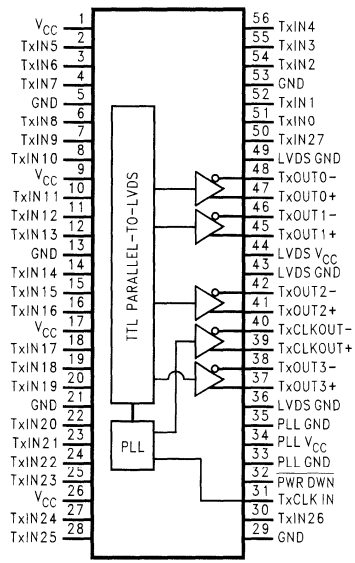
DS90CR282



Order Number DS90CR282MTD
See NS Package Number MTD56

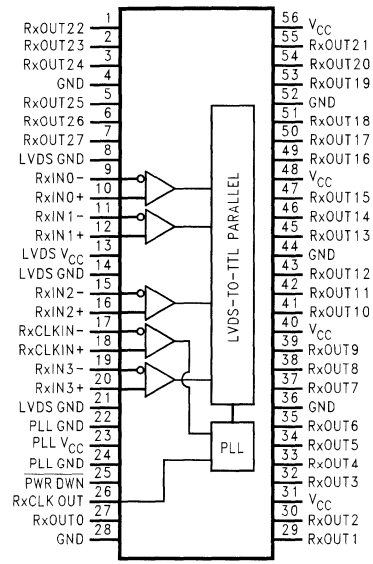
Connection Diagrams

DS90CR281



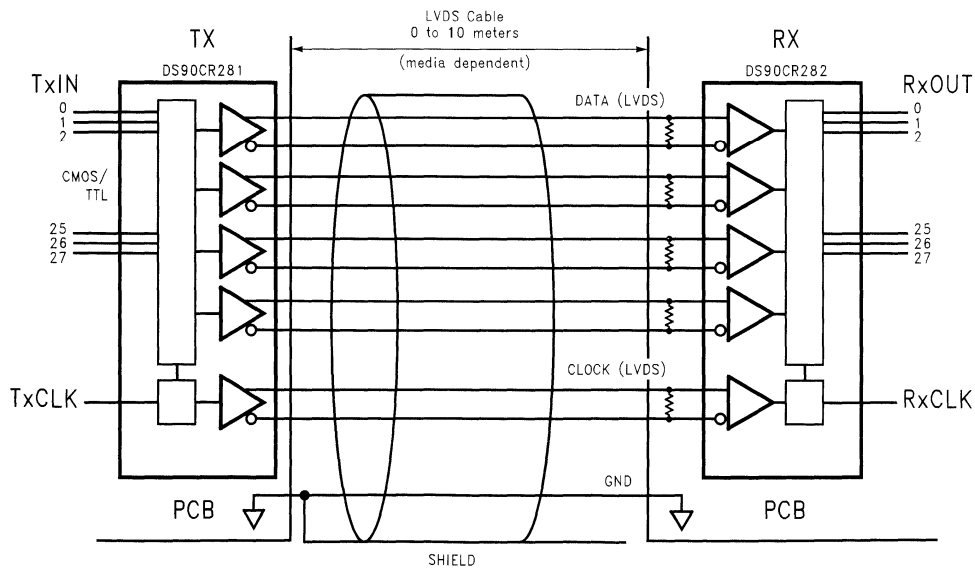
DS012638-2

DS90CR282



DS012638-3

Typical Application



DS012638-19

National Semiconductor

DS90CR283/DS90CR284
28-Bit Channel Link-66 MHz

General Description

The DS90CR283 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR284 receiver converts the LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 66 MHz, 28 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.848 Gbit/s (231 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 28-bit wide data bus and one clock, up to 58 conductors are required. With the Channel Link chipset as few as 11 conductors (4 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

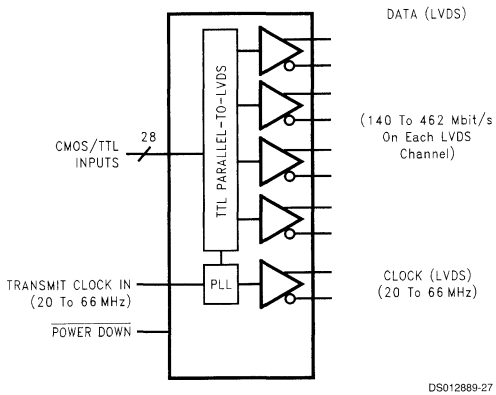
The 28 CMOS/TTL inputs can support a variety of signal combinations. For example, 7 4-bit nibbles or 3 9-bit (byte + parity) and 1 control.

Features

- 66 MHz clock support
- Up to 231 Mbytes/s bandwidth
- Low power CMOS design (< 610 mW)
- Power Down mode (< 0.5 mW total)
- Up to 1.848 Gbit/s data throughput
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS Standard

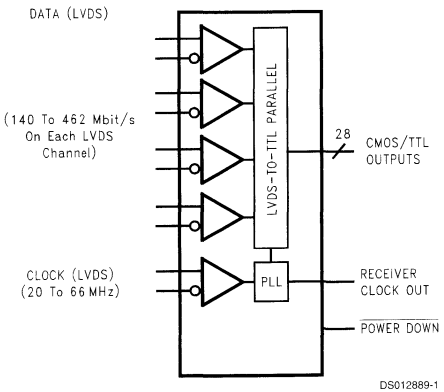
Block Diagrams

DS90CR283



Order Number DS90CR283MTD
See NS Package Number MTD56

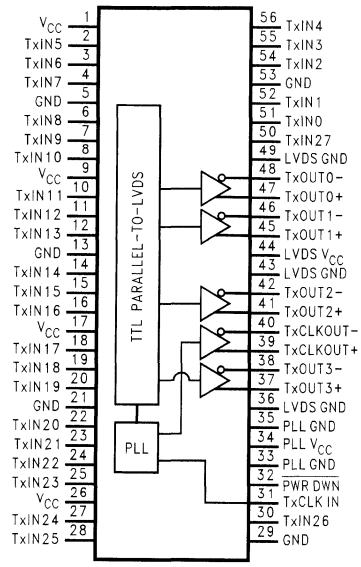
DS90CR284



Order Number DS90CR284MTD
See NS Package Number MTD56

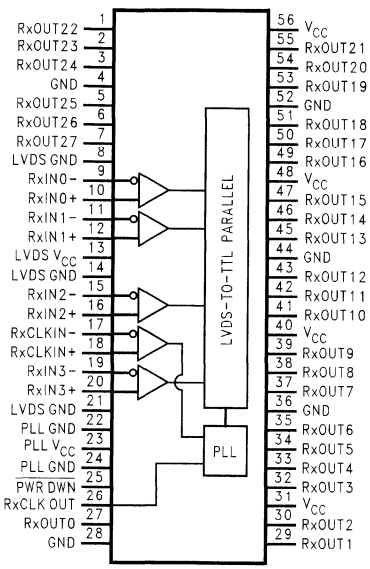
Pin Diagrams

DS90CR283



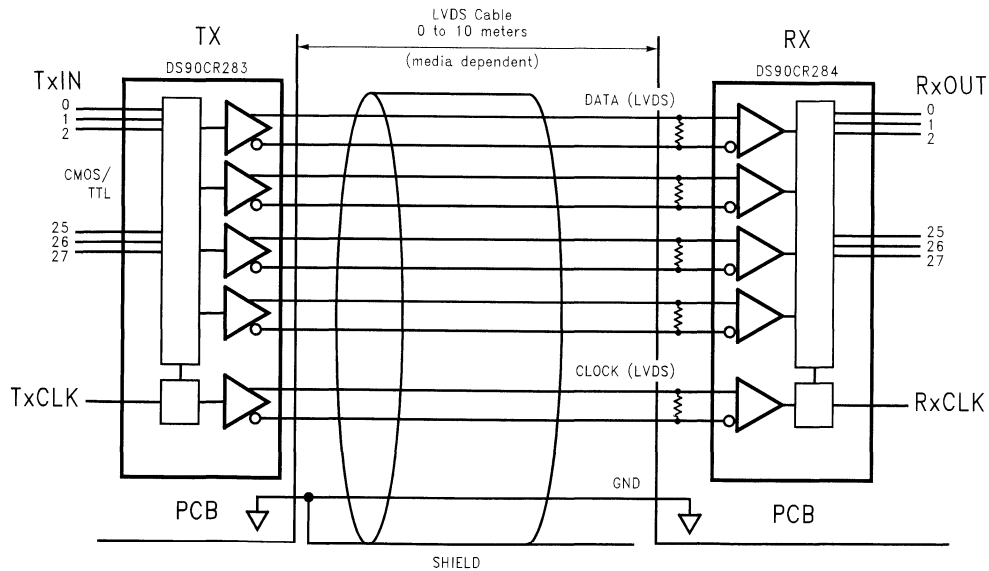
DS012889-21

DS90CR284



DS012889-22

Typical Application



DS012889-23

National Semiconductor

DS90CR285/DS90CR286
+3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-66 MHz

General Description

The DS90CR285 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR286 receiver converts the LVDS data streams back into 28 bits of LVCMOS/LVTTL data. At a transmit clock frequency of 66 MHz, 28 bits of TTL data are transmitted at a rate of 462 Mbps per LVDS data channel. Using a 66 MHz clock, the data throughput is 1.848 Gbit/s (231 Mbytes/s).

The multiplexing of the data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 28-bit wide data and one clock, up to 58 conductors are required. With the Channel Link chipset as few as 11 conductors (4 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides a 80% reduction in required cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 28 LVCMOS/LVTTL inputs can support a variety of signal combinations. For example, seven 4-bit nibbles or three 9-bit (byte + parity) and 1 control.

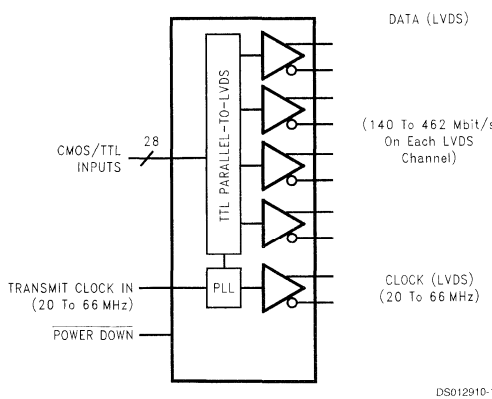
Features

- Single +3.3V supply
- Chipset (Tx + Rx) power consumption <250 mW (typ)
- Power-down mode (<0.5 mW total)
- Up to 231 Megabytes/sec bandwidth
- Up to 1.848 Gbps data throughput
- Narrow bus reduces cable size
- 290 mV swing LVDS devices for low EMI
- +1V common mode range (around +1.2V)
- PLL requires no external components
- Both devices are offered in a Low profile 56-lead TSSOP package
- DS90CR285SLC is offered in a 64 ball, 0.8mm fine pitch ball grid array (FBGA) package for use with the DS90CR286ASLC
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- ESD Rating > 7 kV
- Operating Temperature: −40°C to +85°C

9

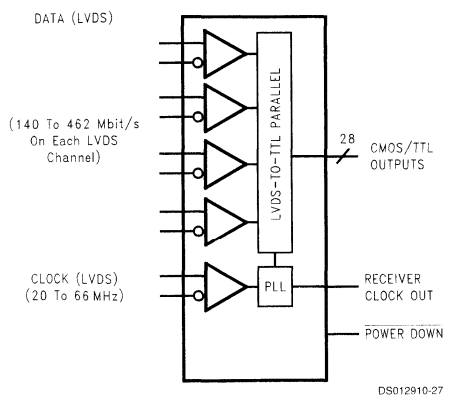
Block Diagrams

DS90CR285



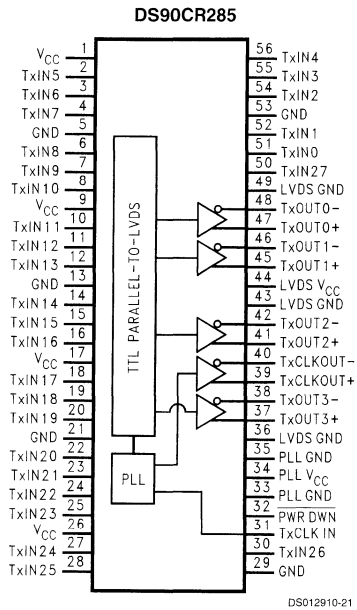
Order Number DS90CR285MTD or DS90CR285SLC
See NS Package Number MTD56 or SLC64A

DS90CR286

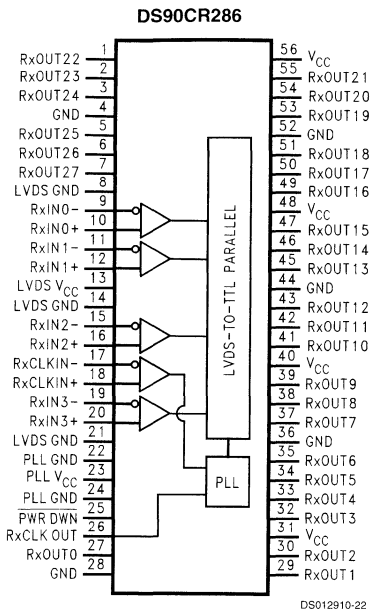


Order Number DS90CR286MTD
See NS Package Number MTD56

Pin Diagrams for TSSOP Packages

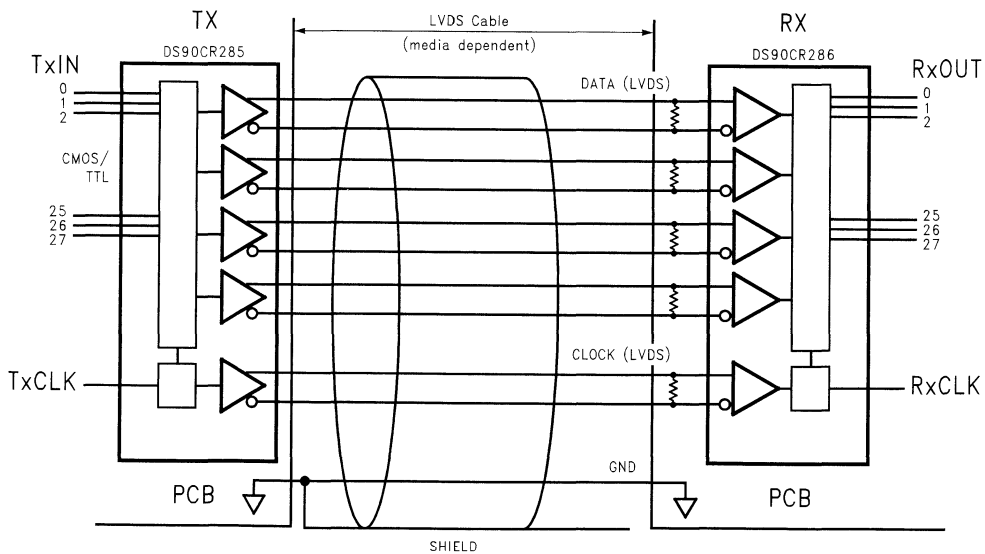


DS012910-21



DS012910-22

Typical Application



DS012910-23

National Semiconductor

DS90CR286A/DS90CR216A
+3.3V Rising Edge Data Strobe LVDS Receiver 28-Bit Channel Link—66 MHz, +3.3V Rising Edge Strobe LVDS Receiver 21-Bit Channel Link—66 MHz

General Description

The DS90CR286A receiver converts the four LVDS data streams (Up to 1.848 Gbps throughput or 231 Megabytes/sec bandwidth) back into parallel 28 bits of CMOS/TTL data. Also available is the DS90CR216A that converts the three LVDS data streams (Up to 1.386 Gbps throughput or 173 Megabytes/sec bandwidth) back into parallel 21 bits of CMOS/TTL data. Both Receivers' outputs are Rising edge strobe.

Both devices are offered in TSSOP packages. In addition the DS90CR286A is also offered in a space saving 64 ball, 0.8mm fine pitch ball grid array (FBGA) which provides a 44% reduction in PCB footprint compared to the 56L TSSOP package.

The DS90CR286A / DS90CR216A devices are enhanced over prior generation receivers and provided a wider data valid time on the receiver output.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

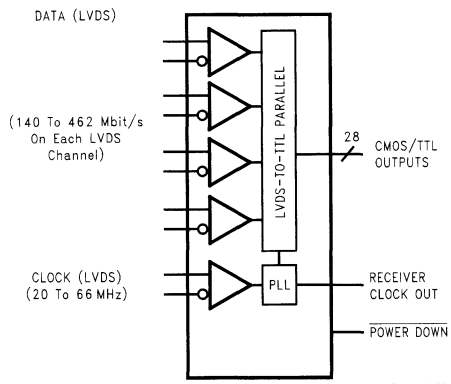
Features

- 20 to 66 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best–in–Class Set & Hold Times on RxOUTPUTs
- Rx power consumption <270 mW (typ) @66MHz Worst Case
- Rx Power-down mode <200µW (max)
- ESD rating >7 kV (HBM), >700V (EIAJ)
- PLL requires no external components
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead or 48-lead TSSOP package
- DS90CR286A is also offered in a space saving 64 ball FBGA package
- Operating Temperature: −40˚C to +85˚C

9

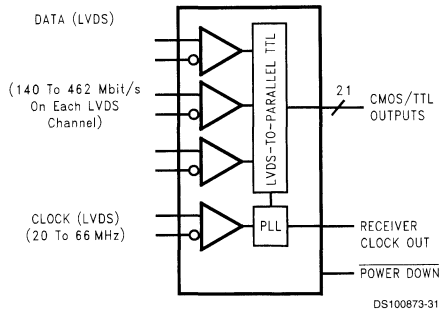
Block Diagrams

DS90CR286A



Order Number DS90CR286AMTD or DS90CR286ASLC
See NS Package Number MTD56 or SLC64A

DS90CR216A



Order Number DS90CR216AMTD
See NS Package Number MTD48

National Semiconductor

DS90CR287/DS90CR288
+3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-75 MHz

General Description

The DS90CR287 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR288 receiver converts the four LVDS data streams back into 28 bits of CMOS/TTL data. At a transmit clock frequency of 75 MHz, 28 bits of TTL data are transmitted at a rate of 525 Mbps per LVDS data channel. Using a 75 MHz clock, the data throughput is 2.10 Gbit/s (262.5 Mbytes/sec).

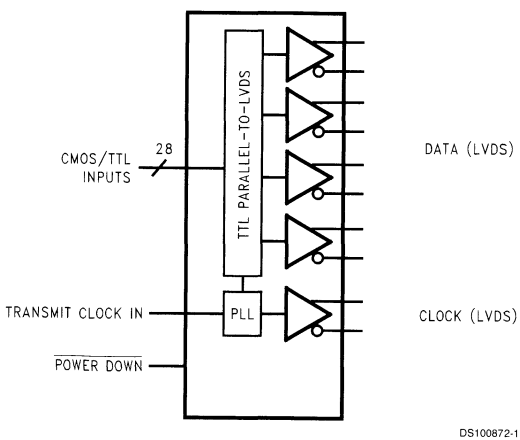
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 75 MHz shift clock support
- 50% duty cycle on receiver output clock
- Best-in-Class Set & Hold Times on TxINPUTs and RxOUTPUTs
- Low power consumption
- Tx + Rx Powerdown mode <400µW (max)
- ±1V common-mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 2.10 Gbps throughput
- Up to 262.5 Mbytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead TSSOP package

Block Diagrams

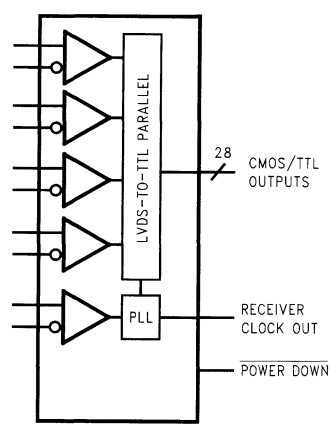
DS90CR287



DS100872-1

Order Number DS90CR287MTD
See NS Package Number MTD56

DS90CR288

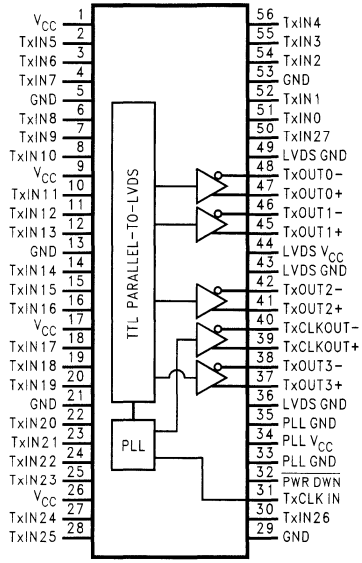


DS100872-27

Order Number DS90CR288MTD
See NS Package Number MTD56

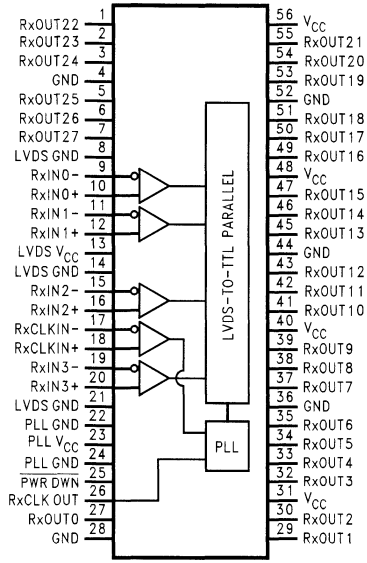
Pin Diagrams

DS90CR287



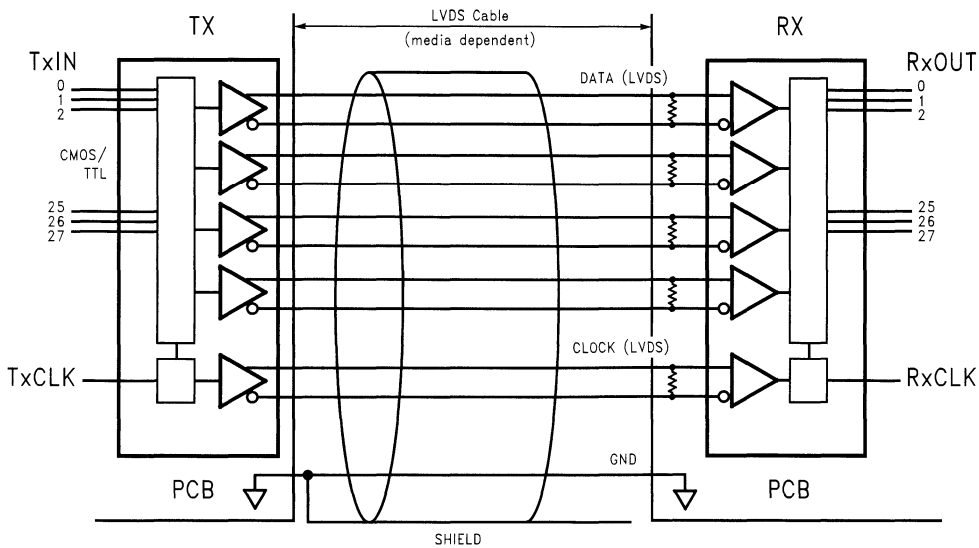
DS100872-21

DS90CR288



DS100872-22

Typical Application



DS100872-23

National Semiconductor

DS90CR287/DS90CR288A
+3.3V Rising Edge Data Strobe LVDS 28-Bit Channel Link-85 MHz

General Description

The DS90CR287 transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. The DS90CR288A receiver converts the four LVDS data streams back into 28 bits of LVCMOS/LVTTL data. At a transmit clock frequency of 85 MHz, 28 bits of TTL data are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 2.38 Gbit/s (297.5 Mbytes/sec). Both devices are also offered in 64 ball, 0.8mm fine pitch ball grid array (FBGA) package which provides a 44% reduction in PCB footprint over the 56L TSSOP package.

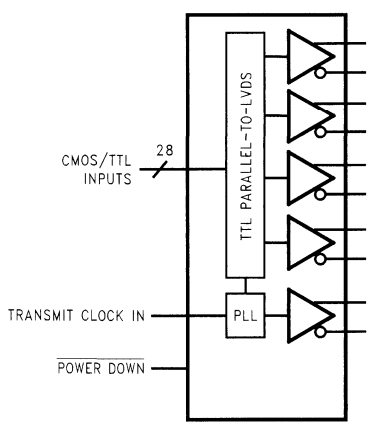
This chipset is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces.

Features

- 20 to 85 MHz shift clock support
- 50% duty cycle on receiver output clock
- 2.5 / 0 ns Set & Hold Times on TxINPUTs
- Low power consumption
- ±1V common-mode range (around +1.2V)
- Narrow bus reduces cable size and cost
- Up to 2.38 Gbps throughput
- Up to 297.5 Mbytes/sec bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard
- Low profile 56-lead TSSOP package
- Both devices are also available in 64 ball, 0.8mm fine pitch ball grid array (FBGA) package

Block Diagrams

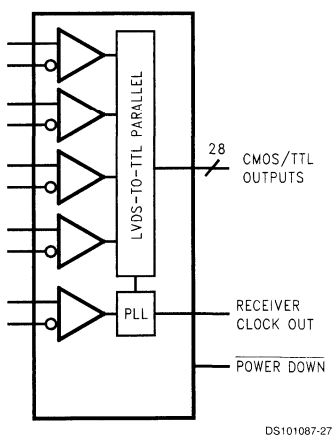
DS90CR287



DS101087-1

Order Number DS90CR287MTD or DS90CR287SLC
See NS Package Number MTD56 or SLC64A

DS90CR288A

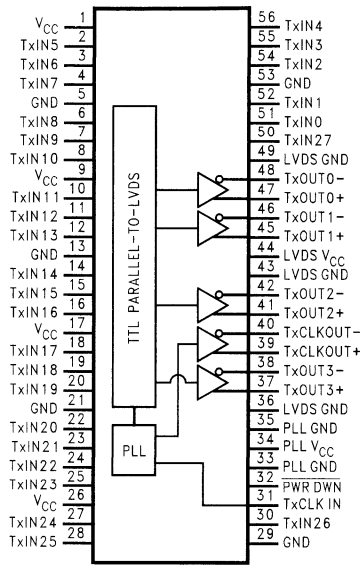


DS101087-27

Order Number DS90CR288AMTD or DS90CR288ASLC
See NS Package Number MTD56 or SLC64A

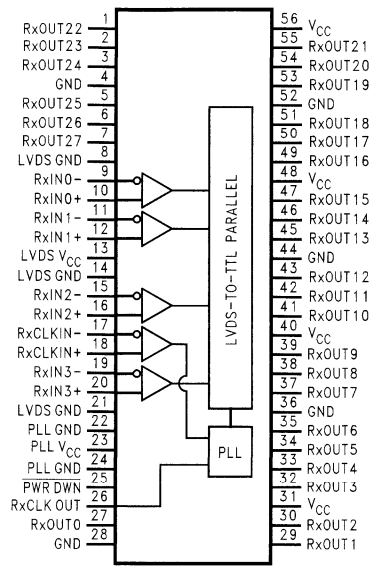
Pin Diagram for TSSOP Packages

DS90CR287



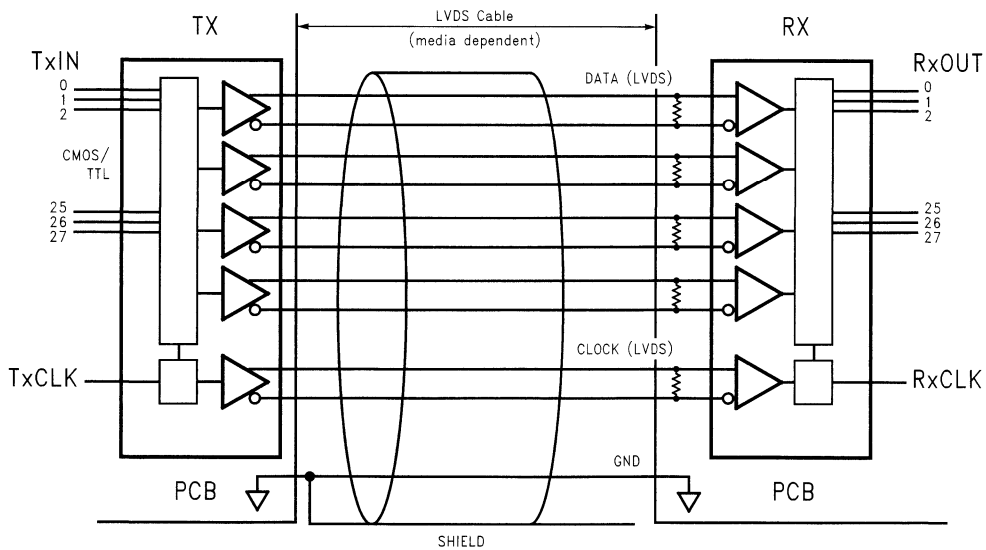
DS101087-21

DS90CR288A



DS101087-22

Typical Application



DS101087-23

National Semiconductor

DS90CR481
48-Bit LVDS Channel Link Serializer – 66 -112 MHz

General Description

The DS90CR481 transmitter converts 48 bits of CMOS/TTL data into eight LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a ninth LVDS link. Every cycle of the transmit clock 48 bits of input data are sampled and transmitted. Using a 66 MHz clock, the data throughput is 3.168 Gbit/s (396 Mbytes/s).

The multiplexing of data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 48-bit wide data and one clock, up to 98 conductors are required. With this Channel Link chipset as few as 19 conductors (8 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 48 CMOS/TTL inputs can support a variety of signal combinations. For example, 6 8-bit words or 5 9-bit (byte + parity) and 3 controls.

The DS90CR481 is intended to be used with the DS90CR484 Channel Link Deserializer. The DS90CR481 is optimized over the DS90CR483 Serializer for 66 MHz operation. The DS90CR481 is footprint compatible with the DS90CR483. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable.

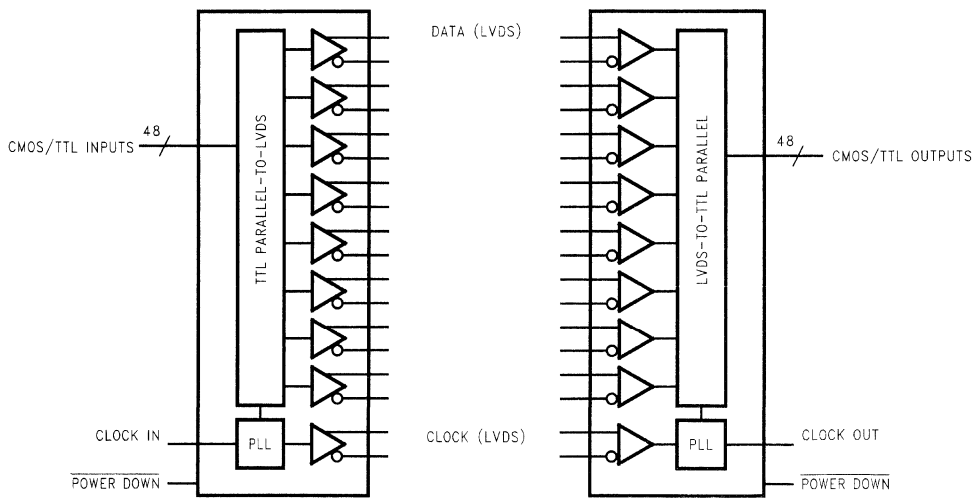
The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

For more details, please refer to the "Applications Information" section of this datasheet.

Features

- 3.168 Gbits/sec bandwidth with 66 MHz Clock
- 5.376 Gbits/sec bandwidth with 112 MHz Clock
- 65 - 112 MHz input clock support
- LVDS SER/DES reduces cable and connector size
- Pre-emphasis reduces cable loading effects
- DC balance data transmission provided by transmitter reduces ISI distortion
- Cable Deskew Support for use with Deskewing Receivers
- 5V Tolerant TxIN and control input pins
- Flow through pinout for easy PCB design
- +3.3V supply voltage
- Transmitter rejects cycle-to-cycle jitter
- Conforms to ANSI/TIA/EIA-644-1995 LVDS Standard

Generalized Block Diagrams (DS90CR481 and DS90CR484)



DS200091-1

National Semiconductor

DS90CR483 / DS90CR484
48-Bit LVDS Channel Link Serializer/Deserializer

General Description

The DS90CR483 transmitter converts 48 bits of CMOS/TTL data into eight LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a ninth LVDS link. Every cycle of the transmit clock 48 bits of input data are sampled and transmitted. The DS90CR484 receiver converts the LVDS data streams back into 48 bits of CMOS/TTL data. At a transmit clock frequency of 112MHz, 48 bits of TTL data are transmitted at a rate of 672Mbps per LVDS data channel. Using a 112MHz clock, the data throughput is 5.38Gbit/s (672Mbytes/s).

The multiplexing of data lines provides a substantial cable reduction. Long distance parallel single-ended buses typically require a ground wire per active signal (and have very limited noise rejection capability). Thus, for a 48-bit wide data and one clock, up to 98 conductors are required. With this Channel Link chipset as few as 19 conductors (8 data pairs, 1 clock pair and a minimum of one ground) are needed. This provides an 80% reduction in cable width, which provides a system cost savings, reduces connector physical size and cost, and reduces shielding requirements due to the cables' smaller form factor.

The 48 CMOS/TTL inputs can support a variety of signal combinations. For example, 6 8-bit words or 5 9-bit (byte + parity) and 3 controls.

The DS90CR483/DS90CR484 chipset is improved over prior generations of Channel Link devices and offers higher bandwidth support and longer cable drive with three areas of enhancement. To increase bandwidth, the maximum clock rate is increased to 112 MHz and 8 serialized LVDS outputs are provided. Cable drive is enhanced with a user selectable pre-emphasis feature that provides additional output current during transitions to counteract cable loading effects. Optional DC balancing on a cycle-to-cycle basis, is also provided to reduce ISI (Inter-Symbol Interference). With pre-emphasis and DC balancing, a low distortion eye-pattern is provided at the receiver end of the cable. A cable deskew capability has been added to deskew long cables of pair-to-pair skew of up to +/−1 LVDS data bit time (up to 80 MHz Clock Rate). These three enhancements allow cables 5+ meters in length to be driven.

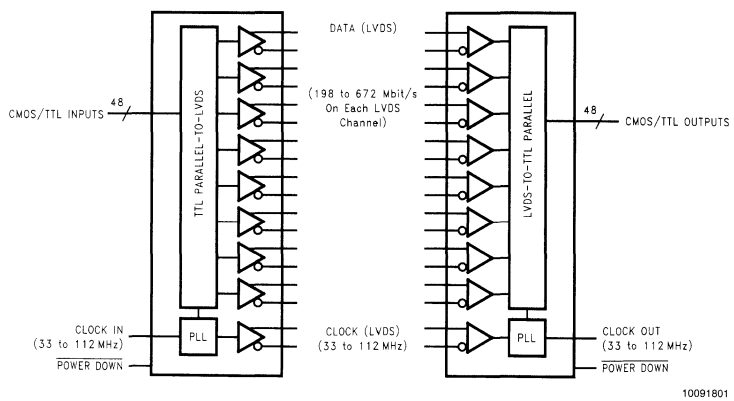
The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

For more details, please refer to the "Applications Information" section of this datasheet.

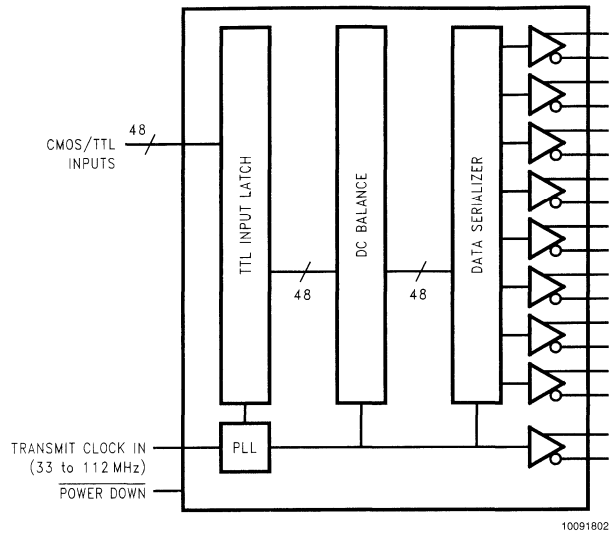
Features

- Up to 5.38 Gbits/sec bandwidth
- 33 MHz to 112 MHz input clock support
- LVDS SER/DES reduces cable and connector size
- Pre-emphasis reduces cable loading effects
- DC balance data transmission provided by transmitter reduces ISI distortion
- Cable Deskew of +/−1 LVDS data bit time (up to 80 MHz Clock Rate)
- 5V Tolerant TxIN and control input pins
- Flow through pinout for easy PCB design
- +3.3V supply voltage
- Transmitter rejects cycle-to-cycle jitter
- Conforms to ANSI/TIA/EIA-644-1995 LVDS Standard
- Both devices are available in 128 lead CSP, 0.5mm pitch or 100 lead TQFP package

Generalized Block Diagrams

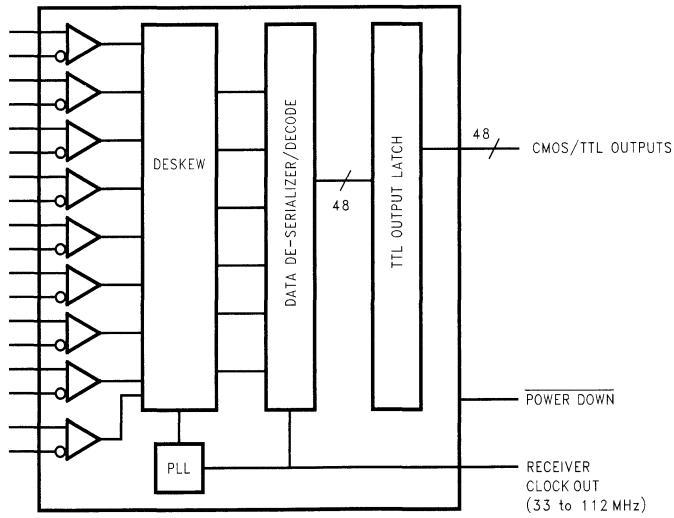


Generalized Transmitter Block Diagram



10091802

Generalized Receiver Block Diagram



10091803

National Semiconductor

DS92LV010A
Bus LVDS 3.3/5.0V Single Transceiver

General Description

The DS92LV010A is one in a series of transceivers designed specifically for the high speed, low power proprietary bus backplane interfaces. The device operates from a single 3.3V or 5.0V power supply and includes one differential line driver and one receiver. To minimize bus loading the driver outputs and receiver inputs are internally connected. The logic interface provides maximum flexibility as 4 separate lines are provided (DIN, DE, $\overline{RE}$, and ROUT). The device also features flow through which allows easy PCB routing for short stubs between the bus pins and the connector. The driver has 10 mA drive capability, allowing it to drive heavily loaded backplanes, with impedance as low as 27 Ohms.

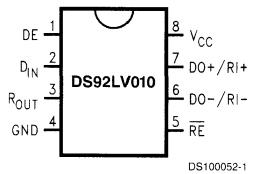
The driver translates between TTL levels (single-ended) to Low Voltage Differential Signaling levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is ±100mV over a ±1V common mode range and translates the low voltage differential levels to standard (CMOS/TTL) levels.

Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Balanced Output Impedance
- Lite Bus Loading 5pF typical
- Glitch free power up/down (Driver disabled)
- 3.3V or 5.0V Operation
- ±1V Common Mode Range
- ±100mV Receiver Sensitivity
- High Signaling Rate Capability (above 100 Mbps)
- Low Power CMOS design
- Product offered in 8 lead SOIC package
- Industrial Temperature Range Operation

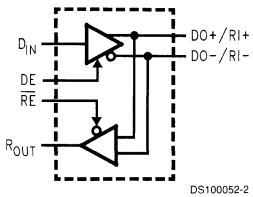
Connection Diagram



DS100052-1

Order Number DS92LV010ATM
See NS Package Number M08A

Block Diagram



DS100052-2

National Semiconductor

DS92CK16
3V BLVDS 1 to 6 Clock Buffer/Bus Transceiver

General Description

The DS92CK16 1 to 6 Clock Buffer/Bus Transceiver is a one to six CMOS differential clock distribution device utilizing Bus Low Voltage Differential Signaling (BLVDS) technology. This clock distribution device is designed for applications requiring ultra low power dissipation, low noise, and high data rates. The BLVDS side is a transceiver with a separate channel acting as a return/source clock.

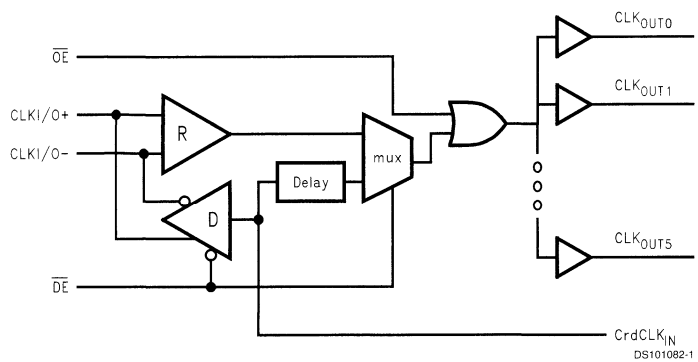
The DS92CK16 accepts BLVDS (300 mV typical) differential input levels, and translates them to 3V CMOS output levels. An output enable pin $\overline{OE}$, when high, forces all CLK_{OUT} pins high.

The device can be used a source synchronous driver. The selection of the source driving is controlled by the $CrdCLK_{IN}$ and $\overline{DE}$ pins. This device can be the master clock, driving the inputs of other clock I/O pins in a multipoint environment. Easy master/slave clock selection is achieved along a backplane.

Features

- Master/Slave clock selection in a backplane application
- 125 MHz operation (typical)
- 100 ps duty cycle distortion (typical)
- 50 ps channel to channel skew (typical)
- 3.3V power supply design
- Glitch-free power on at CLKI/O pins
- Low Power design (20 mA @ 3.3V static)
- Accepts small swing (300 mV typical) differential signal levels
- Industrial temperature operating range (-40˚C to +85˚C)
- Available in 24-pin TSSOP Packaging

Function Diagram and Truth Table



Receive Mode Truth Table

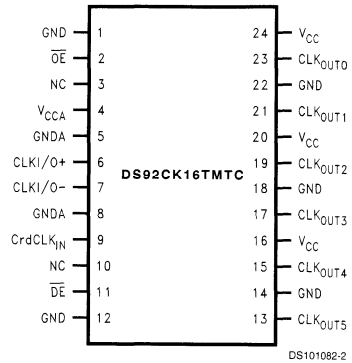
INPUT				OUTPUT
$\overline{OE}$	$\overline{DE}$	$CrdCLK_{IN}$	(CLKI/O+)−(CLKI/O−)	CLK_{OUT}
H	H	X	X	H
L	H	X	VID≥ 0.07V	H
L	H	X	VID≤ −0.07V	L

L = Low Logic State
H = High Logic State
X = Irrelevant
Z = TRI-STATE

Driver Mode Truth Table

INPUT			OUTPUT		
$\overline{OE}$	$\overline{DE}$	$CrdCLK_{IN}$	CLK/I/O+	CLKI/O−	CLK_{OUT}
L	L	L	L	H	L
L	L	H	H	L	H
H	L	L	L	H	H
H	L	H	H	L	H
H	H	X	Z	Z	H

Connection Diagram



Order Number DS92CK16TMTC
See NS Package Number MTC24

TSSOP Package Pin Description

Pin Name	Pin #	Type	Description
CLKI/O+	6	I/O	True (Positive) side of the differential clock input.
CLKI/O–	7	I/O	Complementary (Negative) side of the differential clock input.
$\overline{OE}$	2	I	$\overline{OE}$; this pin is active Low. When High, this pin forces all CLK_{OUT} pins High. When Low, CLK_{OUT} pins logic state is determined by either the $CrdCLK_{IN}$ or the VID at the CLK/I/O pins with respect to the logic level at the $\overline{DE}$ pin. This pin has a weak pullup device to V_{CC}. If $\overline{OE}$ is floating, then all CLK_{OUT} pins will be High.
$\overline{DE}$	11	I	$\overline{DE}$; this pin is active LOW. When Low, this pin enables the $CardCLK_{IN}$ signal to the CLKI/O pins and CLK_{OUT} pins. When High, the Driver is TRI-STATE®, the CLKI/O pins are inputs and determine the state of the CLK_{OUT} pins. This pin has a weak pullup device to V_{CC}. If $\overline{DE}$ is floating, then CLKI/O pins are TRI-STATE.
CLK_{OUT}	13, 15, 17, 19, 21, 23	O	6 Buffered clock (CMOS) outputs.
$CrdCLK_{IN}$	9	I	Input clock from Card (CMOS level or TTL level).
V_{CC}	16, 20, 24	Power	V_{CC}; Analog V_{CCA} (Internally separate from V_{CC}, connect externally or use separate power supplies). No special power sequencing required. Either V_{CCA} or V_{CC} can be applied first, or simultaneously apply both power supplies.
GND	1, 12, 14, 18, 22	Ground	GND
V_{CCA}	4	Power	Analog V_{CCA} (Internally separate from V_{CC}, connect externally or use separate power supplies). No special power sequencing required. Either V_{CCA} or V_{CC} can be applied first, or simultaneously apply both power supplies.
GNDA	5, 8	Ground	Analog Ground (Internally separate from Ground must be connected externally).
NC	3, 10		No Connects

National Semiconductor

DS92LV16
16–Bit Bus LVDS Serializer/Deserializer — 35–80MHz

General Description

The DS92LV16 Serializer/Deserializer (SERDES) pair transparently translates a 16–bit parallel bus into a BLVDS serial stream with embedded clock information. This single serial stream simplifies transferring a 16-bit, or less bus over PCB traces and cables by eliminating the skew problems between parallel data and clock paths. It saves system cost by narrowing data paths that in turn reduce PCB layers, cable width, and connector size and pins.

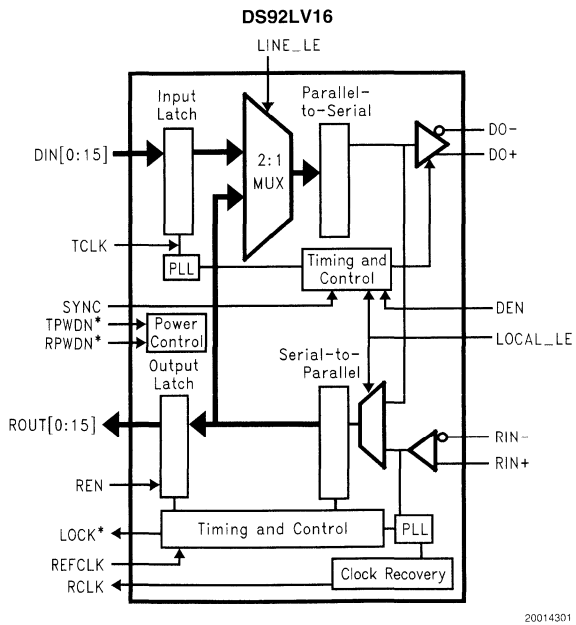
This SERDES pair includes built-in system and device test capability. The line loopback and local loopback features provide the following functionality: the local loopback enables the user to check the integrity of the transceiver from the local parallel-bus side and the system can check the integrity of the data transmission line by enabling the line loopback.

The DS92LV16 incorporates BLVDS signaling on the high-speed I/O. BLVDS provides a low power and low noise environment for reliably transferring data over a serial transmission path. The equal and opposite currents through the differential data path control EMI by coupling the resulting fringing fields together.

Features

- 35–80 MHz 16:1/1:16 serializer/deserializer (2.56Gbps full duplex throughput)
- Independent transmitter and receiver operation with separate clock, enable, power down pins
- Hot plug protection (power up high impedance) and synchronization (receiver locks to random data)
- Wide +/–5% reference clock frequency tolerance for easy system design using locally-generated clocks
- Line and local loopback modes
- Robust BLVDS serial transmission across backplanes and cables for low EMI
- No external coding required
- Internal PLL, no external PLL components required
- Single +3.3V power supply
- Low power: 104mA (typ) transmitter, 119mA (typ) receiver at 80MHz
- ±100mV receiver input threshold
- Loss of lock detection and reporting pin
- Industrial –40 to +85°C temperature range
- >2.5kV HBM ESD
- Compact, standard 80-pin PQFP package

Block Diagram



National Semiconductor

DS92LV040A
4 Channel Bus LVDS Transceiver

General Description

The DS92LV040A is one in a series of Bus LVDS transceivers designed specifically for high speed, low power backplane or cable interfaces. The device operates from a single 3.3V power supply and includes four differential line drivers and four receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

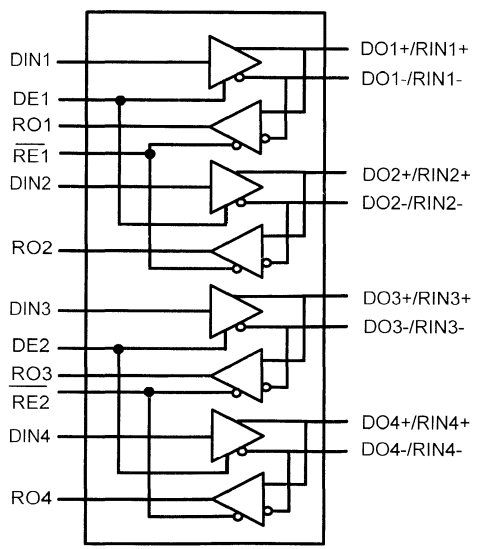
The driver translates 3V LVTTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation while consuming minimal power and reducing EMI. In addition, the differential signaling provides common mode noise rejection greater than ±1V.

The receiver threshold is less than +0/−70 mV. The receiver translates the differential Bus LVDS to standard (LVTTL/LVCMOS) levels. (See Applications Information Section for more details.)

Features

- Bus LVDS Signaling
- Propagation delay: Driver 2.3ns max, Receiver 3.2ns max
- Low power CMOS design
- 100% Transition time 1ns driver typical, 1.3ns receiver typical
- High Signaling Rate Capability (above 155 Mbps)
- 0.1V to 2.3V Common Mode Range for V_{ID} = 200mV
- 70 mV Receiver Sensitivity
- Supports open and terminated failsafe on port pins
- 3.3V operation
- Glitch free power up/down (Driver & Receiver disabled)
- Light Bus Loading (5 pF typical) per Bus LVDS load
- Designed for Double Termination Applications
- Balanced Output Impedance
- Product offered in 44 pin LLP (Leadless Leadframe Package) package
- High impedance Bus pins on power off (V_{CC} = 0V)

Simplified Functional Diagram



DS101336-1

National Semiconductor

DS92LV090A
9 Channel Bus LVDS Transceiver

General Description

The DS92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

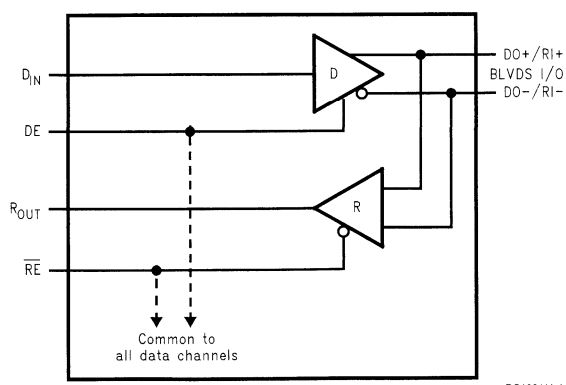
The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of ±1V.

The receiver threshold is less than ±100 mV over a ±1V common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels. (See Applications Information Section for more details.)

Features

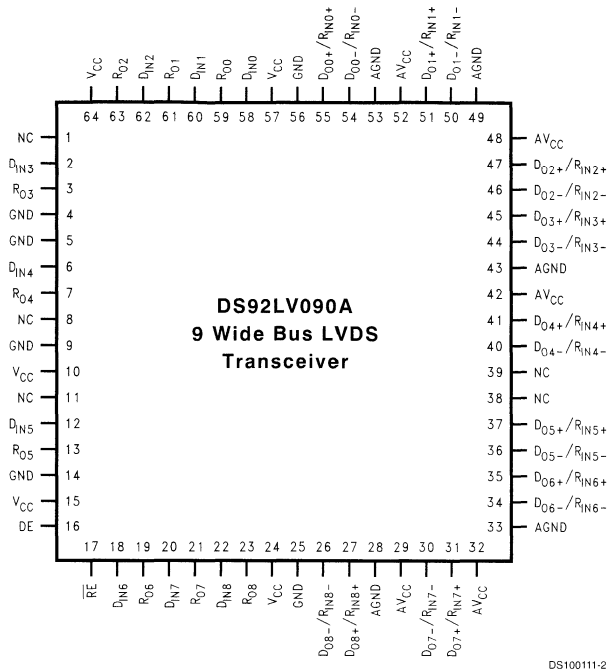
- Bus LVDS Signaling
- 3.2 nanosecond propagation delay max
- Chip to Chip skew ±800ps
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- 0.1V to 2.3V Common Mode Range for V_{ID} = 200mV
- ±100 mV Receiver Sensitivity
- Supports open and terminated failsafe on port pins
- 3.3V operation
- Glitch free power up/down (Driver & Receiver disabled)
- Light Bus Loading (5 pF typical) per Bus LVDS load
- Designed for Double Termination Applications
- Balanced Output Impedance
- Product offered in 64 pin TQFP package
- High impedance Bus pins on power off (V_{CC} = 0V)
- Driver Channel to Channel skew (same device) 230ps typical
- Receiver Channel to Channel skew (same device) 370ps typical

Simplified Functional Diagram



DS100111-1

Connection Diagram



Top View
Order Number DS92LV090ATVEH
See NS Package Number VEH064DB

Pinout Description

Pin Name	Pin #	Input/Output	Descriptions
DO+/RI+	27, 31, 35, 37, 41, 45, 47, 51, 55	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO−/RI−	26, 30, 34, 36, 40, 44, 46, 50, 54	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D_{IN}	2, 6, 12, 18, 20, 22, 58, 60, 62	I	TTL Driver Input.
RO	3, 7, 13, 19, 21, 23, 59, 61, 63	O	TTL Receiver Output.
$\overline{RE}$	17	I	Receiver Enable TTL Input (Active Low).
DE	16	I	Driver Enable TTL Input (Active High).
GND	4, 5, 9, 14, 25, 56	Power	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V_{CC}	10, 15, 24, 57, 64	Power	V_{CC} for digital circuitry (must connect to V_{CC} on PC board). These pins connected internally.
AGND	28, 33, 43, 49, 53	Power	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV_{CC}	29, 32, 42, 48, 52	Power	Analog V_{CC} (must connect to V_{CC} on PC board). These pins connected internally.
NC	1, 8, 11, 38, 39	N/A	Leave open circuit, do not connect.

National Semiconductor

SCAN92LV090
9 Channel Bus LVDS Transceiver w/ Boundary SCAN

General Description

The SCAN92LV090A is one in a series of Bus LVDS transceivers designed specifically for the high speed, low power proprietary backplane or cable interfaces. The device operates from a single 3.3V power supply and includes nine differential line drivers and nine receivers. To minimize bus loading, the driver outputs and receiver inputs are internally connected. The separate I/O of the logic side allows for loop back support. The device also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

The driver translates 3V TTL levels (single-ended) to differential Bus LVDS (BLVDS) output levels. This allows for high speed operation, while consuming minimal power with reduced EMI. In addition, the differential signaling provides common mode noise rejection of ±1V.

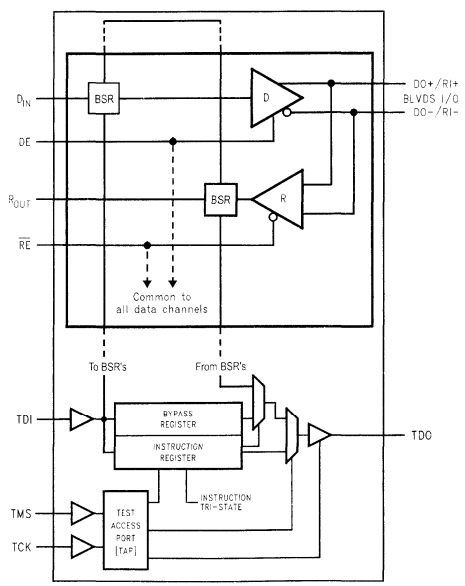
The receiver threshold is less than ±100 mV over a ±1V common mode range and translates the differential Bus LVDS to standard (TTL/CMOS) levels.

This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCK), and the optional Test Reset ($\overline{TRST}$).

Features

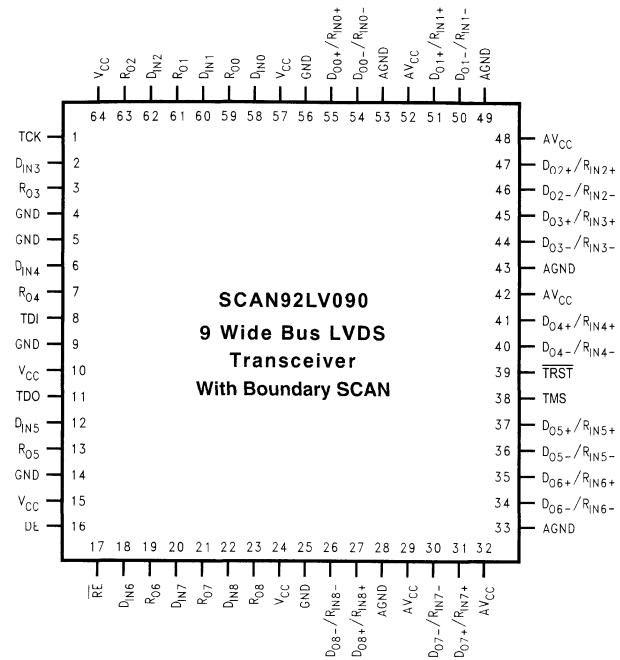
- IEEE 1149.1 (JTAG) Compliant
- Bus LVDS Signaling
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- 0.1V to 2.3V Common Mode Range for V_{ID} = 200mV
- ±100 mV Receiver Sensitivity
- Supports open and terminated failsafe on port pins
- 3.3V operation
- Glitch free power up/down (Driver & Receiver disabled)
- Light Bus Loading (5 pF typical) per Bus LVDS load
- Designed for Double Termination Applications
- Balanced Output Impedance
- Product offered in 64 pin LQFP package and BGA package
- High impedance Bus pins on power off (V_{CC} = 0V)

Simplified Functional Diagram

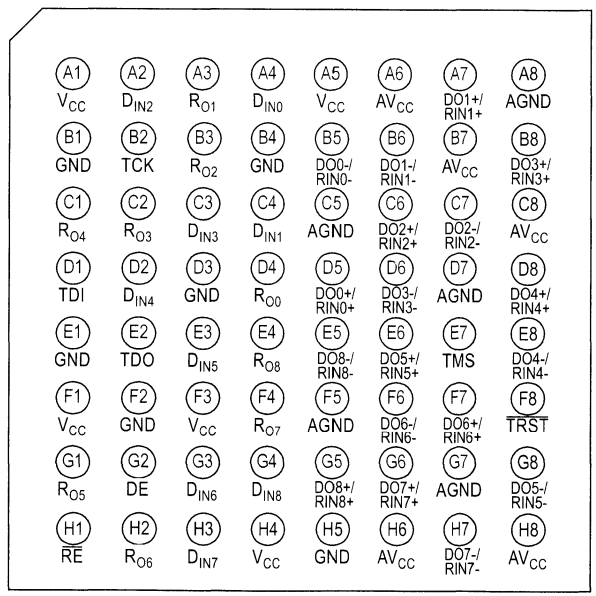


DS101242-1

Connection Diagram



Top View
Order Number SCAN92LV090VEH
See NS Package Number VEH064DB



Top View
Order Number SCAN92LV090SLC
See NS Package Number SLC64A

Pinout Description

Pin Name	TQFP Pin #	BGA Pin #	Input/Output	Descriptions
DO+/RI+	27, 31, 35, 37, 41, 45, 47, 51, 55	A7, B8, C6, D5, D8, E6, F7, G5, G6	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO−/RI−	26, 30, 34, 36, 40, 44, 46, 50, 54	B5, B6, C7, D6, E5, E8, F6, G8, H7	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D_{IN}	2, 6, 12, 18, 20, 22, 58, 60, 62	A2, A4, C3, C4, D2, E3, G3, G4, H3	I	TTL Driver Input.
RO	3, 7, 13, 19, 21, 23, 59, 61, 63	A3, B3, C1, C2, D4, E4, F4, G1, H2	O	TTL Receiver Output.
$\overline{RE}$	17	H1	I	Receiver Enable TTL Input (Active Low).
DE	16	G2	I	Driver Enable TTL Input (Active High).
GND	4, 5, 9, 14, 25, 56	B1, B4, D3, E1, F2, H5	Power	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V_{CC}	10, 15, 24, 57, 64	A1, A5, F1, F3, H4	Power	V_{CC} for digital circuitry (must connect to V_{CC} on PC board). These pins connected internally.
AGND	28, 33, 43, 49, 53	A8, C5, D7, F5, G7	Power	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV_{CC}	29, 32, 42, 48, 52	A6, B7, C8, H6, H8	Power	Analog V_{CC} (must connect to V_{CC} on PC board). These pins connected internally.
$\overline{TRST}$	39	F8	I	Test Reset Input to support IEEE 1149.1 (Active Low)
TMS	38	E7	I	Test Mode Select Input to support IEEE 1149.1
TCK	1	B2	I	Test Clock Input to support IEEE 1149.1
TDI	8	D1	I	Test Data Input to support IEEE 1149.1
TDO	11	E2	O	Test Data Output to support IEEE 1149.1

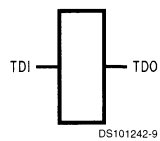
Description of Boundary-Scan Circuitry

The SCAN92LV090 features two unique Scan test modes, each which requires a unique BSDL model depending on the level of test access and fault coverage goals. In the first mode (Mode0), only the TTL Inputs and Outputs of each transceiver are accessible via a 1149.1 compliant protocol. In the second mode (Mode1), the TTL Inputs and Outputs are accessible by a 1149.1 compliant method while the Differential I/O pins are accessible by a 1149.1 compatible technique which evaluates the signal integrity and modifies the data in the differential BSR as appropriate.

All test modes are handled by the ATPG software, and BSDL selection should be invisible to the user.

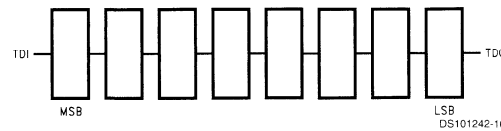
The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



The INSTRUCTION register is an eight-bit register which captures the value 00111101.

Instruction Register Scan Chain Definition



MSB → LSB (Mode0)

Instruction Code	Instruction
00000000	EXTEST
10000010	SAMPLE/PRELOAD
10000111	CLAMP
00000110	HIGHZ
All Others	BYPASS

MSB → LSB (Mode1)

Instruction Code	Instruction
10011001	EXTEST
10010010	SAMPLE/PRELOAD
10001111	CLAMP
00000110	HIGHZ
All Others	BYPASS

National Semiconductor

DS92LV222A
Two Channel Bus LVDS MUXed Repeater

General Description

The DS92LV222A is a repeater designed specifically for the bridging of multiple backplanes in a rack. The DS92LV222A utilizes low voltage differential signaling to deliver high speed while consuming minimal power with reduced EMI. The RSEL pin and DE pins allow maximum flexibility as to which receiver/driver are used. The DS92LV222A repeats signals between backplanes and accepts or drives signals onto the local bus. It also features a flow through pin out which allows easy PCB routing for short stubs between its pins and the connector.

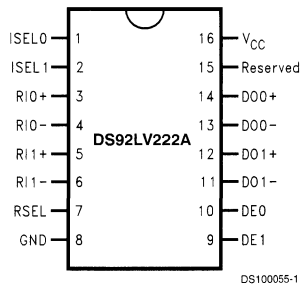
The driver is selectable between 3.5 mA (100Ω load) and 8.5 mA (27Ω load) output loop currents depending upon the level applied to the ISEL pin. This allows for single termination (point-to-point) and also double termination (multipoint) applications while maintain similar differential levels.

The receiver threshold is ±100 mV, while providing ±1V common mode range.

Features

- Bus LVDS Signaling (BLVDS)
- Designed for Double Termination Applications
- Low power CMOS design
- High Signaling Rate Capability (above 100 Mbps)
- Ultra Low Power Dissipation (13.2 mW quiescent)
- Balanced Output Impedance
- Lite Bus Loading 5 pF typical
- Selectable Drive Capability (3.5 mA or 8.5 mA)
- 3.3V operation
- ±1V Common Mode Range
- ±100 mV Receiver Sensitivity
- Available in 16 pin SOIC package.

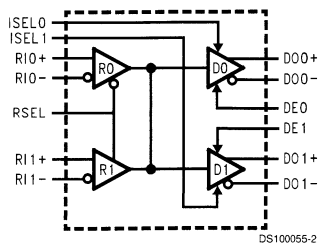
Connection Diagram



DS100055-1

Order Number DS92LV222ATM
See NS Package Number M16A

Block Diagram



DS100055-2

National Semiconductor

DS92LV1021 and DS92LV1210
16-40 MHz 10 Bit Bus LVDS Serializer and Deserializer

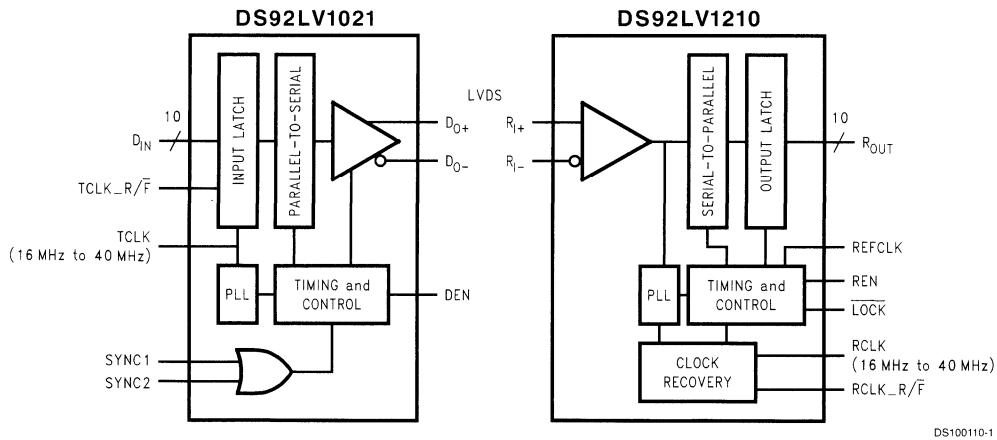
General Description

The DS92LV1021 transforms a 10-bit wide parallel CMOS/TTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. The DS92LV1210 receives the Bus LVDS serial data stream and transforms it back into a 10-bit wide parallel data bus and separates clock. The DS92LV1021 may transmit data over heavily loaded backplanes or 10 meters of cable. The reduced cable, PCB trace count and connector size saves cost and makes PCB design layout easier. Clock-to-data and data-to-data skew are eliminated since one output will transmit both clock and all data bits serially. The powerdown pin is used to save power, by reducing supply current when either device is not in use. The Serializer has a synchronization mode that should be activated upon power-up of the device. The Deserializer will establish lock to this signal within 1024 cycles, and will flag Lock status. The embedded clock guarantees a transition on the bus every 12-bit cycle; eliminating transmission errors due to charged cable conditions. The DS92LV1021 output pins may be TRI-STATE ® to achieve a high impedance state. The PLL can lock to frequencies between 16 MHz and 40 MHz.

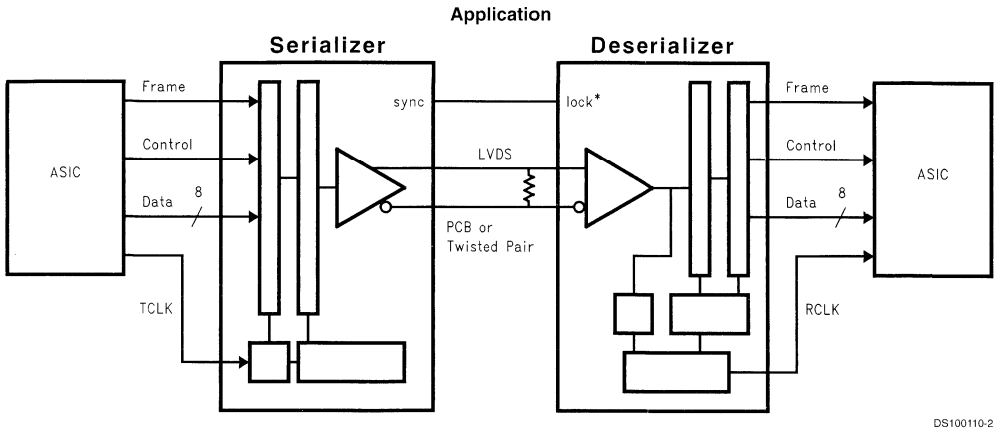
Features

- Guaranteed transition every data transfer cycle
- Single differential pair eliminates multi-channel skew
- Flow-through pinout for easy PCB layout
- 400 Mbps serial Bus LVDS bandwidth (at 40 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits
- Synchronization mode and LOCK indicator
- Programmable edge trigger on clock
- High impedance on receiver inputs when power is off
- Bus LVDS serial output rated for 27Ω load
- Small 28-lead SSOP package-MSA

Block Diagrams



Block Diagrams (Continued)



Functional Description

The DS92LV1021 and DS92LV1210 is a 10-bit Serializer / Deserializer chipset designed to transmit data over a heavily loaded differential backplanes at clock speeds from 16 to 40MHz. It may also be used to drive data over Unshielded Twisted Pair (UTP) cable.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE®.

The following sections describe each operation and passive state.

Initialization

Before data can be transferred both devices must be initialized. Initialization refers to synchronization of the Serializer and the Deserializer PLL's to local clocks that may be the same or separate. Afterward, synchronization of Deserializer to Serializer occurs as the second step of initialization.

Step 1: When V_{CC} is applied to both Serializer and/or Deserializer, the respective outputs are held in TRI-STATE® and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock, TCLK, provided by the source ASIC or other device. For the Deserializer, the local clock is provided by an on-board oscillator or other source and applied to the REFCLK pin. After V_{CC} OK is reached the device's PLL will lock.

The Serializer outputs are held in TRI-STATE while the PLL locks to the TCLK. The Serializer is now ready to send data or SYNC patterns depending on the levels of the SYNC1 and SYNC2 inputs. The SYNC pattern is composed of six ones and six zeros switching at the input clock rate.

The Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL is locking to the local clock- the REFCLK input and then to SYNC patterns on the input.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. The transmission of SYNC patterns to the Deserializer enables the Deserializer to lock to the Serializer signal.

Control of the sync pins is left to the user. A feedback loop between the $\overline{\text{LOCK}}$ pin is one recommendation. Another option is that one or both of the Serializer SYNC inputs are asserted for at least 1024 cycles of TCLK to initiate transmission of SYNC patterns. The Serializer will continue to send SYNC patterns after the minimum of 1024 if either of the SYNC inputs remain high.

When the Deserializer detects edge transitions at the Bus LVDS input it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer inputs DIN0–DIN9 may be used to input data to the Serializer. Data is clocked into the Serializer by the TCLK input. The edge of TCLK used to strobe in data is selectable via the TCLK_R/$\overline{\text{F}}$ pin. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles the data at DIN 0-DIN9 is ignored regardless of the clock edge.

A start bit and a stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

Serialized data and clock bits (10+2 bits) are transmitted from the serial data output (DO) at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 x 12 = 480 Mega bits per second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data rate is 40 x 10 = 400 Mbps. TCLK is provided by the data source and must be in the range 16 MHz to 40 MHz nominal.

The outputs (DO±) can drive a heavily loaded backplane or a point-to-point connection. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ = high and SYNC1 and SYNC2 are low. The DEN pin may be used to TRI-STATE the outputs when driven low.

The $\overline{\text{LOCK}}$ pin on the Deserializer is driven low when it is synchronized with the Serializer. The Deserializer locks to the embedded clock and uses it to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low. Otherwise ROUT0–ROUT9 is invalid.

Data Transfer (Continued)

RCLK pin is the reference to data on the ROUT0-ROUT9 pins. The polarity of the RCLK edge is controlled by the RCLK_R/$\overline{F}$ input.

ROUT(0-9), $\overline{LOCK}$ and RCLK outputs will drive a minimum of three CMOS input gates (15 pF load) with 40 MHz clock.

Resynchronization

The Deserializer $\overline{LOCK}$ pin driven low indicates that the Deserializer PLL is locked to the embedded clock edge. If the Deserializer loses lock, the $\overline{LOCK}$ output will go high and the outputs (including RCLK) will be TRI-STATE.

The $\overline{LOCK}$ pin must be monitored by the system to detect a loss of synchronization and the system must arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. There are multiple approaches possible. One recommendation is to provide a feedback loop using the $\overline{LOCK}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Otherwise, $\overline{LOCK}$ pin needs to be monitored and when it is a high, the system needs to ensure that one or both of the Serializer SYNC inputs area asserted for at least 1024 cycles of TCLK. A minimum of 1024 sync patterns are needed to resynchronize. Dual SYNC pins are provided for multiple control in a multi-drop application.

Powerdown

The Powerdown state is a low power sleep mode that the Serializer and Deserializer may use to reduce power when there is no data to be transferred. Powerdown is entered when $\overline{PWRDN}$ and REN are driven low on the Deserializer, and when the PWRDN is driven low on the Serializer. In Powerdown, the PLL is stopped and the outputs go into TRI-STATE, disabling load current and also reducing supply current to the milliamp range. To exit Powerdown, $\overline{PWRDN}$ is driven high.

Both the Serializer and Deserializer must reinitialize and resynchronize before data can be transferred. Initialization of the Serializer takes 1024 TCLK cycles. The Deserializer will initialize and assert $\overline{LOCK}$ high until it is locked to the Bus LVDS clock.

TRI-STATE

For the Serializer, TRI-STATE is entered when the DEN pin is driven low. This will TRI-STATE both driver output pins (DO+ and DO−). When DEN is driven high the serializer will return to the previous state as long as all other control pins remain static (SYNC1, SYNC2, $\overline{PWRDN}$, TCLK_R/$\overline{F}$).

For the Deserializer, TRI-STATE is entered when the REN pin is driven low. This will TRI-STATE the receiver output pins (ROUT0–ROUT9), $\overline{LOCK}$ and RCLK.

Order Numbers

NSID	Function	Package
DS92LV1021TMSA	Serializer	MSA28
DS92LV1210TMSA	Deserializer	MSA28

National Semiconductor

DS92LV1212A
16-40 MHz 10-Bit Bus LVDS Random Lock Deserializer with Embedded Clock Recovery

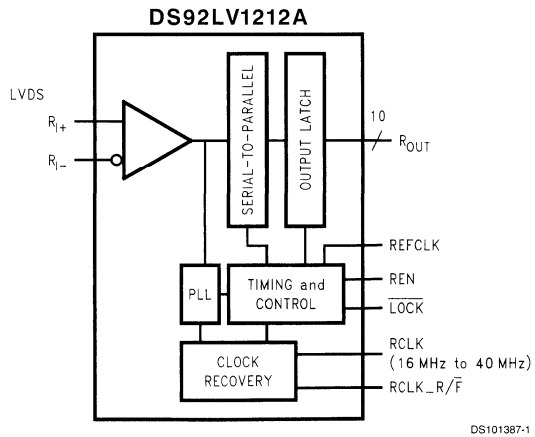
General Description

The DS92LV1212A is an upgrade of the DS92LV1212. It maintains all of the features of the DS92LV1212. The DS92LV1212A is designed to be used with the DS92LV1021 Bus LVDS Serializer. The DS92LV1212A receives a Bus LVDS serial data stream and transforms it into a 10-bit wide parallel data bus and separate clock. The reduced cable, PCB trace count and connector size saves cost and makes PCB layout easier. Clock-to-data and data-to-data skews are eliminated since one input receives both clock and data bits serially. The powerdown pin is used to save power by reducing the supply current when the device is not in use. The Deserializer will establish lock to a synchronization pattern within specified lock times but it can also lock to a data stream without SYNC patterns.

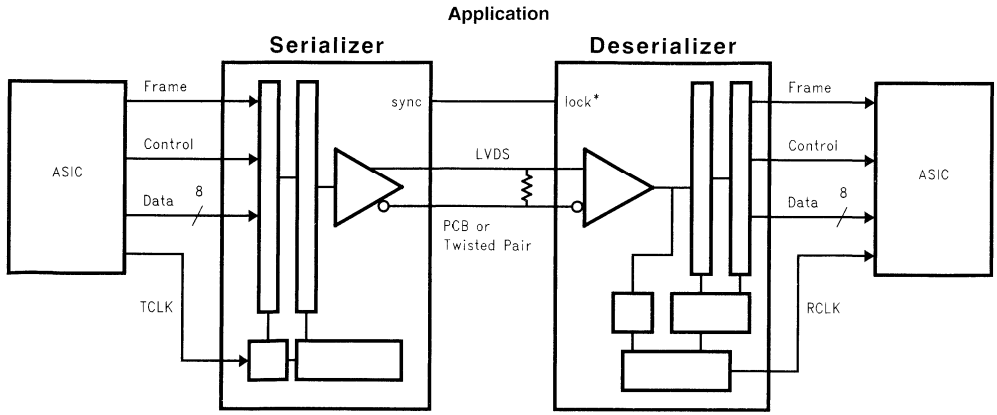
Features

- Clock recovery without SYNC patterns-random lock
- Guaranteed transition every data transfer cycle
- Chipset (Tx + Rx) power consumption < 300mW (typ) @ 40MHz
- Single differential pair eliminates multi-channel skew
- 400 Mbps serial Bus LVDS bandwidth (at 40 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits or UTOPIA I Interface
- Synchronization mode and LOCK indicator
- Flow-through pinout for easy PCB layout
- High impedance on receiver inputs when power is off
- Programmable edge trigger on clock
- Footprint compatible with DS92LV1210
- Small 28-lead SSOP package-MSA

Block Diagram



Block Diagram (Continued)



Functional Description

The DS92LV1212 is a 10-bit Deserializer chip designed to receive data over heavily loaded differential backplanes at clock speeds from 16 MHz to 40 MHz. It may also be used to receive data over Unshielded Twisted Pair (UTP) cable.

The chip has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE®.

The following sections describe each operation of the active and passive states.

Initialization

Before data can be transferred, the Deserializer must be initialized. The Deserializer should be powered up with the PWRDN pin held low. After V_{CC} stabilizes, the PWRDN pin can be forced high. The Deserializer is ready to lock to the incoming data stream.

Step 1: When you apply V_{CC} to the Deserializer, the respective outputs are held in TRI-STATE and internal circuitry is disabled by on-chip power-on circuitry. When V_{CC} reaches V_{CC} OK (2.5V), the PLL is ready to lock to incoming data or synchronization patterns. You must apply the local clock to the REFCLK pin.

The Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL locks to incoming data or to SYNC patterns on the inputs.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete the initialization. The Deserializer will lock to non-repetitive data patterns; however, the transmission of SYNC patterns to the Deserializer enables the Deserializer to lock to the Serializer signal within a specified time. See *Figure 7*.

The user's application determines control of the SYNC1 and SYNC2 pins. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

Serialized data and clock bits (10+2 bits) are received at 12 times the TCLK frequency. For example, if TCLK is 40 MHz, the serial rate is 40 x 12 = 480 Mega bits per second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 40 MHz, the payload data rate is 40 x 10 = 400 Mbps. TCLK is provided by the data source and must be in the range 16 MHz to 40 MHz nominal.

The $\overline{\text{LOCK}}$ pin on the Deserializer is driven low when it is synchronized with the Serializer. The Deserializer locks to the embedded clock and uses it to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low. Otherwise, ROUT0–ROUT9 is invalid.

The ROUT0-ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/$\overline{\text{F}}$ input. See *Figure 5*.

ROUT(0-9), $\overline{\text{LOCK}}$ and RCLK outputs will drive a minimum of three CMOS input gates (15 pF load) with 40 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer $\overline{\text{LOCK}}$ pin asserts a low. If the Deserializer loses lock, the $\overline{\text{LOCK}}$ pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the $\overline{\text{LOCK}}$ pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One

Resynchronization (Continued)

recommendation is to provide a feedback loop using the LOCK pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the DS92LV1212A can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the DS92LV1212A to operate in "open-loop" applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. The primary constraint on "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter "false lock" - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the DS92LV1212A can detect that the possibility of "false lock" exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the LOCK output from becoming active until the potential "false lock" pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown on the following page. Please note that RMT only applies to bits DIN0-DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive PWRDN and REN low. The Serializer enters Powerdown when you drive PWRDN low. In Powerdown, the PLL stops and the outputs enterTRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the PWRDN pin high.

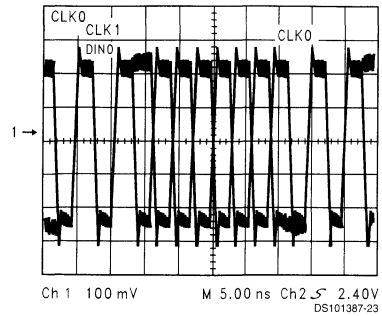
Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert LOCK high until lock to the Bus LVDS clock occurs.

TRI-STATE

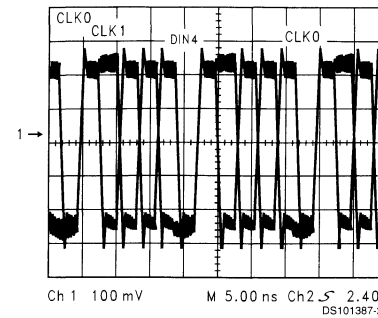
The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, PWRDN, TCLK_R/F).

When you drive the REN pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The LOCK output remains active, reflecting the state of the PLL.

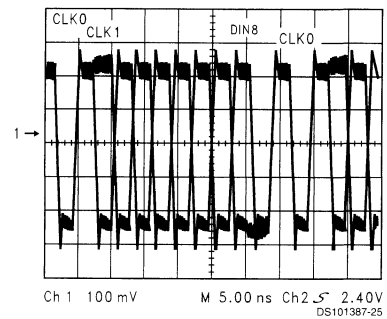
RMT Patterns



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern

Order Numbers

NSID	Function	Package
DS92LV1021TMSA	Serializer	MSA28
DS92LV1212AMSA	Deserializer	MSA28

National Semiconductor

SCAN921023 and SCAN921224
20-66 MHz 10 Bit Bus LVDS Serializer and Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST

General Description

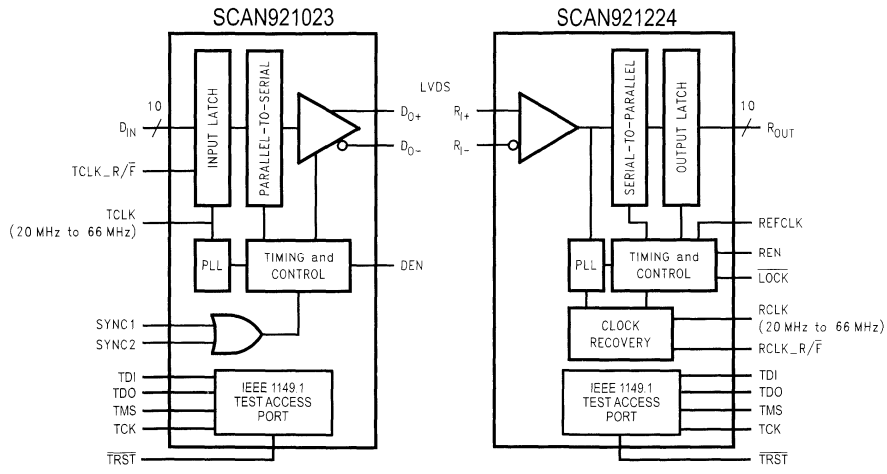
The SCAN921023 transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. The SCAN921224 receives the Bus LVDS serial data stream and transforms it back into a 10-bit wide parallel data bus and recovers parallel clock. Both devices are compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCK), and the optional Test Reset ($\overline{TRST}$). IEEE 1149.1 features provide the designer or test engineer access to the backplane or cable interconnects and the ability to verify differential signal integrity to enhance their system test strategy. The pair of devices also features an at-speed BIST mode which allows the interconnects between the Serializer and Deserializer to be verified at-speed.

The SCAN921023 transmits data over backplanes or cable. The single differential pair data path makes PCB design easier. In addition, the reduced cable, PCB trace count, and connector size tremendously reduce cost. Since one output transmits clock and data bits serially, it eliminates clock-to-data and data-to-data skew. The powerdown pin saves power by reducing supply current when not using either device. Upon power up of the Serializer, you can choose to activate synchronization mode or allow the Deserializer to use the synchronization-to-random-data feature. By using the synchronization mode, the Deserializer will establish lock to a signal within specified lock times. In addition, the embedded clock guarantees a transition on the bus every 12-bit cycle. This eliminates transmission errors due to charged cable conditions. Furthermore, you may put the SCAN921023 output pins into TRI-STATE to achieve a high impedance state. The PLL can lock to frequencies between 20 MHz and 66 MHz.

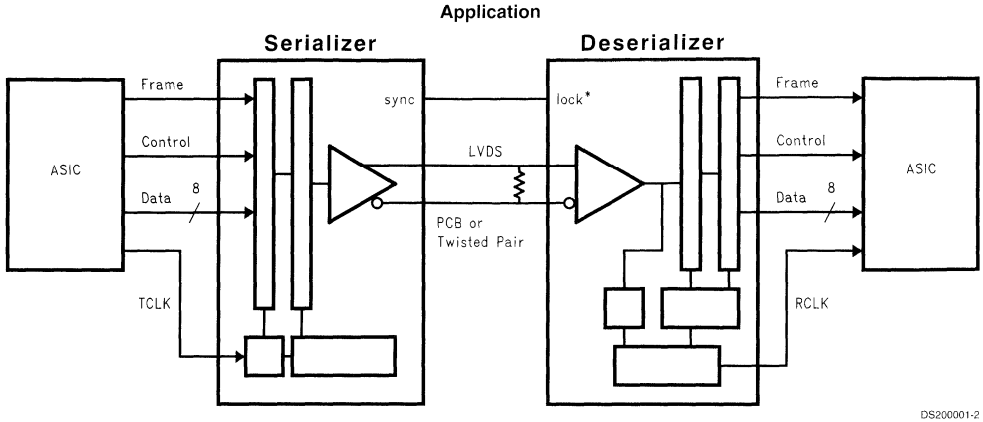
Features

- IEEE 1149.1 (JTAG) Compliant and At-Speed BIST test mode.
- Clock recovery from PLL lock to random data patterns.
- Guaranteed transition every data transfer cycle
- Chipset (Tx + Rx) power consumption < 500 mW (typ) @ 66 MHz
- Single differential pair eliminates multi-channel skew
- Flow-through pinout for easy PCB layout
- 660 Mbps serial Bus LVDS data rate (at 66 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits
- Synchronization mode and LOCK indicator
- Programmable edge trigger on clock
- High impedance on receiver inputs when power is off
- Bus LVDS serial output rated for 27Ω load
- Small 49-lead BGA package

Block Diagrams



Block Diagrams (Continued)



Functional Description

The SCAN921023 and SCAN921224 are a 10-bit Serializer and Deserializer chipset designed to transmit data over differential backplanes at clock speeds from 20 to 66 MHz. The chipset is also capable of driving data over Unshielded Twisted Pair (UTP) cable.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE. In addition to the active and passive states, there are also test modes for JTAG access and at-speed BIST.

The following sections describe each operation and passive state and the test modes.

Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the Serializer and Deserializer PLL's to local clocks, which may be the same or separate. Afterwards, synchronization of the Deserializer to Serializer occurs.

Step 1: When you apply V_{CC} to both Serializer and/or Deserializer, the respective outputs enter TRI-STATE, and on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches V_{CC}OK (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock (TCLK) provided by the source ASIC or other device. For the Deserializer, you must apply a local clock to the REFCLK pin.

The Serializer outputs remain in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer is now ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs or a data stream. The SYNC pattern sent by the Serializer consists of six ones and six zeros switching at the input clock rate.

Note that the Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL locks to the incoming data or to SYNC patterns on the input.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete initialization. The Deserializer will lock to non-repetitive data patterns. However, the transmission of SYNC patterns enables the Deserializer to lock to the Serializer signal within a specified time. See *Figure 9*.

The user's application determines control of the SYNC1 and SYNC 2 pins. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The Serializer transmits serialized data and clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is 66 x 12 = 792 Mega-bits-per-second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz. the payload data rate is 66 x 10 = 660 Mbps. The data source provides TCLK and must be in the range of 20 MHz to 66 MHz nominal.

The Serializer outputs (DO±) can drive a point-to-point connection or in limited multi-point or multi-drop backplanes. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the Serializer output pins will enter TRI-STATE.

When the Deserializer synchronizes to the Serializer, the $\overline{\text{LOCK}}$ pin is low. The Deserializer locks to the embedded

Data Transfer (Continued)

clock and uses it to recover the serialized data. ROUT data is valid when $\overline{LOCK}$ is low. Otherwise ROUT0–ROUT9 is invalid.

The ROUT0-ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/$\overline{F}$ input. See *Figure 13*.

ROUT(0-9), $\overline{LOCK}$ and RCLK outputs will drive a maximum of three CMOS input gates (15 pF load) with a 66 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer $\overline{LOCK}$ pin asserts a low. If the Deserializer loses lock, the $\overline{LOCK}$ pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the $\overline{LOCK}$ pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One recommendation is to provide a feedback loop using the $\overline{LOCK}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the SCAN921224 can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the SCAN921224 to operate in "open-loop" applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. However, please see *Table 1* for some general random lock times under specific conditions. The primary constraint on the "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter "false lock" - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the SCAN921224 can detect that the possibility of "false lock" exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the $\overline{LOCK}$ output from becoming active until the potential "false lock" pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown in *Figure 1*. Please note that RMT only applies to bits DIN0-DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive $\overline{PWRDN}$ and $\overline{REN}$ low. The Serializer enters Powerdown when you drive $\overline{PWRDN}$ low. In Powerdown, the PLL stops and the outputs enterTRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the $\overline{PWRDN}$ pin high.

Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert $\overline{LOCK}$ high until lock to the Bus LVDS clock occurs.

TRI-STATE

The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, $\overline{PWRDN}$, TCLK_R/$\overline{F}$).

When you drive the $\overline{REN}$ pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The $\overline{LOCK}$ output remains active, reflecting the state of the PLL.

TABLE 1.

Random Lock Times for the SCAN921224		
	66 MHz	Units
Maximum	18	µS
Mean	3.0	µS
Minimum	0.43	µS
Conditions:	PRBS 2^{15}, V_{CC} = 3.3V	

1) Difference in lock times are due to different starting points in the data pattern with multiple parts.

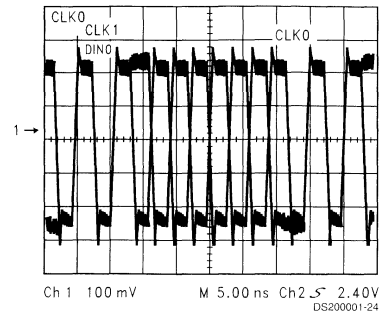
Test Modes

In addition to the IEEE 1149.1 test access to the digital TTL pins, the SCAN921023 and SCAN921224 have two instructions to test the LVDS interconnects. The first is EXTEST. This is implemented at LVDS levels and is only intended as a go no-go test (e.g. missing cables). The second method is the RUNBIST instruction. It is an 'at-system-speed' interconnect test. It is executed in approximately 33mS with a system clock speed of 66MHz. There are two bits in the RX BIST data register for notification of PASS/FAIL and TEST_COMPLETE. Pass indicates that the BER (Bit-Error-Rate) is better than 10^{-7}.

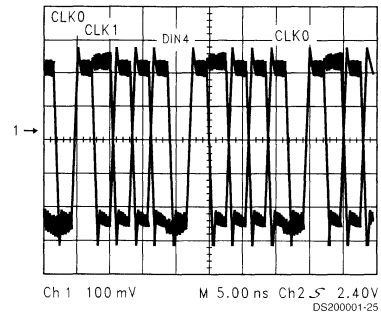
An important detail is that once both devices have the RUNBIST instruction loaded into their respective instruction registers, both devices must move into the RTI state within 4K system clocks (At a SCLK of 66Mhz and TCK of 1MHz this allows for 66 TCK cycles). This is not a concern when both devices are on the same scan chain or LSP, however, it can be a problem with some multi-drop devices. This test mode has been simulated and verified using National's SCANSTA111.

Ordering Information

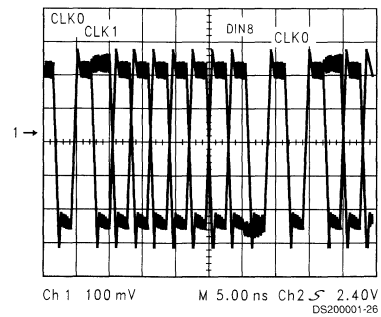
NSID	Function	Package
SCAN921023SLC	Serializer	SLC49a
SCAN921224SLC	Deserializer	SLC49a



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern

FIGURE 1. RMT Patterns Seen on the Bus LVDS Serial Output

National Semiconductor

SCAN921025 and SCAN921226
30-80 MHz 10 Bit Bus LVDS Serializer and Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST

General Description

The SCAN921025 transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. The SCAN921226 receives the Bus LVDS serial data stream and transforms it back into a 10-bit wide parallel data bus and recovers parallel clock.

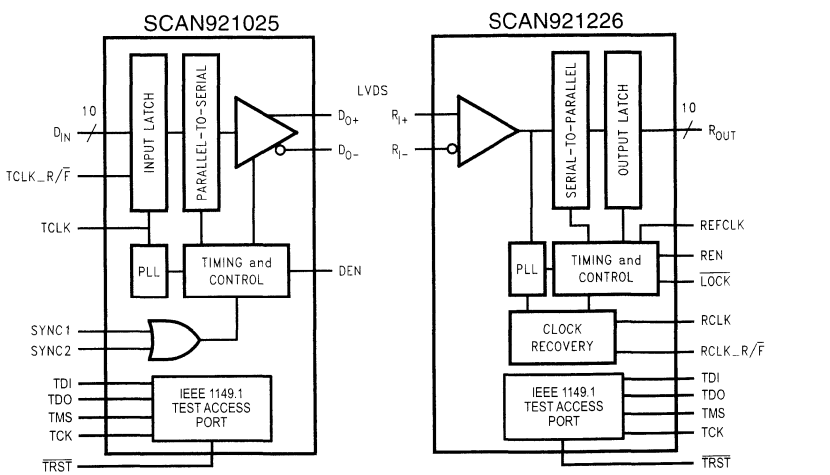
Both devices are compliant with IEEE 1149.1 Standard for Boundary Scan Test. IEEE 1149.1 features provide the design or test engineer access via a standard Test Access Port (TAP) to the backplane or cable interconnects and the ability to verify differential signal integrity. The pair of devices also features an at-speed BIST mode which allows the interconnects between the Serializer and Deserializer to be verified at-speed.

The SCAN921025 transmits data over backplanes or cable. The single differential pair data path makes PCB design easier. In addition, the reduced cable, PCB trace count, and connector size tremendously reduce cost. Since one output transmits clock and data bits serially, it eliminates clock-to-data and data-to-data skew. The powerdown pin saves power by reducing supply current when not using either device. Upon power up of the Serializer, you can choose to activate synchronization mode or allow the Deserializer to use the synchronization-to-random-data feature. By using the synchronization mode, the Deserializer will establish lock to a signal within specified lock times. In addition, the embedded clock guarantees a transition on the bus every 12-bit cycle. This eliminates transmission errors due to charged cable conditions. Furthermore, you may put the SCAN921025 output pins into TRI-STATE to achieve a high impedance state. The PLL can lock to frequencies between 30 MHz and 80 MHz.

Features

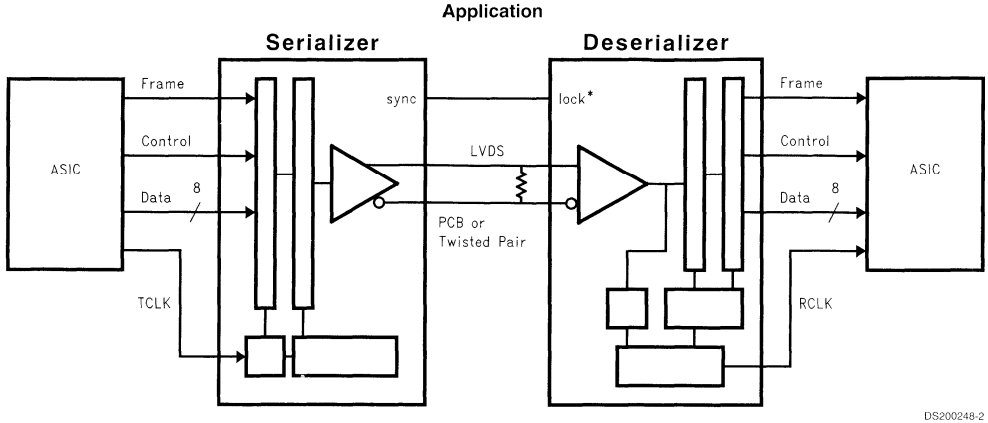
- IEEE 1149.1 (JTAG) Compliant and At-Speed BIST test mode.
- Clock recovery from PLL lock to random data patterns.
- Guaranteed transition every data transfer cycle
- Chipset (Tx + Rx) power consumption < 600 mW (typ) @ 80 MHz
- Single differential pair eliminates multi-channel skew
- 800 Mbps serial Bus LVDS data rate (at 80 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits
- Synchronization mode and LOCK indicator
- Programmable edge trigger on clock
- High impedance on receiver inputs when power is off
- Bus LVDS serial output rated for 27Ω load
- Small 49-lead BGA package

Block Diagrams



DS200248-1

Block Diagrams (Continued)



Functional Description

The SCAN921025 and SCAN921226 are a 10-bit Serializer and Deserializer chipset designed to transmit data over differential backplanes at clock speeds from 30 to 80 MHz. The chipset is also capable of driving data over Unshielded Twisted Pair (UTP) cable.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE. In addition to the active and passive states, there are also test modes for JTAG access and at-speed BIST.

The following sections describe each operation and passive state and the test modes.

Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the Serializer and Deserializer PLL's to local clocks, which may be the same or separate. Afterwards, synchronization of the Deserializer to Serializer occurs.

Step 1: When you apply V_{CC} to both Serializer and/or Deserializer, the respective outputs enter TRI-STATE, and on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches V_{CC}OK (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock (TCLK) provided by the source ASIC or other device. For the Deserializer, you must apply a local clock to the REFCLK pin.

The Serializer outputs remain in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer is now ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs or a data stream. The SYNC pattern sent by the Serializer consists of six ones and six zeros switching at the input clock rate.

Note that the Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL locks to the incoming data or to SYNC patterns on the input.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete initialization. The Deserializer will lock to non-repetitive data patterns. However, the transmission of SYNC patterns enables the Deserializer to lock to the Serializer signal within a specified time. See *Figure 9.*

The user's application determines control of the SYNC1 and SYNC 2 pins. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The Serializer transmits serialized data and clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 80 MHz, the serial rate is 80 x 12 = 960 Mega-bits-per-second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 80 MHz, the payload data rate is 80 x 10 = 800 Mbps. The data source provides TCLK and must be in the range of 30 MHz to 80 MHz nominal.

The Serializer outputs (DO±) can drive a point-to-point connection or in limited multi-point or multi-drop backplanes. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the Serializer output pins will enter TRI-STATE.

When the Deserializer synchronizes to the Serializer, the $\overline{\text{LOCK}}$ pin is low. The Deserializer locks to the embedded

Data Transfer (Continued)

clock and uses it to recover the serialized data. ROUT data is valid when $\overline{LOCK}$ is low. Otherwise ROUT0–ROUT9 is invalid.

The ROUT0-ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/$\overline{F}$ input. See *Figure 13*.

ROUT(0-9), $\overline{LOCK}$ and RCLK outputs will drive a maximum of three CMOS input gates (15 pF load) with a 80 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer $\overline{LOCK}$ pin asserts a low. If the Deserializer loses lock, the $\overline{LOCK}$ pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the $\overline{LOCK}$ pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One recommendation is to provide a feedback loop using the $\overline{LOCK}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the SCAN921226 can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the SCAN921226 to operate in "open-loop" applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. However, please see *Table 1* for some general random lock times under specific conditions. The primary constraint on the "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter "false lock" - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the SCAN921226 can detect that the possibility of "false lock" exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the $\overline{LOCK}$ output from becoming active until the potential "false lock" pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown in *Figure 1*. Please note that RMT only applies to bits DIN0-DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive $\overline{PWRDN}$ and $\overline{REN}$ low. The Serializer enters Powerdown when you drive $\overline{PWRDN}$ low. In Powerdown, the PLL stops and the outputs enter TRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the $\overline{PWRDN}$ pin high.

Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert $\overline{LOCK}$ high until lock to the Bus LVDS clock occurs.

TRI-STATE

The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, $\overline{PWRDN}$, TCLK_R/$\overline{F}$).

When you drive the REN pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The $\overline{LOCK}$ output remains active, reflecting the state of the PLL.

TABLE 1.

Random Lock Times for the SCAN921226		
	80 MHz	Units
Maximum	18	µs
Mean	3.0	µs
Minimum	0.43	µs
Conditions:	PRBS 2^{15}, V_{CC} = 3.3V	

1) Difference in lock times are due to different starting points in the data pattern with multiple parts.

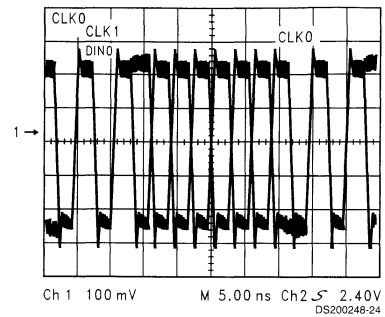
Test Modes

In addition to the IEEE 1149.1 test access to the digital TTL pins, the SCAN921025 and SCAN921226 have two instructions to test the LVDS interconnects. The first is EXTEST. This is implemented at LVDS levels and is only intended as a go no-go test (e.g. missing cables). The second method is the RUNBIST instruction. It is an 'at-system-speed' interconnect test. It is executed in approximately 33mS with a system clock speed of 66MHz. There are two bits in the RX BIST data register for notification of PASS/FAIL and TEST_COMPLETE. Pass indicates that the BER (Bit-Error-Rate) is better than 10^{-7}.

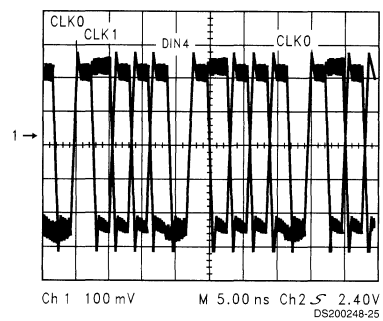
An important detail is that once both devices have the RUNBIST instruction loaded into their respective instruction registers, both devices must move into the RTI state within 4K system clocks (At a SCLK of 66Mhz and TCK of 1MHz this allows for 66 TCK cycles). This is not a concern when both devices are on the same scan chain or LSP, however, it can be a problem with some multi-drop devices. This test mode has been simulated and verified using National's SCANSTA111.

Ordering Information

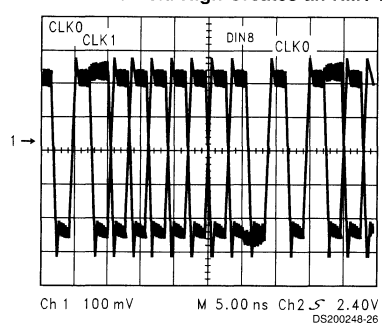
NSID	Function	Package
SCAN921025SLC	Serializer	SLC49a
SCAN921226SLC	Deserializer	SLC49a



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern

FIGURE 1. RMT Patterns Seen on the Bus LVDS Serial Output

National Semiconductor

DS92LV1023 and DS92LV1224
40-66 MHz 10 Bit Bus LVDS Serializer and Deserializer

General Description

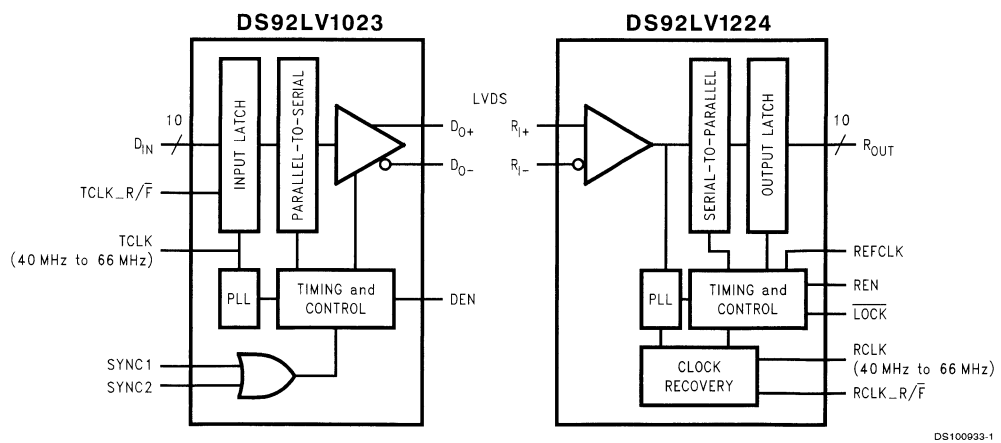
The DS92LV1023 transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. The DS92LV1224 receives the Bus LVDS serial data stream and transforms it back into a 10-bit wide parallel data bus and recovers parallel clock. The DS92LV1023 transmits data over backplanes or cable. The single differential pair data path makes PCB design easier. In addition, the reduced cable, PCB trace count, and connector size tremendously reduce cost. Since one output transmits clock and data bits serially, it eliminates clock-to-data and data-to-data skew. The powerdown pin saves power by reducing supply current when not using either device. Upon power up of the Serializer, you can choose to activate synchronization mode or allow the Deserializer to use the synchronization-to-random-data feature. By using the synchronization mode, the Deserializer will establish lock to a signal within specified lock times. In addition, the embedded clock guarantees a transition on the bus every 12-bit cycle. This eliminates transmission errors due to charged cable conditions. Furthermore, you may put the DS92LV1023 output pins into TRI-STATE ® to achieve a high impedance state. The PLL can lock to frequencies between 40 MHz and 66 MHz.

Features

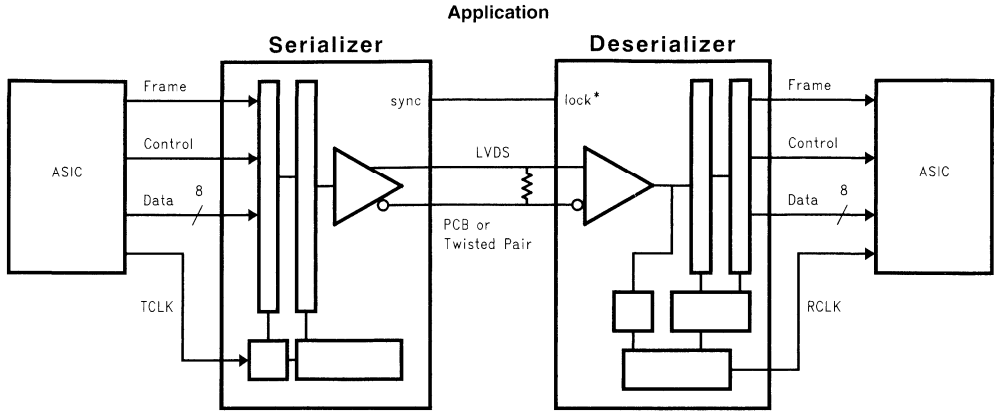
- Clock recovery from PLL lock to random data patterns.
- Guaranteed transition every data transfer cycle
- Chipset (Tx + Rx) power consumption < 500 mW (typ) @ 66 MHz
- Single differential pair eliminates multi-channel skew
- Flow-through pinout for easy PCB layout
- 660 Mbps serial Bus LVDS data rate (at 66 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits
- Synchronization mode and LOCK indicator
- Programmable edge trigger on clock
- High impedance on receiver inputs when power is off
- Bus LVDS serial output rated for 27Ω load
- Small 28-lead SSOP package

9

Block Diagrams



Block Diagrams (Continued)



Functional Description

The DS92LV1023 and DS92LV1224 are a 10-bit Serializer and Deserializer chipset designed to transmit data over differential backplanes at clock speeds from 40 to 66 MHz. The chipset is also capable of driving data over Unshielded Twisted Pair (UTP) cable.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE®.

The following sections describe each operation and passive state.

Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the Serializer and Deserializer PLL's to local clocks, which may be the same or separate. Afterwards, synchronization of the Deserializer to Serializer occurs.

Step 1: When you apply V_{CC} to both Serializer and/or Deserializer, the respective outputs enter TRI-STATE®, and on-chip power-on circuitry disables internal circuitry. When V_{CC} reaches V_{CC}OK (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock (TCLK) provided by the source ASIC or other device. For the Deserializer, you must apply a local clock to the REFCLK pin.

The Serializer outputs remain in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer is now ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs or a data stream. The SYNC pattern sent by the Serializer consists of six ones and six zeros switching at the input clock rate.

Note that the Deserializer $\overline{\text{LOCK}}$ output will remain high while its PLL locks to the incoming data or to SYNC patterns on the input.

Step 2: The Deserializer PLL must synchronize to the Serializer to complete initialization. The Deserializer will lock to non-repetitive data patterns. However, the transmission of SYNC patterns enables the Deserializer to lock to the Serializer signal within a specified time. See *Figure 9*.

The user's application determines control of the SYNC1 and SYNC 2 pins. One recommendation is a direct feedback loop from the $\overline{\text{LOCK}}$ pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the $\overline{\text{LOCK}}$ output will go low. When $\overline{\text{LOCK}}$ is low, the Deserializer outputs represent incoming Bus LVDS data.

Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK_R/$\overline{\text{F}}$ pin selects which edge the Serializer uses to strobe incoming data. TCLK_R/$\overline{\text{F}}$ high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for 5*TCLK cycles, the data at DIN0-DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The Serializer transmits serialized data and clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is 66 x 12 = 792 Mega-bits-per-second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz, the payload data rate is 66 x 10 = 660 Mbps. The data source provides TCLK and must be in the range of 40 MHz to 66 MHz nominal.

The Serializer outputs (DO±) can drive a point-to-point connection or in limited multi-point or multi-drop backplanes. The outputs transmit data when the enable pin (DEN) is high, $\overline{\text{PWRDN}}$ = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the Serializer output pins will enter TRI-STATE.

When the Deserializer synchronizes to the Serializer, the $\overline{\text{LOCK}}$ pin is low. The Deserializer locks to the embedded clock and uses it to recover the serialized data. ROUT data is valid when $\overline{\text{LOCK}}$ is low. Otherwise ROUT0–ROUT9 is invalid.

Data Transfer (Continued)

The ROUT0-ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK_R/$\overline{F}$ input. See *Figure 13*.

ROUT(0-9), $\overline{LOCK}$ and RCLK outputs will drive a maximum of three CMOS input gates (15 pF load) with a 66 MHz clock.

Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer $\overline{LOCK}$ pin asserts a low. If the Deserializer loses lock, the $\overline{LOCK}$ pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the $\overline{LOCK}$ pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One recommendation is to provide a feedback loop using the $\overline{LOCK}$ pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the DS92LV1224 can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the DS92LV1224 to operate in "open-loop" applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. However, please see *Table 1* for some general random lock times under specific conditions. The primary constraint on the "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter "false lock" - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the DS92LV1224 can detect that the possibility of "false lock" exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the $\overline{LOCK}$ output from becoming active until the potential "false lock" pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in the serial data stream. Graphical representations of RMT are shown in *Figure 1*. Please note that RMT only applies to bits DIN0-DIN8.

Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive $\overline{PWRDN}$ and REN low. The Serializer enters Powerdown when you drive $\overline{PWRDN}$ low. In Powerdown, the PLL stops and the outputs enterTRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the $\overline{PWRDN}$ pin high.

Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert $\overline{LOCK}$ high until lock to the Bus LVDS clock occurs.

TRI-STATE

The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2, $\overline{PWRDN}$, TCLK_R/$\overline{F}$).

When you drive the REN pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The $\overline{LOCK}$ output remains active, reflecting the state of the PLL.

TABLE 1.

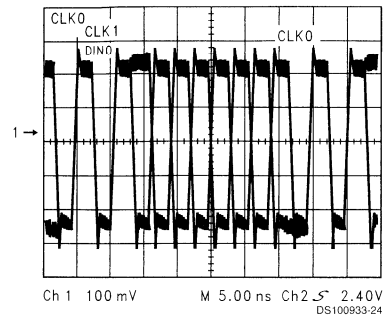
Random Lock Times for the DS92LV1224			
	40 MHz	66 MHz	Units
Maximum	26	18	µS
Mean	4.5	3.0	µS
Minimum	0.77	0.43	µS
Conditions:	PRBS 2^{15}, V_{CC} = 3.3V		

1) Difference in lock times are due to different starting points in the data pattern with multiple parts.

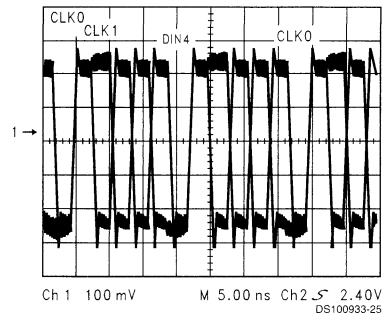
9

Ordering Information

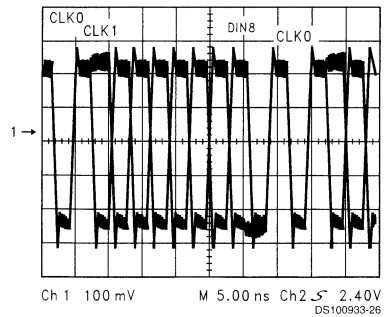
NSID	Function	Package
DS92LV1023TMSA	Serializer	MSA28
DS92LV1224TMSA	Deserializer	MSA28



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern

FIGURE 1. RMT Patterns Seen on the Bus LVDS Serial Output

National Semiconductor

DS92LV1260
Six Channel 10 Bit BLVDS Deserializer

General Description

The DS92LV1260 integrates six deserializer devices into a single chip. The chip uses a 0.25u CMOS process technology. The DS92LV1260 can simultaneously deserialize up to six data streams that have been serialized by the National Semiconductor DS92LV1021 or DS92LV1023 Bus LVDS serializers. The device also includes a seventh serial input channel that serves as a redundant input.

Each deserializer block in the DS92LV1260 operates independently with its own clock recovery circuitry and lock-detect signaling.

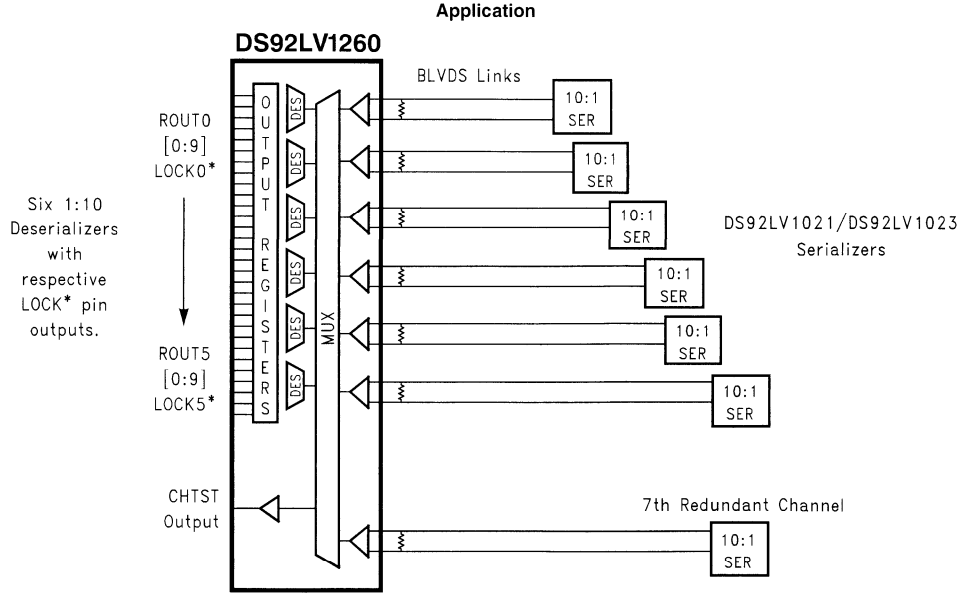
The DS92LV1260 uses a single +3.3V power supply with a typical power dissipation of 1.2W at 3.3V with a PRBS-15 pattern. Refer to the Connection Diagrams for packaging information.

Features

- Deserializes one to six BusLVDS input serial data streams with embedded clocks
- Seven selectable serial inputs to support n+1 redundancy of deserialized streams
- Seventh channel has single pin monitor output that reflects input from seventh channel input
- Parallel clock rate up to 40MHz
- On chip filtering for PLL
- Absolute maximum worst case power dissipation = 1.9W at 3.6V
- High impedance inputs upon power off (V_{CC} = 0V)
- Single power supply at +3.3V
- 196-pin LBGA package (Low-profile Ball Grid Array) package
- Industrial temperature range operation: −40°C to +85°C

Block Diagram

Application



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National Semiconductor

SCAN921260
X6 1:10 Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST

General Description

The SCAN921260 integrates six deserializer devices into a single chip. The SCAN921260 can simultaneously deserialize up to six data streams that have been serialized by the National Semiconductor SCAN921023 Bus LVDS serialiser. The device also includes a seventh serial input channel that serves as a redundant input.

Each deserializer block in the SCAN921260 operates independently with its own clock recovery circuitry and lock-detect signaling.

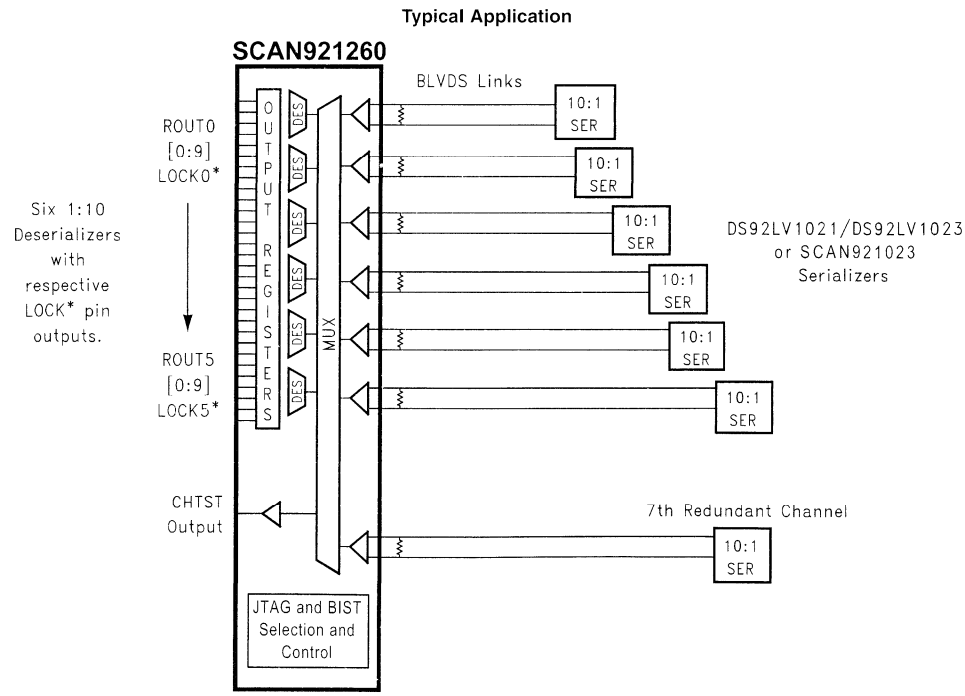
The SCAN921260 uses a single +3.3V power supply with an estimated power dissipation of 1.2W at 3.3V with a PRBS-15 pattern. Refer to the Connection Diagrams for packaging information.

Features

- IEEE 1149.1 (JTAG) Compliant and at-speed BIST test modes
- Deserializes one to six BusLVDS input serial data streams with embedded clocks
- Seven selectable serial inputs to support n+1 redundancy of deserialized streams
- Seventh channel has single pin monitor output that reflects input from seventh channel input
- Parallel clock rate up to 66MHz
- On chip filtering for PLL
- High impedance inputs upon power off (V_{CC} = 0V)
- Single power supply at +3.3V
- 196-pin LBGA package (Low-profile Ball Grid Array) package
- Industrial temperature range operation: −40 to +85

Functional Block Diagram

Typical Application



DS200147-2

National Semiconductor

PRELIMINARY

DS92LV8028
8 Channel 10:1 Serializer

General Description

The DS92LV8028 integrates eight serializer devices into a single chip. The DS92LV8028 can simultaneously serialize up to eight 10-bit data streams. The 10-bit parallel inputs are LVTTL signal levels. The serialized outputs are LVDS signals with extra drive current for point-to-point and lightly loaded multidrop applications. Each serializer block in the DS92LV8028 operates independently by using strobes from a single shared PLL.

The DS92LV8028 uses a single +3.3V power supply with a typical power dissipation of 740mW (3.3V / PRBS / 66 MHz). Each serializer channel has a unique power down control to further conserve power consumption.

For high-speed LVDS serial data transmission, line quality is essential, thus the DS92LV8028 includes an @SPEED TEST function. Each Serializer channel has the ability internally generated a PRBS data pattern. This pattern is received by specific deserializers (SCAN921224) which have the complement PRBS verification circuit. The deserializer checks the data pattern for bit errors and reports any errors on the test verification pins on the deserializer.

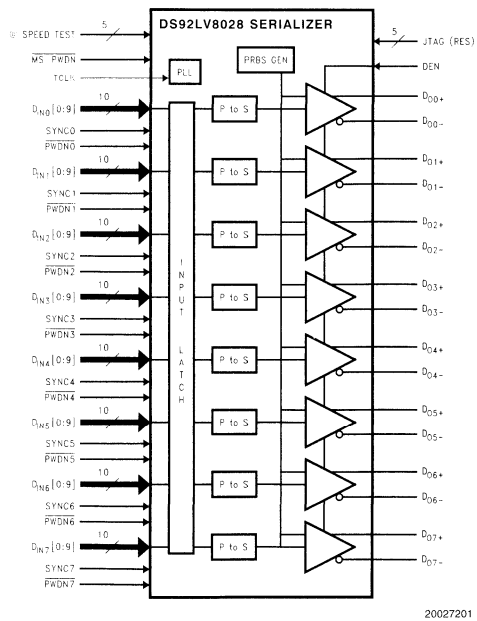
For additional information - please see the **Applications Information** section in this datasheet.

Features

- All 8 channels synchronous to one parallel clock rate, from 25 to 66 MHz
- Duplicates function of multiple DS92LV1021 and '1023 10-bit Serializer devices
- Serializes from one to eight 10-bit parallel inputs into data streams with embedded clock
- Eight 5 mA modified Bus LVDS outputs that are capable to drive double terminations
- @Speed Test - PRBS generation to check LVDS transmission path to SCAN921224 or SCAN921260
- On chip filtering for PLL
- 740mW typ power dissipation (loaded, PRBS, 66MHz, 3.3V)
- High impedance inputs and outputs on power off
- Single power supply at +3.3V (+/-10%)
- 196-pin LBGA package
- JTAG pins reserved for next version of device
- Industrial temperature range operation: -40 to +85 C

9

Block Diagram



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National Semiconductor

SCANSTA111 Enhanced SCAN bridge Multidrop Addressable IEEE 1149.1 (JTAG) Port

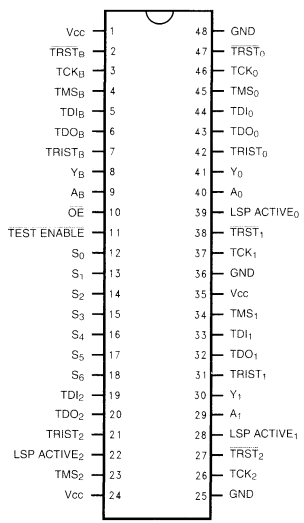
General Description

The SCANSTA111 extends the IEEE Std. 1149.1 test bus into a multidrop test bus environment. The advantage of a multidrop approach over a single serial scan chain is improved test throughput and the ability to remove a board from the system and retain test access to the remaining modules. Each SCANSTA111 supports up to 3 local IEEE1149.1 scan rings which can be accessed individually or combined serially. Addressing is accomplished by loading the instruction register with a value matching that of the Slot inputs. Backplane and inter-board testing can easily be accomplished by parking the local TAP Controllers in one of the stable TAP Controller states via a Park instruction. The 32-bit TCK counter enables built in self test operations to be performed on one port while other scan chains are simultaneously tested.

Features

- True IEEE 1149.1 hierarchical and multidrop addressable capability
- The 7 slot inputs support up to 121 unique addresses, an Interrogation Address, Broadcast Address, and 4 Multi-cast Group Addresses (address 000000 is reserved)
- 3 IEEE 1149.1-compatible configurable local scan ports
- Mode Register$_0$ allows local TAPs to be bypassed, selected for insertion into the scan chain individually, or serially in groups of two or three
- Transparent Mode can be enabled with a single instruction to conveniently buffer the backplane IEEE 1149.1 pins to those on a single local scan port
- LSP ACTIVE outputs provide local port enable signals for analog busses supporting IEEE 1149.4.
- General purpose local port passthrough bits are useful for delivering write pulses for FPGA programming or monitoring device status.
- Known Power-up state
- $\overline{\text{TRST}}$ on all local scan ports
- 32-bit TCK counter
- 16-bit LFSR Signature Compactor
- Local TAPs can become TRI-STATE via the $\overline{\text{OE}}$ input to allow an alternate test master to take control of the local TAPs (LSP$_{0\text{-}2}$ have a TRI-STATE notification output)
- 3.0-3.6V V_{CC} Supply Operation
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal

Connection Diagram



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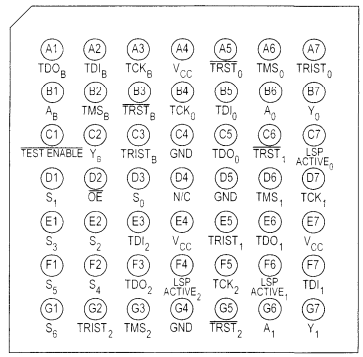


DS101245-16

Connection Diagram (Continued)

TABLE 1. Glossary

LFSR	Linear Feedback Shift Register. When enabled, will generate a 16-bit signature of sampled serial test data.
LSP	Local Scan Port. A four signal port that drives a local (i.e. non-backplane) scan chain. (e.g., TCK_0, TMS_0, TDO_0, TDI_0).
Local	Local is used to describe IEEE Std. 1149.1 compliant scan rings and the SCANSTA111 Test Access Port that drives them. The term local was adopted from the system test architecture that the 'STA111 will most commonly be used in; namely, a system test backplane with a 'STA111 on each card driving up to 3 local scan rings per card. (Each card can contain multiple 'STA111s, with 3 local scan ports per 'STA111.)
Park/Unpark/Unparked	Parked, unpark, and unparked, are used to describe the state of the LSP controller and the state of the local TAP controllers (the local TAP controllers refers to the TAP controllers of the scan components that make up a local scan ring). Park is also used to describe the action of parking a LSP (transitioning into one of the Parked LSP controller states). It is important to understand that when a LSP controller is in one of the parked states, TMS_n is held constant, thereby holding or parking the local TAP controllers in a given state.
TAP	Test Access Port as defined by IEEE Std. 1149.1.
Selected/Unselected	Selected and Unselected refers to the state of the 'STA111 Selection Controller. A selected 'STA111 has been properly addressed and is ready to receive Level 2 protocol. Unselected 'STA111s monitor the system test backplane, but do not accept Level 2 protocol (except for the *GOTOWAIT* instruction). The data registers and LSPs of unselected 'STA111s are not accessible from the system test master.
Active Scan Chain	The Active Scan Chain refers to the scan chain configuration as seen by the test master at a given moment. When a 'STA111 is selected with all of its LSPs parked, the active scan chain is the current scan register only. When a LSP is unparked, the active scan chain becomes: $TDI_B \rightarrow$ the current 'STA111 register $\rightarrow$ the local scan ring registers $\rightarrow$ a PAD bit $\rightarrow TDO_B$. Refer to *Table 7* for Unparked configurations of the LSP network.
Level 1 Protocol	Level 1 is the protocol used to address a 'STA111.
Level 2 Protocol	Level 2 is the protocol that is used once a 'STA111 is selected. Level 2 protocol is IEEE Std. 1149.1 compliant when an individual 'STA111 is selected.
PAD	A one bit register that is placed at the end of each local scan port scan-chain. The PAD bit eliminates the prop delay that would be added by the 'STA111 LSPN logic between TDI_n and $TDO_{(n+1)}$ or TDO_B by buffering and synchronizing the LSP TDI inputs to the falling edge of TCK_B, thus allowing data to be scanned at higher frequencies without violating set-up and hold times.
LSB	Least Significant Bit, the right-most position in a register (bit 0).
MSB	Most Significant Bit, the left-most position in a register.

Architecture

Figure 1 shows the basic architecture of the 'STA111. The device's major functional blocks are illustrated here. The TAP Controller, a 16-state state machine, is the central control for the device. The instruction register and various test data registers can be scanned to exercise the various functions of the 'STA111 (these registers behave as defined in IEEE Std. 1149.1). The 'STA111 selection controller provides the functionality that allows the 1149.1 protocol to be used in a multi-drop environment. It primarily compares the address input to the slot identification and enables the 'STA111 for subsequent scan operations. The Local Scan Port Network (LSPN) contains multiplexing logic used to select different port configurations. The LSPN control block contains the Local Scan Port Controllers (LSPC) for each Local Scan Port (LSP_0, LSP_1 ... LSP_n). This control block receives input from the 'STA111 instruction register, mode registers, and the TAP controller. Each local port contains all four boundary scan signals needed to interface with the local TAPs plus the optional Test Reset signal (TRST).

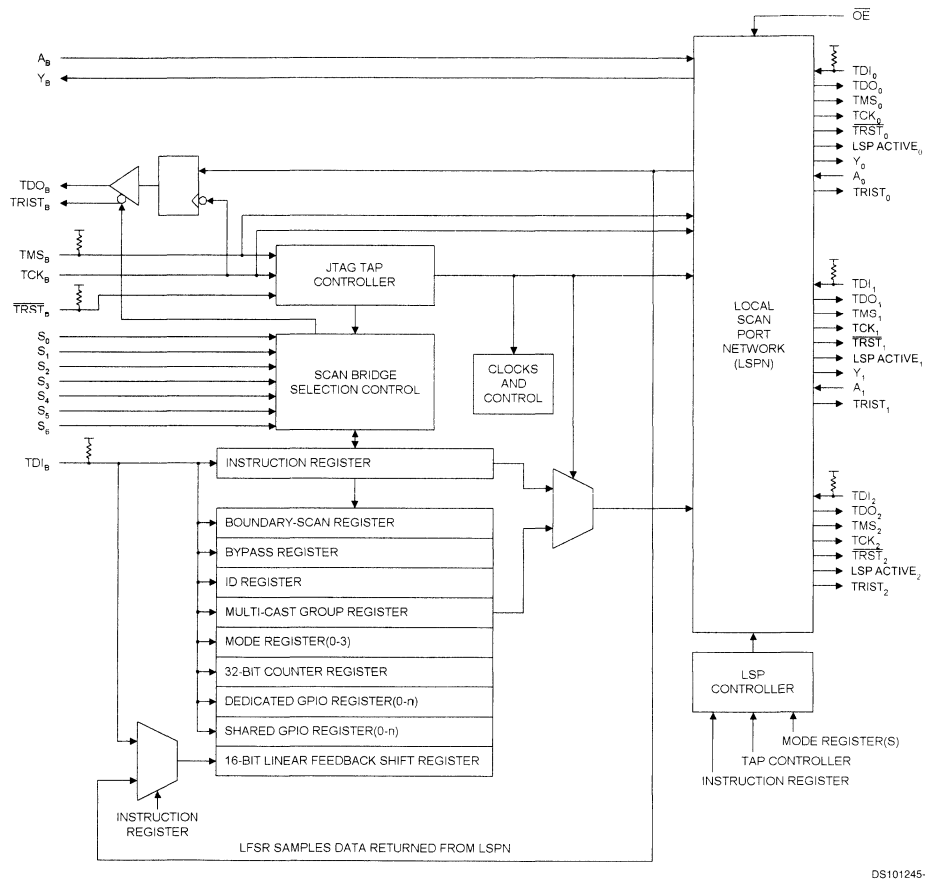


FIGURE 1. SCANSTA111 Block Diagram

Architecture (Continued)

TABLE 2. Pin Descriptions

Pin Name	No. Pins	I/O	Description
VCC	3	N/A	Power
GND	3	N/A	Ground
TMS_B	1	I	BACKPLANE TEST MODE SELECT: Controls sequencing through the TAP Controller of the 'STA111. Also controls sequencing of the TAPs which are on the local scan chains.
TDI_B	1	I	BACKPLANE TEST DATA INPUT: All backplane scan data is supplied to the 'STA111 through this input pin.
TDO_B	1	O	BACKPLANE TEST DATA OUTPUT: This output drives test data from the 'STA111 and the local TAPs, back toward the scan master controller. This output has 24mA of drive current.
TCK_B	1	I	TEST CLOCK INPUT FROM THE BACKPLANE: This is the master clock signal that controls all scan operations of the 'STA111 and of the local scan ports.
$\overline{TRST}_B$	1	I	TEST RESET: An asynchronous reset signal (active low) which initializes the 'STA111 logic.
$TRIST_B$	1	O	BACKPLANE TRI-STATE NOTIFICATION OUTPUT: This signal is high when the backplane scan port is TRI-STATEd. This pin is used for backplane physical layer changes (i.e.; TTL to LVDS). This output has 12mA of drive current.
A_B	1	I	BACKPLANE PASS-THROUGH INPUT: A general purpose input which is driven to the Y_n of a single selected LSP. (Not available when multiple LSPs are selected). This input has an internal pull-up resistor.
Y_B	1	O	BACKPLANE PASS-THROUGH OUTPUT: A general purpose output which is driven from the A_n of a single selected LSP. (Not available when multiple LSPs are selected). This output has 24mA of drive current.
$S_{(0-6)}$	7	I	SLOT IDENTIFICATION: The configuration of these pins is used to identify (assign a unique address to) each 'STA111 on the system backplane (Note 1).
$\overline{OE}$	1	I	OUTPUT ENABLE for the Local Scan Ports, active low. When high, this active-low control signal TRI-STATEs all local scan ports on the 'STA111, to enable an alternate resource to access one or more of the three local scan chains.
$TDO_{(0-2)}$	3	O	TEST DATA OUTPUTS: Individual output for each of the local scan ports (Note 2). These outputs have 24mA of drive current.
$TDI_{(0-2)}$	3	I	TEST DATA INPUTS: Individual scan data input for each of the local scan ports (Note 2).
$TMS_{(0-2)}$	3	O	TEST MODE SELECT OUTPUTS: Individual output for each of the local scan ports. TMS_n does not provide a pull-up resistor (which is assumed to be present on a connected TMS input, per the IEEE 1149.1 requirement) (Note 2). These outputs have 24mA of drive current.
$TCK_{(0-2)}$	3	O	LOCAL TEST CLOCK OUTPUTS: Individual output for each of the local scan ports. These are buffered versions of TCK_B (Note 2). These outputs have 24mA of drive current.
$\overline{TRST}_{(0-2)}$	3	O	LOCAL TEST RESETS: A gated version of $\overline{TRST}_B$ (Note 2). These outputs have 24mA of drive current.
$A_{(0-1)}$	2	I	LOCAL PASS-THROUGH INPUTS: General purpose inputs which can be driven to the backplane pin Y_B. (Only on LSP_0 and LSP_1. Only available when a single LSP is selected) (Note 2). These inputs have an internal pull-up resistor.
$Y_{(0-1)}$	2	O	LOCAL PASS-THROUGH OUTPUT: General purpose outputs which can be driven from the backplane pin A_B. (Only on LSP_0 and LSP_1. Only available when a single LSP is selected) (Note 2). These outputs have 24mA of drive current.
$LSP\_ACTIVE_{(0-2)}$	3	O	LOCAL ANALOG TEST BUS ENABLE: These analog pins serve as enable signals for analog busses supporting the IEEE 1149.4 Mixed-Signal Test Bus standard (Note 2), or for backplane physical layer changes (i.e.; TTL to LVDS). These outputs have 12mA of drive current.
$TRIST_{(0-2)}$	3	O	LOCAL TRI-STATE NOTIFICATION OUTPUTS: This signal is high when the local scan ports are TRI-STATEd (Note 2). These pins are used for backplane physical layer changes (i.e.; TTL to LVDS). These outputs have 12mA of drive current.

Architecture (Continued)

TABLE 2. Pin Descriptions (Continued)

Pin Name	No. Pins	I/O	Description
GPI_n	N/A	I	DEDICATED GENERAL PURPOSE INPUTS: These dedicated inputs (available in HDL) are controlled by registers that can be read or written using the dot1 backplane pins (TDI_B, TDO_B, TMS_B and TCK_B) (Note 3).
GPO_n	N/A	O	DEDICATED GENERAL PURPOSE OUTPUTS: These dedicated outputs (available in HDL) are controlled by registers that can be read or written using the dot1 backplane pins (TDI_B, TDO_B, TMS_B and TCK_B) (Note 3).
$\overline{\text{TEST ENABLE}}$	1	I	TEST ENABLE INPUT: This pin is used for factory test and should be tied to V_{CC} for normal operation.

Note 1: The Silicon device will have seven (7) slot address pins. The HDL version is paramaterized to optionally allow 6, 7 or 8.

Note 2: The Silicon device will have three (3) LSP's. The HDL version is paramaterized to optionally allow up to 8 total LSPs.

Note 3: Up to four (4) GPI/O's per LSP. This feature only available in the HDL version.

Section 10
Interface - Serial Digital

Section 10 Contents

National Semiconductor

Serial Digital Interface (SDI) Introduction

The Serial Digital Interface product family consists of two groups of products optimized for Digital Video and Telecommunications applications. The line driver, receiver/equalizer, and crosspoint switch devices may also be employed in general applications where there exists a need to transfer high-speed serial information great distances.

The **Serial Digital Video (SDV)** products provide line driving, receiving/equalization, retiming/clock-data separation, and switching functions. Also encoding/decoding functions are provided for Society of Motion Picture and Television Engineers (SMPTE) standards 125M Component video and 244M composite video transmission. The devices are most commonly for use in source, routing and destination equipment. Applications include: Video Cameras, Signal Generators, Digital Video Routers and Switchers, Distribution Amplifiers, Video Tape Recorders, Telecines and similar applications.

The **Synchronous Digital Hierarchy (SDH)** products provide line driving, receiving/equalization, retiming/clock-data separation, and switching functions. This family of parts is targeted at Telecommunications applications in SDH/Sonet, ATM equipment, and other high speed serial data transmission applications. These devices may be utilized in ADMs (Add Drop Mux), DCC (Digital Cross Connect) and repeater applications in the digital telecommunication infrastructure.

These products provide Interface Designers with new alternatives for use in "high speed - long distance" data transmission applications.

National Semiconductor

SDI Selection Guide

SDV—Serial Digital Video Products

Part No.	Function	Temperature Range	Data Rate (Mbps)	Jitter (ps)	Page No.
CLC001	3V Driver	−40°C to +85°C	622	25	10-5
CLC006	Driver	−40°C to +85°C	400	25	10-8
CLC007	Driver with Dual Outputs	−40°C to +85°C	400	25	10-9
CLC011B	Decoder	0°C to +70°C	360	50	10-10
CLC014	Equalizer	−40°C to +85°C	650	180	10-14
CLC016	Retimer	0°C to +70°C, −40°C to +85°C	400	130	10-16
CLC018	8x8 Cross Point Switch	−40°C to +85°C	1400	50	10-18
CLC020	Serializer	0°C to +70°C	400	220	10-19
CLC021	Serializer (5V or 3V)	0°C to +70°C	400	220	10-21

SDH—Serial Digital Hierarchy (Telecom)

Part No.	Function	Temperature Range	Data Rate (Mbps)	Jitter (ps)	Page No.
CLC001	3V Driver	−40°C to +85°C	622	25	10-5
CLC005	Driver	−40°C to +85°C	622	25	10-6
CLC012	Equalizer	−40°C to +85°C	622	150	10-12

National Semiconductor

CLC001
Serial Digital Cable Driver with Adjustable Outputs

General Description

The CLC001 is a monolithic, high-speed cable driver designed for use in SMPTE 259M serial digital video and ITU-T G.703 serial digital data transmission applications. The CLC001 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 622 Mbps. Controlled output rise and fall times (400 ps typical) minimize transition-induced jitter. The output voltage swing is adjustable from 800 mV_{p-p} to 1.0 V_{p-p} using an external resistor.

The CLC001's output stage consumes less power than other designs. The differential inputs accept LVDS signal levels, LVPECL levels directly or PECL with attenuation networks.

All these make the CLC001 an excellent general purpose high speed driver for high-speed, long distance data transmission applications.

The CLC001 is powered from a single +3.3V supply and comes in a small 8-pin SOIC package.

Key Specifications

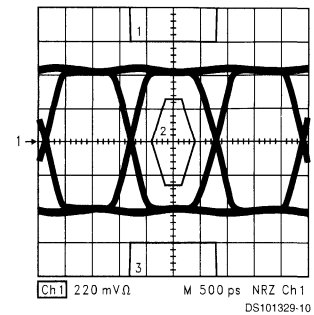
- 400 ps rise and fall times
- Data rates to 622 Mbps
- 100 mV differential input threshold
- Low residual jitter

Features

- Adjustable output amplitude
- Differential input and output
- Accepts LVPECL or LVDS input swings
- Low power dissipation
- Single +3.3V supply

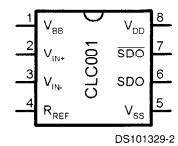
Applications

- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission lines
- Twisted pair driver
- Serial digital video interfaces for the commercial and broadcast industry
- SMPTE, Sonet/SDH, and ATM compatible driver
- Buffer applications



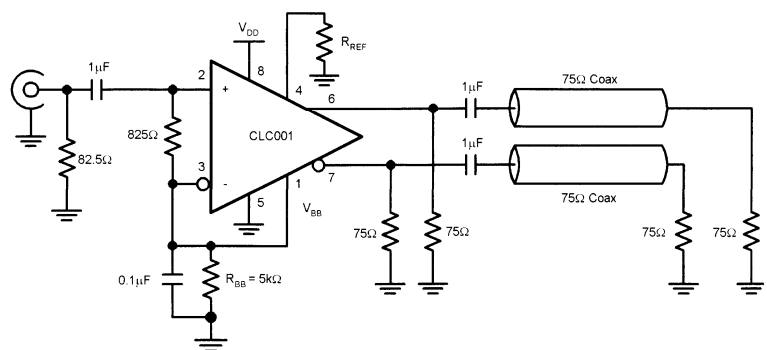
622 Mbps Eye Pattern with STM-4 Signal Mask

Connection Diagram (8-Pin SOIC)



Order Number CLC001AJE
See NS Package Number M08A

Typical Application



National Semiconductor

CLC005
ITU-T G.703 Cable Driver with Adjustable Outputs

General Description

National's Comlinear CLC005 is a monolithic, high-speed cable driver designed for the ITU-T G.703 serial digital data transmission standard. The CLC005 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates from DC to over 622 Mbps. Output signal waveforms produced by the CLC005 comply with G.703 specifications. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 2.0V, set by an accurate, low-drift internal bandgap reference, delivers a 1.0V swing to back-matched and terminated 75Ω cable. Output swing is adjustable from 0.7 V_{p-p} to 2.2 V_{p-p} using external resistors.

The CLC005's class AB output stage consumes less power than other designs, 185 mW with both outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{p-p} to G.703 levels within the specified common-mode limits. All this make the CLC005 an excellent general purpose high speed driver for digital applications.

The CLC005 is powered from a single +5V or −5.2V supply and comes in an 8-pin SOIC package.

Key Specifications

- 650 ps rise and fall times
- Data rates to 622 Mbps
- 200 mV differential input
- Low residual jitter (25 ps_{pp})

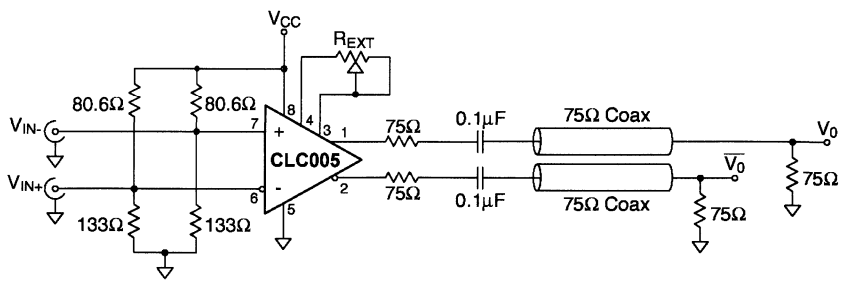
Features

- No external pull-down resistors
- Adjustable output amplitude
- Differential input and output
- Low power dissipation
- Single +5V or −5.2V supply

Applications

- ITU-T G.703, Sonet/SDH, and ATM compatible driver
- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission line
- Twisted pair driver
- Buffer applications

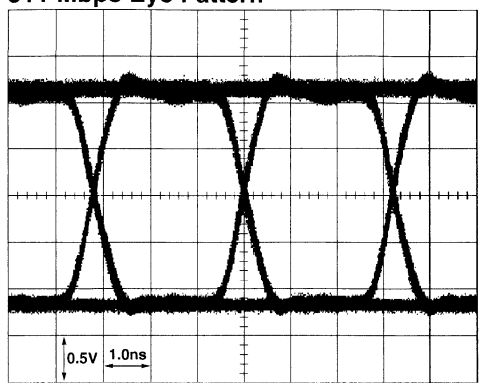
Typical Application



DS100144-2

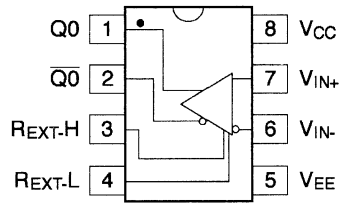
Typical Performance Characteristic

311 Mbps Eye Pattern



DS100144-1

Connection Diagram (8-Pin SOIC)



DS100144-3

Order Number CLC005AJE
See NS Package Number M08A

National Semiconductor

CLC006
Serial Digital Cable Driver with Adjustable Outputs

General Description

National's Comlinear CLC006 is a monolithic, high-speed cable driver designed for the SMPTE 259M serial digital video data transmission standard. The CLC006 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable. Output swing is adjustable from 0.7 V_{p-p} to 2 V_{p-p} using external resistors.

The CLC006's class AB output stage consumes less power than other designs, 185 mW with both outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{p-p} to ECL levels within the specified common-mode limits. All this make the CLC006 an excellent general purpose high speed driver for digital applications.

The CLC006 is powered from a single +5V or −5.2V supply and comes in an 8-pin SOIC package.

Key Specifications

- 650 ps rise and fall times
- Data rates to 400 Mbps
- 200 mV differential input
- Low residual jitter (25 ps_{pp})

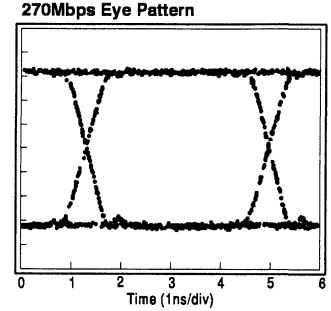
Features

- No external pull-down resistors
- Adjustable output amplitude
- Differential input and output
- Low power dissipation
- Single +5V or −5.2V supply
- Replaces GS9008 in most applications

Applications

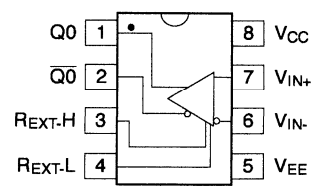
- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission line
- Twisted pair driver
- Serial digital video interfaces for the commercial and broadcast industry
- SMPTE, Sonet/SDH, and ATM compatible driver
- Buffer applications

270Mbps Eye Pattern



DS100084-1

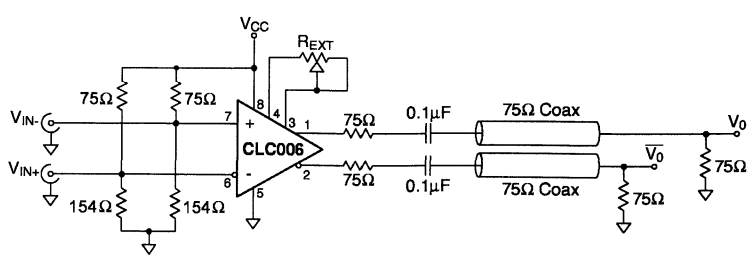
Connection Diagram (8-Pin SOIC)



DS100084-3

Order Number CLC006AJE
See NS Package Number M08A

Typical Application



DS100084-2

National Semiconductor

CLC007
Serial Digital Cable Driver with Dual Complementary Outputs

General Description

National's Comlinear CLC007 is a monolithic, high-speed cable driver designed for the SMPTE 259M serial digital video data transmission standard. The CLC007 drives 75Ω transmission lines (Belden 8281 or equivalent) at data rates up to 400 Mbps. Controlled output rise and fall times (650 ps typical) minimize transition-induced jitter. The output voltage swing, typically 1.65V, set by an accurate, low-drift internal bandgap reference, delivers an 800 mV swing to back-matched and terminated 75Ω cable.

The CLC007's class AB output stage consumes less power than other designs, 195 mW with all outputs terminated, and requires no external bias resistors. The differential inputs accept a wide range of digital signals from 200 mV_{p-p} to ECL levels within the specified common-mode limits. All this make the CLC007 an excellent general purpose high speed driver for digital applications.

The CLC007 is powered from a single +5V or −5.2V supply and comes in an 8-pin SOIC package.

Key Specifications

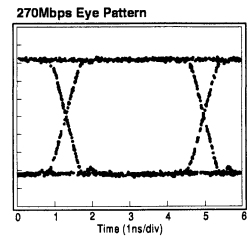
- 650 ps rise and fall times
- Data rates to 400 Mbps
- 2 sets of complimentary outputs
- 200 mV differential input
- Low residual jitter (25 ps_{pp})

Features

- No external pull-down resistors
- Differential input and output
- Low power dissipation
- Single +5V or −5.2V supply
- Replaces GS9007 in most applications

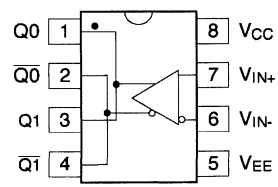
Applications

- Digital routers and distribution amplifiers
- Coaxial cable driver for digital transmission line
- Twisted pair driver
- Digital distribution amplifiers
- SMPTE, Sonet/SDH, and ATM compatible driver
- Buffer applications



DS100085-1

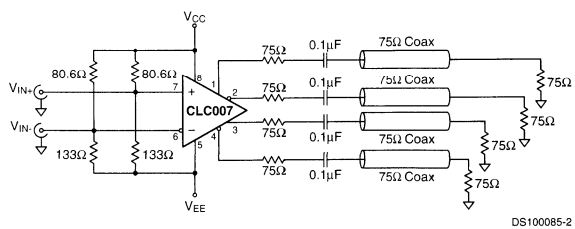
Connection Diagram (8-Pin SOIC)



DS100085-3

Order Number CLC007AJE
See NS Package Number M08A

Typical Application



DS100085-2

National Semiconductor

CLC011
Serial Digital Video Decoder

General Description

National's Comlinear CLC011, Serial Digital Video Decoder, decodes and descrambles SMPTE 259M standard Serial Digital Video datastreams with serial clock into 10-bit parallel words and a corresponding word-rate clock. SMPTE 259M standard parallel data is encoded and scrambled using a 9-bit shift register and is also converted from NRZ to NRZI. The CLC011 restores the original parallel data by reversing the encoding process. The CLC011 also extracts timing information embedded in the SDV data. These reserved code words, known as Timing Reference Signals (TRS), indicate the start and end of each active video line. By decoding the TRS, the CLC011 correctly identifies the word boundaries of the encoded input data. Detection of the TRS reserved codes is indicated by low-true signals at the TRS and End of Active Video (EAV) outputs.

The CLC011's design using current-mode logic (CML) reduces noise injection into the power supply thereby easing board layout and interfacing. The CMOS compatible outputs, which feature controlled rise and fall times, may be set for either 3.3V or 5V swings with the VDP and VCP inputs.

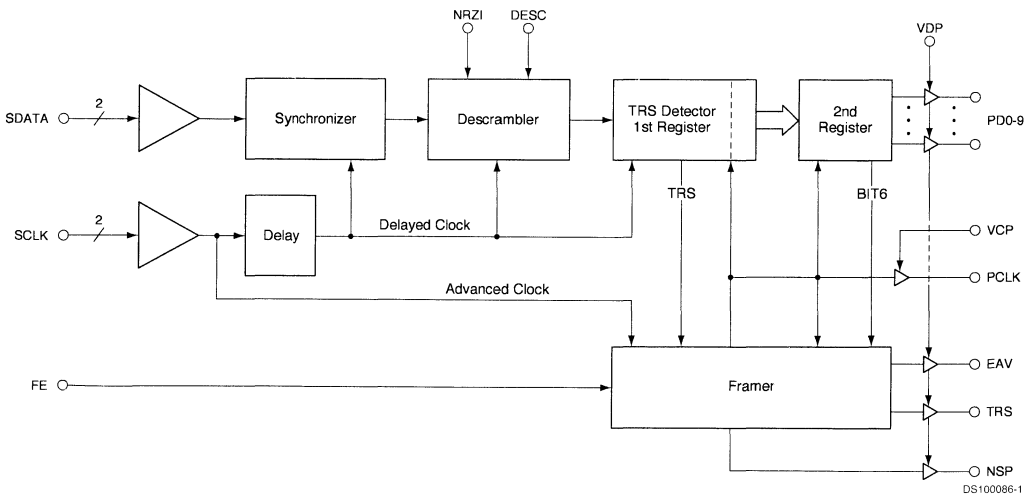
The CLC011 Serial Digital Video Decoder, CLC014 Adaptive Cable Equalizer and the CLC016 Data Retiming PLL combine to provide a complete Serial Digital Video receiver system.

The CLC011 is packaged in a 28-pin PLCC.

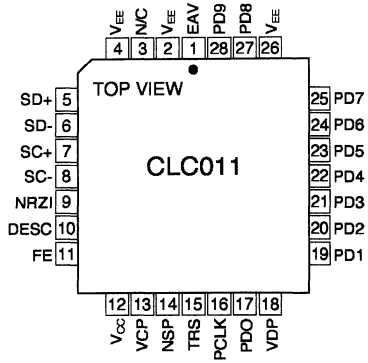
Features

- Data decoding and deserializing
- CLC011B operates to 360Mbps
- Low noise injection to power supplies
- Single +5V or −5.2V supply operation
- Output levels programmable for interface to 5V or 3.3V logic
- Low power
- Low cost

Block Diagram



Connection Diagram



DS100086-2

28-Pin PLCC
Order Number CLC011BCQ
See NS Package Number V28A

Pin Descriptions

Name	Pin No.	Description
EAV	1	End of active video flag. For component video, a logic low is output for one cycle of the parallel clock every time an EAV timing reference is detected. The pulse is aligned with the fourth word of the timing reference (the XYZ word). For composite video, this line is always asserted high.
V_{EE}	2, 4, 26	Negative supply pins.
NC	3	Unused pin.
SDI+, SDI–	5, 6	Differential serial data inputs.
SCI+, SCI–	7, 8	Differential serial clock inputs.
NRZI	9	A logic high at this pin enables NRZI-to-NRZ conversion.
DESC	10	A logic high at this pin enables descrambling.
FE	11	Frame enable. Enables resynchronization of the parallel word at the next TRS.
V_{CC}	12	Positive supply pin.
VCP	13	Parallel clock high level programming pin. The voltage at this supply pin defines the logic high level for the parallel clock output.
NSP	14	New sync position. Indicates that the most recent TRS is in a new position relative to the previous TRS. Remains high until the parallel rate clock is aligned properly with the TRS.
TRS	15	Timing reference flag. A logic low is output for the duration of the TRS.
PCLK	16	Parallel clock output. The rising edge of this clock is located at the center of the parallel data window.
PD0–9	17, 19–25, 27, 28	Parallel data outputs.
VDP	18	Parallel data high level programming pin. The voltage at this supply pin defines the logic high level for the data outputs.

National Semiconductor

CLC012
Adaptive Cable Equalizer for ITU-T G.703 Data Recovery

General Description

National's CLC012 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The CLC012 simplifies the task of high-speed data recovery with a one-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40 dB at 200 MHz. This corresponds to 300 meters of Belden 8281 or 120 meters of Category 5 UTP (unshielded twisted pair).

The CLC012 provides superior jitter performance: $180ps_{pp}$ for 270 Mbps data that has passed through 200 meters of Belden 8281 cable. This exceptional performance provides wide error margin in digital data links. The equalizer operates on a single supply with a power consumption of only 290 mW. The small 14-pin SOIC package allows for high-density placement of components for multi-channel applications such as routers. The equalizer operates over a wide range of data rates from less than 50 Mbps to rates in excess of 650 Mbps.

The equalizer is flexible in allowing either single-ended or differential input drive. Its high common mode rejection provides excellent immunity to interference from noise sources. On-chip quantized feedback eliminates baseline wander.

Additional features include a Loss of Signal output and an output mute pin which, when tied together, mute the output when no signal is present. A buffered eye monitor output is provided, for viewing the equalized signal prior to the comparator. Differential AEC pins allow the user to set the internal adaptive loop time constant with one external capacitor.

Features

- Automatic equalization of coaxial and twisted pair cables
- Loss of Signal detect and output mute
- Output eye monitor
- Single supply operation: +5V or −5.2V
- Single-ended or differential input
- Low cost

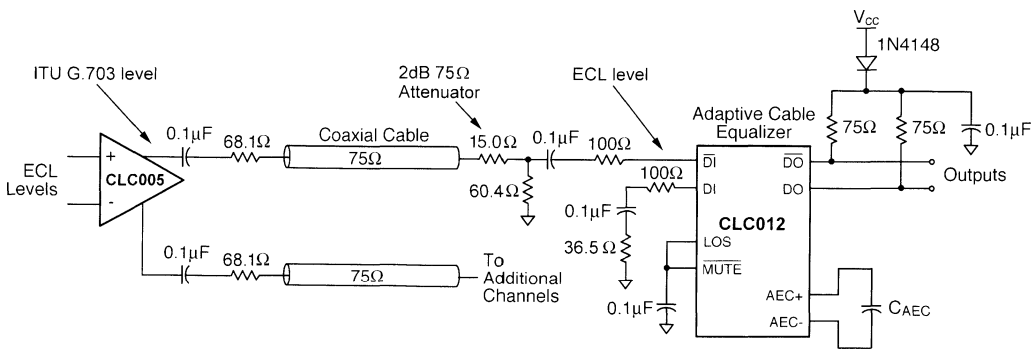
Applications

- ITU-T G.703 serial data recovery
- Serial digital data routing and distribution
- Serial digital data equalization and reception
- Data recovery equalization: ATM, CAD networks, medical, set top terminals, industrial video networks

Key Specifications

- Low jitter: $180ps_{pp}$ @ 270 Mbps through 200 meters of Belden 8281 coaxial cable
- High data rates: < 50 Mbps to > 650 Mbps
- Excellent input return loss: 19 dB @ 270 MHz
- Low supply current: 68 mA
- Equalizes up to 300+ meters of Belden 8281 or 120 meters of Cat 5 UTP cable

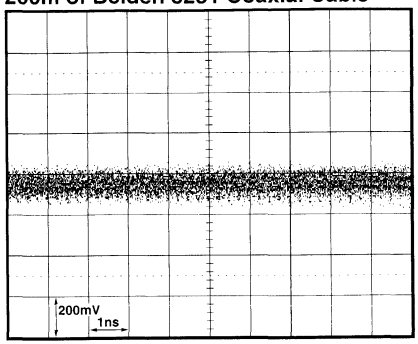
Typical Application



DS100145-4

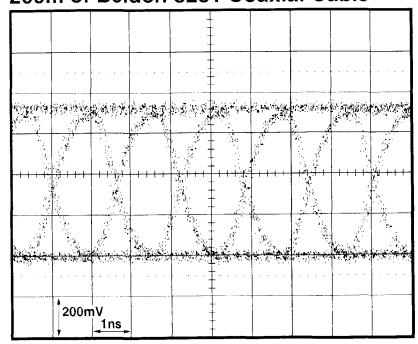
Typical Application (Continued)

Before Equalization: 622Mbps
200m of Belden 8281 Coaxial Cable



DS100145-2

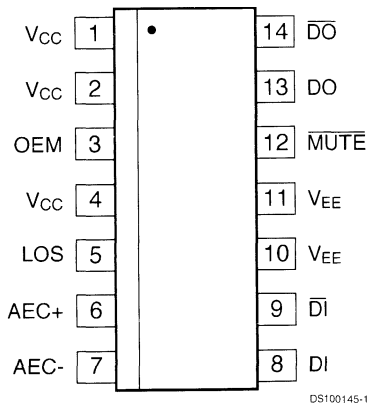
After Equalization: 622Mbps
200m of Belden 8281 Coaxial Cable



DS100145-3

Connection Diagram

Pinout SOIC



DS100145-1

14-Pin SOIC
Order Number CLC012AJE
See NS Package Number M14A

National Semiconductor

CLC014
Adaptive Cable Equalizer for High-Speed Data Recovery

General Description

National's CLC014 adaptive cable equalizer is a low-cost monolithic solution for equalizing data transmitted over cable (or any media with similar dispersive loss characteristics). The CLC014 simplifies the task of high-speed data recovery with a one-chip solution and a minimal number of external components. The equalizer automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40 dB at 200 MHz. This corresponds to 300 meters of Belden 8281 or 120 meters of Category 5 UTP (unshielded twisted pair).

The CLC014 provides superior jitter performance: 180ps$_{pp}$ for 270 Mbps data that has passed through 200 meters of Belden 8281 cable. This exceptional performance provides wide error margin in digital data links. The equalizer operates on a single supply with a power consumption of only 290 mW. The small 14-pin SOIC package allows for high-density placement of components for multi-channel applications such as routers. The equalizer operates over a wide range of data rates from less than 50 Mbps to rates in excess of 650 Mbps.

The equalizer is flexible in allowing either single-ended or differential input drive. Its high common mode rejection provides excellent immunity to interference from noise sources. On-chip quantized feedback eliminates baseline wander.

Additional features include a carrier detect output and an output mute pin which, when tied together, mute the output when no signal is present. A buffered eye monitor output is provided, for viewing the equalized signal prior to the comparator. Differential AEC pins allow the user to set the internal adaptive loop time constant with one external capacitor. Also, the CLC014 is insensitive to the pathological patterns inherent in the video industry standards.

Features

- Automatic equalization of coaxial and twisted pair cables
- Carrier detection and output mute
- Output eye monitor
- Single supply operation: +5V or −5.2V
- Single-ended or differential input
- Low cost

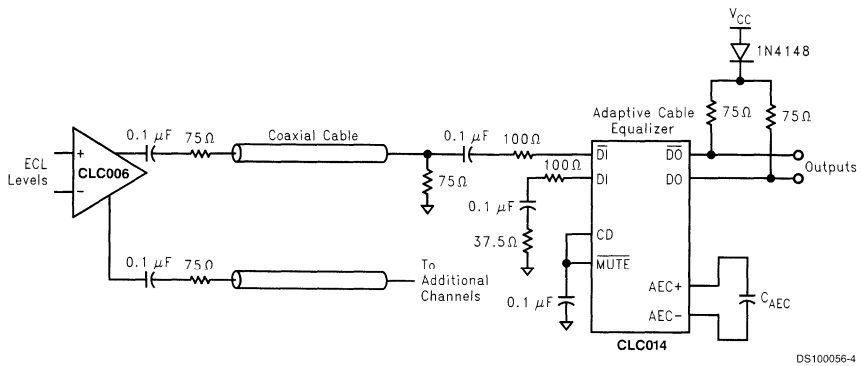
Applications

- SMPTE 259M serial digital interfaces: NTSC/PAL, 4:2:2 component and wide screen; also 540 Mbps (4:4:4:4)
- Serial digital video routing and distribution
- Serial digital data equalization and reception
- Data recovery equalization: ATM, CAD networks, medical, set top terminals, industrial video networks

Key Specifications

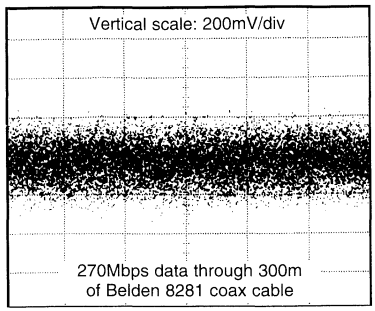
- Low jitter: 180ps$_{pp}$ @ 270 Mbps through 200 meters of Belden 8281 coaxial cable
- High data rates: < 50 Mbps to > 650 Mbps
- Excellent input return loss: 19 dB @ 270 MHz
- Low supply current: 58 mA
- Equalizes up to 300+ meters of Belden 8281 or 120 meters of Cat 5 UTP cable

Typical Application



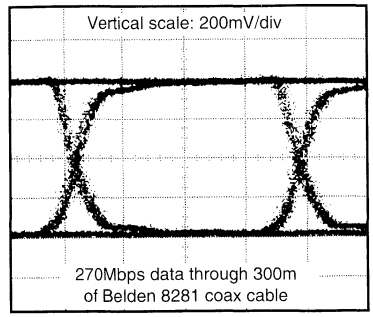
Typical Application (Continued)

Before Equalization



DS100056-2

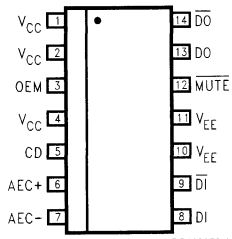
After Equalization



DS100056-3

Connection Diagram

Pinout SOIC



DS100056-1

14-Pin SOIC
Order Number CLC014AJE
See NS Package Number M14A

National Semiconductor

CLC016
Data Retiming PLL with Automatic Rate Selection

General Description

National's Comlinear CLC016 is a low-cost, monolithic, data retiming phase-locked loop (PLL) designed for high-speed serial clock and data recovery. The CLC016 simplifies high-speed data recovery in multi-rate systems by incorporating auto-rate select (ARS) circuitry on chip. This function allows the user to configure the CLC016 to recognize up to four different data rates and automatically adjust to provide accurate, low-jitter clock and data recovery. A single resistor is used to set each data rate anywhere between 40 Mbps and 400 Mbps. No potentiometers, crystals, or other external ICs are required to set the rate.

The CLC016 has output jitter of only 130 ps_{pp} at a 270 Mbps data rate and 0.25% fractional loop bandwidth. Low phase detector output offset and low VCO injection combine to ensure that the CLC016 does not generate bit errors or large phase transients in response to extreme fluctuations in data transition density. The result is improved performance when handling the pathological patterns inherent in the SMPTE 259M video industry standard.

The carrier detect and output mute functions may be used together to automatically latch the outputs when no data is present, preventing random transitions. The external loop filter allows the user to tailor the loop response to the specific application needs. The CLC016 will operate with either +5V or −5.2V power supplies. The serial data inputs and outputs, as well as the recovered clock outputs, allow single- or differential-ECL interfacing. The logic control inputs are TTL-compatible.

Applications

- SMPTE 259M serial digital interfaces: NTSC/PAL, 4:2:2 component, 360 Mbps wide screen
- Serial digital video routing and distribution
- Clock and data recovery for high-speed data transmission
- Re-synchronization of serial data for SONET/SDH, ATM, CAD networks, medical and industrial imaging

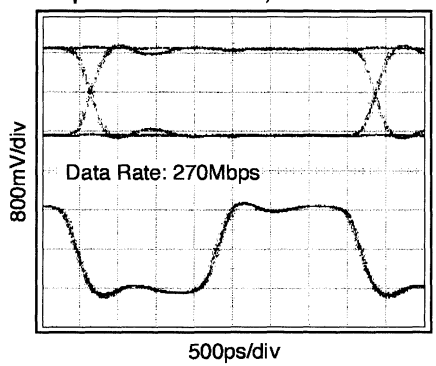
Features

- Retimed data output
- Recovered clock output
- Auto and manual rate select modes
- Four user-configurable data rates
- No potentiometers required
- External loop bandwidth control
- Frequency detector for lock acquisition
- Carrier detect output
- Output MUTE function
- Single supply operation: +5V or −5.2V
- Low cost

Key Specifications

- Low jitter: 130 ps_{pp} @ 270 Mbps, 0.25% fractional loop bandwidth (0.675 MHz)
- High data rates: 40 Mbps – 400 Mbps
- Low supply current: 100 mA, including output biasing
- Flexible fractional loop bandwidth: from 0.05% to 0.5%

Output Data and Clock, Differential



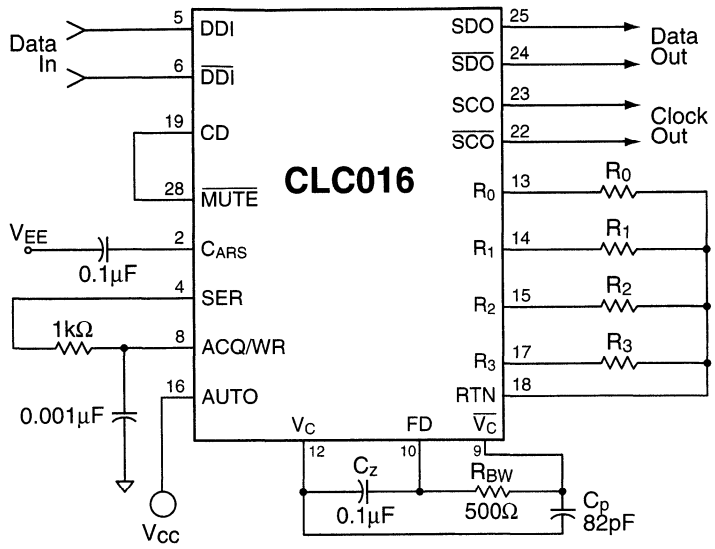
DS100087-1

Ordering Information

Order Number	Temperature	Package
CLC016ACQ	0°C to +70°C	PLCC V28A
CLC016AJQ	−40°C to +85°C	PLCC V28A
CLC016MTC	−40°C to +85°C	TSSOP MTC28

Typical Application

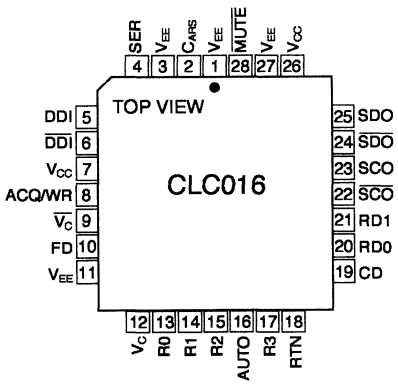
Four-Rate Clock and Data Recovery with Automatic Rate Selection - PLCC Package shown



DS100087-2

Connection Diagrams

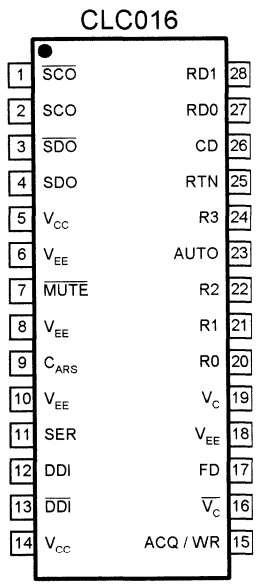
Pinout -Top View



DS100087-3

28-pin PLCC

Pinout -Top View



DS100087-57

28-pin TSSOP

National Semiconductor

CLC018
8 x 8 Digital Crosspoint Switch, 1.485 Gbps

General Description

National's Comlinear CLC018 is a fully differential 8x8 digital crosspoint switch capable of operating at data rates exceeding 1.485 Gbps per channel. Its non-blocking architecture utilizes eight independent 8:1 multiplexers to allow each output to be independently connected to any input and any input to be connected to any or all outputs. Additionally, each output can be individually disabled and set to a high-impedance state. This TRI-STATE feature allows flexible expansion to larger switch array sizes.

Low channel-to-channel crosstalk allows the CLC018 to provide superior all-hostile jitter of 50 ps_{PP}. This excellent signal fidelity along with low power consumption of 850 mW make the CLC018 ideal for digital video switching plus a variety of data communication and telecommunication applications.

The fully differential signal path provides excellent noise immunity, and the I/Os support ECL and PECL logic levels. In addition, the inputs may be driven single-ended or differentially and accept a wide range of common mode levels including the positive supply. Single +5V or −5V supplies or dual +5V supplies are supported. Dual supply mode allows the control signals to be referenced to the positive supply (+5V) while the high-speed I/O remains ECL compatible.

The double row latch architecture utilized in the CLC018 allows switch reprogramming to occur in the background during operation. Activation of the new configuration occurs with a single "configure" pulse. Data integrity and jitter performance on unchanged outputs are maintained during reconfiguration. Two reset modes are provided. Broadcast reset results in all outputs being connected to input port DI0. TRI-STATE Reset results in all outputs being disabled.

The CLC018 is fabricated on a high-performance BiCMOS process and is available in a 64-lead plastic quad flat pack (PQFP).

Features

- Fully differential signal path
- Non-Blocking
- Flexible expansion to larger array sizes with very low power
- Single +5/−5V or dual ±5V operation
- TRI-STATE outputs
- Double row latch architecture
- 64-lead PQFP package

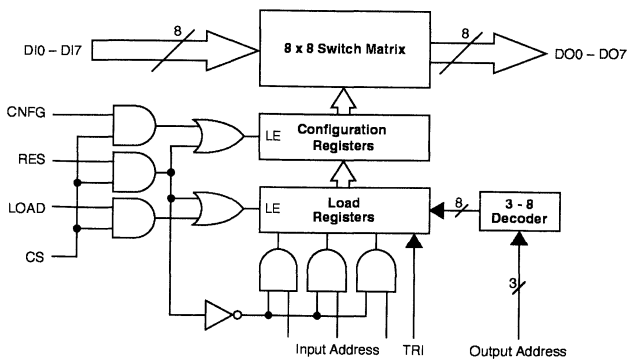
Applications

- Serial digital video routing:
  SMPTE 259M for SD rates
  SMPTE 292M for HD rates
- Telecom/datacom switching
- ATM SONET

Key Specifications

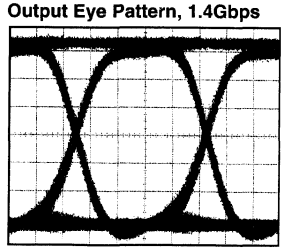
- High speed: >1.485 Gbps
- Low jitter:
  <50 ps_{PP} for rates <500 Mbps
  <100 ps $_{PP}$ for rates <1.485 Gbps
- Low power; 850 mW with all outputs active
- Fast output edge speeds: 250 ps

CLC018 Block Diagram



DS100088-2

Output Eye Pattern, 1.4Gbps



150ps/div

DS100088-1

National Semiconductor

CLC020
SMPTE 259M Digital Video Serializer with Integrated Cable Driver

General Description

The CLC020 SMPTE 259M Digital Video Serializer with Integrated Cable Driver is a monolithic integrated circuit that encodes, serializes and transmits bit-parallel digital data conforming to SMPTE 125M and SMPTE 267M component video and SMPTE 244M composite video standards. The CLC020 can also serialize other 8 or 10-bit parallel data. The CLC020 operates at data rates from below 100 Mbps to over 400 Mbps. The serial data clock frequency is internally generated and requires no external frequency setting components, trimming or filtering*. Functions performed by the CLC020 include: parallel-to-serial data conversion, data encoding using the polynomial (X^9+X^4+1), data format conversion from NRZ to NRZI, parallel data clock frequency multiplication and encoding with the serial data, and coaxial cable driving. Input for sync (TRS) detection disabling and a PLL lock detect output are provided. The CLC020 has an exclusive built-in self-test (BIST) and video test pattern generator (TPG) with 4 component video test patterns, reference black, PLL and EQ pathologicals and modified colour bars, in 4:3 and 16:9 raster and both NTSC and PAL formats*. Separate power pins for the output driver, VCO and the digital logic improve power supply rejection, output jitter and noise performance.

The CLC020 is the ideal complement to the CLC011B SMPTE 259M Serial Digital Video Decoder, CLC014 Active Cable Equalizer, CLC016 Data Retiming PLL (clock-data separator), CLC018 8X8 Digital Crosspoint Switch and CLC006 or CLC007 Cable Drivers, for a complete parallel-serial-parallel, high-speed data processing and transmission system.

The CLC020 is powered from a single 5V supply. Power dissipation is typically 235 mW including two 75Ω back-matched output loads. The device is packaged in a JEDEC 28-lead PLCC.

Features

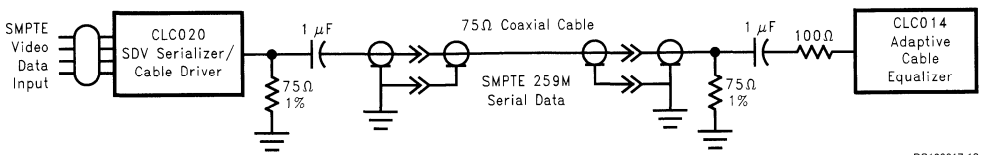
- SMPTE 259M serial digital video standard compliant
- No external serial data rate setting or VCO filtering components required*
- Built-in self-test (BIST) and video test pattern generator (TPG) with 16 internal patterns*
- Supports all NTSC and PAL standard component and composite serial video data rates
- HCMOS/TTL-compatible data and control inputs and outputs
- 75Ω ECL-compatible, differential, serial cable-driver outputs
- Fast VCO lock time: <75 µs
- Single +5V TTL or −5V ECL supply operation
- Low power: 235 mW typical
- 28-lead PLCC package
- Commercial temperature range 0°C to +70°C

Applications

- SMPTE 259M parallel-to-serial digital video interfaces for:
  - — Video cameras
  - — VTRs
  - — Telecines
  - — Video test pattern generators and digital video test equipment
- Non-SMPTE video applications
- Other high data rate parallel/serial video and data systems

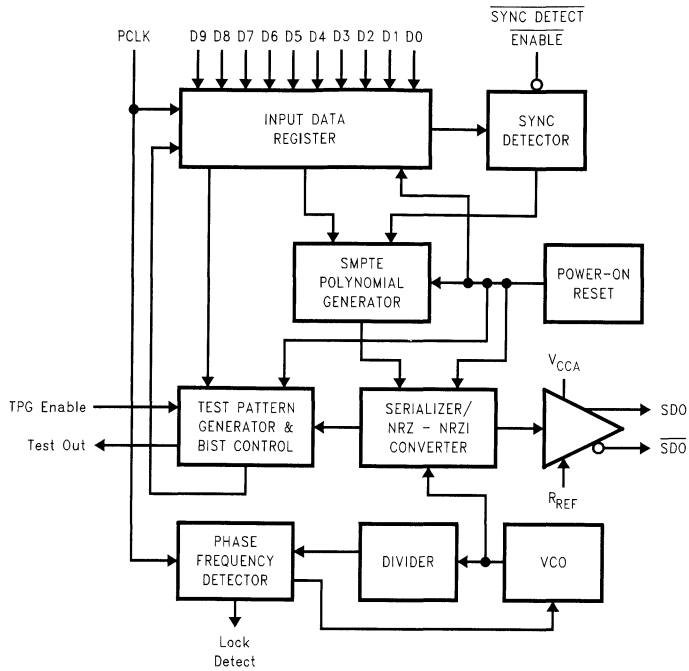
* Patents applications made or pending.

Typical Application



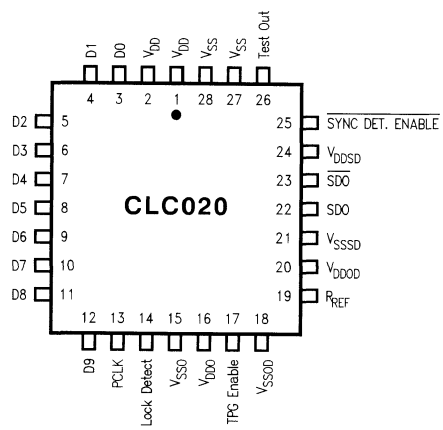
DS100917-12

Block Diagram



DS100917-1

Connection Diagram



DS100917-2

28-Pin PLCC
Order Number CLC020ACQ
See NS Package Number V28A

National Semiconductor

PRELIMINARY

CLC021
SMPTE 259M Digital Video Serializer with EDH Generation and Insertion

General Description

The CLC021 SMPTE 259M Digital Video Serializer with EDH Generation and Insertion is a monolithic integrated circuit that encodes, serializes and transmits bit-parallel digital data conforming to SMPTE 125M and 267M component video and SMPTE 244M composite video standards. The CLC021 can also serialize other 8- or 10-bit parallel data. The CLC021 operates at data rates from below 100 Mbps to over 400 Mbps. The serial data clock frequency is internally generated and requires no external frequency setting, trimming or filtering components*.

Functions performed by the CLC021 include: parallel-to-serial data conversion, ITU-R BT.601-4 input data clipping, data encoding using the SMPTE polynomial (X^9+X^4+1), data format conversion from NRZ to NRZI, parallel data clock frequency multiplication and encoding with the serial data, and differential, serial output data driving. The CLC021 has circuitry for automatic EDH character and flag generation and insertion per SMPTE RP-165. The CLC021 has an exclusive built-in self-test (BIST) and video test pattern generator (TPG) with 16 component video test patterns: reference black, PLL and EQ pathologicals and modified colour bars in 4:3 and 16:9 raster formats for NTSC and PAL formats*.

The CLC021 has inputs for enabling sync detection, non-SMPTE mode operation, enabling the EDH function, NRZ/NRZI mode control and an external reset control. Outputs are provided for H, V and F bits, new TRS sync character position indication, ancilliary data header detection, NTSC/PAL raster indication and PLL lock detect. Separate power pins for the output driver, VCO and the serializer improve power supply rejection, output jitter and noise performance.

The CLC021VGZ-5.0V is powered by a single +5V supply. The CLC021VGZ-3.3V is powered by a single +3.3V supply. Power dissipation is typically 235 mW including two 75Ω back-matched output loads. The device is packaged in a JEDEC metric 44-lead PQFP.

Features

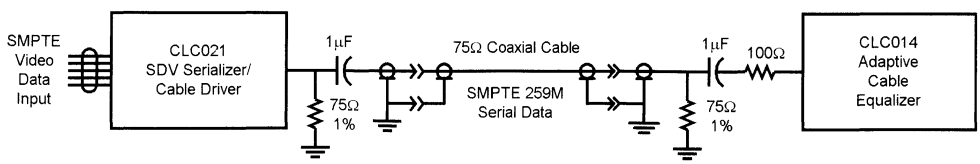
- SMPTE 259M serial digital video standard compliant
- Supports all NTSC and PAL standard component and composite serial video data rates
- No external serial data rate setting or VCO filtering components required*
- Fast VCO lock time: <75 µs at 270 Mbps
- Built-in self-test (BIST) and video test pattern generator (TPG) with 16 internal patterns*
- Automatic EDH character and flag generation and insertion per SMPTE RP 165
- Non-SMPTE mode operation as parallel-to-serial converter
- NRZ-to-NRZI conversion control
- HCMOS/LSTTL-compatible data and control inputs and outputs for CLC021VGZ-5.0, LVCMOS for CLC021VGZ-3.3
- 75Ω ECL-compatible, differential, serial cable-driver outputs
- Single power supply operation: 5V (CLC021VGZ-5.0) or 3.3V (CLC021VGZ-3.3) in TTL or ECL systems
- Low power: typically 235 mW
- JEDEC 44-lead metric PQFP package
- Commercial temperature range 0°C to +70°C

* Patents applications made or pending.

Applications

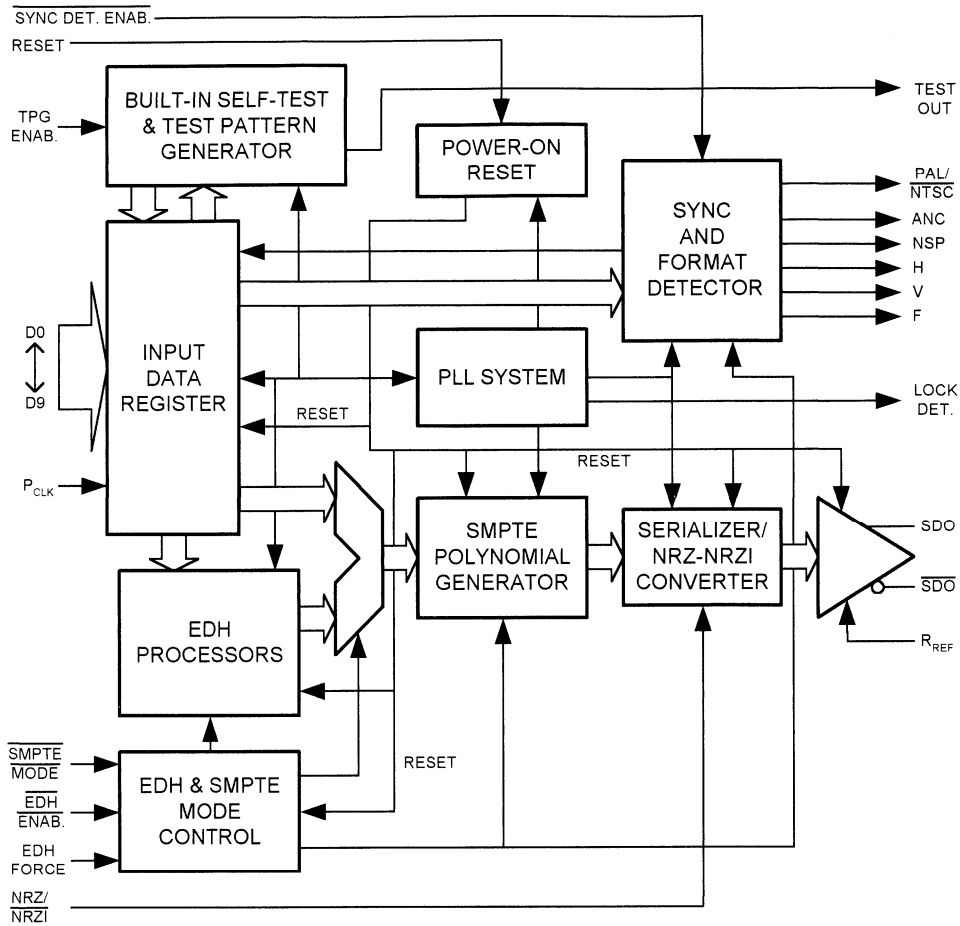
- SMPTE 259M parallel-to-serial digital video interfaces for:
  - — Video cameras
  - — VTRs
  - — Telecines
  - — Video test pattern generators and digital video test equipment
  - — Video signal generators
- Non-SMPTE video applications
- Other high data rate parallel/serial video and data applications

Typical Application



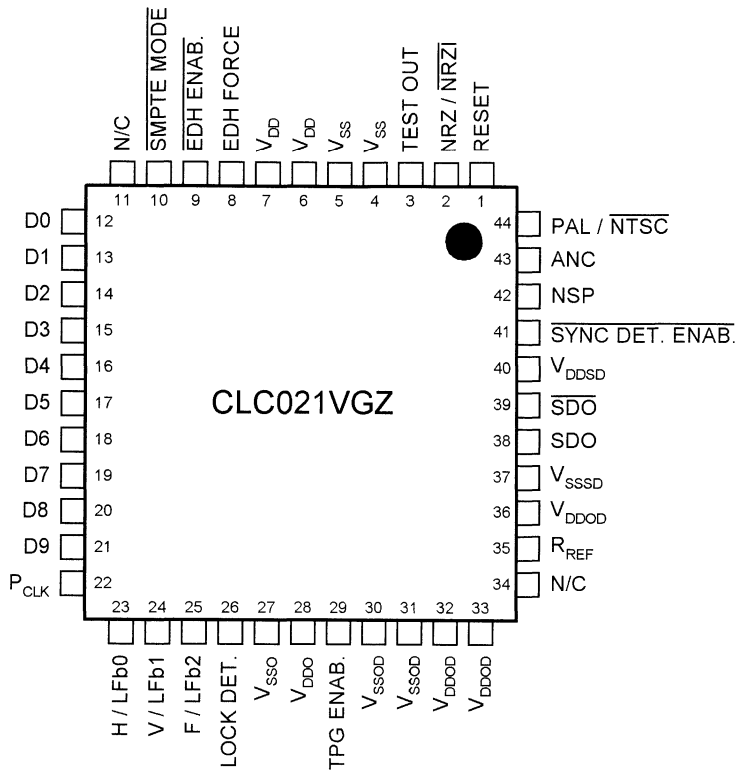
DS101368-12

Block Diagram



DS101368-1

Connection Diagram



DS101368-2

44-Pin Metric PQFP
Order Number CLC021VGZ-5.0 or CLC021VGZ-3.3
See NS Package Number VGZ44A

National Semiconductor

SDI Nomenclature

Note: The SDI (SDV & SDH) family part numbering nomenclature adheres to the following methodology:

PART NUMBER: CLC###ABCCC where:

Example: CLC006AJE

CLC = National's Comlinear Product

= 3 digit unique part number

A = 1 digit denoting differentiation in:

die revision, or

specification revision, or

screening, or

other feature noted in the datasheet.

B = 1 digit denoting operating temperature range:

C = Commercial (0˚C to 70˚C)

J = Industrial (−40˚C to 85˚C)

CCC = 1 to 3 digits denoting package type:

E = SOIC (SOP) Package

Q = PLCC Package

VJQ = PQFP Package

MSA = SSOP Package

Exceptions:

Special Part Number Suffix (ABCCC) of "PCASM" denotes assembled Evaluation PCB

CLC016MTC follows standard National nomenclature - (TSSOP version only)

Section 11
Special Functions

Section 11 Contents

National Semiconductor

CLC532
High Speed 2:1 Analog Multiplexer

General Description

The CLC532 is a high speed 2:1 multiplexer with active input and output stages. The CLC532 innovative design employs a closed loop design which dramatically improves accuracy. This monolithic device is constructed using an advanced high performance bipolar process.

The CLC532 has been specifically designed to provide settling times of 17ns to 0.01%. Fast settling time, coupled with the adjustable bandwidth, and channel-to-channel isolation is better than 80dB @10MHz. Low distortion (–80dBc) makes the CLC532 an ideal choice for infrared and CCD imaging systems and spurious signal levels make the CLC532 a very suitable choice for both I/Q processors and receivers.

The CLC532 is offered in two industrial versions, CLC532AJP\AJE, specified from -40°C to +85°C and packaged in 14-pin plastic DIP14-pin and SOIC packages.

Enhanced Solutions (Military/Aerospace)

SMD Number: 5962-92035

*Space level versions also available.

*For more information, visit http://www.national.com/mil

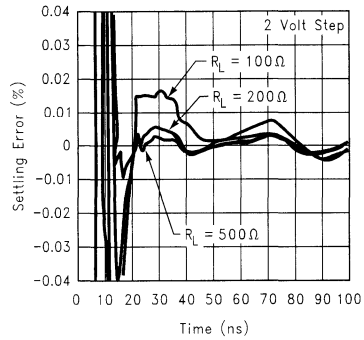
Features

- 17ns 12-bit settling time to .01%
- Low noise – 32μVrms
- High isolation – 80dB @ 10MHz
- Low distortion – 80dBc @ 5MHz
- Adjustable bandwidth–190MHz(max)

Applications

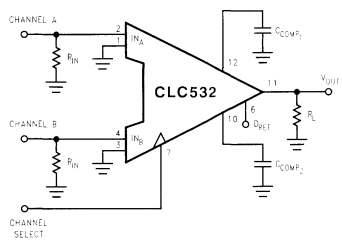
- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

Settling Time vs. R_L



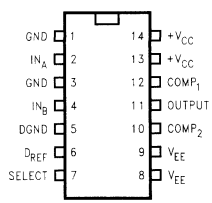
DS012716-24

Typical Application



DS012716-2

Connection Diagram



DS012716-4

Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
14-Pin Plastic DIP	–40°C to +85°C	CLC532AJP	CLC532AJP	N14E
14-Pin Plastic SOIC	–40°C to +85°C	CLC532AJE	CLC532AJE	M14A

National Semiconductor

CLC533
High Speed 4:1 Analog Multiplexer

General Description

The CLC533 is a high speed 4:1 multiplexer employing active input and output stages. The CLC533 innovative closed loop design dramatically improves accuracy over conventional analog multiplexer circuits. This monolithic device is constructed using an advanced high performance bipolar process.

The CLC533 has been specifically designed to provide a 17ns settling time to 0.01%. Fast settling time, coupled with adjustable bandwidth, and channel-to-channel isolation of 80dB @ 10MHz makes the CLC533 an ideal choice for infrared and CCD imaging systems. Low distortion and spurious signal levels (–80dBc) make the CLC533 a very suitable choice for I/Q processors in radar receivers.

The CLC533 is offered in two industrial versions, CLC533AJP\AJE specified from –40°C to +85°C and are packaged in 16-pin plastic DIP and SOIC packages.

Enhanced solutions (Military/Aerospace

SMD Number: 5962-93203

*Space level versions also available.

*For more information, visit http://www.national.com/

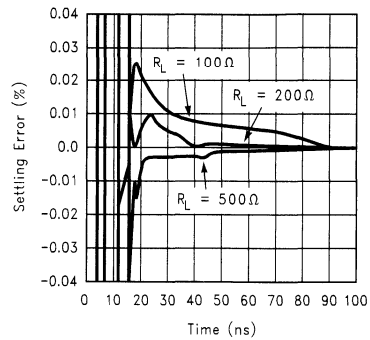
Features

- 17ns 12-bit settling time to .01%
- Low noise – 42μVrms
- High Isolation – 80dBc @ 10MHz
- 110MHz – 3dB bandwidth (A_V = +2)
- Low distortion – 80dBc @ 5MHz
- Adjustable bandwidth –180MHz (max)

Applications

- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

Settling Time vs. Load

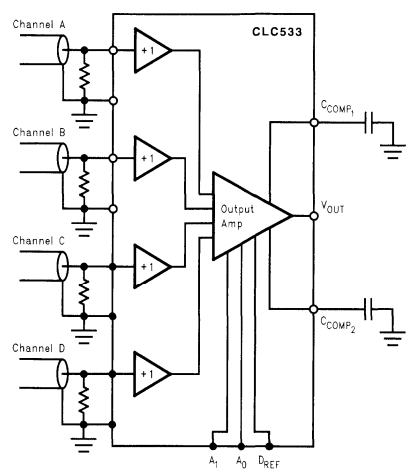


DS012722-1

Functional Diagram

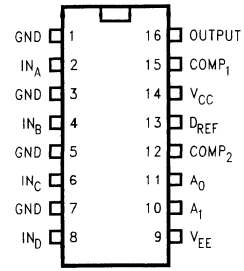
A_1	A_0	OUT
0	0	A
0	1	B
1	0	C
1	D	D

ECL Mode – D_{REF} = open
TTL Mode – D_{REF} = +5V



DS012722-2

Connection Diagram



Pinout
DIP & SOIC

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
16-Pin Plastic DIP	−40˚C to +85˚C	CLC533AJP	CLC533AJP	N16E
16-Pin Plastic SOIC	−40˚C to +85˚C	CLC533AJE	CLC533AJE	M16A

National Semiconductor

LF198/LF298/LF398, LF198A/LF398A Monolithic Sample-and-Hold Circuits

General Description

The LF198/LF298/LF398 are monolithic sample-and-hold circuits which utilize BI-FET technology to obtain ultra-high dc accuracy with fast acquisition of signal and low droop rate. Operating as a unity gain follower, dc gain accuracy is 0.002% typical and acquisition time is as low as 6 µs to 0.01%. A bipolar input stage is used to achieve low offset voltage and wide bandwidth. Input offset adjust is accomplished with a single pin, and does not degrade input offset drift. The wide bandwidth allows the LF198 to be included inside the feedback loop of 1 MHz op amps without having stability problems. Input impedance of $10^{10}\Omega$ allows high source impedances to be used without degrading accuracy.

P-channel junction FET's are combined with bipolar devices in the output amplifier to give droop rates as low as 5 mV/min with a 1 µF hold capacitor. The JFET's have much lower noise than MOS devices used in previous designs and do not exhibit high temperature instabilities. The overall design guarantees no feed-through from input to output in the hold mode, even for input signals equal to the supply voltages.

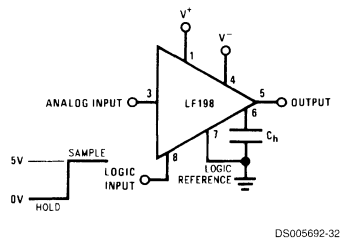
Features

- Operates from ±5V to ±18V supplies
- Less than 10 µs acquisition time
- TTL, PMOS, CMOS compatible logic input
- 0.5 mV typical hold step at C_h = 0.01 µF
- Low input offset
- 0.002% gain accuracy
- Low output noise in hold mode
- Input characteristics do not change during hold mode
- High supply rejection ratio in sample or hold
- Wide bandwidth
- Space qualified, JM38510

Logic inputs on the LF198 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The LF198 will operate from ±5V to ±18V supplies.

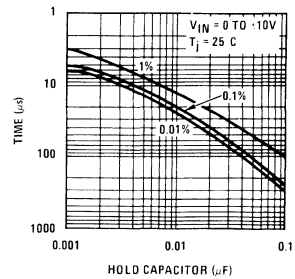
An "A" version is available with tightened electrical specifications.

Typical Connection and Performance Curve



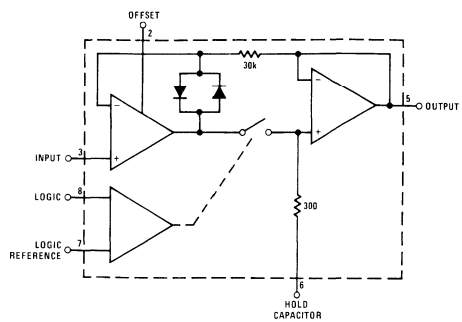
DS005692-32

Acquisition Time



DS005692-16

Functional Diagram



DS005692-1

National Semiconductor

LM231A/LM231/LM331A/LM331
Precision Voltage-to-Frequency Converters

General Description

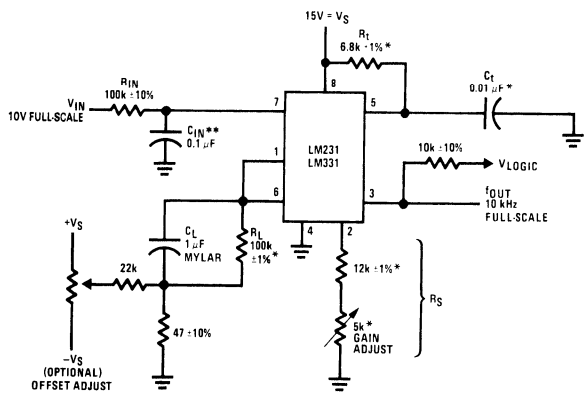
The LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM231A/LM331A attain a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM231/331 are ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM231/LM331 utilize a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output are capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



$$f_{OUT} = \frac{V_{IN}}{2.09\ V} \bullet \frac{R_S}{R_L} \bullet \frac{1}{R_T C_t}$$

*Use stable components with low temperature coefficients. See Typical Applications section.
**0.1µF or 1µF, See "Principles of Operation."

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

National Semiconductor

LM195/LM395
Ultra Reliable Power Transistors

General Description

The LM195/LM395 are fast, monolithic power integrated circuits with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

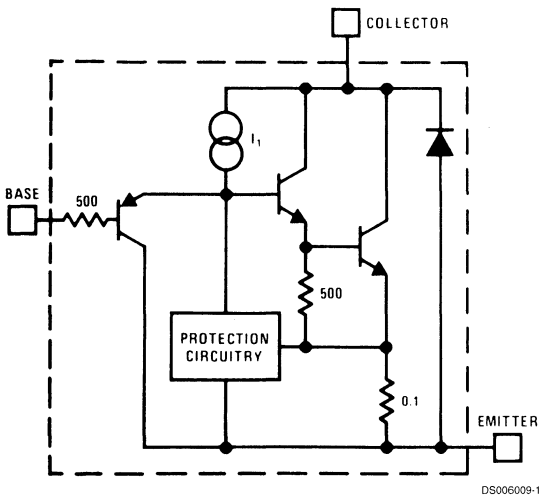
For low-power applications (under 100 mA), refer to the LP395 Ultra Reliable Power Transistor.

The LM195/LM395 are available in the standard TO-3, Kovar TO-5, and TO-220 packages. The LM195 is rated for operation from −55°C to +150°C and the LM395 from 0°C to +125°C.

Features

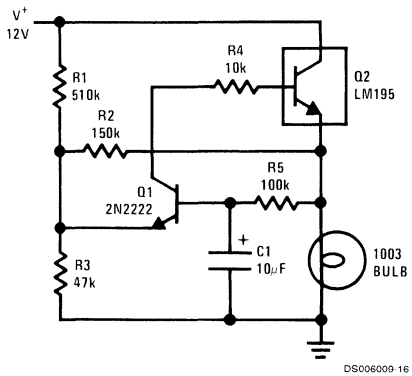
- Internal thermal limiting
- Greater than 1.0A output current
- 3.0 µA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

Simplified Circuit



DS006009-1

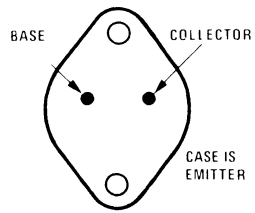
1.0 Amp Lamp Flasher



DS006009-16

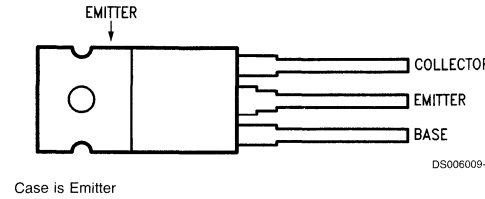
Connection Diagrams

TO-3 Metal Can Package



Bottom View
Order Number LM195K/883
See NS Package Number K02A
(Note 5)

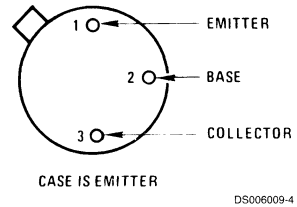
TO-220 Plastic Package



Case is Emitter

Top View
Order Number LM395T
See NS Package Number T03B

TO-5 Metal Can Package



Bottom View
Order Number LM195H/883
See NS Package Number H03B
(Note 5)

National Semiconductor

LM3046
Transistor Array

General Description

The LM3046 consists of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3046 is supplied in a 14-lead molded small outline package.

Features

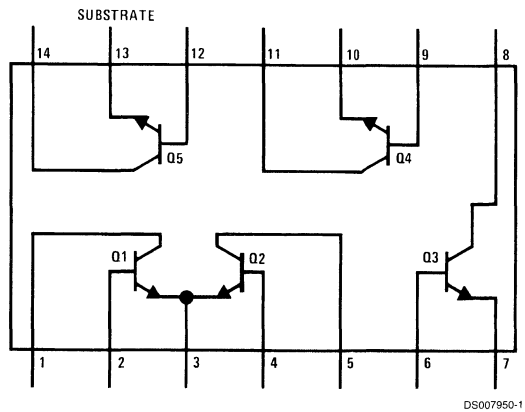
- Two matched pairs of transistors
  V_{BE} matched ±5 mV
  Input offset current 2 μA max at I_C = 1 mA
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure: 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Small Outline Package



Top View
Order Number LM3046M
See NS Package Number M14A

National Semiconductor

LM555
Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200mA or drive TTL circuits.

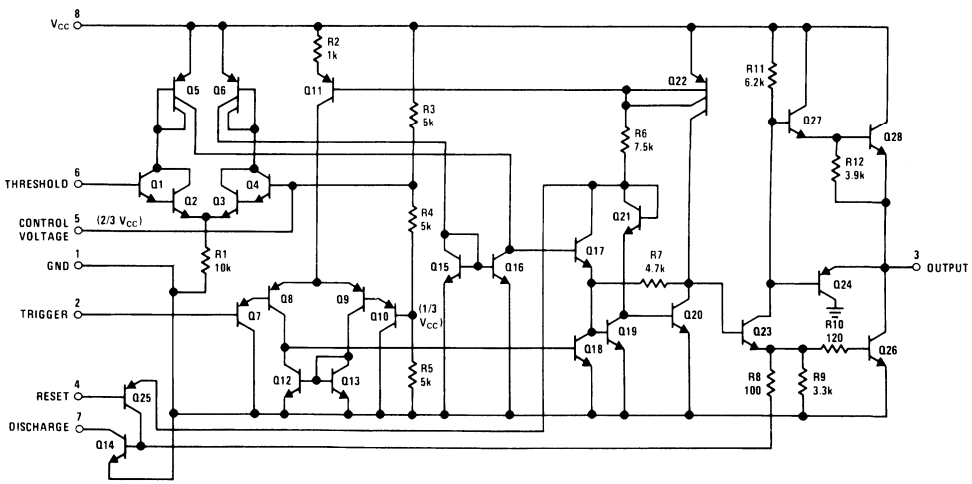
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output
- Available in 8-pin MSOP package

Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

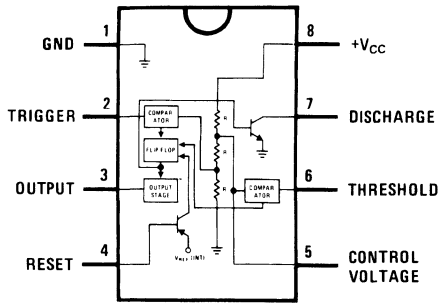
Schematic Diagram



DS007851-1

Connection Diagram

Dual-In-Line, Small Outline and Molded Mini Small Outline Packages



DS007851-3

Top View

Ordering Information

Package	Part Number	Package Marking	Media Transport	NSC Drawing
8-Pin SOIC	LM555CM	LM555CM	Rails	M08A
	LM555CMX	LM555CM	2.5k Units Tape and Reel	
8-Pin MSOP	LM555CMM	Z55	1k Units Tape and Reel	MUA08A
	LM555CMMX	Z55	3.5k Units Tape and Reel	
8-Pin MDIP	LM555CN	LM555CN	Rails	N08E

National Semiconductor

LMC555
CMOS Timer

General Description

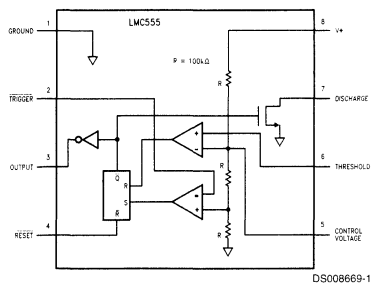
The LMC555 is a CMOS version of the industry standard 555 series general purpose timers. In addition to the standard package (SOIC, MSOP, and MDIP) the LMC555 is also available in a chip sized package (8 Bump micro SMD) using National's micro SMD package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the stable mode the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of National Semiconductor's LMCMOS™ process extends both the frequency range and low supply capability.

Features

- Less than 1 mW typical power dissipation at 5V supply
- 3 MHz astable frequency capability
- 1.5V supply operating voltage guaranteed
- Output fully compatible with TTL and CMOS logic at 5V supply
- Tested to −10 mA, +50 mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers
- Available in 8 pin MSOP Package and 8-Bump micro SMD package

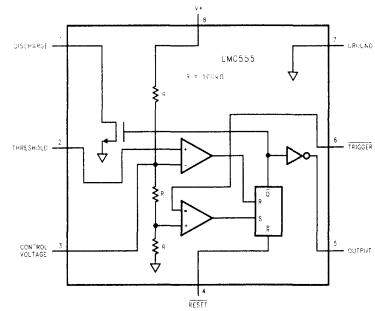
Block and Connection Diagrams

8-Pin SOIC, MSOP, and MDIP Packages



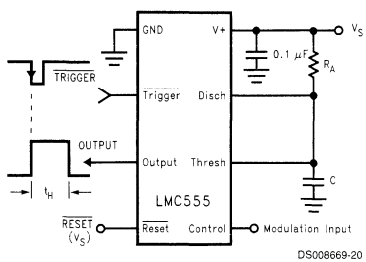
Top View

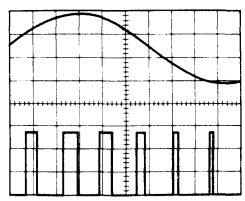
8-Bump micro SMD



Top View
(bump side down)

Pulse Width Modulator





Ordering Information

Package	Temperature Range	Package Marking	Transport Media	NSC Drawing
	Industrial −40°C to +85°C			
8-LeadSmall Outline (SO)	LMC555CM	LMC555CM	Rails	M08A
	LMC555CMX	LMC555CM	2.5k Units Tape and Reel	
8-Lead Mini Small Outline (MSOP)	LMC555CMM	ZC5	1k Units Tape and Reel	MUA08A
	LMC555CMMX	ZC5	3.5k Units Tape and Reel	
8-Lead Molded Dip (MDIP)	LMC555CN	LMC555CN	Rails	N08E
8-Bump micro SMD	LMC555CBP	F1	250 Units Tape and Reel	BPA08EFB
	LMC555CBPX	F1	3k Units Tape and Reel	
Metronome Circuit	LMC555CBPEVAL	N/A	N/A	N/A

National Semiconductor

LM1815
Adaptive Variable Reluctance Sensor Amplifier

General Description

The LM1815 is an adaptive sense amplifier and default gating circuit for motor control applications. The sense amplifier provides a one-shot pulse output whose leading edge coincides with the negative-going zero crossing of a ground referenced input signal such as from a variable reluctance magnetic pick-up coil.

In normal operation, this timing reference signal is processed (delayed) externally and returned to the LM1815. A Logic input is then able to select either the timing reference or the processed signal for transmission to the output driver stage.

The adaptive sense amplifier operates with a positive-going threshold which is derived by peak detecting the incoming signal and dividing this down. Thus the input hysteresis varies with input signal amplitude. This enables the circuit to sense in situations where the high speed noise is greater than the low speed signal amplitude. Minimum input signal is $150mV_{P-P}$.

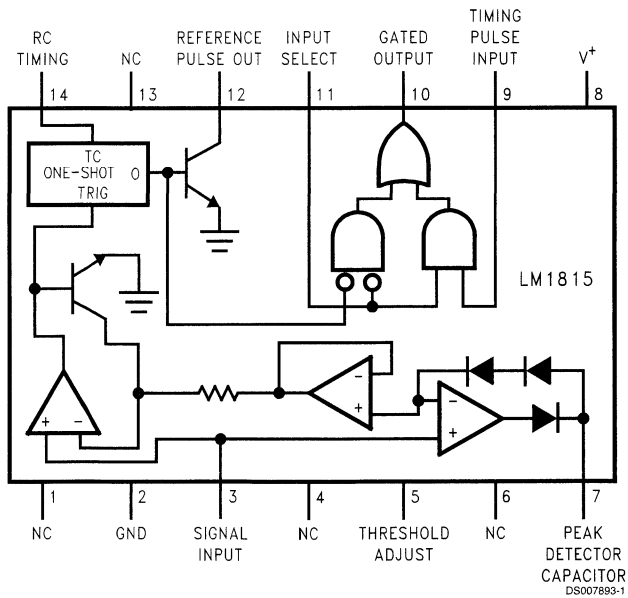
Features

- Adaptive hysteresis
- Single supply operation
- Ground referenced input
- True zero crossing timing reference
- Operates from 2V to 12V supply voltage
- Handles inputs from 100 mV_{P-P} to over $120V_{P-P}$ with external resistor
- CMOS compatible logic

Applications

- Position sensing with notched wheels
- Zero crossing switch
- Motor speed control
- Tachometer
- Engine testing

Connection Diagram



Top View
Order Number LM1815M or LM1815N
See NS Package Number M14A or N14A

National Semiconductor

LM1949
Injector Drive Controller

General Description

The LM1949 linear integrated circuit serves as an excellent control of fuel injector drive circuitry in modern automotive systems. The IC is designed to control an external power NPN Darlington transistor that drives the high current injector solenoid. The current required to open a solenoid is several times greater than the current necessary to merely hold it open; therefore, the LM1949, by directly sensing the actual solenoid current, initially saturates the driver until the "peak" injector current is four times that of the idle or "holding" current (*Figure 3–Figure 7*). This guarantees opening of the injector. The current is then automatically reduced to the sufficient holding level for the duration of the input pulse. In this way, the total power consumed by the system is dramatically reduced. Also, a higher degree of correlation of fuel to the input voltage pulse (or duty cycle) is achieved, since opening and closing delays of the solenoid will be reduced.

Normally powered from a 5V ± 10% supply, the IC is typically operable over the entire temperature range (−55°C to +125°C ambient) with supplies as low as 3 volts. This is particularly useful under "cold crank" conditions when the battery voltage may drop low enough to deregulate the 5-volt power supply.

The LM1949 is available in the plastic miniDIP, (contact factory for other package options).

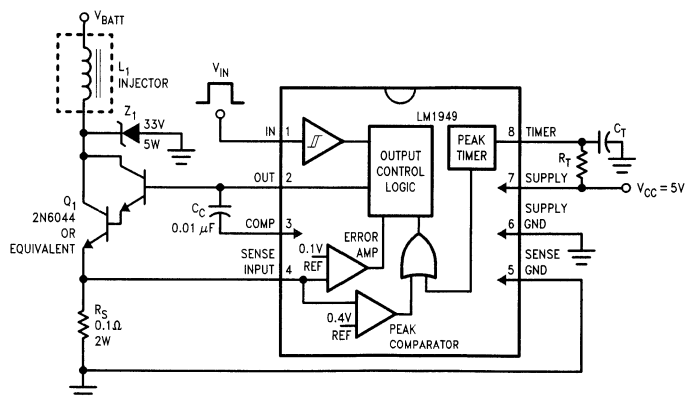
Features

- Low voltage supply (3V–5.5V)
- 22 mA output drive current
- No RFI radiation
- Adaptable to all injector current levels
- Highly accurate operation
- TTL/CMOS compatible input logic levels
- Short circuit protection
- High impedance input
- Externally set holding current, I_H
- Internally set peak current (4 x I_H)
- Externally set time-out
- Can be modified for full switching operation
- Available in plastic 8-pin minDIP

Applications

- Fuel injection
- Throttle body injection
- Solenoid controls
- Air and fluid valves
- DC motor drives

Typical Application Circuit



Order Number LM1949M or LM1949N
See NS Package Number M08A or N08E

FIGURE 1. Typical Application and Test Circuit

National Semiconductor

LM2907/LM2917
Frequency to Voltage Converter

General Description

The LM2907, LM2917 series are monolithic frequency to voltage converters with a high gain op amp/comparator designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low ripple, full input protection in two versions (LM2907-8, LM2917-8) and its output swings to ground for a zero frequency input.

The op amp/comparator is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28V.

The two basic configurations offered include an 8-pin device with a *ground referenced tachometer* input and an internal connection between the tachometer output and the op amp non-inverting input. This version is well suited for single speed or frequency switching or fully buffered frequency to voltage conversion applications.

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency to voltage and frequency to current operations are possible with any supply voltage and a suitable resistor.

Advantages

- Output swings to ground for zero frequency input
- Easy to use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Only one RC network provides frequency doubling
- Zener regulator on chip allows accurate and stable frequency to voltage or current conversion (LM2917)

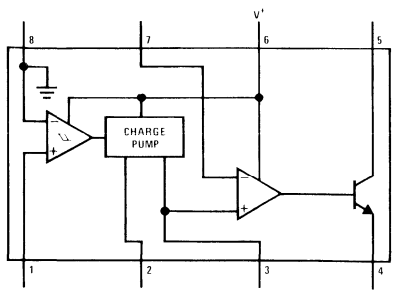
Features

- Ground referenced tachometer input interfaces directly with variable reluctance magnetic pickups
- Op amp/comparator has floating transistor output
- 50 mA sink or source to operate relays, solenoids, meters, or LEDs
- Frequency doubling for low ripple
- Tachometer has built-in hysteresis with either differential input or ground referenced input
- Built-in zener on LM2917
- ±0.3% linearity typical
- Ground referenced tachometer is fully protected from damage due to swings above V_{CC} and below ground

Applications

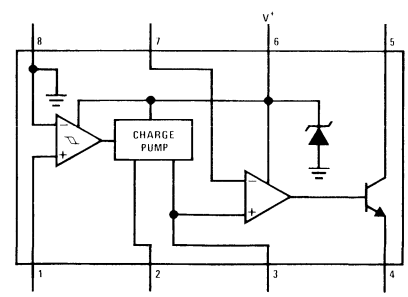
- Over/under speed sensing
- Frequency to voltage conversion (tachometer)
- Speedometers
- Breaker point dwell meters
- Hand-held tachometer
- Speed governors
- Cruise control
- Automotive door lock control
- Clutch control
- Horn control
- Touch or sound switches

Block and Connection Diagrams Dual-In-Line and Small Outline Packages, Top Views



DS007942-1

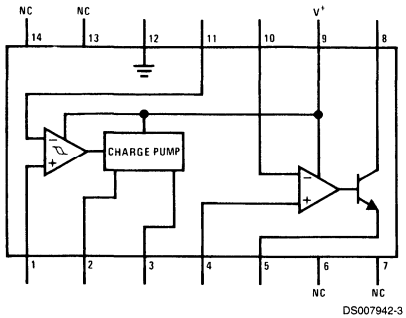
Order Number LM2907M-8 or LM2907N-8
See NS Package Number M08A or N08E



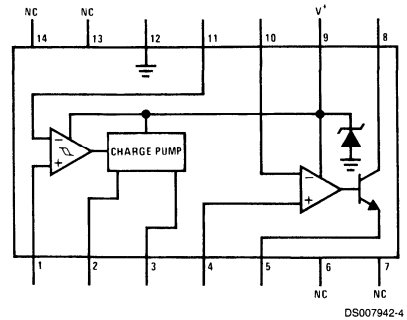
DS007942-2

Order Number LM2917M-8 or LM2917N-8
See NS Package Number M08A or N08E

Block and Connection Diagrams Dual-In-Line and Small Outline Packages, Top Views (Continued)



Order Number LM2907M or LM2907N
See NS Package Number M14A or N14A



Order Number LM2917M or LM2917N
See NS Package Number M14A or N14A

National Semiconductor

LM9011
Electronic Ignition Interface

General Description

The LM9011 is an interface circuit which integrates the timing detection and logic control functions required for an automotive electronic ignition system into one device.

A VRS interface is provided for crankshaft position information via a toothed-wheel.

Four voltage comparators are provided for hardware diagnostics.

An electronic timing interface with output fault diagnostics is provided to enable a micro-processor to drive an external four channel ignition spark circuit.

The LM9011 is fully specified over the automotive temperature range of -40˚C to +125˚C, and is available in a 28 pin Small Outline surface mount package.

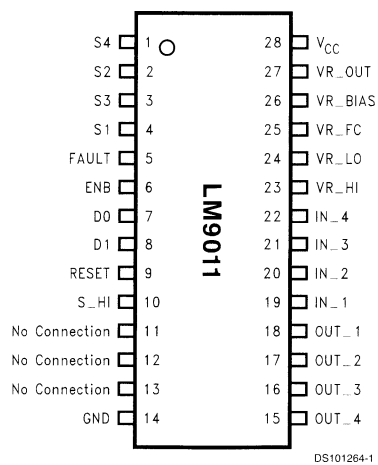
Key Specifications

Features

- Single 5V supply operation
- VR Sensor Interface with dynamic hysteresis
- Four Channel Electronic Timing spark driver with output diagnostics
- Electronic Timing Interface spark driver output voltage from 5V to 16V
- One Non-Inverting voltage comparator with hysteresis
- Three Inverting voltage comparators with hysteresis

Connection Diagram

Top View



DS101264-1

Ordering Information LM9011M
See NS Package M28B

National Semiconductor

LM9022
Vacuum Fluorescent Display Filament Driver

General Description

The LM9022 is a bridged power amplifier capable of delivering typically 2W of continuous average power into a 10Ω filament load when powered by a 5V power supply.

To conserve power in portable applications, the LM9022's micropower shutdown mode (I_Q = 0.6µA, typ) is activated when V_{DD} is applied to the SHUTDOWN pin.

Additional LM9022 features include thermal shutdown protection, unity-gain stability, and external gain set.

Key Specifications

- I_{DD} during shutdown 0.6µA (typ)
- Thermal Shutdown Protection

Features

- No transformers required
- SO or DIP packaging

Applications

- VCR/DVD Displays
- RADIO/TUNER Displays

Typical Application

T_A = 25˚C, V_{DD} = 5V, unless otherwise specified.

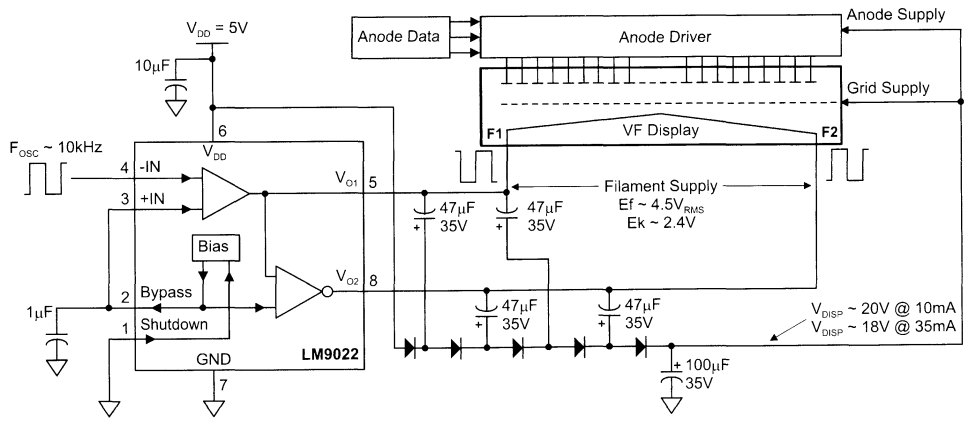
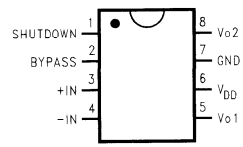


FIGURE 1. Typical Application Circuit

Connection Diagram

MSOP, Small Outline, and DIP Package



Top View
Order Number LM9022M or LM9022N
See NS Package Number M08A or N08E

National Semiconductor

LM9040
Dual Lambda Sensor Interface Amplifier

General Description

The LM9040 is a dual sensor interface circuit consisting of two independent sampled input differential amplifiers designed for use with conventional Lambda Oxygen Sensors. The Lambda Sensor is used for monitoring the oxygen concentration in the exhaust of gasoline engines using catalytic after treatment and will deliver a voltage signal which is dependent on the air-fuel mixture. The gain of the amplifiers are internally set and can directly convert the Lambda sensor output voltage to a level suitable for A/D conversion in a system using a 5V reference.

The input common mode voltage range of each amplifier is ±2V with respect to the IC ground pin. This will allow the IC to connect to sensors which are remotely grounded at the engine exhaust manifold or exhaust pipe.

Each amplifier is capable of independent default operation should either, or both, of the leads to a sensor become open circuited.

Noise filtering is provided by an internal switched capacitor low pass filter as part of each amplifier, and by external components.

The LM9040 is fully specified over the automotive temperature range of −40°C to +125°C and is provided in a 14-pin Small Outline surface mount package.

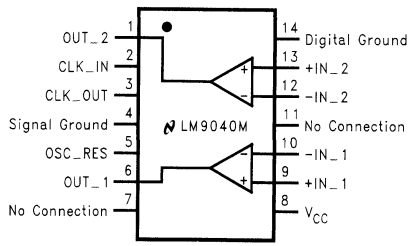
Features

- Single 5V supply operation
- Common mode input voltage range of ±2V
- Differential input voltage range of 50 mV to 950 mV
- Sampled differential input
- Switched capacitor low pass filter
- Internal oscillator and V_{BB} generator
- Open input default operation
- Cold sensor default operation
- Low power consumption (42 mW max)
- Gain set by design and guaranteed over the operating temperature range

Applications

- Closed loop emissions control
- Catalytic converter monitoring

Connection Diagram



01237201

Top View
Ordering Information
LM9040M
See NS Package Number M14B

National Semiconductor

LM9044
Lambda Sensor Interface Amplifier

General Description

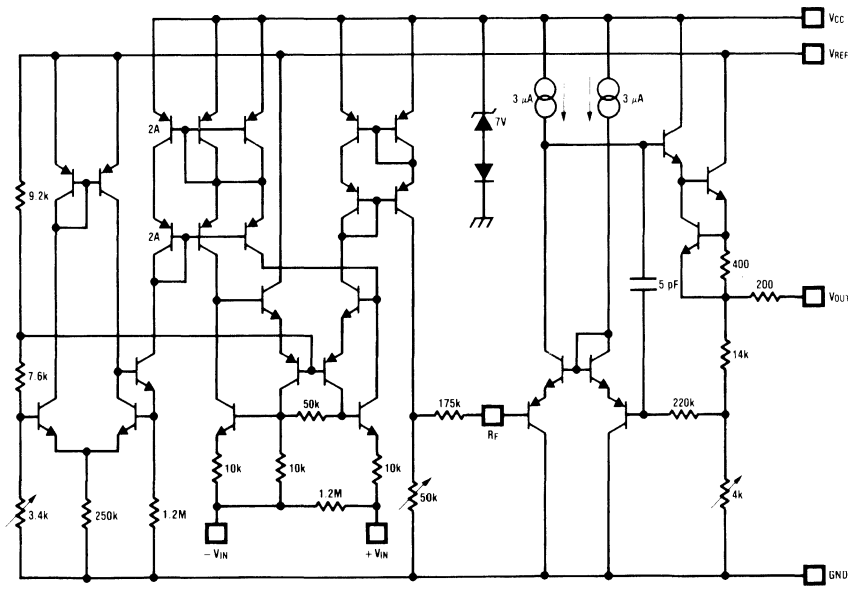
The LM9044 is a precision differential amplifier specifically designed for operation in the automotive environment. Gain accuracy is guaranteed over the entire automotive temperature range (−40˚C to +125˚C) and is factory trimmed after package assembly. The input circuitry has been specifically designed to reject common-mode signals as much as 3V below ground on a single positive power supply. This facilitates the use of sensors which are grounded at the engine block while the LM9044 itself is grounded at chassis potential. An external capacitor sets the maximum operating frequency of the amplifier, thereby filtering high frequency transients. Both inputs are protected against accidental shorting to the battery and against load dump transients. The input impedance is typically 1 MΩ.

The output op amp is capable of driving capacitive loads and is fully protected. Also, internal circuitry has been provided to detect open circuit conditions on either or both inputs and force the output to a "home" position (a ratio of the external reference voltage).

Features

- Normal circuit operation guaranteed with inputs up to 3V below ground on a single supply.
- Gain factory trimmed and guaranteed over temperature (±3% of full-scale from −40˚C to +125˚C)
- Low power consumption (typically 1 mA)
- Fully protected inputs
- Input open circuit detection
- Operation guaranteed over the entire automotive temperature range (−40˚C to +125˚C)
- Single supply operation

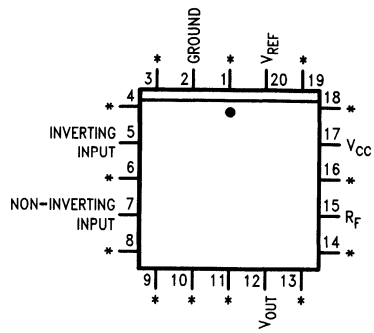
Schematic and Connection Diagrams



00674401

Schematic and Connection Diagrams (Continued)

Plastic Chip Carrier Package



00674406

Top View
Order Number LM9044V
See NS Package Number V20A

*Pins 1, 3, 4, 6, 8, 9, 10, 11, 13, 14, 16, 18, 19 are trim pins and should be left floating.

National Semiconductor

LM9061
Power MOSFET Driver with Lossless Protection

General Description

The LM9061 is a charge-pump device which provides the gate drive to any size external power MOSFET configured as a high side driver or switch. A CMOS logic compatible ON/OFF input controls the output gate drive voltage. In the ON state, the charge pump voltage, which is well above the available V_{CC} supply, is directly applied to the gate of the MOSFET. A built-in 15V zener clamps the maximum gate to source voltage of the MOSFET. When commanded OFF a 110 µA current sink discharges the gate capacitances of the MOSFET for a gradual turn-OFF characteristic to minimize the duration of inductive load transient voltages and further protect the power MOSFET.

Lossless protection of the power MOSFET is a key feature of the LM9061. The voltage drop (V_{DS}) across the power device is continually monitored and compared against an externally programmable threshold voltage. A small current sensing resistor in series with the load, which causes a loss of available energy, is not required for the protection circuitry. Should the V_{DS} voltage, due to excessive load current, exceed the threshold voltage, the output is latched OFF in a more gradual fashion (through a 10 µA output current sink) after programmable delay time interval.

Designed for the automotive application environment the LM9061 has a wide operating temperature range of −40°C to +125°C, remains operational with V_{CC} up to 26V, and can withstand 60V power supply transients. The LM9061 is available in an 8-pin small outline package, and an 8-pin dual in-line package.

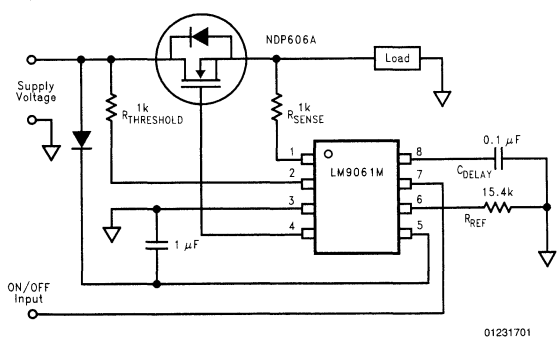
Features

- Built-in charge pump for gate overdrive of high side drive applications
- Lossless protection of the power MOSFET
- Programmable MOSFET protection voltage
- Programmable delay of protection latch-OFF
- Fast turn-ON (1.5 ms max with gate capacitance of 25000 pF)
- Undervoltage shut OFF with V_{CC} < 7V
- Overvoltage shut OFF with V_{CC} > 26V
- Withstands 60V supply transients
- CMOS logic compatible ON/OFF control input
- Surface mount and dual-in-line packages available

Applications

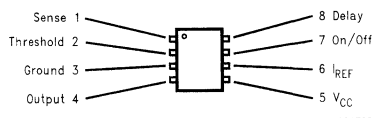
- Valve, relay and solenoid drivers
- Lamp drivers
- DC motor PWM drivers
- Logic controlled power supply distribution switch
- Electronic circuit breaker

Typical Application



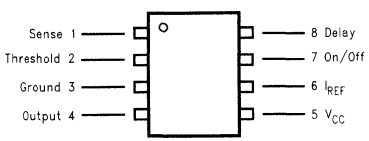
01231701

Connection Diagrams



01231703

Top View
Order Number LM9061M
See NS Package Number M08A



01231702

Top View
Order Number LM9061N
See NS Package Number N08E

National Semiconductor

LMF100
High Performance Dual Switched Capacitor Filter

General Description

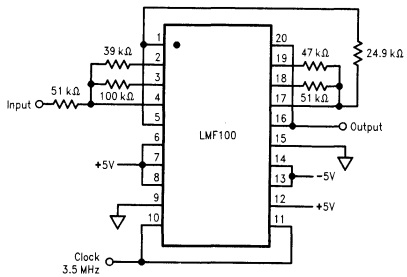
The LMF100 consists of two independent general purpose high performance switched capacitor filters. With an external clock and 2 to 4 resistors, various second-order and first-order filtering functions can be realized by each filter block. Each block has 3 outputs. One output can be configured to perform either an allpass, highpass, or notch function. The other two outputs perform bandpass and lowpass functions. The center frequency of each filter stage is tuned by using an external clock or a combination of a clock and resistor ratio. Up to a 4th-order biquadratic function can be realized with a single LMF100. Higher order filters are implemented by simply cascading additional packages, and all the classical filters (such as Butterworth, Bessel, Elliptic, and Chebyshev) can be realized.

The LMF100 is fabricated on National Semiconductor's high performance analog silicon gate CMOS process, LMCMOS™. This allows for the production of a very low offset, high frequency filter building block. The LMF100 is pin-compatible with the industry standard MF10, but provides greatly improved performance.

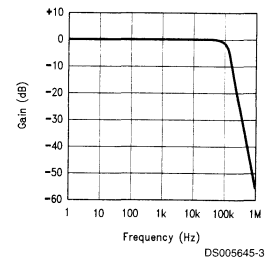
Features

- Wide 4V to 15V power supply range
- Operation up to 100 kHz
- Low offset voltage: typically
  (50:1 or 100:1 mode): Vos1 = ±5 mV
  Vos2 = ±15 mV
  Vos3 = ±15 mV
- Low crosstalk –60 dB
- Clock to center frequency ratio accuracy ±0.2% typical
- f_0 x Q range up to 1.8 MHz
- Pin-compatible with MF10

4th Order 100 kHz Butterworth Lowpass Filter



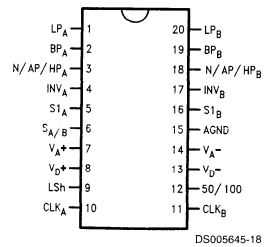
DS005645-2



DS005645-3

Connection Diagram

Surface Mount and Dual-In-Line Package



DS005645-18

Top View
Order Number
LMF100CCN or LMF100CIWM
See NS Package Number N20A or M20B

National Semiconductor

LP395
Ultra Reliable Power Transistor

General Description

The LP395 is a fast monolithic transistor with complete overload protection. This very high gain transistor has included on the chip, current limiting, power limiting, and thermal overload protection, making it difficult to destroy from almost any type of overload. Available in an epoxy TO-92 transistor package this device is guaranteed to deliver 100 mA.

Thermal limiting at the chip level, a feature not available in discrete designs, provides comprehensive protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive die temperature.

The LP395 offers a significant increase in reliability while simplifying protection circuitry. It is especially attractive as a small incandescent lamp or solenoid driver because of its low drive requirements and blowout-proof design.

The LP395 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LP395 as with any transistor. When the device is used as an emitter follower with a low source impedance, it is necessary to insert a 4.7 kΩ resistor in series with the base lead to prevent possible emitter follower oscillations. Also since it has good high frequency response, supply by-passing is recommended.

Areas where the LP395 differs from a standard NPN transistor are in saturation voltage, leakage (quiescent) current and in base current. Since the internal protection circuitry requires voltage and current to function, the minimum voltage across the device in the on condition (saturated) is typically 1.6 Volts, while in the off condition the quiescent (leakage) current is typically 200 µA. Base current in this device flows out of the base lead, rather than into the base as is the case with conventional NPN transistors. Also the base can be driven positive up to 36 Volts without damage, but will draw current if driven negative more than 0.6 Volts. Additionally, if the base lead is left open, the LP395 will turn on.

The LP395 is a low-power version of the 1-Amp LM195/LM295/LM395 Ultra Reliable Power Transistor.

The LP395 is rated for operation over a −40°C to +125°C range.

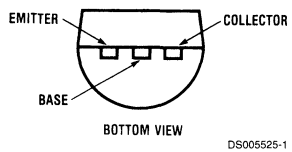
Features

- Internal thermal limiting
- Internal current and power limiting
- Guaranteed 100 mA output current
- 0.5 µA typical base current
- Directly interfaces with TTL or CMOS
- +36 Volts on base causes no damage
- 2 µs switching time

11

Connection Diagram

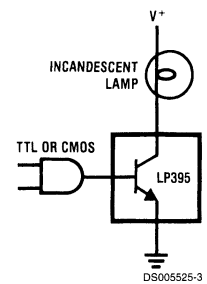
TO-92 Package



Order Number LP395Z
See NS Package Z03A

Typical Applications

Fully Protected Lamp Driver



National Semiconductor

MF10
Universal Monolithic Dual Switched Capacitor Filter

General Description

The MF10 consists of 2 independent and extremely easy to use, general purpose CMOS active filter building blocks. Each block, together with an external clock and 3 to 4 resistors, can produce various 2nd order functions. Each building block has 3 output pins. One of the outputs can be configured to perform either an allpass, highpass or a notch function; the remaining 2 output pins perform lowpass and bandpass functions. The center frequency of the lowpass and bandpass 2nd order functions can be either directly dependent on the clock frequency, or they can depend on both clock frequency and external resistor ratios. The center frequency of the notch and allpass functions is directly dependent on the clock frequency, while the highpass center frequency depends on both resistor ratio and clock. Up to 4th order functions can be performed by cascading the two 2nd order building blocks of the MF10; higher than 4th order functions can be obtained by cascading MF10 packages.

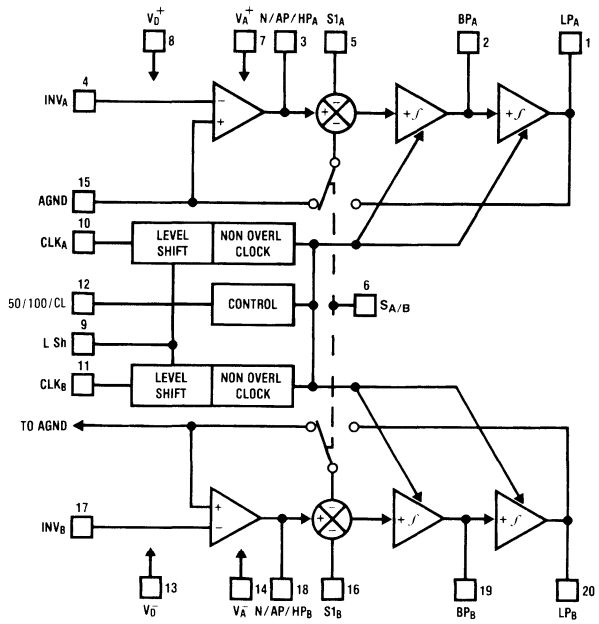
Any of the classical filter configurations (such as Butterworth, Bessel, Cauer and Chebyshev) can be formed.

For pin-compatible device with improved performance refer to LMF100 datasheet.

Features

- Easy to use
- Clock to center frequency ratio accuracy ±0.6%
- Filter cutoff frequency stability directly dependent on external clock quality
- Low sensitivity to external component variation
- Separate highpass (or notch or allpass), bandpass, lowpass outputs
- f_O x Q range up to 200 kHz
- Operation up to 30 kHz
- 20-pin 0.3" wide Dual-In-Line package
- 20-pin Surface Mount (SO) wide-body package

System Block Diagram



01039901

Package in 20 pin molded wide body surface mount and 20 pin molded DIP.

National Semiconductor

MM58342
High Voltage Display Driver

General Description

The MM58342 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P- and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58342 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block Diagram

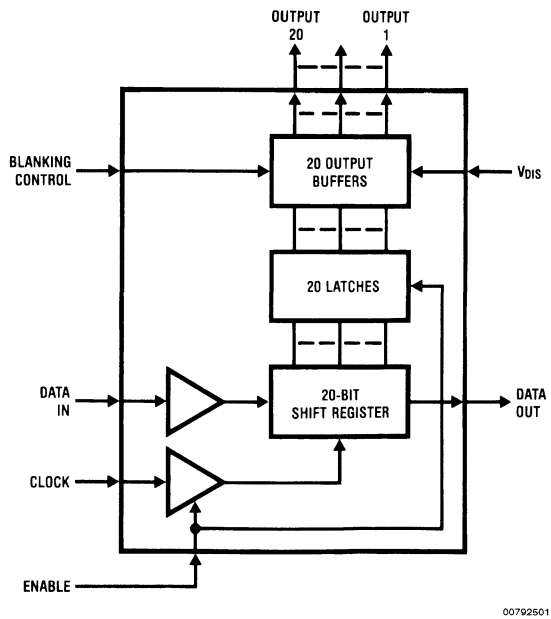


FIGURE 1.

National Semiconductor

Imaging Products

National Semiconductor

Imaging Products Selection Guide

Device	Description	Output Resolution (Bits)	Pixel Conv Rate (MSPS)	Supply Voltage (V)	Power Consumption (mW, typ)	Full Channel INL (LSB, typ)	Full Channel DNL (LSB, typ)
LM9822	42-Bit, 3 Channel Color Scanner AFE	14	6	5	375	±2.2*	+0.4/−0.9*
LM9823	48-Bit, 3 Channel Color Scanner AFE	16	6	5	375	+2.2*	+0.4/−0.9*
LM98501	10-Bit 27MSPS Camera AFE	10	27	3	195	−1.5/+3.0	±0.5
LM98503	10-Bit 18MSPS Camera AFE	10	18	3	86	−1.5/+3.0	±0.5

* referred to 12 bits

National Semiconductor

LM9822
3 Channel 42-Bit Color Scanner Analog Front End

General Description

The LM9822 is a high performance Analog Front End (AFE) for image sensor processing systems. It performs all the analog and mixed signal functions (correlated double sampling, color specific gain and offset correction, and analog to digital conversion) necessary to digitize the output of a wide variety of CIS and CCD sensors. The LM9822 has a 14-bit 6 MHz ADC.

Features

- 6 million pixels/s conversion rate
- Digitally programmed gain and offset for red, green and blue color balancing
- Correlated Double Sampling for lowest noise from CCD sensors
- Compatible with CCD and CIS type image sensors
- Internal Voltage Reference Generation
- TTL/CMOS compatible input/output

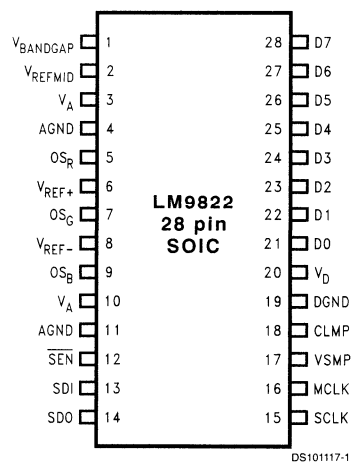
Key Specifications

■ Output Data Resolution	14 Bits
■ Pixel Conversion Rate	6 MHz
■ Analog Supply Voltage	5V±5%
■ I/O Supply Voltage	3.3V±10% or 5V±5%
■ Power Dissipation (typical)	375 mW

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Scanners
- Multifunction Imaging Products
- Digital Copiers
- General Purpose Linear Array Imaging

Connection Diagram



DS101117-1

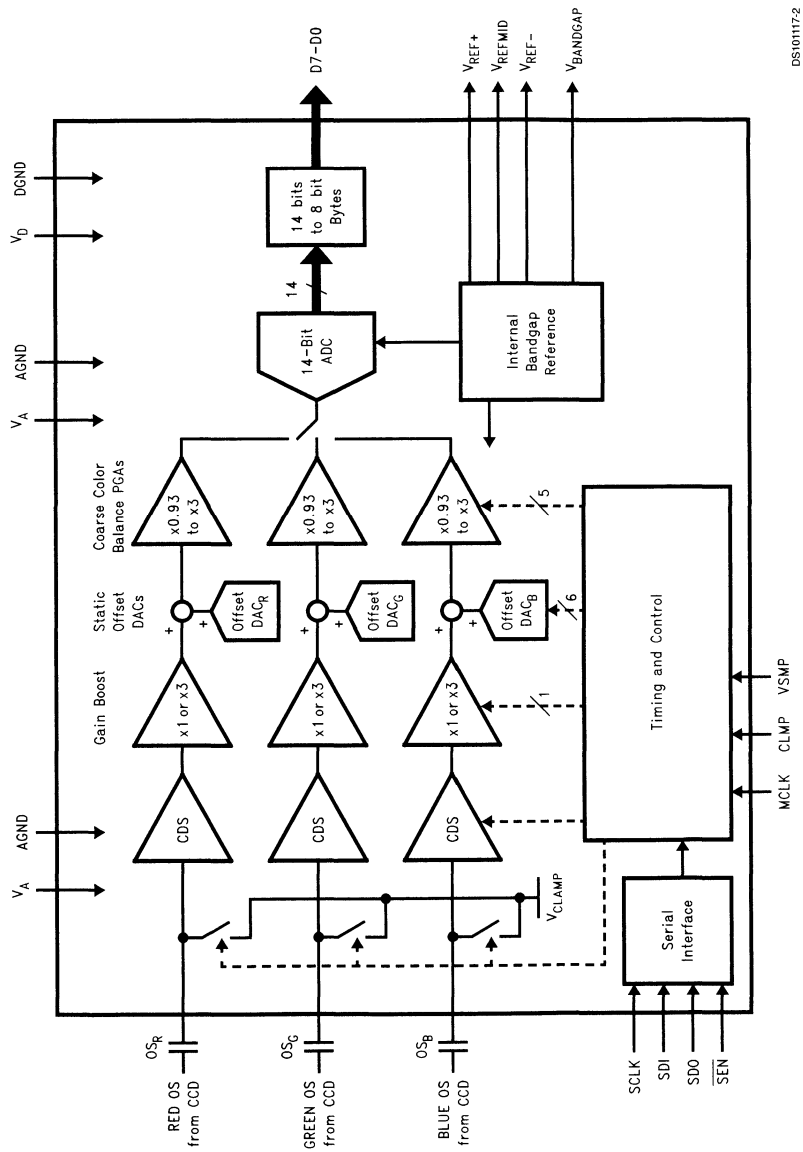
Ordering Information

Temperature Range $0°C \le T_A \le +70°C$		NS Package Number
Order Number	Device Marking	
LM9822CCWM (Note 1)	LM9822CCWM	M28B
LM9822CCWMX (Note 2)	LM9822CCWM	M28B

Note 1: Rail transport media, 26 parts per rail.

Note 2: Tape and reel transport media, 1000 parts per reel.

LM9822 Block Diagram



11

National Semiconductor

LM9823
3 Channel 48-Bit Color Scanner Analog Front End

General Description

The LM9823 is a high performance Analog Front End (AFE) for image sensor processing systems. It performs all the analog and mixed signal functions (correlated double sampling, color specific gain and offset correction, and analog to digital conversion) necessary to digitize the output of a wide variety of CIS and CCD sensors. The LM9823 has a 16-bit 6 MHz ADC.

Features

- 6 million pixels/s conversion rate
- Digitally programmed gain and offset for red, green and blue color balancing
- Correlated Double Sampling for lowest noise from CCD sensors
- Compatible with CCD and CIS type image sensors
- Internal Voltage Reference Generation
- TTL/CMOS Compatible input/output

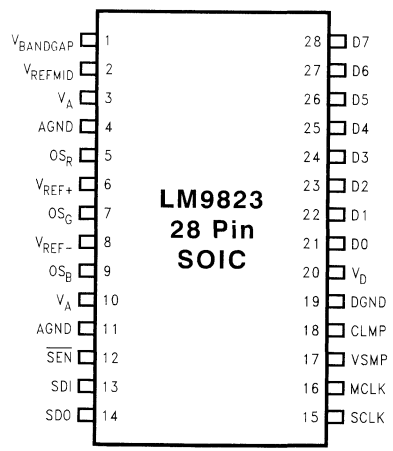
Key Specifications

■ Output Data Resolution	16 Bits
■ Pixel Conversion Rate	6 MHz
■ Analog Supply Voltage	5V±5%
■ I/O Supply Voltage	3.3V±10% or 5V±5%
■ Power Dissipation (typical)	375 mW

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Scanners
- Multifunction Imaging Products
- Digital Copiers
- General Purpose Linear Array Imaging

Connection Diagram



20033801

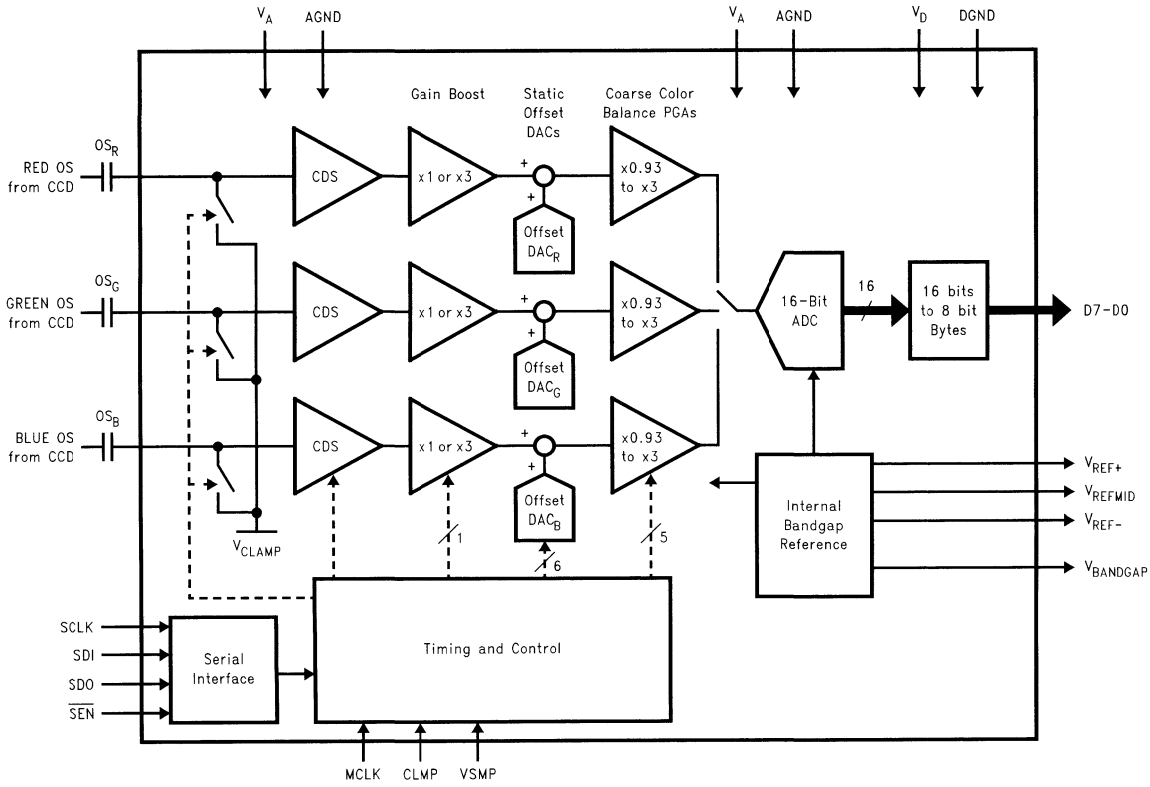
Ordering Information

Temperature Range $0^{\circ}C \le T_A \le +70^{\circ}C$		NS Package Number
Order Number	Device Marking	
LM9823CCWM (Note 1)	LM9823CCWM	M28B
LM9823CCWMX (Note 2)	LM9823CCWM	M28B

Note 1: Rail transport media, 26 parts per rail.

Note 2: Tape and reel transport media, 1000 parts per reel.

Block Diagram



National Semiconductor

LM98501
10-Bit, 27 MSPS Camera Signal Processor

General Description

The LM98501 is a CCD signal processor for electronic cameras. The processor provides a common interface to a number of different image sensors including CCD, CMOS, and CIS. Correlated double sampling reduces kTC noise from the image signal. A fast, temperature stable, 8-bit digitally programmable gain amplifier enables pixel-rate white-balancing. An auxiliary input is provided, allowing for the selection of an external signal, useful for electronic titling and video overlay. The 10-bit A/D converter preserves the image quality with excellent noise performance. The LM98501 also includes the supporting functions of digital black level clamp and power down, ideally suited for portable video applications. This low-power processor is a natural choice for the most demanding imaging systems.

Applications

- Digital still camera
- Digital video camcorder
- Video conferencing
- Security camera
- Plain paper copier
- Flatbed or handheld color scanner
- Video processing for x-ray or infrared
- Barcode scanner

Features

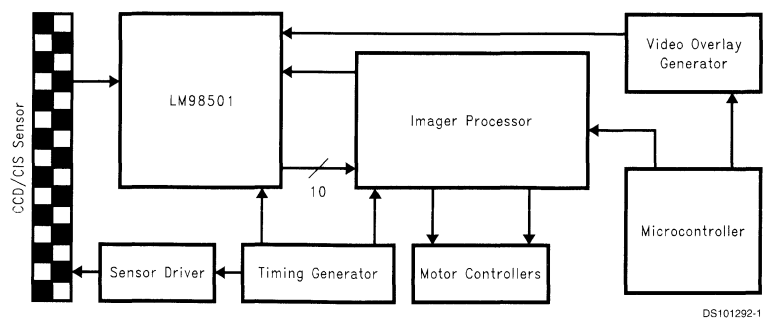
- +3V single power supply
- Low power CMOS design
- 4-wire serial interface
- 2.5V data output voltage swing
- No missing codes
- AUX input with input clamp and programmable gain
- Four color gain and offset registers
- Digital black level clamp
- Small 48-lead LQFP package

Key Specifications

■Maximum Input Level	1.0V peak-peak
■CDS Sampling Rate	27 MSPS
■PGA Gain Steps	256 Steps
■PGA Gain Range	0.0 dB-32.0 dB
■ADC Resolution	10-Bit
■ADC Sampling Rate	27 MSPS
■*Signal-to-Noise Ratio	60 dB @ 0 dB Gain, 1.0V Input
■Power Dissipation AV+ = DV+ = DV+ I/O = 3.0V	195 mW (typical)
■Operating Temperature	0°C to 70°C

*20 $\log_{10}$ (V_{IN}/RMS Output Noise)

Typical Digital Camera Block Diagram



Overall Chip Block Diagram

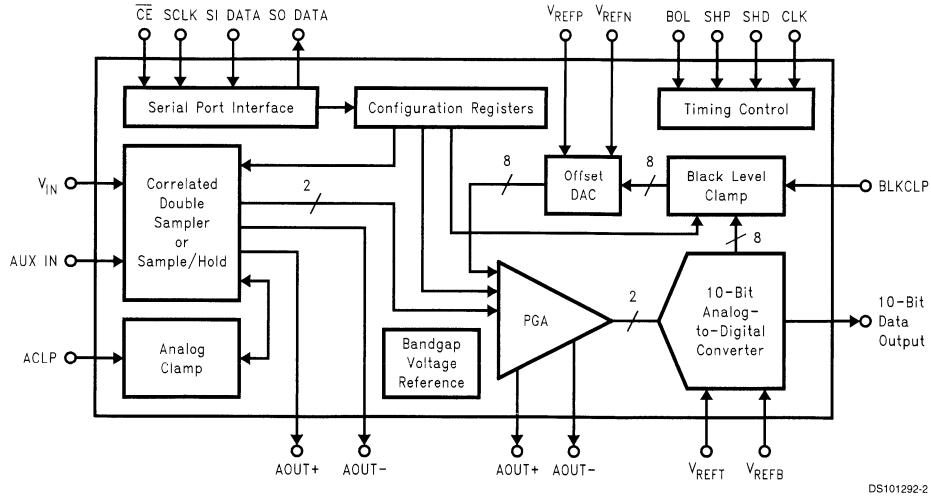


FIGURE 1. Chip Block Diagram

LM98501 Chip Pin Out

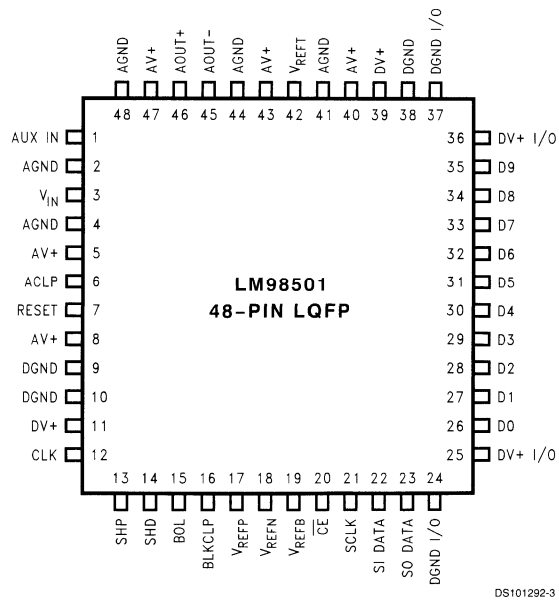


FIGURE 2. Pin Out Diagram

Ordering Information

Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)	NS Package
LM98501CCVBH	LQFP

National Semiconductor

LM98503
10-Bit, 18 MSPS Camera Signal Processor

General Description

The LM98503 is a CCD signal processor for digital cameras. The processor provides a common interface to a number of different image sensors including CCD, CMOS, and CIS. Correlated double sampling reduces kTC noise from the image signal. A fast, temperature stable, 8-bit digitally programmable gain amplifier enables pixel-rate white-balancing. An auxiliary input is provided, allowing for the selection of an external signal, useful for sampling analog video signals. The 10-bit A/D converter preserves the image quality with excellent noise performance. The LM98503 also includes the supporting functions of digital black level clamp and power down, ideally suited for portable video applications. This low-power processor is a natural choice for the most demanding imaging systems.

Applications

- Digital still cameras
- Digital video camcorders
- Video conferencing
- Security cameras
- Plain paper copiers
- Flatbed or handheld color scanners
- Video processing for X-ray or infrared
- Barcode scanners

Features

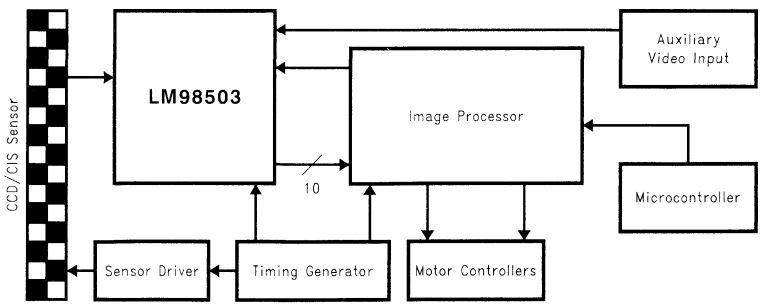
- +3V single power supply
- Low power CMOS design
- 4-Wire serial interface
- 2.5V data output voltage swing
- AUX input with analog clamp and programmable gain
- Four color gain and offset registers
- Digital black level clamp
- Small 48-lead LQFP package
- Supports interface and progressive scan CCDs.

Key Specifications

Maximum Input Level	1.0V peak-peak
CDS Sampling Rate	18 MSPS
PGA Gain Steps	256 Steps
PGA Gain Range	0.0 - 32.0 dB
ADC Resolution	10-Bit
ADC Sampling Rate	18 MSPS
*Signal-to-Noise Ratio	68 dB @ 0 dB Gain, 1.0V Input
Power Dissipation AV+ = DV+ = 2.7V	86 mW (typical)
Operating Temperature	0°C to +70°C

*20 $\log_{10}$ (V_{IN}/RMS Output Noise)

Typical Digital Camera Block Diagram



20033901

Block Diagram

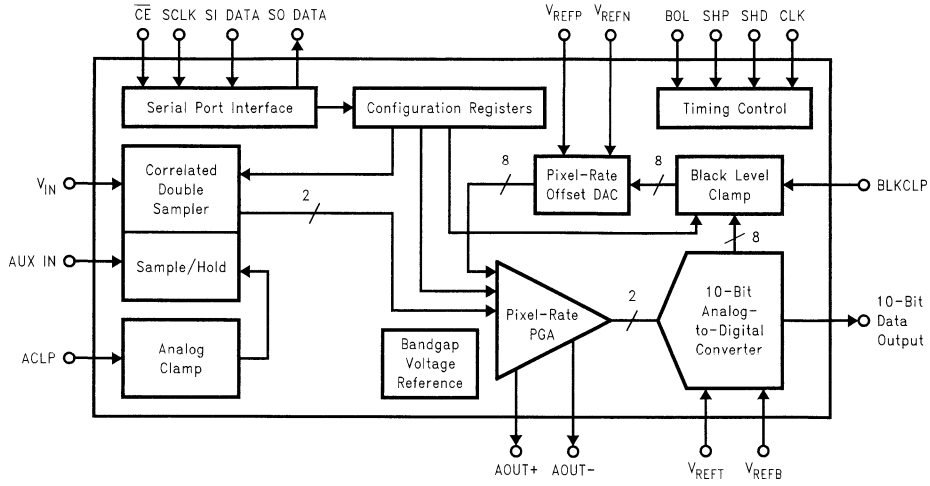


FIGURE 1. Chip Block Diagram

Pin Out

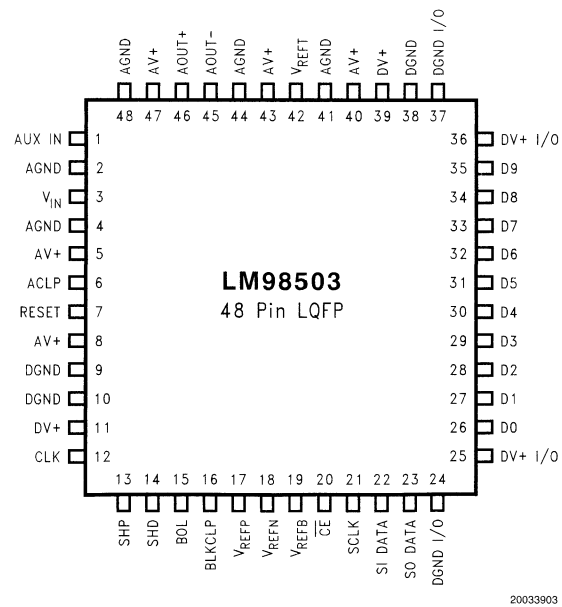


FIGURE 2. Pin Out Diagram

Ordering Information

Commercial ($0^{\circ}C \leq T_A \leq 70^{\circ}C$)	NS Package
LM98503CCVV	LQFP

Typical Application Circuit

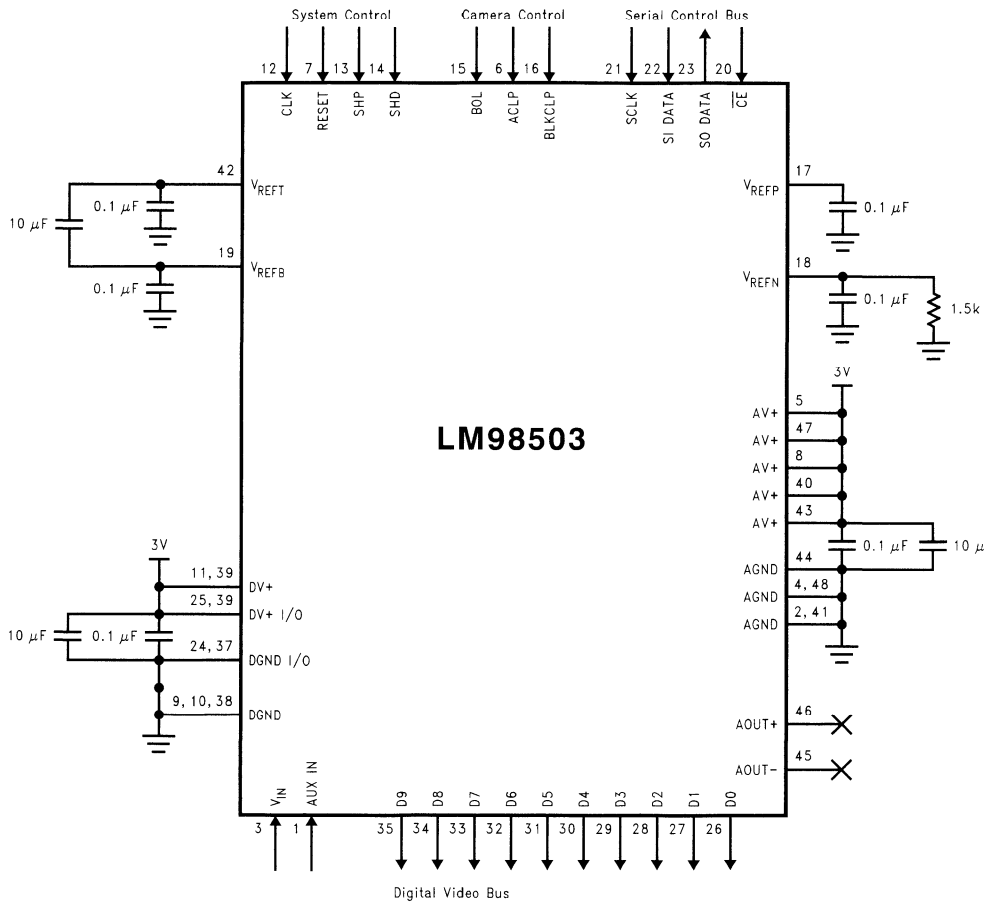


FIGURE 3. Typical Application Circuit Diagram

Pin Descriptions

Pin	Name	I/O	Typ	Description
1	AUX IN	I	A	Auxiliary analog input.
2	AGND		P	Analog ground return.
3	V_{IN}	I	A	Analog input. AC-couple input signal through a 0.1 µF capacitor.
4	AGND		P	Analog ground return.
5	AV+		P	+3V power supply for the analog circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
6	ACLP	I	D	Analog clamp switch.
7	RESET	I	D	Active-high master reset. Float pin when function not being used.
8	AV+		P	+3V power supply for the analog circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
9	DGND		P	Digital ground return.
10	DGND		P	Digital ground return.
11	DV+		P	+3V power supply for the digital circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
12	CLK	I	D	18 MHz clock input.
13	SHP	I	D	Correlated double sampler reset voltage clamp override. Programmable active-high or active-low through serial interface. Connect to +3V digital supply when function not being used (register values in default condition).
14	SHD	I	D	Correlated double sampler video signal voltage sample override. Programmable active-high or active-low through serial interface. Connect to +3V digital supply when function not being used (register values in default condition).
15	BOL	I	D	Active-high beginning of line switch input. Hold high during entire line of effective pixels. Hold low during blanking period.
16	BLKCLP	I	D	Active-high black level clamp switch input. Pulse high during black pixels to set black pixel level to the value stored in Output Black Level register. (See page 15).
17	V_{REFP}	IO	A	Top of DAC reference ladder. Normally bypassed with a 0.1 µF capacitor. An external DAC reference voltage may be applied to this pin.
18	V_{REFN}	IO	A	Bottom of DAC reference ladder. Normally bypassed with a 0.1 µF capacitor. An external DAC reference voltage may be applied to this pin. Alternately, an external pull-down resistor may be used to extend the DAC range. (See section 3.0).
19	V_{REFB}	IO	A	Bottom of ADC reference ladder. Normally bypassed with a 0.1 µF capacitor and 10 µF capacitors in parallel. An external ADC reference voltage may be applied to this pin.
20	$\overline{CE}$	I	D	Active-low chip enable for the serial interface.
21	SCLK	I	D	Serial interface clock used to decode the serial input data.
22	SI DATA	I	D	Serial interface input port.
23	SO DATA	O	D	Serial interface output port.
24	DGND I/O		P	Digital output driver ground return.
25	DV+ I/O		P	+3V power supply for the digital output driver circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
26	D0	O	D	Digital output. Bit 0 of 9 (LSB) of the digital video output bus.
27	D1	O	D	Digital output. Bit 1 of 9 of the digital video output bus.
28	D2	O	D	Digital output. Bit 2 of 9 of the digital video output bus.
29	D3	O	D	Digital output. Bit 3 of 9 of the digital video output bus.
30	D4	O	D	Digital output. Bit 4 of 9 of the digital video output bus.
31	D5	O	D	Digital output. Bit 5 of 9 of the digital video output bus.
32	D6	O	D	Digital output. Bit 6 of 9 of the digital video output bus.
33	D7	O	D	Digital output. Bit 7 of 9 of the digital video output bus.
34	D8	O	D	Digital output. Bit 8 of 9 of the digital video output bus.
35	D9	O	D	Digital output. Bit 9 of 9 (MSB) of the digital video output bus.

Pin Descriptions (Continued)

Pin	Name	I/O	Typ	Description
36	DV+ I/O		P	+3V power supply for the digital output driver circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
37	DGND I/O		P	Digital output driver ground return.
38	DGND		P	Digital ground return.
39	DV+		P	+3V power supply for the digital circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
40	AV+		P	+3V power supply for the analog circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
41	AGND		P	Analog ground return.
42	V_{REFT}	IO	A	Top of ADC reference ladder. Normally bypassed with a 0.1 µF capacitor and 10 µF capacitors in parallel. An external ADC reference voltage may be applied to this pin.
43	AV+		P	+3V power supply for the analog circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
44	AGND		P	Analog ground return.
45	AOUT−	O	A	Negative differential analog output from correlated double sampler or PGA (selectable through the serial interface).
46	AOUT+	O	A	Positive differential analog output from correlated double sampler or PGA (selectable through the serial interface).
47	AV+		P	+3V power supply for the analog circuits. Bypass each supply pin with 0.1 µF and 10 µF capacitors in parallel.
48	AGND		P	Analog ground return.

Legend: (I=Input), (O=Output), (IO=Bi-directional), (P=Power), (D=Digital), (A=Analog)

National Semiconductor

LCD Drivers

National Semiconductor

MM5452/MM5453
Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores display data in latches after it is clocked in, and holds the data until new display data is received.

Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block Diagram

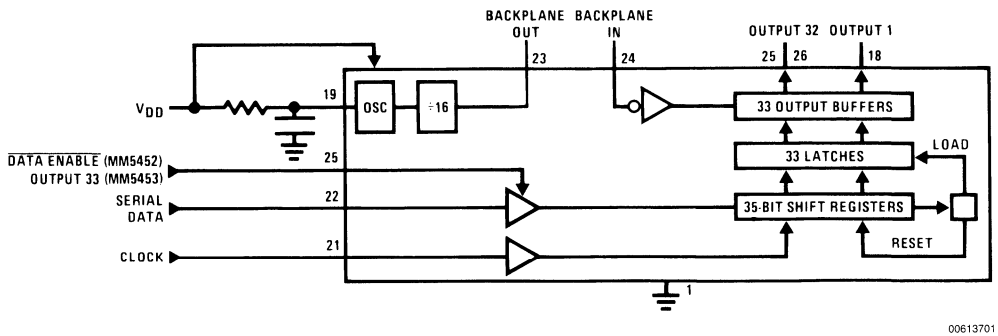


FIGURE 1.

National Semiconductor

MM5483
Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received.

Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block and Connection Diagrams

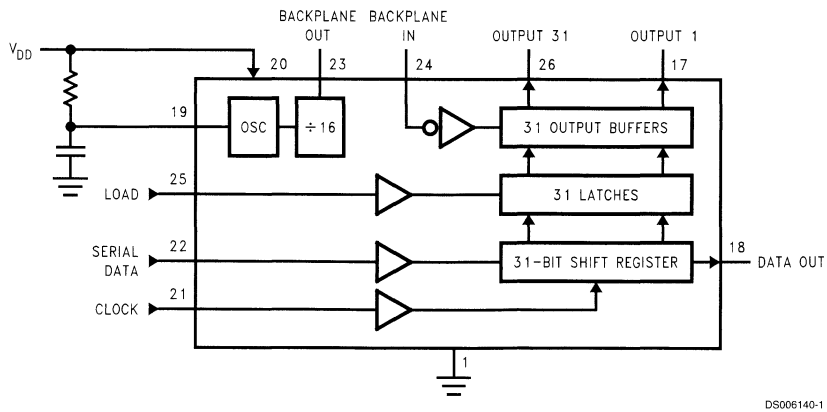
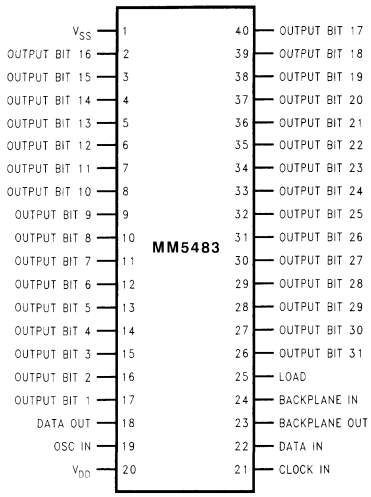


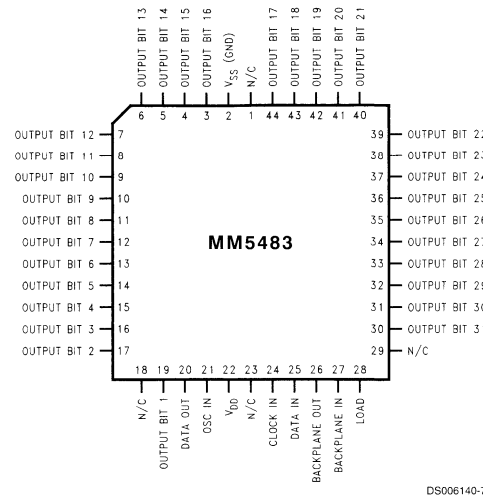
FIGURE 1.

Block and Connection Diagrams (Continued)

Dual-In-Line Package



Top View
Order Number MM5483N
See NS Package Number N40A



Order Number MM5483V
See NS Package Number V44A

FIGURE 2.

National Semiconductor

MM145453
Liquid Crystal Display Driver

General Description

The MM145453 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. The chip can drive up to 33 LCD segments and can be paralleled to increase this number. The chip is capable of driving a 4½ digit 7-segment display with minimal interface between the display and the data source.

The MM145453 stores display data in latches after it is clocked in, and holds the data until new display data is received.

The MM145453 is available in a molded 44 pin surface mount PLCC package. The MM145453 is pin out and functionally compatible with the MC145453.

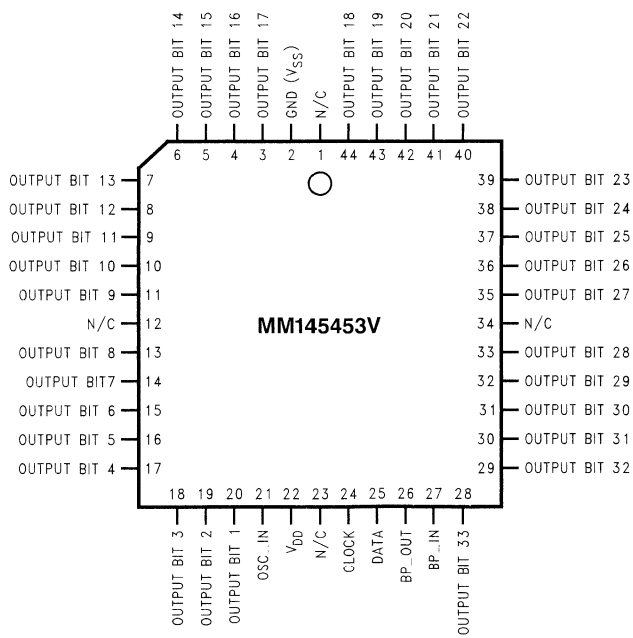
Features

- Serial Data Input
- Wide Power Supply operation
- TTL Compatibility
- Up to 33 LCD Segments
- Alphanumeric or Bar Graph capability
- Cascaded operation capability
- Pin Compatible with MC145453

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation displays
- Remote displays

Connection Diagram



Top View
Order Number MM145453V
See NS Package Number V44A

National Semiconductor

Lithium Battery Chargers

National Semiconductor

Lithium Battery Charger Selection Guide

Part Number	Function	Input Range (V)	Output	Features	Package (Note 1)
LM3420	CV charge control for 1, 2, 3, 4, or 5 Li-Ion cells	4.2, 8.2, 8.4, 12.6, 16.8	Current for driving power stage in constant-voltage control of charger	1% & 0.5% tolerances.	M5
LM3620	CV charge control for 1 or 2 Li-Ion cells	4 to 30	Current for driving external PNP in constant-voltage control of charger	1.2% tolerance. Selectable battery type(coke vs graphite anode).	M5
LM3621	Full-function CVCC charge controller for 1 Li-Ion cell	3.0 to 5.5	Analog control of constant-current / constant-voltage charger	0.5% tolerance. Selectable battery type (coke vs graphite anode). 5 charge modes plus fault detection	M16
LM3622	CVCC charge control for 1 or 2 Li-Ion cells	4.5 to 24	Current for driving external PNP or P-FET in constant-voltage / constant-current control of charger	0.7% and 1.2% tolerances. Versions for coke or graphite battery type. 'Wake up' mode for pre-conditioning deeply discharged cells.	M08

Note 1: Package designation includes number of pins:

M = plastic surface-mount

M5 = 5 Lead SOT-23

National Semiconductor

LM3420-4.2, -8.2, -8.4, -12.6, -16.8 Lithium-Ion Battery Charge Controller

General Description

The LM3420 series of controllers are monolithic integrated circuits designed for charging and end-of-charge control for Lithium-Ion rechargeable batteries. The LM3420 is available in five fixed voltage versions for one through four cell charger applications (4.2V, 8.2V/8.4V, 12.6V and 16.8V respectively).

Included in a very small package is an (internally compensated) op amp, a bandgap reference, an NPN output transistor, and voltage setting resistors. The amplifier's inverting input is externally accessible for loop frequency compensation. The output is an open-emitter NPN transistor capable of driving up to 15 mA of output current into external circuitry.

A trimmed precision bandgap reference utilizes temperature drift curvature correction for excellent voltage stability over the operating temperature range. Available with an initial tolerance of 0.5% for the A grade version, and 1% for the standard version, the LM3420 allows for precision end-of-charge control for Lithium-Ion rechargeable batteries.

The LM3420 is available in a sub-miniature 5-lead SOT23-5 surface mount package thus allowing very compact designs.

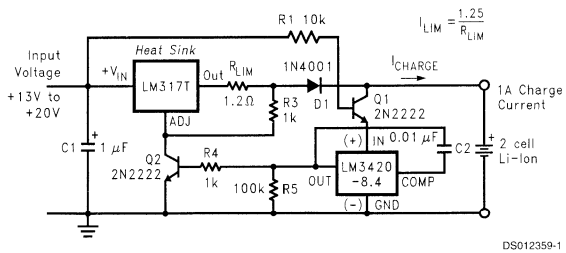
Features

- Voltage options for charging 1, 2, 3 or 4 cells
- Tiny SOT23-5 package
- Precision (0.5%) end-of-charge control
- Drive capability for external power stage
- Low quiescent current, 85 µA (typ.)

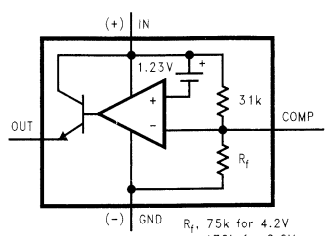
Applications

- Lithium-Ion battery charging
- Suitable for linear and switching regulator charger designs

Typical Application and Functional Diagram



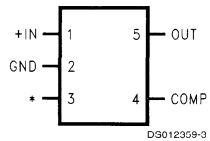
Typical Constant Current/Constant Voltage Li-Ion Battery Charger



LM3420 Functional Diagram

Connection Diagrams and Order Information

5-Lead Small Outline Package (M5)



DS012359-3

*No internal connection, but should be soldered to PC board for best heat transfer.

Top View

Actual Size

DS012359-4

For Ordering Information
See *Figure 1* in this Data Sheet
See NS Package Number MF05A

National Semiconductor

LM3620
Lithium-Ion Battery Charger Controller

General Description

The LM3620 series of controllers are monolithic integrated circuits designed to control the charging and end-of-charge control for lithium-ion rechargeable batteries. The LM3620 is available in two versions for one or two cell charger applications. Each version provides the option of selecting the appropriate termination voltage for either coke or graphite anode lithium cells.

The LM3620 can operate from a wide range of DC input sources (4V to 30V). With no charger supply connected, the controller draws a quiescent current of only 10nA to minimize discharging of a connected battery pack.

The LM3620 consists of an operational transconductance amplifier, a bandgap voltage reference, a NPN driver transistor and precision voltage setting resistors. The output of the amplifier is made available to drive an external power transistor if higher drive currents are required.

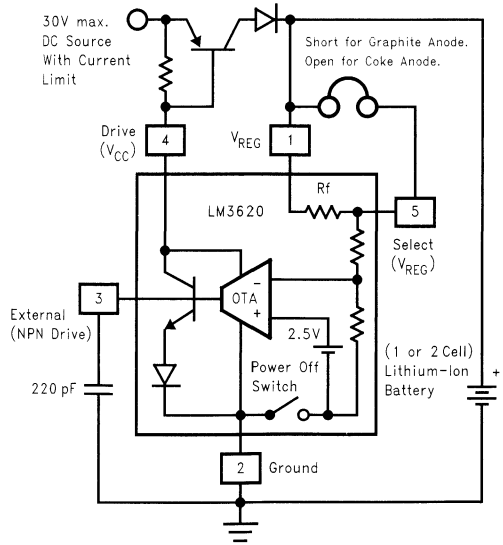
With a trimmed output voltage regulation of ±1.2% initial accuracy, the LM3620 provides a simple, precise solution for end-of-charge control of lithium-ion rechargeable cells.

The LM3620 is packaged in a miniature 5-lead SOT-23 surface mount package for very compact designs.

Features

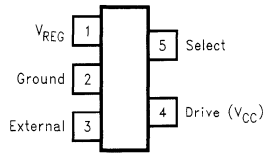
- Voltage options for charging 1 or 2 cell stacks
- Adjustable output voltage for coke or graphite anodes
- Precision end-of-charge voltage control
- Wide input voltage range (4V to 30V)
- Low off state current (<10nA)
- Drive provided for external power stage
- Tiny SOT-23 package

Typical Application



Connection Diagram

5-Lead SOT23-5 Surface Mount Package



Refer to the Ordering Information Table in this Data Sheet for Specific Part Number

See NS Package MF05A

Ordering Information

Device Order Number	Package Marking	Output Voltage	Initial Accuracy (25°C)	Over Temperature Accuracy (0 to 70°C)	Number of Cells	Supplied as
LM3620M5-4	D10B	4.1V/4.2V	1.2%	2%	1	1000 Unit increments on Tape and Reel
LM3620M5X-4	D10B	4.1V/4.2V	1.2%	2%	1	3000 Unit increments on Tape and Reel
LM3620M5-8	D11B	8.2V/8.4V	1.2%	2%	2	1000 Unit increments on Tape and Reel
LM3620M5X-8	D11B	8.2V/8.4V	1.2%	2%	2	3000 Unit increments on Tape and Reel

The small physical size of the SOT23-5 Package does not allow for the full part number marking. Devices will be marked with the designation shown in the column Package Marking.

The devices are shipped in tape-and-reel format. The standard quantity is 250 units on a reel (indicated by the letters "M5" in the part number), or 3000 units on a reel (indicated by the letters "M5X" in the part number).

National Semiconductor

LM3621
Single Cell Lithium-Ion Battery Charger Controller

General Description

The LM3621 is a full function constant voltage, constant current (CVCC) lithium-ion (Li+) battery charger controller. It provides 1% regulation accuracy over the specified temperature range without requiring the use of external precision resistors. The IC controls five charge modes: conditioning, fast, top-off, monitor and maintenance. In addition, the LM3621 detects and flags defective batteries as well as over current and over voltage fault events. The architecture of the IC is based on high gain constant voltage and constant current control loops.

The LM3621 is designed to control a switching charger, a linear charger or an off-line ac adapter charger.

The LM3621 consists of a logic controller, precision bandgap reference, wide bandwidth transconductance error amplifiers, comparators, and an output buffer. The LM3621 is available in a 16-pin SOIC package and is specified over the range of 0°C to 70°C.

Key Specifications

- Tight output voltage accuracy (±0.5% at T_A = 25°C)
- Two selectable output voltages (4.2V or 4.1V)
- Less than 1 µA current drain from fully charged battery
- Preconditioning severely discharged cells (0V to 2.55V)

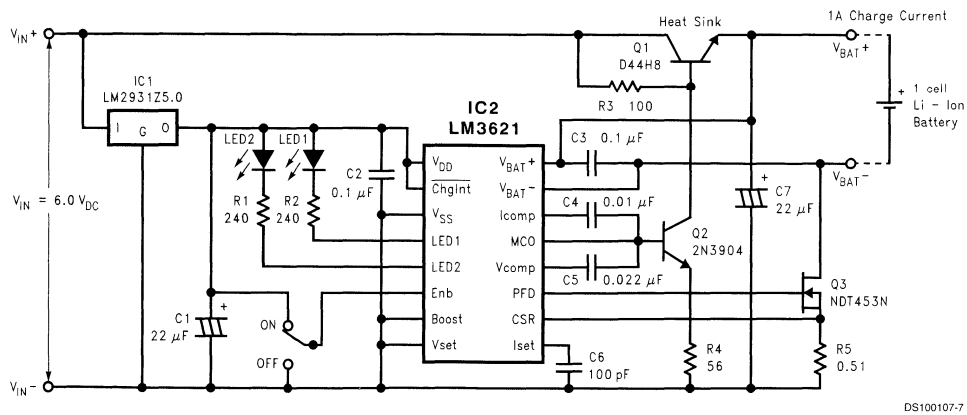
Features

- Automatic end-of-charge control
- Preset or user adjustable charge current regulation
- LED drivers for charging status and fault indication
- Battery self-discharge refresh (maintenance)
- Overvoltage/overcurrent fault detection and protection
- Defective battery pack detection
- Charge current boost control for cellular phone applications
- Charge interruption control input

Applications

- Complete, full function, protected battery charger for coke or graphite anode, single cell Lithium-Ion battery packs
- Linear voltage regulator controlled chargers
- High efficiency switching regulator controlled chargers
- Cost effective wall adapter chargers

Typical Application

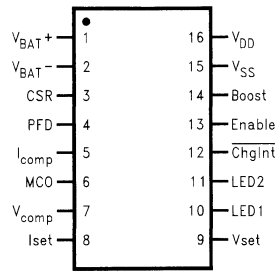


DS100107-7

1A, 4.1V CVCC Linear Charger for Graphite Anode Lithium-Ion Battery

Connection Diagram

16-Lead SOIC



Top View
Order Number LM3621M or LM3621M-3.0
NSC Package Number M16A

Pin Description

Pin No.	Symbol	I/O	Description
1	$V_{BAT}+$	I	Battery pack high side sense input.
2	$V_{BAT}-$	I	Battery pack low side sense input.
3	CSR	I	**C**urrent **S**ense **R**esistor high side input.
4	PFD	O	**P**ass **F**ET gate **D**rive output. (N-channel).
5	I_{COMP}	I	Compensation pin for current regulation loop.
6	MCO	O	**M**odulation **C**ontrol **O**utput- analog control signal output
7	V_{COMP}	I	Compensation pin for voltage regulation loop.
8	I_{SET}	I	Charge current adjust input pin (see application section).
9	V_{SET}	I	Charge termination voltage control input (V_{SET} = HI for 4.2V or V_{SET} = LO for 4.1V).
10	LED1	O	LED driver #1 output (open drain).
11	LED2	O	LED driver #2 output (open drain).
12	$\overline{ChgInt}$	I	Charge current interrupt (active LO).
13	Enable	I	Enable charge cycle control.
14	Boost	I	Maximum output current boost control (max output current increased by 80%).
15	V_{SS}	S	IC common.
16	V_{DD}	S	IC power supply.

National Semiconductor

LM3622
Lithium-Ion Battery Charger Controller

General Description

The LM3622 is a charge controller for Lithium-Ion batteries. This monolithic integrated circuit accurately controls an external pass transistor for precision Lithium-Ion battery charging. The LM3622 provides a constant voltage or constant current (CVCC) configuration that changes, as necessary, to optimally charge lithium-ion battery cells. Voltage charging versions (4.1V, 4.2V, 8.2V, and 8.4V) are available for one or two cell battery packs and for coke or graphite anode battery chemistry.

The LM3622 accepts input voltages from 4.5V to 24V. Controller accuracy over temperature is ±30mV/cell for A grade and ±50mV/cell for the standard grade. No precision external resistors are required. Furthermore, the LM3622's proprietary output voltage sensing circuit drains less than 200nA from the battery when the input source is disconnected.

The LM3622 circuitry includes functions for regulating the charge voltage with a temperature compensated bandgap reference and regulating the current with an external sense resistor. The internal bandgap insures excellent controller performance over the operating temperature and input supply range.

The LM3622 can sink 15mA minimum at the EXT pin to drive the base of an external PNP pass transistor. It also has low-voltage battery threshold circuitry that removes this drive when the cell voltage drops below a preset limit. The LV_{SEL} pin programs this threshold voltage to either 2.7V/cell or 2.15V/cell. The low-voltage detection, which is a user enabled feature, provides an output signal that can be used to enable a 'wake up charge' source automatically to precondition a deeply discharged pack.

The LM3622 is available in a standard 8-lead SOIC surface mount package.

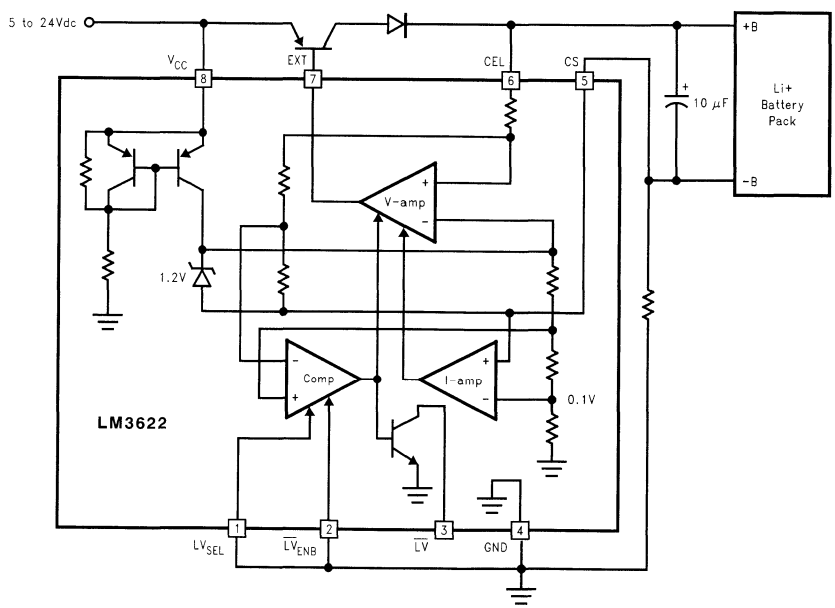
Features

- Versions for charging of 1 cell (4.1V or 4.2V) or 2 cells (8.2V or 8.4V)
- Versions for coke or graphite anode
- Precision (±30mV/cell) end-of-charge control
- Wide input range: 4.5V-24V
- Low battery drain leakage: 200nA
- 15 mA available to drive low cost PNP

Applications

- Cellular phone cradle charger
- PDA/Notebook cradle charger
- Camcorder cradle charger

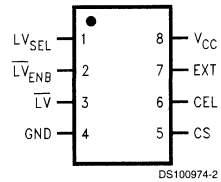
Typical Application



DS100974-1

Connection Diagram

8-Lead Surface Mount Package



Refer to the Ordering Information Table in this Datasheet for Specific Part Number
See NS Package M08A

Pin Description

Pin No.	Name	I/O	Description
1	LV_{SEL}	Input	Low-voltage detection threshold Select. The threshold is 2.15V/cell when this pin is pulled low to GND and 2.70V/cell when it is pulled up to V_{CC}. The battery voltage is sensed between CEL and CS pins.
2	$\overline{LV}_{ENB}$	Input	Low-voltage detection Enable. The low-voltage detection is enabled when this pin is pulled Low to GND. Pulling this pin HIGH to V_{CC} disables the low-voltage detection.
3	$\overline{LV}$	Output	Output of the low-voltage detection. This pin is a NPN open-collector output that goes to low impedance state when $\overline{LV}_{ENB}$ is pulled LOW and the battery voltage is below the threshold set by LV_{SEL}. $\overline{LV}$ stays in HIGH impedance state at any battery voltage when $\overline{LV}_{ENB}$ is pulled HIGH to V_{CC}. $\overline{LV}$ can be used for turning on a low current source to recondition a deeply depleted battery.
4	GND	Ground	IC common.
5	CS	Input	Input for battery charge current and battery negative-terminal voltage sensing. Battery charging current is sensed through an external resistor, R_{CS}, connected between the battery's negative terminal and GND. The maximum charge current is regulated to a value of $100mV/R_{CS}$.
6	CEL	Input	Battery positive-terminal voltage sensing.
7	EXT	Output	Output of the controller for driving a PNP transistor or P-MOSFET. The controller modulates the current sinking into this pin to control the regulation of either the charge current or the battery voltage.
8	V_{CC}	Power Supply	IC power supply

Ordering Information

Voltage	Grade	Accuracy	Order Information	Supplied As
4.1V	A	±30mV	LM3622AM-4.1	95 unit increments in rail
4.1V	A	±30mV	LM3622AMX-4.1	2500 unit increments in tape and reel
4.1V	Standard	±50mV	LM3622M-4.1	95 unit increments in rail
4.1V	Standard	±50mV	LM3622MX-4.1	2500 unit increments in tape and reel
4.2V	A	±30mV	LM3622AM-4.2	95 unit increments in rail
4.2V	A	±30mV	LM3622AMX-4.2	2500 unit increments in tape and reel
4.2V	Standard	±50mV	LM3622M-4.2	95 unit increments in rail
4.2V	Standard	±50mV	LM3622MX-4.2	2500 unit increments in tape and reel
8.2V	A	±60mV	LM3622AM-8.2	95 unit increments in rail
8.2V	A	±60mV	LM3622AMX-8.2	2500 unit increments in tape and reel
8.2V	Standard	±100mV	LM3622M-8.2	95 unit increments in rail
8.2V	Standard	±100mV	LM3622MX-8.2	2500 unit increments in tape and reel
8.4V	A	±60mV	LM3622AM-8.4	95 unit increments in rail
8.4V	A	±60mV	LM3622AMX-8.4	2500 unit increments in tape and reel
8.4V	Standard	±100mV	LM3622M-8.4	95 unit increments in rail
8.4V	Standard	±100mV	LM3622MX-8.4	2500 unit increments in tape and reel

National Semiconductor

LM3647
Universal Battery Charger for Li-Ion, Ni-MH and Ni-Cd Batteries

General Description

The LM3647 is a charge controller for Lithium-Ion (Li-Ion), Nickel-Metal Hydride (Ni-MH) and Nickel-Cadmium (Ni-Cd) batteries. The device can use either a pulsed-current charging or a constant-current charging technique. The device can also be configured to discharge before charging. Throughout the charging sequence the LM3647 monitors voltage and/or temperature and time in order to terminate charging.

Charge termination methods are:

- Negative delta voltage ($-\Delta V$)
- Optional: Delta temperature/delta time ($\Delta T/\Delta t$)
- Backup: Maximum temperature
- Backup: Maximum time
- Backup: Maximum voltage

If both voltage and temperature fail to trigger the termination requirements, then the maximum time (configured by external hardware) steps in which terminates the charging.

In Ni-Cd/Ni-MH mode, four different charging stages are used:

- Soft-start charge
- Fast charge
- Topping charge
- Maintenance charge

In Li-Ion mode, four different charging stages are used:

- Qualification
- Fast Charge Phase 1, Constant Current
- Fast Charge Phase 2, Constant Voltage
- Maintenance charge

The charge current of the LM3647 is configured via external resistors, which in turn controls the duty cycle of the PWM switching control output. For cost-sensitive applications, the LM3647 charge controller cab be configured to use an external current source and no temperature sensor.

When using an external current source, the current is controlled by the LM3647 which turns the current source on and off. The LM3647 automatically detects the presence of a battery and starts the charging procedure when the battery is installed. Whenever an error occurs (e.g., short circuit, temperature too high, temperature too low, bad battery, charge time over, etc.) the LM3647 will stay in error mode until the battery is removed or it gets within the allowed charging temperature range. The LM3647 is available in a standard 20-lead SOIC surface mount package.

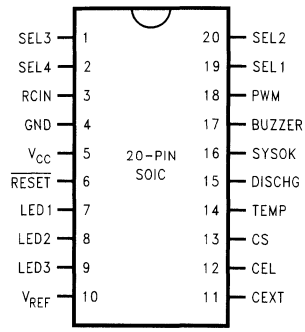
Features

- Auto-adaptive fast charge
- High-resolution, accurate voltage monitoring prevents Li-Ion undercharge or overcharge
- Fast charge, pre-charge and maintenance currents are provided. Different currents are selectable via external resistors.
- Fast-charge termination by Δ temperature/Δ time, maximum voltage, maximum temperature, negative Δ voltage and maximum time
- Dynamically detects battery insertion, removal, short circuit and bad battery without additional hardware
- Supports charging of battery packs with 2–8 cells of Ni-Cd/Ni-MH or 1–4 cells of Li-Ion (1 cell of NiCd/NiMH can be supported by added external 2x voltage amplifier)
- Three optional LED indicators and Buzzer output indicate operational modes
- Ni-MH/Ni-Cd charge mode, Li-Ion charge mode or discharge mode can be selected manually
- Supports control of current feedback power supply and constant current power supply

Applications

- Battery charging systems for:
  - — Portable consumer electronics
  - — Audio/video equipment
  - — Communications equipment
  - — Point of sale devices
  - — Power tools
  - — Personal convenience products

2.0 Connection Diagram



Top View
Order Number LM3647IM
See NS Package Number M20B

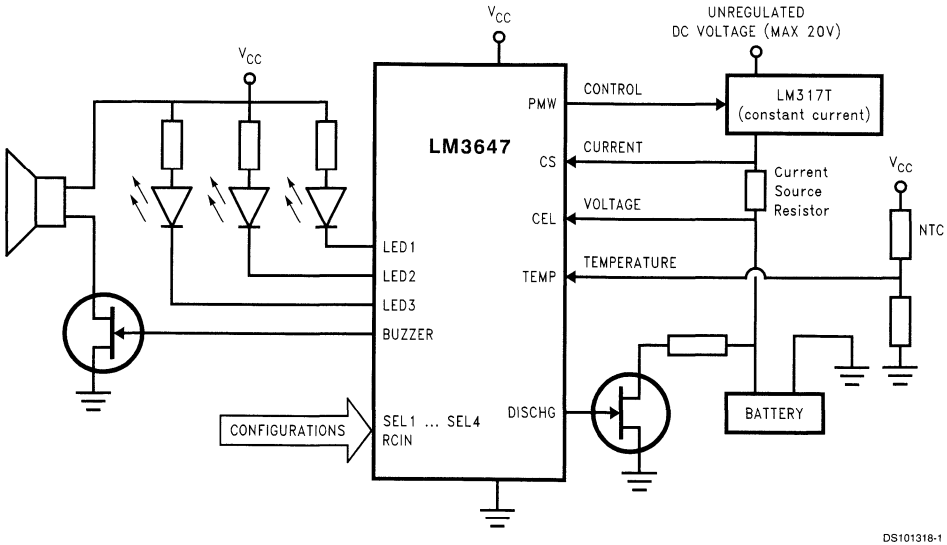
2.1 PIN DESCRIPTIONS

Pin No.	Name	I/O	Description
1	SEL3	I	Input to Select Power Source or Li-Ion Cell Voltage
2	SEL4	I	Input to Select Maintenance Charge Time Out, Connected to an RC-Network
3	RCIN		RC-Timing Pin
4	GND		Ground
5	V_{CC}		5V, Power Supply
6	RESET	I	Reset Pin, Active Low
7	LED1	O	LED Output
8	LED2	O	LED Output
9	LED3	O	LED Output
10	V_{REF}	I	Voltage Reference Analog Input
11	CEXT		External Capacitor
12	CEL	I	Battery Voltage Input (through resistor divider)
13	CS	I	Current Sense Input
14	TEMP	I	NTC-Temperature Sensor Input
15	DISCHG	O	High when Discharging, Else Low
16	SYSOK	O	System Monitor Output
17	BUZZER	O	Buzzer Output
18	PWM	O	Charge Control Output
19	SEL1	I	Tri-Level Input, Discharge/Maintenance Charge Select
20	SEL2	I	Tri-Level Input, Battery Type Select (NiCd, NiMH, Li-Ion)

2.2 ORDERING INFORMATION

Device	Package	Temperature
LM3647	20 SOIC	−40°C to +85°C

Typical Application



Motion Control

National Semiconductor

Motion Control and Motor Drive Selection Guide

Motor Drive Circuits-Bridges

Device	Description	Output Current (A)	Max Input Voltage (V)	Operating Temperature (T_J)	Package Availability
LMD18200	DMOS H-Bridge with Internal Current Sense	3	55	−40°C to +125°C	11-Lead TO-220
LMD18200-2D	Mil-Std 883. Dual DMOS H-Bridge	3	55	−55°C to +125°C	24-Lead Ceramic DIP
LMD18201	DMOS H-Bridge	3	55	−40°C to +125°C	11-Lead TO-220
LMD18245	DMOS H-Bridge with Digital or Analog Control	3	55	−40°C to +125°C	15-Lead TO-220

Motor Drive Circuits-Linear

Device	Description	Output Current (A)	Max Input Voltage (V)	Operating Temperature (T_C)	Package Availability
LM12CL	Monolithic Power Op-Amp	±10	±30	0°C to + 70°C	4-Lead TO-3
LM675	Monolithic Power Op-Amp	3	60	0°C to + 70°C	5-Lead TO-220
LM2876	Monolithic *Overture* Power Amplifier (Note 1)	3	60	20°C to +85°C	11-Lead TO-220
LM3875	Monolithic *Overture* Power Amplifier (Note 1)	4	84	20°C to +85°C	11-Lead TO-220
LM3876	Monolithic *Overture* Power Amplifier (Note 1)	4	84	20°C to +85°C	11-Lead TO-220
LM3886	Monolithic *Overture* Power Amplifier (Note 1)	7	84	20°C to +85°C	11-Lead TO-220
LM4700	Monolithic *Overture* Power Amplifier (Note 1)	2.9	64	20°C to +85°C	11-Lead TO-220

Quad High Side Driver

Device	Description	Output Current (A)	Max Input Voltage (V)	Operating Temperature (T_j)	Package Availability
LMD18400	Four Channel DMOS High Side Driver with diagnostics	1A per channel	28V	-40°C to 150°C	20 Lead DIP (N20)

Precision Motion Control Processor

Device	Features	Operating Temperature (T_A)	Max Clock Speed (MHz)	Package Availability
LM628	32-Bit Position, Velocity, and Acceleration Registers; Position and Velocity Modes; 16-Bit PID Filter with programmable Coefficients; 8 or 12-Bit DAC Output Data; Quadrature Incremental Encoder Interface; 8-Bit Asynchronous Host Interface	−40°C to + 85°C	6 or 8	28-Lead DIP
LM629	Same Features as LM628, but with 8-Bit PWM Sign/Magnitude output Data	−55°C to + 85°C	6 or 8	28-Lead DIP

Note 1: Refer to Audio Section for product data on the *Overture* power amplifiers.

National Semiconductor

LM12CL
80W Operational Amplifier

General Description

The LM12 is a power op amp capable of driving ±25V at ±10A while operating from ±30V supplies. The monolithic IC can deliver 80W of sine wave power into a 4Ω load with 0.01% distortion. Power bandwidth is 60 kHz. Further, a peak dissipation capability of 800W allows it to handle reactive loads such as transducers, actuators or small motors without derating. Important features include:

- input protection
- controlled turn on
- thermal limiting
- overvoltage shutdown
- output-current limiting
- dynamic safe-area protection

The IC delivers ±10A output current at any output voltage yet is completely protected against overloads, including shorts to the supplies. The dynamic safe-area protection is provided by instantaneous peak-temperature limiting within the power transistor array.

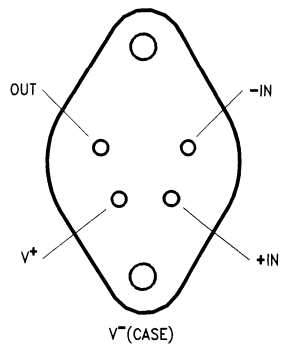
The turn-on characteristics are controlled by keeping the output open-circuited until the total supply voltage reaches 14V. The output is also opened as the case temperature exceeds 150°C or as the supply voltage approaches the BV_{CEO} of the output transistors. The IC withstands overvoltages to 80V.

This monolithic op amp is compensated for unity-gain feedback, with a small-signal bandwidth of 700 kHz. Slew rate is 9V/μs, even as a follower. Distortion and capacitive-load stability rival that of the best designs using complementary output transistors. Further, the IC withstands large differential input voltages and is well behaved should the common-mode range be exceeded.

The LM12 establishes that monolithic ICs can deliver considerable output power without resorting to complex switching schemes. Devices can be paralleled or bridged for even greater output capability. Applications include operational power supplies, high-voltage regulators, high-quality audio amplifiers, tape-head positioners, x-y plotters or other servo-control systems.

The LM12 is supplied in a four-lead, TO-3 package with V– on the case. A gold-eutectic die-attach to a molybdenum interface is used to avoid thermal fatigue problems. The LM12 is specified for either military or commercial temperature range.

Connection Diagram

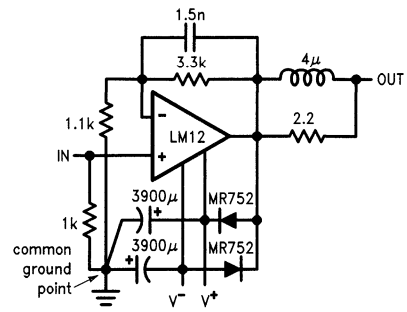


DS008704-1

4-pin glass epoxy TO-3 socket is available from AUGAT INC. Part number 8112-AG7

Bottom View
Order Number LM12CLK
See NS Package Number K04A

Typical Application*



DS008704-2

*Low distortion (0.01%) audio amplifier

National Semiconductor

LM628/LM629
Precision Motion Controller

General Description

The LM628/LM629 are dedicated motion-control processors designed for use with a variety of DC and brushless DC servo motors, and other servomechanisms which provide a quadrature incremental position feedback signal. The parts perform the intensive, real-time computational tasks required for high performance digital motion control. The host control software interface is facilitated by a high-level command set. The LM628 has an 8-bit output which can drive either an 8-bit or a 12-bit DAC. The components required to build a servo system are reduced to the DC motor/actuator, an incremental encoder, a DAC, a power amplifier, and the LM628. An LM629-based system is similar, except that it provides an 8-bit PWM output for directly driving H-switches. The parts are fabricated in NMOS and packaged in a 28-pin dual in-line package or a 24-pin surface mount package (LM629 only). Both 6 MHz and 8 MHz maximum frequency versions are available with the suffixes -6 and -8, respectively, used to designate the versions. They incorporate an SDA core processor and cells designed by SDA.

Features

- 32-bit position, velocity, and acceleration registers
- Programmable digital PID filter with 16-bit coefficients
- Programmable derivative sampling interval
- 8- or 12-bit DAC output data (LM628)
- 8-bit sign-magnitude PWM output data (LM629)
- Internal trapezoidal velocity profile generator
- Velocity, target position, and filter parameters may be changed during motion
- Position and velocity modes of operation
- Real-time programmable host interrupts
- 8-bit parallel asynchronous host interface
- Quadrature incremental encoder interface with index pulse input
- Available in a 28-pin dual in-line package or a 24-pin surface mount package (LM629 only)

Block Diagram

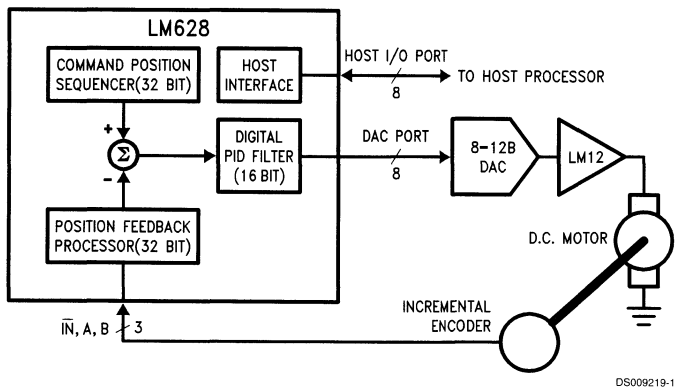
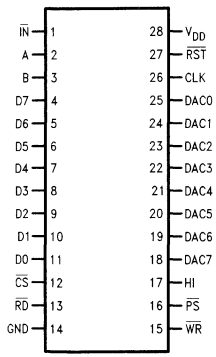


FIGURE 1. Block Diagram

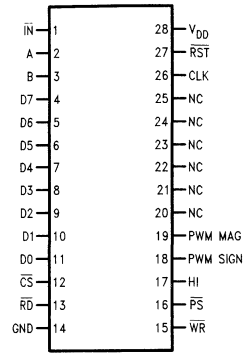
Connection Diagrams

LM628N



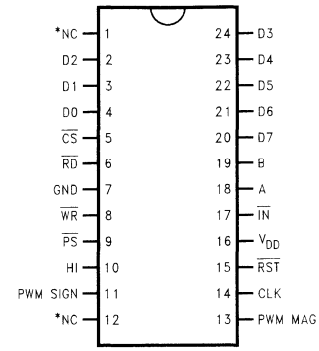
DS009219-2

LM629N



DS009219-3

LM629M



DS009219-21

*Do not connect.

Order Number LM629M-6, LM629M-8, LM628N-6, LM628N-8, LM629N-6 or LM629N-8
See NS Package Number M24B or N28B

National Semiconductor

LMD18200
3A, 55V H-Bridge

General Description

The LMD18200 is a 3A H-Bridge designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. Ideal for driving DC and stepper motors; the LMD18200 accommodates peak output currents up to 6A. An innovative circuit which facilitates low-loss sensing of the output current has been implemented.

Features

- Delivers up to 3A continuous output
- Operates at supply voltages up to 55V
- Low $R_{DS}(ON)$ typically 0.3Ω per switch
- TTL and CMOS compatible inputs
- No "shoot-through" current
- Thermal warning flag output at 145°C
- Thermal shutdown (outputs off) at 170°C
- Internal clamp diodes
- Shorted load protection
- Internal charge pump with external bootstrap capability

Applications

- DC and stepper motor drives
- Position and velocity servomechanisms
- Factory automation robots
- Numerically controlled machinery
- Computer printers and plotters

Functional Diagram

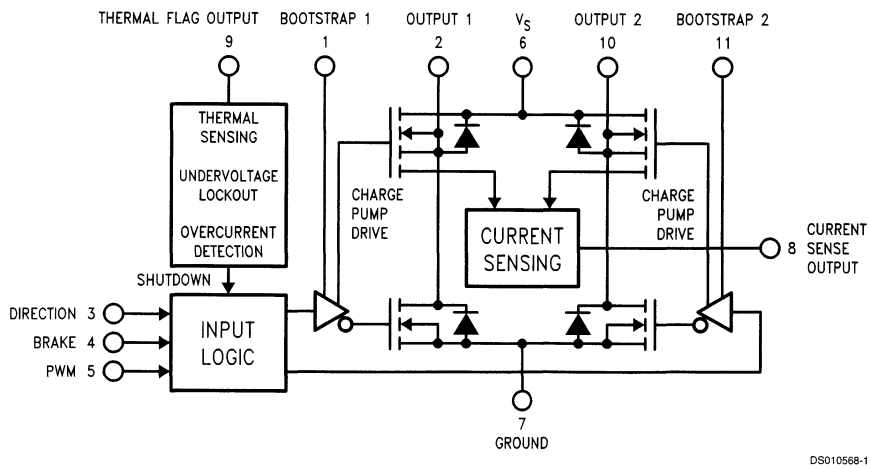
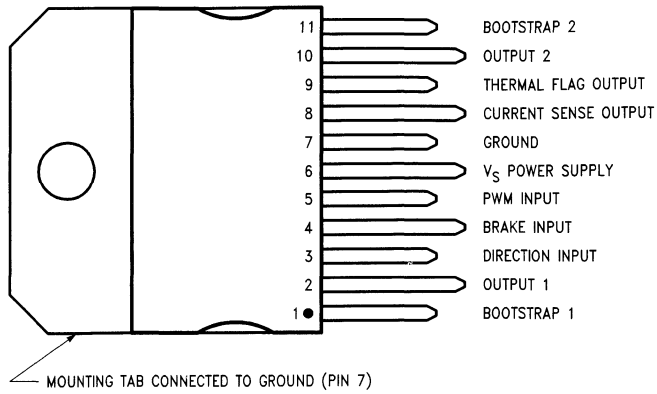


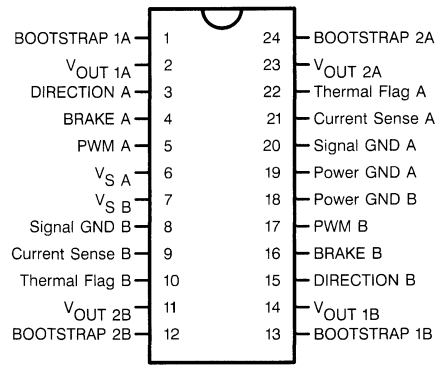
FIGURE 1. Functional Block Diagram of LMD18200

Connection Diagrams and Ordering Information



DS010568-2

11-Lead TO-220 Package
Top View
Order Number LMD18200T
See NS Package TA11B



DS010568-25

24-Lead Dual-in-Line Package
Top View
Order Number LMD18200-2D-QV
5962-9232501VXA
LMD18200-2D/883
5962-9232501MXA
See NS Package DA24B

National Semiconductor

LMD18201
3A, 55V H-Bridge

General Description

The LMD18201 is a 3A H-Bridge designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices on the same monolithic structure. The H-Bridge configuration is ideal for driving DC and stepper motors. The LMD18201 accommodates peak output currents up to 6A. Current sensing can be achieved via a small sense resistor connected in series with the power ground lead. For current sensing without disturbing the path of current to the load, the LMD18200 is recommended.

Features

- Delivers up to 3A continuous output
- Operates at supply voltages up to 55V
- Low $R_{DS(ON)}$ typically 0.33Ω per switch
- TTL and CMOS compatible inputs
- No "shoot-through" current
- Thermal warning flag output at 145°C
- Thermal shutdown (outputs off) at 170°C
- Internal clamp diodes
- Shorted load protection
- Internal charge pump with external bootstrap capability

Applications

- DC and stepper motor drives
- Position and velocity servomechanisms
- Factory automation robots
- Numerically controlled machinery
- Computer printers and plotters

Functional Diagram

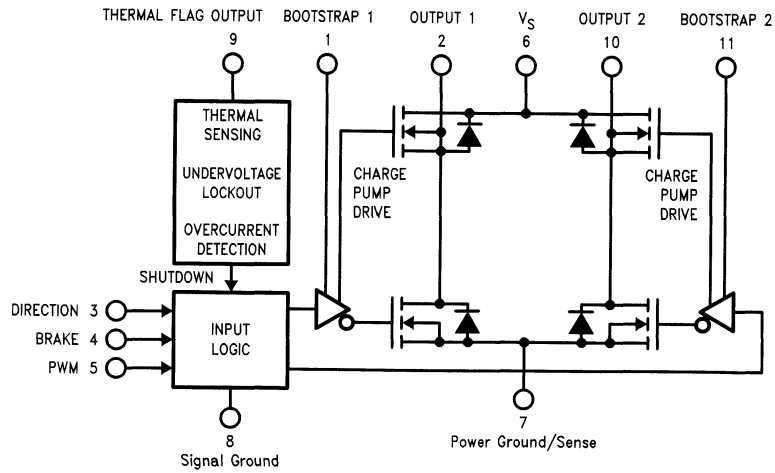
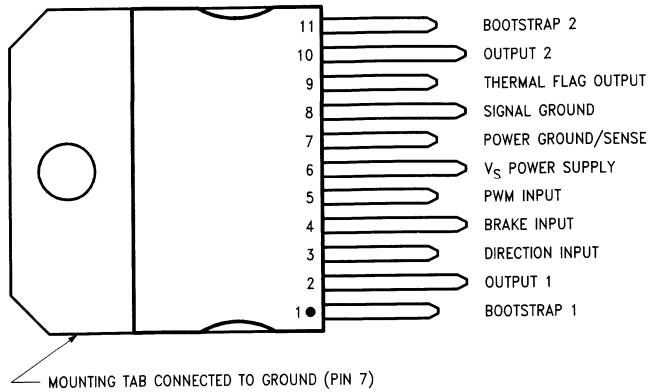


FIGURE 1. Functional Block Diagram of LMD18201

Connection Diagram and Ordering Information



DS010793-2

Top View
Order Number LMD18201T
See NS Package Number TA11B

National Semiconductor

LMD18245
3A, 55V DMOS Full-Bridge Motor Driver

General Description

The LMD18245 full-bridge power amplifier incorporates all the circuit blocks required to drive and control current in a brushed type DC motor or one phase of a bipolar stepper motor. The multi-technology process used to build the device combines bipolar and CMOS control and protection circuitry with DMOS power switches on the same monolithic structure. The LMD18245 controls the motor current via a fixed off-time chopper technique.

An all DMOS H-bridge power stage delivers continuous output currents up to 3A (6A peak) at supply voltages up to 55V. The DMOS power switches feature low $R_{DS(ON)}$ for high efficiency, and a diode intrinsic to the DMOS body structure eliminates the discrete diodes typically required to clamp bipolar power stages.

An innovative current sensing method eliminates the power loss associated with a sense resistor in series with the motor. A four-bit digital-to-analog converter (DAC) provides a digital path for controlling the motor current, and, by extension, simplifies implementation of full, half and microstep stepper motor drives. For higher resolution applications, an external DAC can be used.

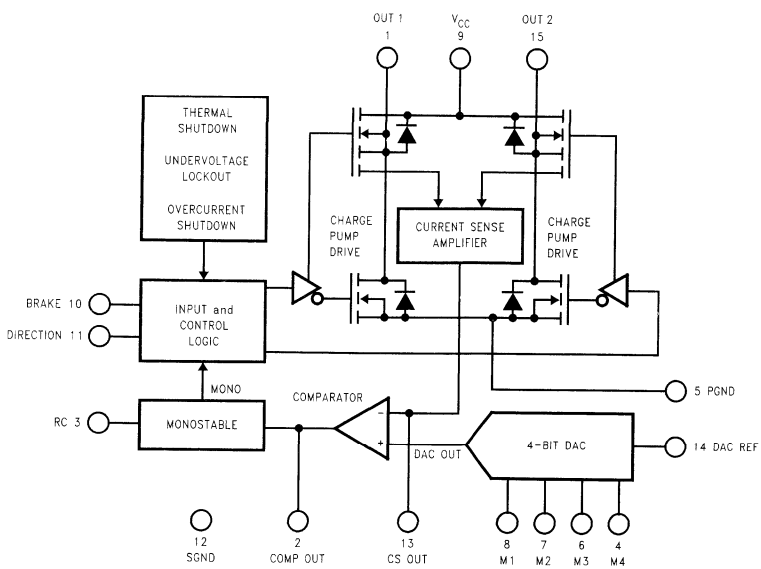
Features

- DMOS power stage rated at 55V and 3A continuous
- Low $R_{DS(ON)}$ of typically 0.3Ω per power switch
- Internal clamp diodes
- Low-loss current sensing method
- Digital or analog control of motor current
- TTL and CMOS compatible inputs
- Thermal shutdown (outputs off) at T_J = 155°C
- Overcurrent protection
- No shoot-through currents
- 15-lead TO-220 molded power package

Applications

- Full, half and microstep stepper motor drives
- Stepper motor and brushed DC motor servo drives
- Automated factory, medical and office equipment

Functional Block and Connection Diagram (15-Lead TO-220 Molded Power Package (T))



Order Number LMD18245T
See NS Package Number TA15A

National Semiconductor

LMD18400
Quad High Side Driver

General Description

The LMD18400 is a fully protected quad high side driver. It contains four common-drain DMOS N-channel power switches, each capable of switching a continuous 1 Amp load (>3 Amps transient) to a common positive power supply. The switches are fully protected from excessive voltage, current and temperature. An instantaneous power sensing circuit calculates the product of the voltage across and the current through each DMOS switch and limits the power to a safe level. The device can be disabled to produce a "sleep" condition reducing the supply current to less than 10 µA. Separate ON/OFF control of each switch is provided through standard LSTLL/CMOS logic compatible inputs.

A MICROWIRE™ compatible serial data interface is built in to provide extensive diagnostic information. This information includes switch status readback, output load fault conditions and thermal and overvoltage shutdown status. There are also two direct-output error flags to provide an immediate indication of a general system fault and an indication of excessive operating temperature.

The LMD18400 is packaged in a special power dissipating leadframe that reduces the junction to case thermal resistance to approximately 20°C/W.

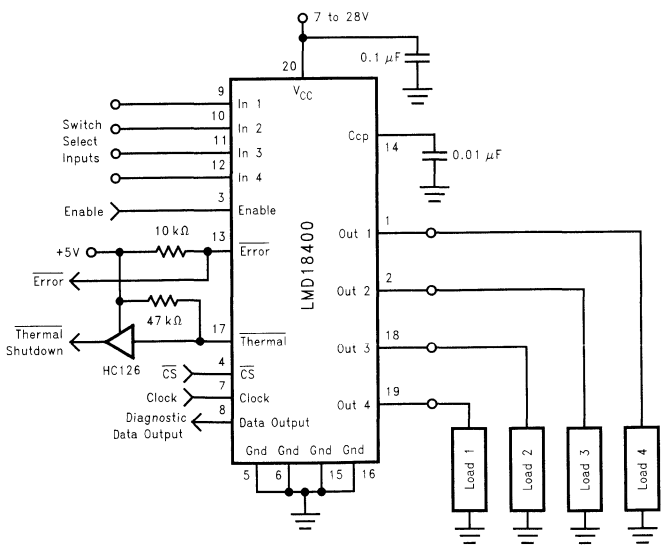
Features

- Four independent outputs with >3A peak, 1A continuous current capability
- 1.3Ω maximum ON resistance over temperature
- True instantaneous power limit for each switch
- High survival voltage (60 V_{DC}, 80V transient)
- Shorted load (to ground and supply) protection
- Overvoltage shutdown at V_{CC} > 35V
- LS TTL/CMOS compatible logic inputs and outputs
- <10 µA supply current in "sleep" mode
- −5V output clamp for discharging inductive loads
- Serial data interface for 11 diagnostic checks:
  - — Switch ON/OFF status
  - — Open or shorted load
  - — Operating temperature
  - — Excessive supply voltage
- Two direct-output error flags

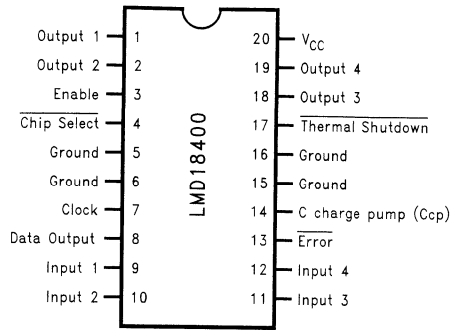
Applications

- Relay and solenoid drivers
- High impedance automotive fuel injector drivers
- Lamp drivers
- Power supply switching
- Motor drivers

Typical Application



Connection Diagram



01102602

Order Number LMD18400N
See NS Package Number N20A

National Semiconductor

Peripheral Drivers

National Semiconductor

DP8310/DP8311
Octal Latched Peripheral Drivers

General Description

The DP8310 and DP8311 Octal Latched Peripheral Drivers provide the function of latching eight bits of data with open collector outputs, each driving up to 100 mA DC with an operating voltage range of 30V. Both devices are designed for low input currents, high input/output voltages, and feature a power up clear (outputs off) function.

The DP8310 is positive edge latching. Two active low write/enable inputs are available for convenient data bussing without external gating.

The DP8311 is positive edge latching. The active low strobe input latches data or allows fall through operation when held at logic "0". The latches are cleared (outputs off) with a logic "0" on the clear pin.

Features

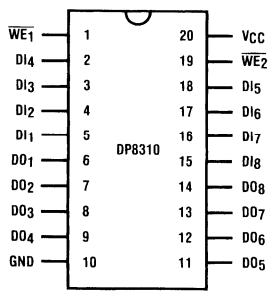
- High current, high voltage open collector outputs
- Low current, high voltage inputs
- All outputs simultaneously sink rated current "DC" with no thermal derating at maximum rated temperature
- Parallel latching or buffering
- Separate active low enables for easy data bussing
- Internal "glitch free" power up clear
- 10% V_{CC} tolerance

Applications

- High current high voltage drivers
- Relay drivers
- Lamp drivers
- LED drivers
- TRIAC drivers
- Solenoid drivers
- Stepper motor drivers
- Level translators
- Fiber-optic LED drivers

Connection Diagrams

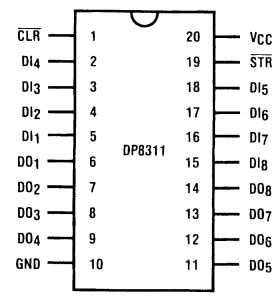
Dual-In-Line Package



DS005246-1

Top View

Dual-In-Line Package



DS005246-2

Top View

Order Number DP8310N or DP8311N
See NS Package Number N20A

National Semiconductor

DS0026
Dual High-Speed MOS Driver

General Description

DS0026 is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL outputs and converts them to MOS logic levels. The device may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 is intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

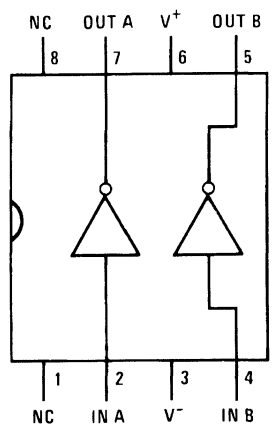
The DS0026 is designed to fulfill a wide variety of MOS interface requirements. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76.

Features

- Fast rise and fall times—20 ns 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

Connection Diagram (Top View)

Dual-In-Line Package



Order Number DS0026CN
See NS Package Number N08E

National Semiconductor

DS2003
High Current/Voltage Darlington Drivers

General Description

The DS2003 is comprised of seven high voltage, high current NPN Darlington transistor pairs. All units feature common emitter, open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads and appropriate emitter base resistors for leakage.

The DS2003 has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5.0V.

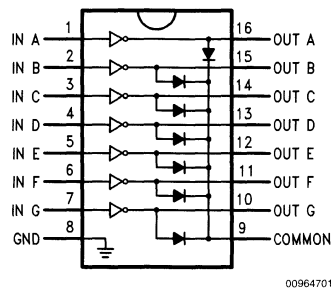
The DS2003 offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

Features

- Seven high gain Darlington pairs
- High output voltage (V_{CE} = 50V)
- High output current (I_C = 350 mA)
- TTL, PMOS, CMOS compatible
- Suppression diodes for inductive loads
- Extended temperature range

Connection Diagram

16-Lead DIP



Top View

Order Numbers

N Package Number N16E	M Package Number M16A
DS2003TN	DS2003TM
DS2003CN	DS2003CM

National Semiconductor

DS3658
Quad High Current Peripheral Driver

General Description

The DS3658 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. A unique input circuit combines TTL compatibility with high impedance. In fact, its extreme low input current allows it to be driven directly by a CMOS device.

The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch-up during turn off (inductive fly back protection—refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3658 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special cooper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

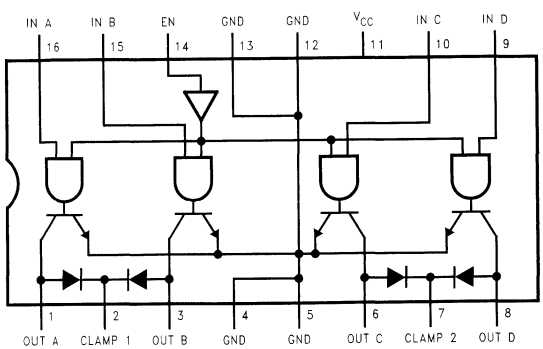
- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

Features

- Single saturated transistor outputs
- Low standby power, 10 mW typical
- High impedance TTL compatible inputs
- Outputs may be tied together for increased current capacity
- High output current
  — 600 mA per output
  — 2.4A per package
- No output latch-up at 35V
- Low output ON voltage (350 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly back protection
- NPN inputs for minimal input currents (1 μA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS3658N
See NS Package Number N16E

National Semiconductor

DS3668
Quad Fault Protected Peripheral Driver

General Description

The DS3668 quad peripheral driver is designed for those applications where low operating power, high breakdown voltage, high output current and low output ON voltage are required. Unlike most peripheral drivers available, a unique fault protected circuit is incorporated on each output. When the load current exceeds 1.0A (approximately) on any output for more than a built-in delay time, nominally 12 µs, that output will be shut off by its protection circuitry with no effect on other outputs. This condition will prevail until that protection circuitry is reset by toggling the corresponding input or the enable pin low for at least 1.0 µs. This built-in delay is provided to ensure that the protection circuitry is not triggered by turn-on surge currents associated with certain kinds of loads.

The DS3668's inputs combine TTL compatibility with high input impedance. In fact, its extreme low input current allows it to be driven directly by a MOS device. The outputs are capable of sinking 600 mA each and offer a 70V breakdown. However, for inductive loads the output should be clamped to 35V or less to avoid latch up during turn off (inductive fly-back protection — refer AN-213). An on-chip clamp diode capable of handling 800 mA is provided at each output for this purpose. In addition, the DS3668 incorporates circuitry that guarantees glitch-free power up or down operation and a fail-safe feature which puts the output in a high impedance state when the input is open.

The molded package is specifically constructed to allow increased power dissipation over conventional packages. The four ground pins are directly connected to the device chip with a special copper lead frame. When the quad driver is soldered into a PC board, the power rating of the device improves significantly.

Applications

- Relay drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Level translators
- Fiber optic LED drivers

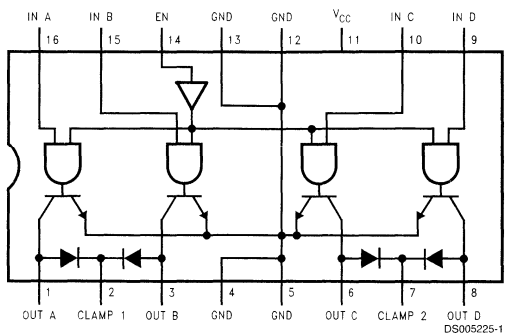
Features

- Output fault protection
- High impedance TTL compatible inputs
- High output current—600 mA per output
- No output latch-up at 35V
- Low output ON voltage (550 mV typ @ 600 mA)
- High breakdown voltage (70V)
- Open collector outputs
- Output clamp diodes for inductive fly-back protection
- NPN inputs for minimal input currents (1 µA typical)
- Low operating power
- Standard 5V power supply
- Power up/down protection
- Fail-safe operation
- 2W power package
- Pin-for-pin compatible with SN75437

11

Connection Diagram

Dual-In-Line Package



Top View
Order Number DS3668N
See NS Package Number N16E

Truth Table

IN	EN	OUT
H	H	L
L	H	Z
H	L	Z
L	L	Z

H = High state
L = Low state
Z = High impedance state

National Semiconductor

DS3680
Quad Negative Voltage Relay Driver

General Description

The DS3680 is a quad high voltage negative relay driver designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA sink capability. These drivers are intended for switching the ground end of loads which are directly connected to the negative supply, such as in telephone relay systems.

Since there may be considerable noise and IR drop between logic ground and negative supply ground in many applications, these drivers are designed to operate with a high common-mode range (±20V referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which permits input signals from more than one element of the system.

With low differential input current requirements (typically 100 µA), these drivers are compatible with TTL, LS and CMOS logic. Differential inputs permit either inverting or non-inverting operation.

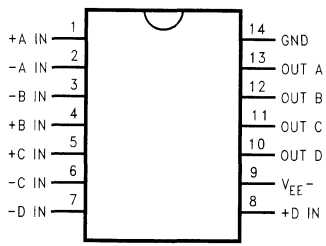
The driver outputs incorporate transient suppression clamp networks, which eliminate the need for external networks when used in applications of switching inductive loads. A fail-safe feature is incorporated to ensure that, if the + IN input or both inputs are open, the driver will be OFF.

Features

- −10V to −60V operation
- Quad 50 mA sink capability
- TTL/LS/CMOS or voltage comparator input
- High input common-mode voltage range
- Very low input current
- Fail-safe disconnect feature
- Built-in output clamp diode

Connection Diagram

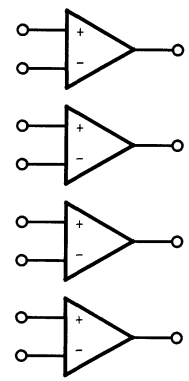
Dual-In-Line Package



00582101

Top View
Order Number DS3680J, DS3680M or DS3680N
See NS Package Number J14A, M14A, N14A

Logic Diagram



00582102

Truth Table

Differential Inputs	Outputs
$V_{ID} \geq 2V$	On
$V_{ID} \leq 0.8V$	Off
Open	Off

National Semiconductor

DS75451/2/3
Series Dual Peripheral Drivers

General Description

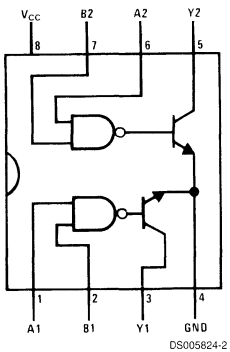
The DS7545X series of dual peripheral drivers is a family of versatile devices designed for use in systems that use TTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

The DS75451, DS75452 and DS75453 are dual peripheral AND, NAND and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

Features

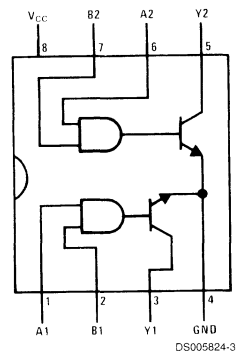
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

Connection Diagrams (Dual-In-Line and Metal Can Packages)



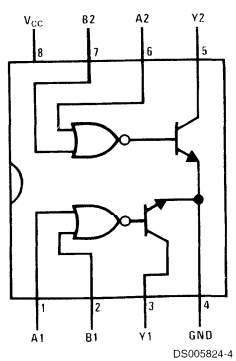
*See (Note 5) and Appendix E regarding S.O. package power dissipation constraints.

Top View
Order Number DS75451M or DS75451N



Top View
Order Number DS75452M or DS75452N

See NS Package Numbers M08A* or N08E



*See (Note 5) and Appendix E regarding S.O. package power dissipation constraints.

Top View
Order Number DS75453M or DS75453N

See NS Package Numbers M08A* or N08E

National Semiconductor

Universal Serial Bus

National Semiconductor

Universal Serial Bus Products Selection Guide

Part Number	Channels	Switch On-Resistance (mΩ, typ.)	Supply Current, Switches ON (µA, typ.)	Supply Current, Switches OFF (µA, max.)	Input Voltage V (Min)	Input Voltage V (Max)	Output Current - Max per Channel (mA)
LM3525	Single	80	65	1	2.7	5.5	500
LM3526	Dual	100	115	1	2.7	5.5	500
LM3543	Triple	90	375	1	2.7	5.5	500
LM3544	Quad	90	375	1	2.7	5.5	500

National Semiconductor

LM3525
Single Port USB Power Switch and Over-Current Protection

General Description

The LM3525 provides Universal Serial Bus standard power switch and over-current protection for all host port applications. The single port device is ideal for Notebook PC and Handheld PC applications that supply power to one port.

A 1 ms delay on fault flag output prevents erroneous over-current reporting caused by inrush currents during the hot-plug events.

The LM3525 accepts an input voltage between 2.7V and 5.5V allowing use as a device-based inrush current limiter for 3.3V USB peripherals, as well as Root and Self-Powered Hubs at 5.5V. The Enable input accepts both 3.3V and 5.0V logic thresholds.

The small size, low R_{ON}, and 1 ms fault flag delay make the LM3525 a good choice for root hubs as well as ganged power control in space-critical self-powered hubs.

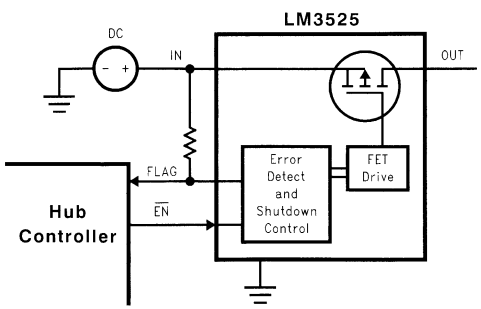
Features

- 1 ms Fault Flag Delay During Hot-Plug Events
- Smooth Turn-On Eliminates Inrush Induced Voltage Drop
- UL Recognized Component: REF # 205202
- 1A Nominal Short Circuit Output Current Protects Notebook PC Power Supplies
- Thermal Shutdown Protects Device in Direct Short Condition
- 500mA Minimum Continuous Load Current
- Small SO-8 Package Minimizes Board Space
- 2.7V to 5.5V Input Voltage Range
- Switch Resistance ≤ 120 mΩ Max. at V_{IN} = 5V
- 1µA Max Standby Current
- 100 µA Max Operating Current
- Undervoltage Lockout (UVLO)

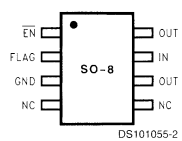
Applications

- Universal Serial Bus (USB) Root Hubs including Desktop and Notebook PC
- USB Monitor Hubs
- Other Self-Powered USB Hub Devices
- High Power USB Devices Requiring Inrush Limiting
- General Purpose High Side Switch Applications

Typical Operating Circuit and Connection Diagram



DS101055-1

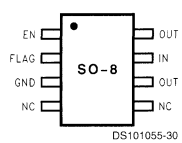


DS101055-2

LM3525M-L

UL Recognized Component

DS101055-31



DS101055-30

LM3525M-H

Ordering Information

Part Number	Enable, Delivery Option	Package Type
LM3525M-H	Active High Enable, 95 units per rail	SO-8, NS Package Number M08A
LM3525M-L	Active Low Enable, 95 units per rail	
LM3525MX-H	Active High Enable, 2500 units per reel	
LM3525MX-L	Active Low Enable, 2500 units per reel	

National Semiconductor

LM3526
Dual Port USB Power Switch and Over-Current Protection

General Description

The LM3526 provides Universal Serial Bus standard power switch and over-current protection for all host port applications. The dual port device is ideal for Notebook and desktop PC's that supply power to more than one port.

A 1 ms delay on the fault flag output prevents erroneous overcurrent reporting caused by in-rush currents during hot-plug events.

The dual stage thermal protection circuit in the LM3526 provides individual protection to each switch and the entire device. In a short-circuit/over-current event, the switch dissipating excessive heat is turned off, allowing the second switch to continue to function uninterrupted.

The LM3526 accepts an input voltage between 2.7V and 5.5V allowing use as a device-based in-rush current limiter for 3.3V USB peripherals, as well as Root and Self-Powered Hubs at 5.5V. The Enable inputs accept both 3.3V and 5.0V logic thresholds.

The small size, low R_{ON}, and 1 ms fault flag delay make the LM3526 a good choice for root hubs as well as per-port power control in embedded and stand-alone hubs.

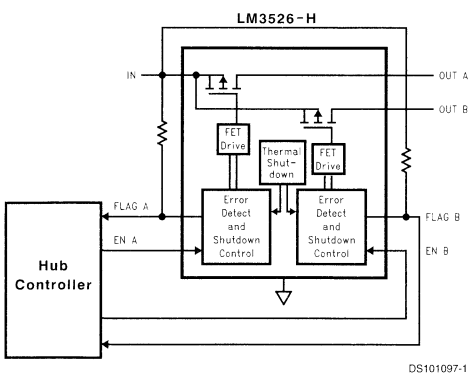
Features

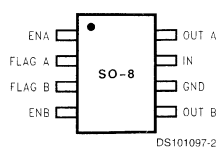
- 1 ms fault flag delay filters Hot-Plug events
- Smooth turn-on eliminates in-rush induced voltage drop
- UL recognized component: REF# 205202
- 1A nominal short circuit output current protects PC power supplies
- Thermal shutdown protects device in direct short condition
- 500mA minimum continuous load current
- Small SO-8 package minimizes board space
- 2.7V to 5.5V input voltage range
- 140 mΩ Max. switch resistance
- 1 µA Max. standby current
- 200 µA Max. operating current
- Under-voltage lockout (UVLO)

Applications

- Universal Serial Bus (USB) Root Hubs including Desktop and Notebook PC
- USB Monitor Hubs
- Other Self-Powered USB Hub Devices
- High Power USB Devices Requiring In-rush Limiting
- General Purpose High Side Switch Applications

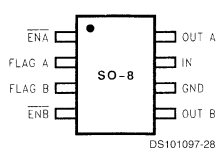
Typical Operating Circuit and Connection Diagram





LM3526-H

UL Recognized Component
DS101097-40



LM3526-L

Ordering Information

Part Number	Enable, Delivery Option	Package Type
LM3526M-H	Active High Enable, 95 units per rail	SO-8, NS Package Number M08A
LM3526M-L	Active Low Enable, 95 units per rail	
LM3526MX-H	Active High Enable, 2500 units per reel	
LM3526MX-L	Active Low Enable, 2500 units per reel	

National Semiconductor

LM3543
Triple Port USB Power Distribution Switch and Over-Current Protection

General Description

The LM3543 is a triple high-side power switch that is an excellent choice for use in Root, Self-Powered and Bus-Powered USB (Universal Serial Bus) Hubs. Independent port enables, flag signals to alert USB controllers of error conditions, controlled start-up in hot-plug events, and short circuit protection all satisfy USB requirements.

The LM3543 accepts input voltages between 2.7V and 5.5V. The Enable logic inputs, available in active-high and active-low versions, can be powered off any voltage in the 2.7V to 5.5V range. The LM3543 limits the continuous current through a single port to 1.25A (max.) when it is shorted to ground.

The low on-state resistance of the LM3543 switches ensures the LM3543 will satisfy USB voltage drop requirements, even when current through a switch reaches 500 mA. Thus, High-Powered USB Functions, Low-Powered USB Functions, and Bus-Powered USB Hubs can all be powered off a Root or Self-Powered USB Hub containing the LM3543.

Added features of the LM3543 include current foldback to reduce power consumption in current overload conditions, thermal shutdown to prevent device failure caused by high-current overheating, and undervoltage lockout to keep switches from operating if the input voltage is below acceptable levels.

Features

- 90mΩ (typ.) High-Side MOSFET Switch
- 500mA Continuous Current per Port
- 7 ms Fault Flag Delay Filters Hot-Plug Events
- Industry Standard Pin Order
- Short Circuit Protection with Power-Saving Current Foldback
- Thermal Shutdown Protection
- Undervoltage Lockout
- Recognized by UL and Nemko
- Input Voltage Range: 2.7V to 5.5V
- 5 µA Maximum Standby Supply Current
- 16-Pin SOIC Package
- Ambient Temperature Range: −40°C to 85°C

Applications

- USB Root, Self-Powered, and Bus-Powered Hubs
- USB Devices such as Monitors and Printers
- General Purpose High Side Switch Applications

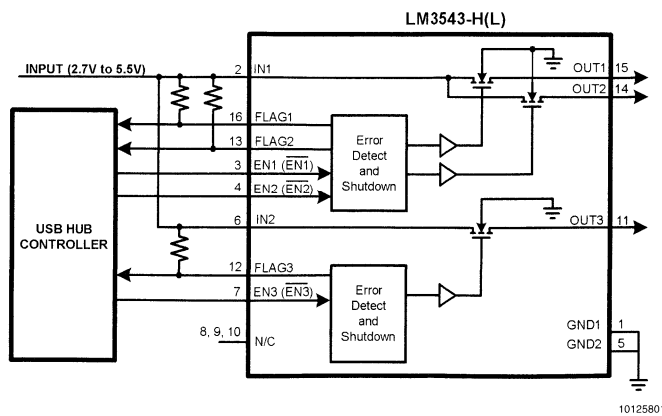
UL Recognized Component

10125832

10125833

11

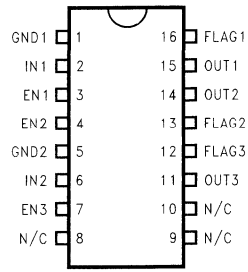
Functional Diagram



10125801

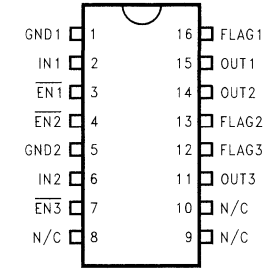
Connection Diagrams

LM3543-H
16-Pin SOIC



Top View

LM3543-L
16-Pin SOIC



Top View

Ordering Information

Part Number	Enable, Delivery Option	Package Type
LM3543M-H	Active High Enable	SO-16 NS Package Number M16A
LM3543M-L	Active Low Enable	
LM3543MX-H	Active High Enable, 2500 units per reel	
LM3543MX-L	Active Low Enable, 2500 units per reel	

Typical Application Circuit

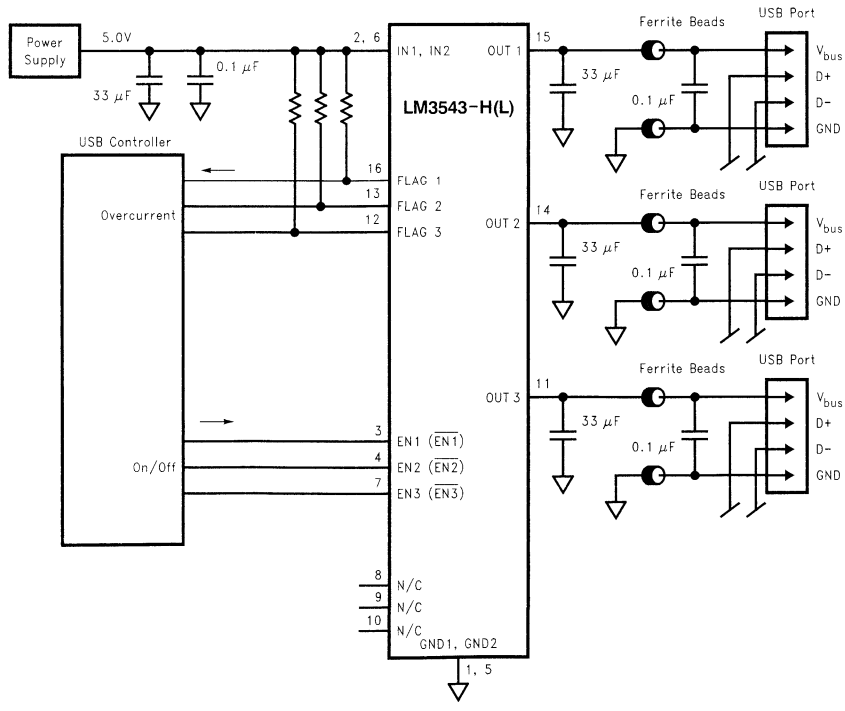


FIGURE 1. The LM3543 used in a Self-Powered or Root USB Hub

National Semiconductor

LM3544
Quad Port USB Power Distribution Switch and Over-Current Protection

General Description

The LM3544 is a quad high-side power switch that is an excellent choice for use in Root, Self-Powered and Bus-Powered USB (Universal Serial Bus) Hubs. Independent port enables, flag signals to alert USB controllers of error conditions, controlled start-up in hot-plug events, and short circuit protection all satisfy USB requirements.

The LM3544 accepts input voltages between 2.7V and 5.5V. The Enable logic inputs, available in active-high and active-low versions, can be powered off any voltage in the 2.7V to 5.5V range. The LM3544 limits the continuous current through a single port to 1.25A (max.) when it is shorted to ground.

The low on-state resistance of the LM3544 switches ensures the LM3544 will satisfy USB voltage drop requirements, even when current through a switch reaches 500 mA. Thus, High-Powered USB Functions, Low-Powered USB functions, and Bus-Powered USB Hubs can all be powered off a Root or Self-Powered USB Hub containing the LM3544.

Added features of the LM3544 include current foldback to reduce power consumption in current overload conditions, thermal shutdown to prevent device failure caused by high-current overheating, and undervoltage lockout to keep switches from operating if the input voltage is below acceptable levels.

Features

- 90mΩ (typ.) High-Side MOSFET Switch
- 500mA Continuous Current per Port
- 7 ms Fault Flag Delay Filters Hot-Plug Events
- Industry Standard Pin Order
- Short Circuit Protection with Power-Saving Current Foldback
- Thermal Shutdown Protection
- Undervoltage Lockout
- Recognized by UL and Nemko CB
- Input Voltage Range: 2.7V to 5.5V
- 5µA Maximum Standby Supply Current
- 16-Pin SOIC Package
- Ambient Temperature Range: −40°C to 85°C

Applications

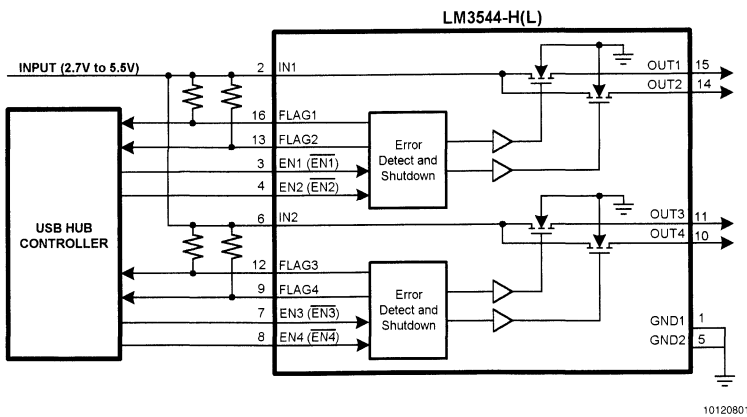
- USB Root, Self-Powered, and Bus-Powered Hubs
- USB Devices such as Monitors and Printers
- General Purpose High Side Switch Applications

UL Recognized Component

10120832

10120833

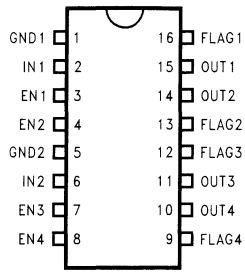
Functional Diagram



10120801

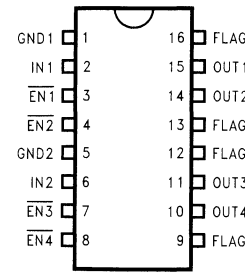
Connection Diagrams

LM3544-H
16-Pin SOIC



Top View

LM3544-L
16-Pin SOIC



Top View

Ordering Information

Part Number	Enable, Delivery Option	Package Type
LM3544M-H	Active High Enable	SO-16 NS Package Number M16A
LM3544M-L	Active Low Enable	
LM3544MX-H	Active High Enable, 2500 units per reel	
LM3544MX-L	Active Low Enable, 2500 units per reel	

Typical Application Circuit

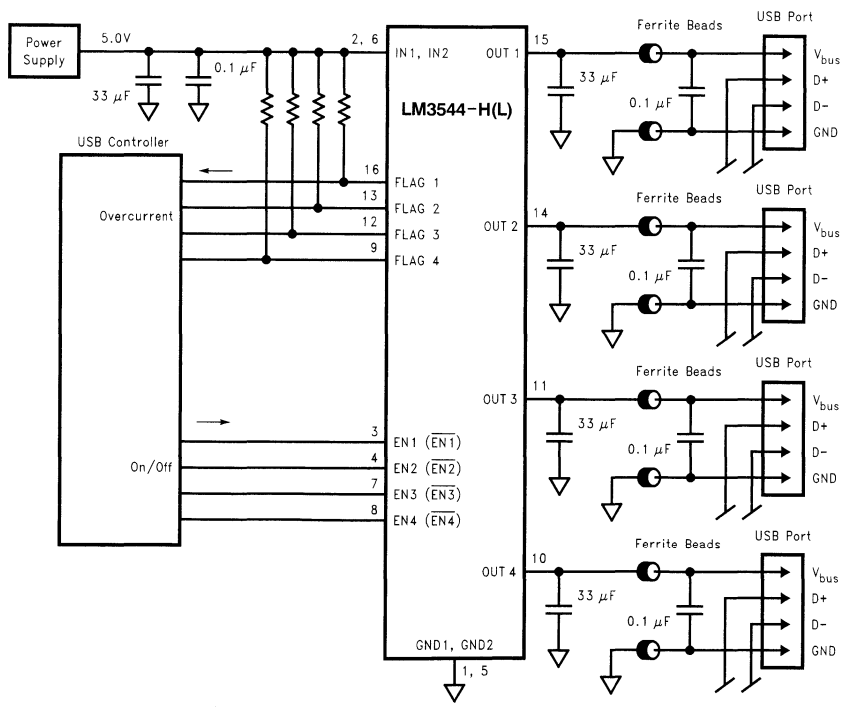


FIGURE 1. The LM3544 used in a Self-Powered or Root USB Hub

Section 12
Supervisory Circuits

Section 12 Contents

National Semiconductor

Voltage Control and Supervisor Products Selection Guide

VOLTAGE CONTROL PRODUCTS

Part Number	Function	Input Range (V)	Output	Features	Package (Note 1)
LM3411	Power Supply Feedback	3.3, 5	Current for control of regulator (20mA to 15mA)	1% & 0.5% tolerances. Custom voltages available (3V to 17V)	M5, N8
LM3420	Charge Control for 1, 2, 3, 4, or 5 Li-Ion Cells	4.2, 8.2, 8.4, 12.6, 16.8	Current for control of charger (20mA to 15mA)	1% & 0.5% tolerances	M5
LM3460 (Note 2)	GTL, GTLp Bus Control	1.2, 1.5	Current for control of regulator (up to 15mA)	1% tolerance.	M5
LM3620 (Note 2)	Charge Control for 1 or 2 Li-Ion Cells	4 to 30	Current for control of charger (up to 15mA)	1.2% tolerance, selectable battery type	M5
LM3621 (Note 2)	Full-Function Charge Controller for 1 Li-Ion Cell	3.0 to 5.5	Analog control of constant-current constant-voltage charger	0.5% tolerance, selectable battery type	M16
LM3622(Note 2)	Charge Control for 1 or 2 Li-Ion Cells	4.5 to 20	Analog control of CVCC charger	0.7% & 1.2% tolerance.	M8
LM3647 (Note 2)	High precision, Fast Charger for 2-8 NiMH, NiCD Cells or 1-4 Li-Ion Cells	1.0 to 20	Li-Ion: constant-current constant-voltage charge NiMH, NiCD: $-\Delta V$ charge termination	Selectable battery type, 4 charge stages plus fault detection	M20

CURRENT GAUGE PRODUCTS

Part Number	Function	Input Range	Output	Features	Package (Note 1)
LM3812-1.0	High-Side Precision Current Gauge	up to 1A	PWM with duty cycle proportional to input current	Sampling interval of 50ms for 4% tolerance.	M8
LM3812-7.0	High-Side Precision Current Gauge	up to 7A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 50ms for 6% tolerance.	M8
LM3813-1.0	Low-Side Precision Current Gauge	up to 1A	PWM with duty cycle proportional to input current	Sampling interval of 50ms for 4% tolerance.	M8
LM3813-7.0	Low-Side Precision Current Gauge	up to 7A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 50ms for 6% tolerance.	M8
LM3814-1.0	High-Side Fast Current Gauge	up to 1A	PWM with duty cycle proportional to input current	Sampling interval of 6ms for 5.5% tolerance.	M8

CURRENT GAUGE PRODUCTS (Continued)

Part Number	Function	Input Range	Output	Features	Package (Note 1)
LM3814-7.0	High-Side Fast Current Gauge	up to 7A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 6ms for 8.5% tolerance.	M8
LM3815-1.0	Low-Side Fast Current Gauge	up to 1A	PWM with duty cycle proportional to input current	Sampling interval of 6ms for 5.5% tolerance.	M8
LM3815-7.0	Low-Side Fast Current Gauge	up to 7A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 6ms for 8.5% tolerance.	M8
LM3822-1.0	High-Side Precision Current Gauge	up to 1A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 50ms for 4% tolerance.	M8
LM3822-2.0	High-Side Precision Current Gauge	up to 2A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 50ms for 4% tolerance.	M8
LM3824-1.0	High-Side Precision Current Gauge	up to 1A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 6ms for 6% tolerance.	M8
LM3822-2.0	High-Side Precision Current Gauge	up to 2A (10A peak)	PWM with duty cycle proportional to input current	Sampling interval of 6ms for 6% tolerance.	M8

POWER SUPPLY SUPERVISOR PRODUCTS

Part Number	Function	Input Range or Threshold	Output	Features	Package
LM809	Power-on Reset	2.63, 2.93, 3.08, 4.00, 4.38, 4.63V	Reset Flag	Active Low $\overline{\text{RESET}}$ Output	M3
LM810	Power-on Reset	2.63, 2.93, 3.08, 4.00, 4.38, 4.63V	Reset Flag	Active High RESET Output	M3
LM2601	External Charger Power Source Detector for Portable Computer	5V - 24V	Logic Flags	Adapter Present and Charger Present Logic Outputs to Inform CPU of Proper Bus Power Configuration	TSSOP-14
LM3700	Active Low	3.08V (Note 3)		Selectable timeout, low line output	BP
LM3701	Active High	3.08V (Note 3)		Selectable timeout, low line output	BP
LM3702	Active Low	3.08V (Note 3)		LM3700 plus manual reset	BP
LM3703	Active High	3.08V (Note 3)		LM3701 plus manual reset	BP
LM3704	Active Low	3.08V (Note 3)		LM3701 plus power fail comparator	BP, MM
LM3705	Active High	3.08V (Note 3)		LM3703 plus power fail comparator	BP, MM
LM3706	Active Low	3.08V (Note 3)		LM3700 plus Watchdog	BP
LM3707	Active High	3.08V (Note 3)		LM3701 plus Watchdog	BP
LM3708	Active Low	3.08V (Note 3)		LM3702 plus Watchdog	BP
LM3709	Active High	3.08V (Note 3)		LM3703 plus Watchdog	BP
LM3710	Active Low	3.08V (Note 3)		LM3708 plus power fail comparator	BP, MM

POWER SUPPLY SUPERVISOR PRODUCTS (Continued)

Part Number	Function	Input Range or Threshold	Output	Features	Package
LM3711	Active High	3.08V (Note 3)		LM3709 plus power fail comparator	BP, MM
LM3712	Active Low	3.08V (Note 3)		LM3710 without low line output	BP
LM3713	Active High	3.08V (Note 3)		LM3711 without low line output	BP
LM3722	Active Low	2.32, 3.08, 4.63V (Note 3)		Manual reset, push-pull output	M5
LM3723	Active High	2.32, 3.08, 4.63V (Note 3)		Manual reset, push-pull output	M5
LM3724	Active High	2.32, 3.08, 4.63V (Note 3)		Manual reset, open-drain output	M5
LMC6953	PCI Local Bus Supervisor	1.5-6, 3.3, 5V (Note 3)	Reset Flag	Power-on reset with adjustable delay.	M8
LP3470	Power-on Reset	2.63, 2.93, 3.08, 4.00, 4.38, 4.63V (Note 3)	Reset Flag	Adjustable delay. Custom voltages available (2.4V-5.0V)	M5
MCP809	Power-on Reset	2.63, 2.93, 3.08, 4.00, 4.38, 4.63V	Reset Flag	Active Low $\overline{\text{RESET}}$ Output	M3
MCP810	Power-on Reset	2.63, 2.93, 3.08, 4.00, 4.38, 4.63V	Reset Flag	Active High RESET Output	M3

Note 1: Package designation includes number of pins:

BP = micro SMD

M = plastic surface-mount

MM = MSOP-8

M3 = 3 Lead SOT-23

M5 = 5 Lead SOT-23

N = plastic dual-in-line

TSSOP-14 = 14-Lead Thin Shrink Small-Outline Package

Note 2: Refer to the Low Dropout Linear Voltage Regulators for product data for the LM3460 voltage controller.

Note 3: For additional voltage options contact National Semiconductor.

National Semiconductor

LM2601
Adapter Interface Circuit

General Description

The Adapter Interface Circuit (AIC) is used to sense the presence of an external power source for a portable computer. It notifies the computer if a source is present and indicates if the source is appropriate for charging battery packs inside the computer. The AIC also senses an adapter current and its direction. AIC isolates the adapter and signals the computer when peak current threshold is exceeded.

LM2601 drives P-channel FETs. No high current rated Schottky diode is required to implement an adapter switchover circuit. This significantly decreases additional heat dissipation during simultaneous fast battery charging while running a computer, particularly in Maximum Performance mode of operation

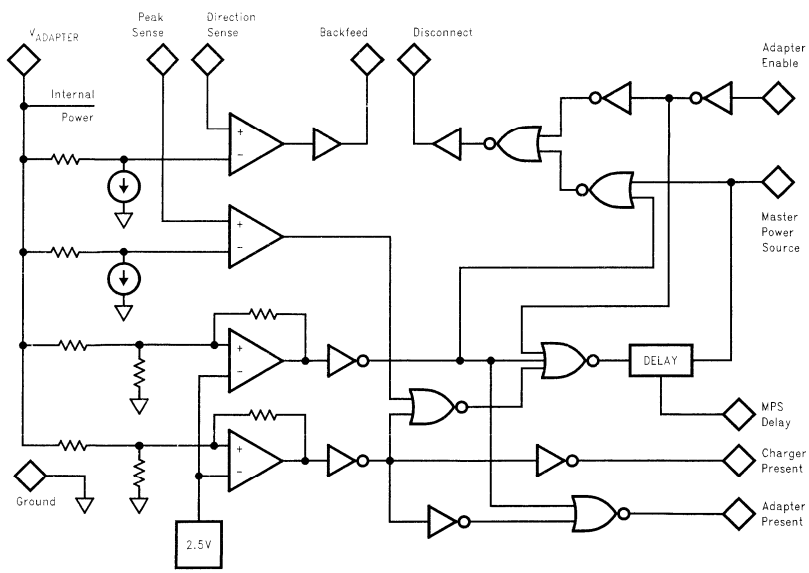
Features

- Detects an AC-DC adapter suitable for battery charging or an airplane or car power line adapter that should not be used for battery charging
- Allows the implementation of intelligent switchover circuits for portable systems
- LM2601 shuts down automatically when adapter is removed
- Low leakage current from battery when not powered
- Drives P-channel FETs, no Schottky diodes are required
- No reverse inrush current from battery into the adapter output capacitance
- Allows for battery capacity gas-gauge calibration under system software/firmware control
- Adapter over current threshold programmable with external resistors
- Wide input range: 5V - 24V
- Available in TSSOP-14 package

Applications

- Portable Computers
- Portable IAs (Internet Appliances, Information Appliances)
- Other Battery Powered Devices

Block Diagram



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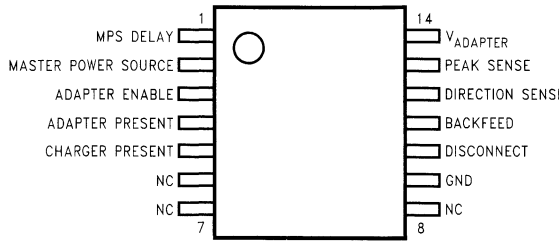
Pin Configuration

TSSOP-14



10130902

Ordering Information

Order Number	Package Number	Package Type	Supplied As*
LM2601MTC	MTC14	TSSOP-14	Rail (94 Units/Rail)
LM2601MTCX	MTC14	TSSOP-14	Tape and Reel (2500 Units/Reel)

* Partial Rails are available, there is no minimum order quantity. Tape and Reel is supplied as full reels only.

Pin Description

Pin No.	Name	Function
1	MPS DELAY	A capacitor between this pin and ground sets the delay of the MPS risetime. See MPS DELAY description in Typical Application section.
2	MASTER POWER SOURCE	Bi-directional logic pin. If driven high by an external source, indicates that a battery is powering the power bus. If driven high by the AIC, indicates the adapter is powering the bus. AIC cannot drive MPS low. If there is no valid adapter voltage present, the pin is not an output but a high impedance logic input. The input is pulled-down via an internal 40k resistor.
3	ADAPTER ENABLE	Logic input pin. Active high. Grants permission to the adapter to drive both the power bus and the MPS signal.
4	ADAPTER PRESENT	Logic output pin. High when 12 volts < $V_{ADAPTER}$ < 17 volts. The output typically has 40k pull-down resistor. The source current is not internally limited and the part can be damaged if the output is shorted to ground when driven HIGH.
5	CHARGER PRESENT	Logic output pin. High when $V_{ADAPTER}$ > 17 volts. The output typically has 40k pull-down resistor. The source current is not internally limited and the part can be damaged if the output is shorted to ground when driven HIGH.
9	GND	IC ground pin.
10	DISCONNECT	Drives the gate of the disconnect P-ch FET.
11	BACKFEED	Drives the gate of the backfeed P-ch FET.
12	DIRECTION SENSE	Connection for current sense resistor to control BACKFEED.
13	PEAK SENSE	Connection for current sense resistor to control DISCONNECT.
14	$V_{ADAPTER}$	Power input pin. Output of AC adapter, auto adapter or airline adapter.

National Semiconductor

LM3700/LM3701
Microprocessor Supervisory Circuit with Low Line Output

General Description

The LM3700/LM3701 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3700/LM3701 series are available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

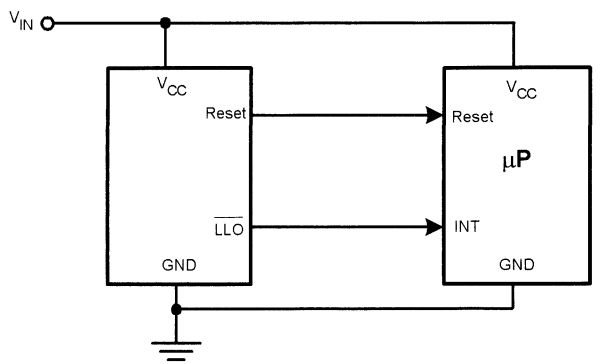
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- $\overline{\text{RESET}}$ (LM3700) or RESET (LM3701) outputs
- Precision supply voltage monitor
- Factory programmable Reset Timeout Delay
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

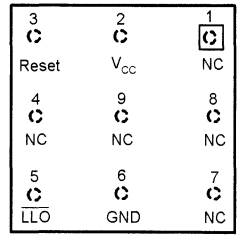
Typical Application



20011403

Connection Diagram

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

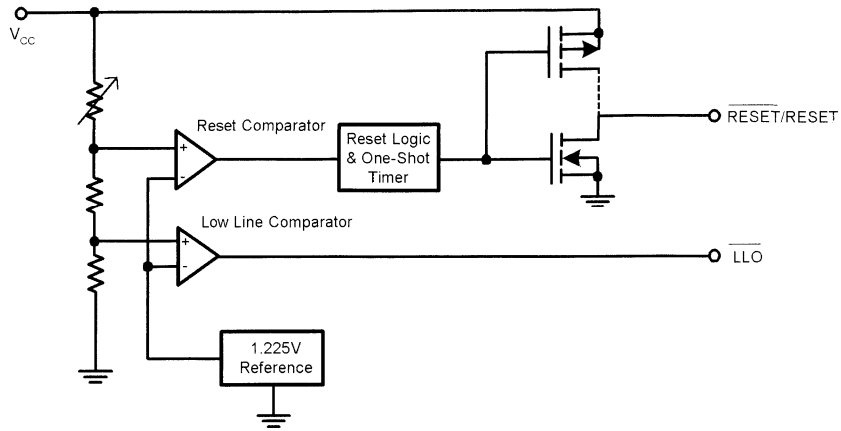


20011401

Pin Descriptions

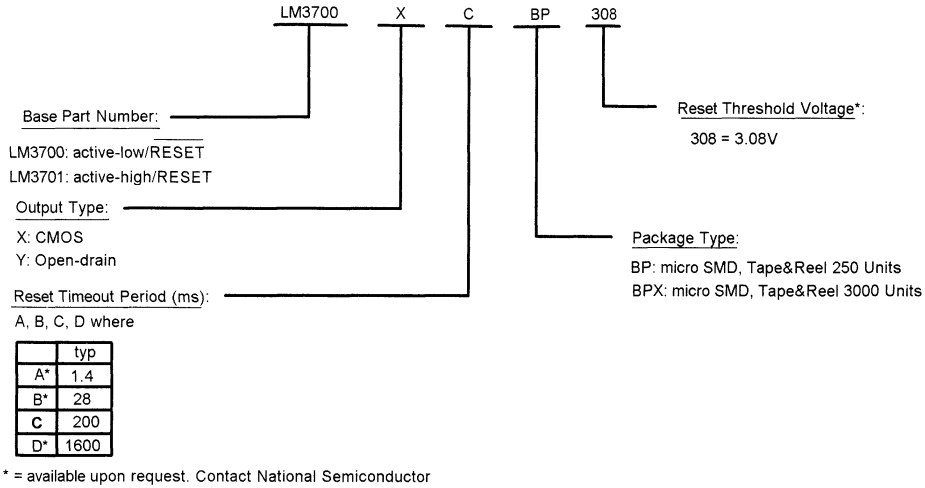
Bump No.	Name	Function
2	V_{CC}	Power Supply input.
3	$\overline{\text{RESET}}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3700 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{\text{RESET}}$ (LM3701 only).
5	$\overline{\text{LLO}}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
6	GND	Ground reference for all signals.
1, 4, 7, 8	NC	No Connect.
9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram



20011405

Ordering Information



	typ
A*	1.4
B*	28
C	200
D*	1600

* = available upon request. Contact National Semiconductor

20011404

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3700/LM3701

Part Number	Output	Reset Timeout Period	Package Marking
LM3700XCBP-308	totem-pole	200ms	%%I0
LM3700XCBPX-308	totem-pole	200ms	%%I0
LM3701XCBP-308	totem-pole	200ms	%%I1
LM3701XCBPX-308	totem-pole	200ms	%%I1

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Low Line Output
LM3700	x		X, Y*	Customized	x
LM3701		x	X	Customized	x

* = available upon request. Contact National

National Semiconductor

LM3702/LM3703
Microprocessor Supervisory Circuits with Low Line Output and Manual Reset

General Description

The LM3702/LM3703 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3702/LM3703 series are available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

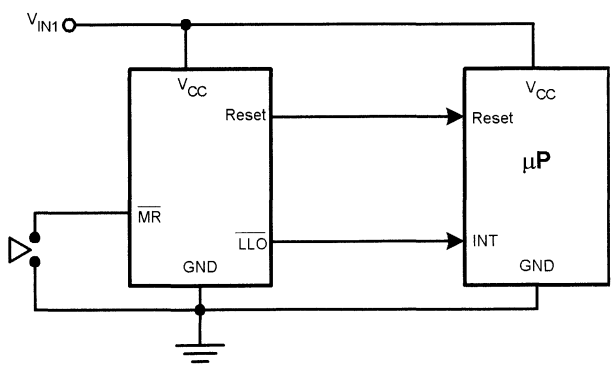
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ (LM3702) or RESET (LM3703) outputs
- Precision supply voltage monitor
- Factory programmable Reset Timeout Delay
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

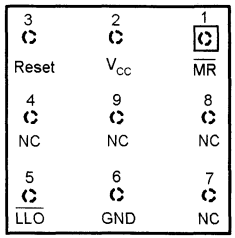
Typical Application



20011503

Connection Diagram

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

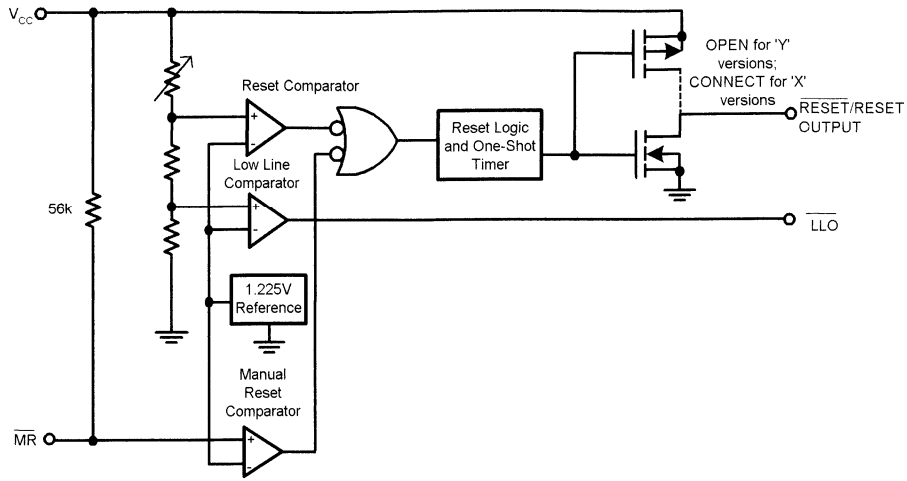


20011501

Pin Descriptions

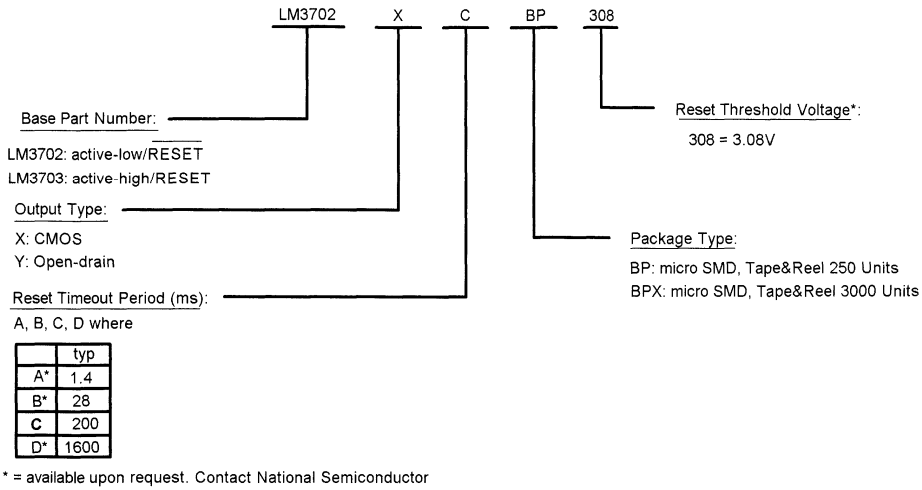
Bump No.	Name	Function
1	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
2	V_{CC}	Power Supply input.
3	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3702 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3703 only).
5	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
6	GND	Ground reference for all signals.
4, 7, 8	NC	No Connect.
9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram



20011505

Ordering Information



20011504

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3702/LM3703

Part Number	Output	Reset Timeout Period	Package Marking
LM3702XCBP-308	totem-pole	200ms	%%I2
LM3702XCBPX-308	totem-pole	200ms	%%I2
LM3703XCBP-308	totem-pole	200ms	%%I3
LM3703XCBPX-308	totem-pole	200ms	%%I3

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Manual Reset	Low Line Output
LM3702	x		X, Y*	Customized	x	x
LM3703		x	X	Customized	x	x

* = available upon request. Contact National

12

National Semiconductor

LM3704/LM3705
Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output and Manual Reset

General Description

The LM3704/LM3705 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3704/LM3705 series are available in MSOP-10 and 9-bump micro SMD packages.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

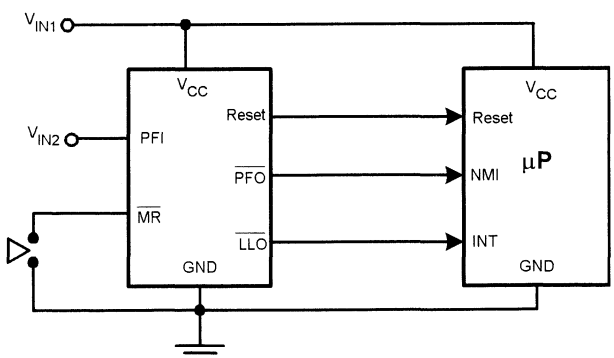
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ (LM3704) or RESET (LM3705) outputs
- Precision supply voltage monitor
- Factory programmable Reset Timeout Delay
- Separate Power Fail comparator
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

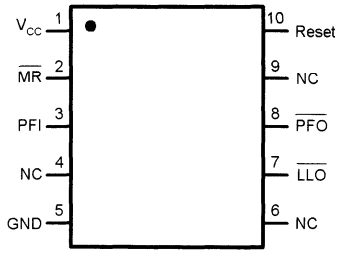
Typical Application



10136903

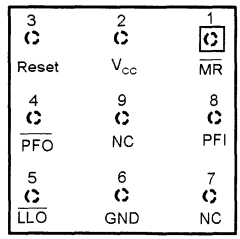
Connection Diagrams

MSOP-10



10136902

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

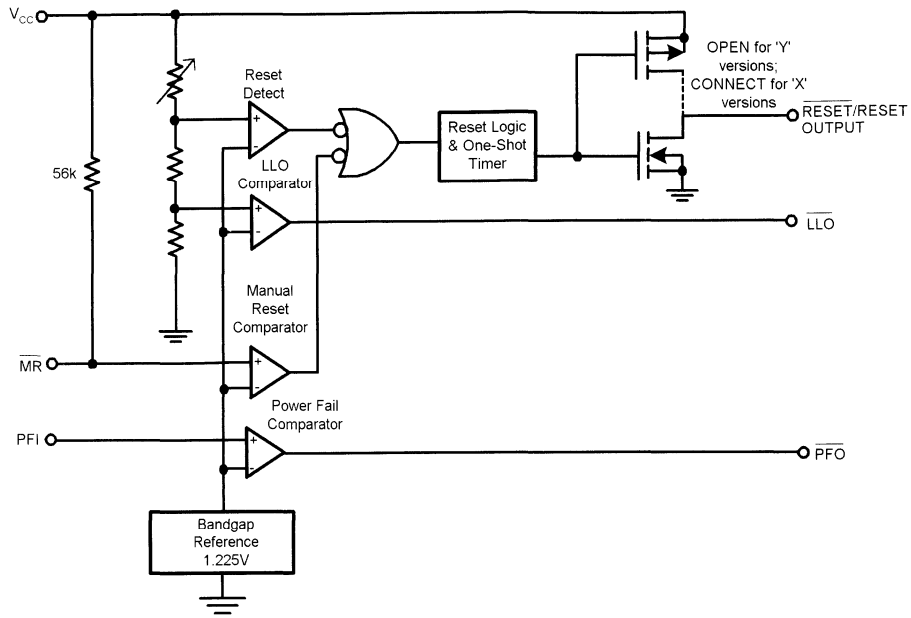


10136901

Pin Description

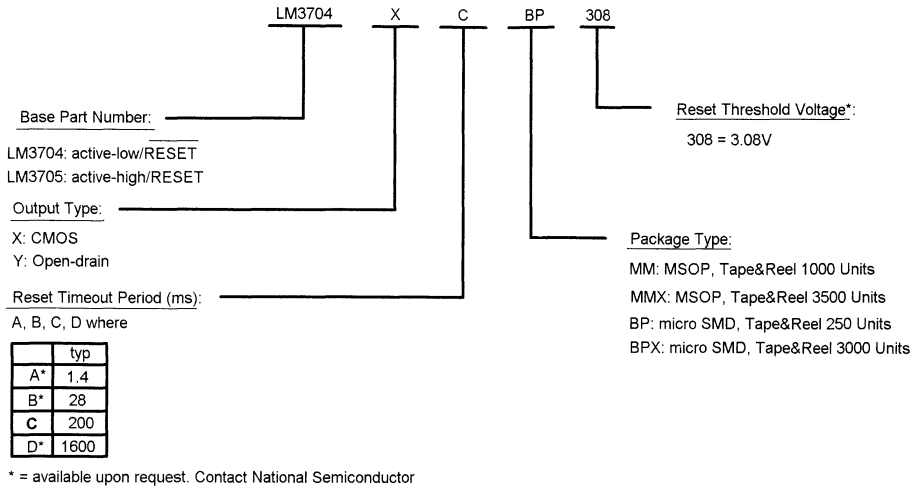
Pin No.		Name	Function
micro SMD	MSOP		
1	2	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
2	1	V_{CC}	Power Supply input.
3	10	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3704 only).
		RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3705 only).
4	8	$\overline{PFO}$	Power-Fail Logic Output. When PFI is below V_{PFT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
5	7	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
6	5	GND	Ground reference for all signals.
7	4, 6	NC	No Connect.
8	3	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
9	9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram



10136926

Ordering Information



* = available upon request. Contact National Semiconductor

10136904

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3704/LM3705

Part Number	Output	Reset Timeout Period	Package		Package Marking
			MSOP	micro SMD	
LM3704XCBP-308	totem-pole	200ms		x	%%I4
LM3704XCBPX-308	totem-pole	200ms		x	%%I4
LM3704XCMM-308	totem-pole	200ms	x		R35B
LM3704XCMMX-308	totem-pole	200ms	x		R35B
LM3705XCBP-308	totem-pole	200ms		x	%%I5
LM3705XCBPX-308	totem-pole	200ms		x	%%I5
LM3705XCMM-308	totem-pole	200ms	x		R36B
LM3705XCMMX-308	totem-pole	200ms	x		R36B

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Manual Reset	Power Fail Comparator	Low Line Output
LM3704	x		X, Y*	Customized	x	x	x
LM3705		x	X	Customized	x	x	x

* = available upon request. Contact National

National Semiconductor

LM3706/LM3707
Microprocessor Supervisory Circuits with Low Line Output and Watchdog Timer

General Description

The LM3706/LM3707 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3706/LM3707 series are available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, reset is activated.

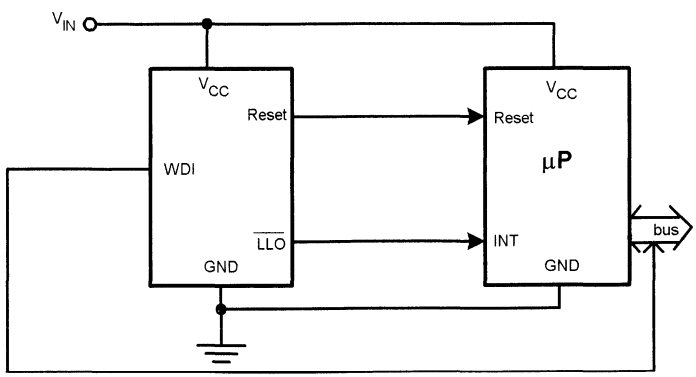
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- $\overline{\text{RESET}}$ (LM3706) or RESET (LM3707) outputs
- Precision supply voltage monitor
- Factory programmable Reset and Watchdog Timeout Delays
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

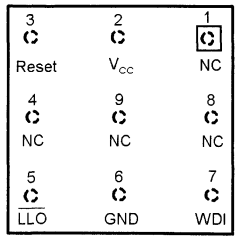
Typical Application



20011603

Connection Diagram

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

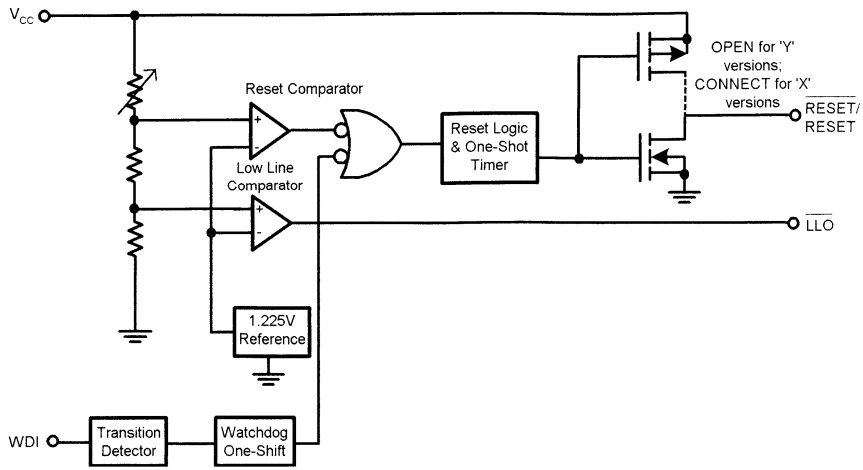


20011601

Pin Descriptions

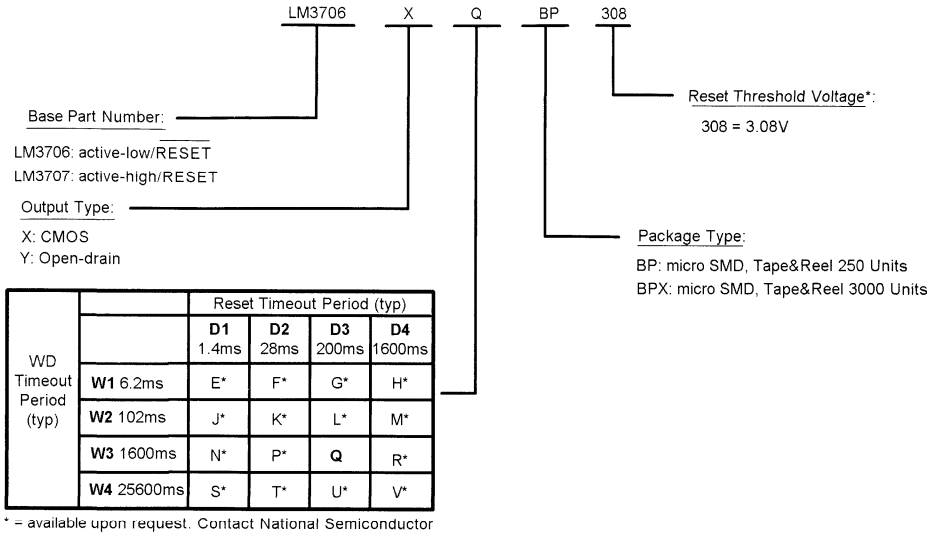
Bump No.	Name	Function
2	V_{CC}	Power Supply input.
3	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3706 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3707 only).
5	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
6	GND	Ground reference for all signals.
7	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
1, 4, 8	NC	No Connect.
9	NC	No Connect. Bump 9 is test input used at factory only. Leave floating.

Block Diagram



20011605

Ordering Information



WD Timeout Period (typ)		Reset Timeout Period (typ)			
		D1 1.4ms	**D2** 28ms	**D3** 200ms	**D4** 1600ms
	W1 6.2ms	E*	F*	G*	H*
	W2 102ms	J*	K*	L*	M*
	W3 1600ms	N*	P*	**Q**	R*
	W4 25600ms	S*	T*	U*	V*

* = available upon request. Contact National Semiconductor

20011604

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3706/LM3707

Part Number	Output	Reset Timeout Period	Watchdog Timeout Period	Package Marking
LM3706XQBP-308	totem-pole	200ms	1600ms	%%I6
LM3706XQBPX-308	totem-pole	200ms	1600ms	%%I6
LM3707XQBP-308	totem-pole	200ms	1600ms	%%I7
LM3707XQBPX-308	totem-pole	200ms	1600ms	%%I7

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Low Line Output
LM3706	x		X, Y*	Customized	Customized	x
LM3707		x	X	Customized	Customized	x

* = available upon request. Contact National

12

National Semiconductor

LM3708/LM3709
Microprocessor Supervisory Circuits with Low Line Output, Manual Reset and Watchdog Timer

General Description

The LM3708/LM3709 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3708/LM3709 series are available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, reset is activated.

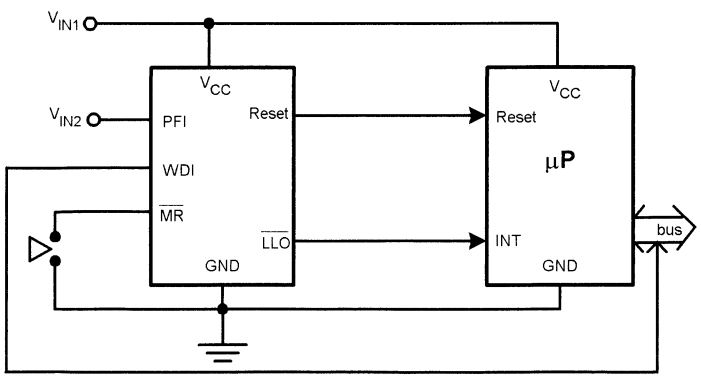
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ (LM3708) or RESET (LM3709) outputs
- Precision supply voltage monitor
- Factory programmable Reset and Watchdog Timeout Delays
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

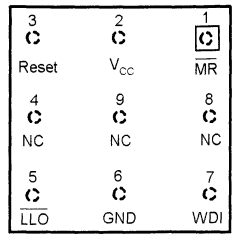
Typical Application



20011703

Connection Diagram

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

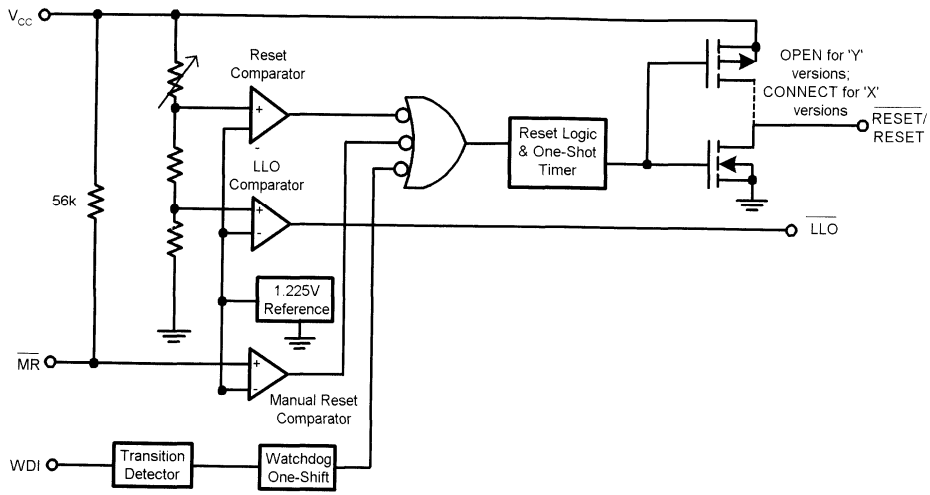


20011701

Pin Descriptions

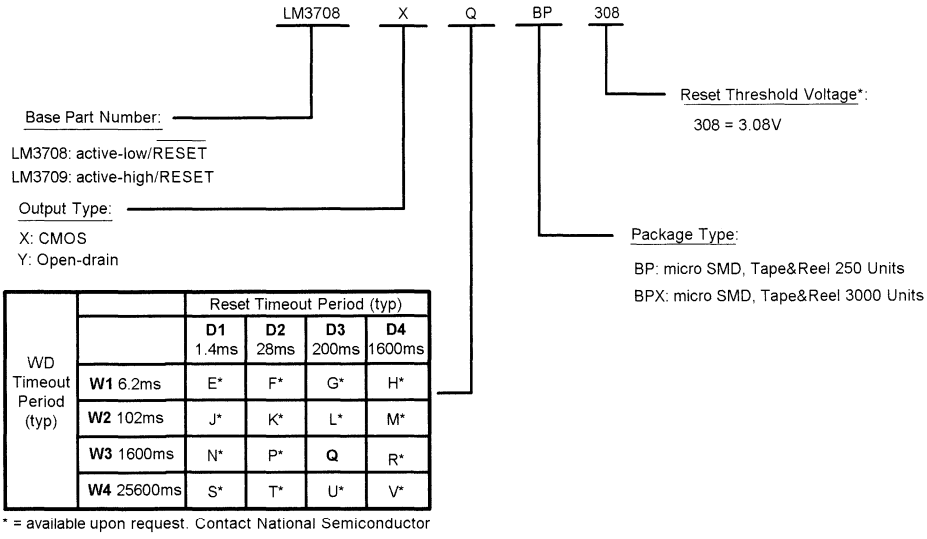
Bump No.	Name	Function
1	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
2	V_{CC}	Power Supply input.
3	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3708 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3709 only).
5	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
6	GND	Ground reference for all signals.
7	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
4, 8	NC	No Connect.
9	NC	No Connect. Bump 9 is test input used at factory only. Leave floating.

Block Diagram



200:1705

Ordering Information



		Reset Timeout Period (typ)			
		D1 1.4ms	**D2** 28ms	**D3** 200ms	**D4** 1600ms
WD Timeout Period (typ)	**W1** 6.2ms	E*	F*	G*	H*
	W2 102ms	J*	K*	L*	M*
	W3 1600ms	N*	P*	**Q**	R*
	W4 25600ms	S*	T*	U*	V*

* = available upon request. Contact National Semiconductor

20011704

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3708/LM3709

Part Number	Output	Reset Timeout Period	Watchdog Timeout Period	Package Marking
LM3708XQBP-308	totem-pole	200ms	1600ms	%%I8
LM3708XQBPX-308	totem-pole	200ms	1600ms	%%I8
LM3709XQBP-308	totem-pole	200ms	1600ms	%%I9
LM3709XQBPX-308	totem-pole	200ms	1600ms	%%I9

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Manual Reset	Low Line Output
LM3708	x		X, Y*	Customized	Customized	x	x
LM3709		x	X	Customized	Customized	x	x

* = available upon request. Contact National

12

National Semiconductor

LM3710/LM3711
Microprocessor Supervisory Circuits with Power Fail Input, Low Line Output, Manual Reset and Watchdog Timer

General Description

The LM3710/LM3711 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3710/LM3711 series are available in MSOP-10 and 9-bump micro SMD packages.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

Low Line Output: This early power failure warning indicator goes low when the supply voltage drops to a value which is 2% higher than the reset threshold voltage.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, reset is activated.

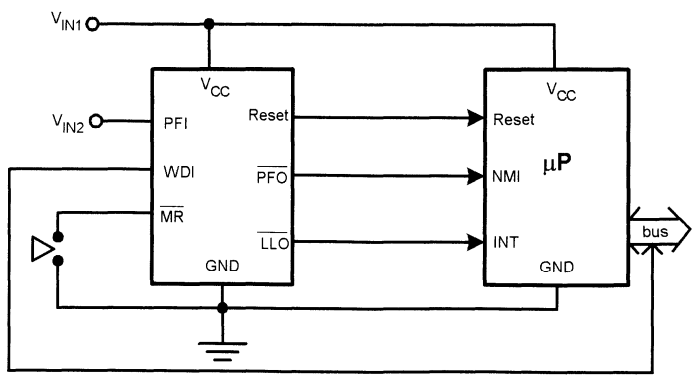
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ (LM3710) or RESET (LM3711) outputs
- Precision supply voltage monitor
- Factory programmable Reset and Watchdog Timeout Delays
- Separate Power Fail comparator
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

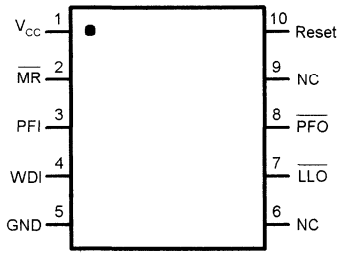
Typical Application



20011803

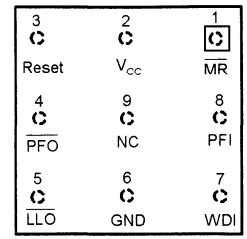
Connection Diagrams

MSOP-10



20011802

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

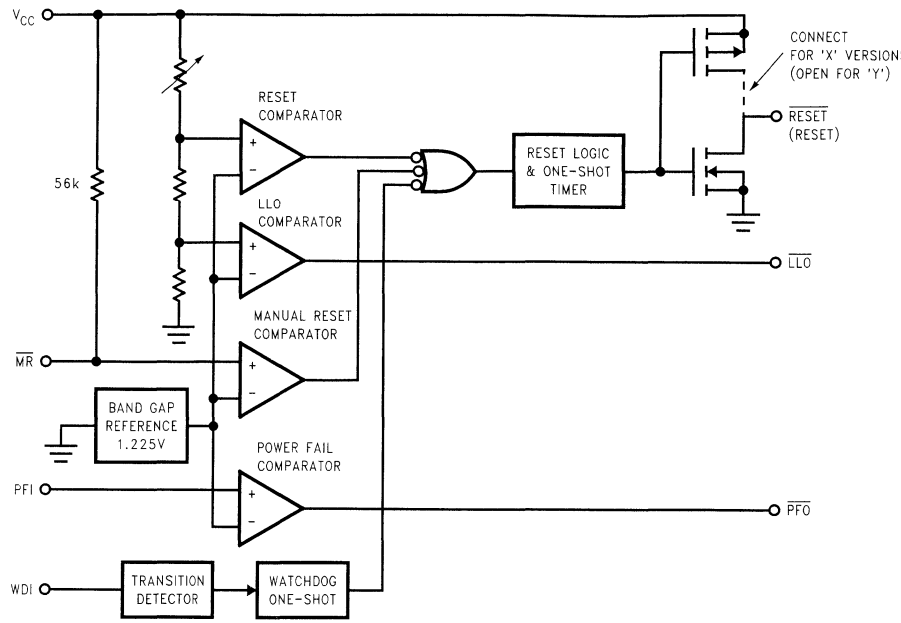


20011801

Pin Descriptions

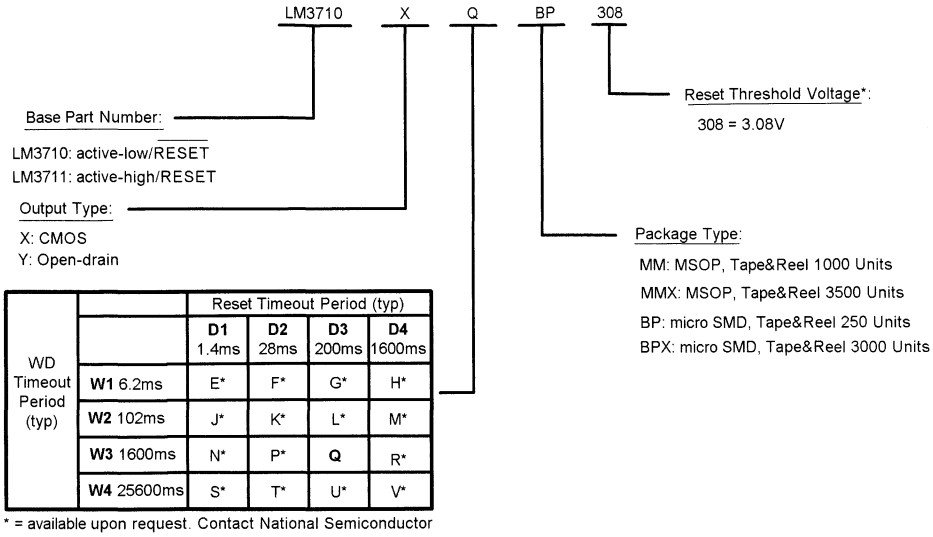
Pin No.		Name	Function
micro SMD	MSOP		
1	2	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
2	1	V_{CC}	Power Supply input.
3	10	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3710 only).
		RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3711 only).
4	8	$\overline{PFO}$	Power-Fail Logic Output. When PFI is below V_{PFT}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
5	7	$\overline{LLO}$	Low-Line Logic Output. Early Power-Fail warning output. Low when V_{CC} falls below V_{LLOT} (Low-Line Output Threshold). This output can be used to generate an NMI (Non-Maskable Interrupt) to provide an early warning of imminent power-failure.
6	5	GND	Ground reference for all signals.
7	4	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
8	3	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
9	6, 9	NC	No Connect. Test input used at factory only. Leave floating.

Block Diagram



20011805

Ordering Information



WD Timeout Period (typ)		Reset Timeout Period (typ)			
		D1 1.4ms	**D2** 28ms	**D3** 200ms	**D4** 1600ms
	W1 6.2ms	E*	F*	G*	H*
	W2 102ms	J*	K*	L*	M*
	W3 1600ms	N*	P*	**Q**	R*
	W4 25600ms	S*	T*	U*	V*

* = available upon request. Contact National Semiconductor

20011804

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3710/LM3711

Part Number	Output	Reset Timeout Period	Watchdog Timeout Period	Package		Package Marking
				MSOP	micro SMD	
LM3710XQBP-308	totem-pole	200ms	1600ms		x	%%IA
LM3710XQBPX-308	totem-pole	200ms	1600ms		x	%%IA
LM3710XQMM-308	totem-pole	200ms	1600ms	x		R37B
LM3710XQMMX-308	totem-pole	200ms	1600ms	x		R37B
LM3711XQBP-308	totem-pole	200ms	1600ms		x	%%IB
LM3711XQBPX-308	totem-pole	200ms	1600ms		x	%%IB
LM3711XQMM-308	totem-pole	200ms	1600ms	x		R38B
LM3711XQMMX-308	totem-pole	200ms	1600ms	x		R38B

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Manual Reset	Power Fail Comparator	Low Line Output
LM3710	x		X, Y*	Customized	Customized	x	x	x
LM3711		x	X	Customized	Customized	x	x	x

* = available upon request. Contact National

National Semiconductor

LM3712/LM3713
Microprocessor Supervisory Circuits with Separate Watchdog Timer Output, Power Fail Input and Manual Reset

General Description

The LM3712/LM3713 series of microprocessor supervisory circuits provide the maximum flexibility for monitoring power supplies and battery controlled functions in systems without backup batteries. The LM3712/LM3713 series are available in a 9-bump micro SMD package.

Built-in features include the following:

Reset: Reset is asserted during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed down to V_{CC} of 1.0V.

Manual Reset Input: An input that asserts reset when pulled low.

Power-Fail Input: A 1.225V threshold detector for power fail warning, or to monitor a power supply other than V_{CC}.

Watchdog Timer: The WDI (Watchdog Input) monitors one of the µP's output lines for activity. If no output transition occurs during the watchdog timeout period, the watchdog output ($\overline{\text{WDO}}$) pulls low.

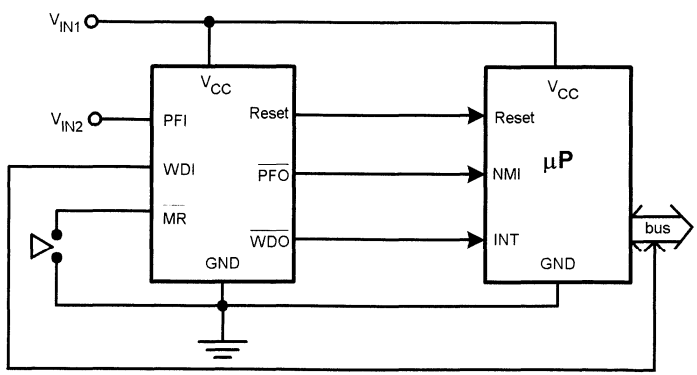
Features

- Standard Reset Threshold voltage: 3.08V
- Custom Reset Threshold voltages: For other voltages between 2.2V and 5.0V in 10mV increments, contact National Semiconductor Corp.
- No external components required
- Manual-Reset input
- $\overline{\text{RESET}}$ (LM3712) or RESET (LM3713) outputs
- Precision supply voltage monitor
- Factory programmable Reset and Watchdog Timeout Delays
- Separate Watchdog output
- Separate Power Fail comparator
- Available in micro SMD package for minimum footprint
- ±0.5% Reset threshold accuracy at room temperature
- ±2% Reset threshold accuracy over temperature extremes
- Reset assertion down to 1V V_{CC} ($\overline{\text{RESET}}$ option only)
- 28 µA V_{CC} supply current

Applications

- Embedded Controllers and Processors
- Intelligent Instruments
- Automotive Systems
- Critical µP Power Monitoring

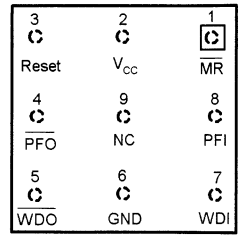
Typical Application



20011903

Connection Diagram

Top View
(looking from the coating side)
micro SMD 9 Bump Package
BPA09

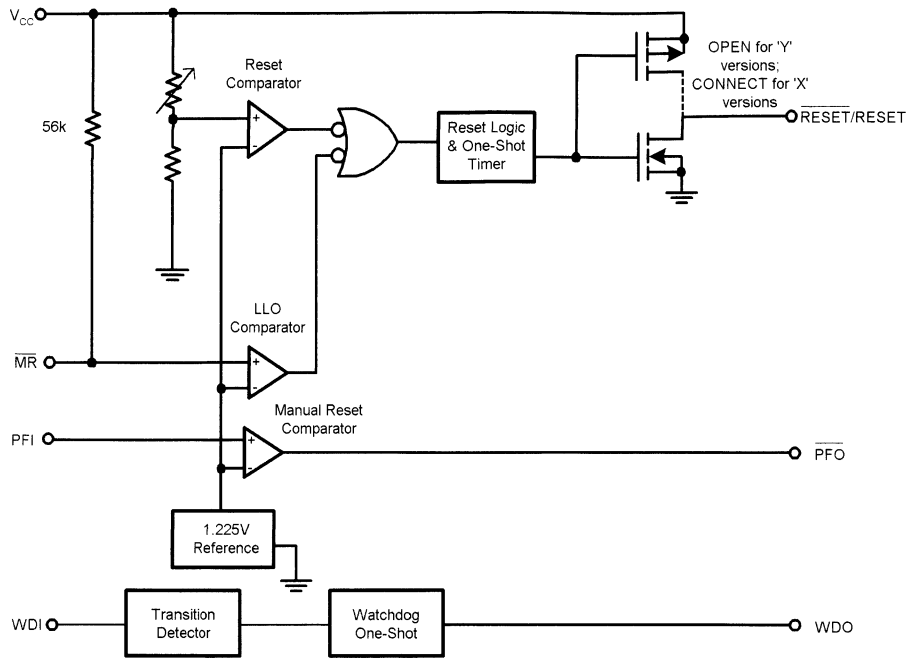


20011901

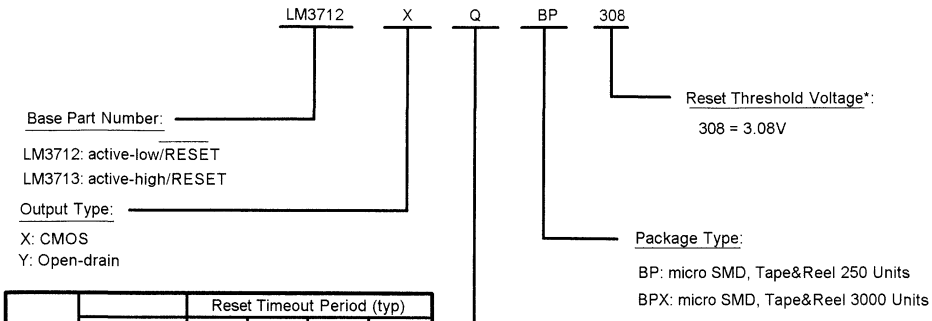
Pin Description

Bump No.	Name	Function
1	$\overline{MR}$	Manual-Reset input. When $\overline{MR}$ is less than V_{MRT} (Manual Reset Threshold) $\overline{RESET}$/RESET is engaged.
2	V_{CC}	Power Supply input.
3	$\overline{RESET}$	Reset Logic Output. Pulses low for t_{RP} (Reset Timeout Period) when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is below V_{MRT}. It remains low for t_{RP} after either V_{CC} rises above the reset threshold, or after $\overline{MR}$ input rises above V_{MRT} (LM3712 only).
	RESET	Reset Logic Output. RESET is the inverse of $\overline{RESET}$ (LM3713 only).
4	$\overline{PFO}$	Power-Fail Logic Output. When PFI is below V_{PFT} $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
5	$\overline{WDO}$	Watchdog Output. If no digital activity is detected on WDI (Watchdog Input) for a period exceeding t_{WD}, this output pulls low.
6	GND	Ground reference for all signals.
7	WDI	Watchdog Input Transition Monitor: If no transition activity occurs for a period exceeding t_{WD} (Watchdog Timeout Period), reset is engaged.
8	PFI	Power-Fail Comparator Input. When PFI is less than V_{PFT} (Power-Fail Reset Threshold), the $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high.
9	NC	No Connect. Bump 9 is test input used at factory only. Leave floating.

Block Diagram



Ordering Information



		Reset Timeout Period (typ)			
		D1 1.4ms	**D2** 28ms	**D3** 200ms	**D4** 1600ms
WD Timeout Period (typ)	**W1** 6.2ms	E*	F*	G*	H*
	W2 102ms	J*	K*	L*	M*
	W3 1600ms	N*	P*	**Q**	R*
	W4 25600ms	S*	T*	U*	V*

* = available upon request. Contact National Semiconductor

20011904

*For other voltages between 2.2V and 5.0V, please contact National Semiconductor sales office.

LM3712/LM3713

Part Number	Output	Reset Timeout Period	Watchdog Timeout Period	Package Marking
LM3712XQBP-308	totem-pole	200ms	1600ms	%%IC
LM3712XQBPX-308	totem-pole	200ms	1600ms	%%IC
LM3713XQBP-308	totem-pole	200ms	1600ms	%%ID
LM3713XQBPX-308	totem-pole	200ms	1600ms	%%ID

%% is the datecode and will vary with time.

Table Of Functions

Part Number	Active Low Reset	Active High Reset	Output (X = totem-pole) (Y = open-drain)	Reset Timeout Period	Watchdog Timeout Period	Manual Reset	Power Fail Comparator
LM3712	x		X, Y*	Customized	Customized	x	x
LM3713		x	X	Customized	Customized	x	x

* = available upon request. Contact National

12

National Semiconductor

LM3722/LM3723/LM3724
5-Pin Microprocessor Reset Circuits

General Description

The LM3722/LM3723/LM3724 microprocessor supervisory circuits monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down, brown-out conditions, and manual reset.

The LM3722/LM3723/LM3724 asserts a reset signal whenever the supply decreases below the factory-programmed reset threshold for at least 100 ms. The reset signal remains asserted for 190 ms after V_{CC} rises above the threshold.

The LM3722 has an active-low $\overline{\text{RESET}}$ push-pull output. The LM3723 has an active-high RESET push-pull output. The LM3724 has an active-low open-drain $\overline{\text{RESET}}$ output.

Three standard reset voltage options are available, suitable for monitoring 5V, 3.3V, and 2.5V supply voltages. Additional reset voltages are also available; contact National Semiconductor for details.

With a low supply current of only 6µA, the LM3722/LM3723/LM3724 are ideal for use in portable equipment. The LM3722/LM3723/LM3724 are available in the 5-pin SOT23 package.

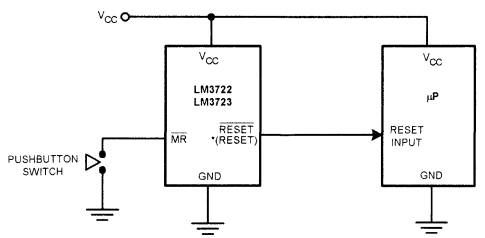
Features

- Precise monitoring of 2.5V, 3.3V, and 5V supply voltages
- Fully specified over temperature
  - Industrial: −40˚C to +85˚C
  - Extended: −40˚C to +125˚C
- 100 ms minimum Power-On Reset pulse width, 190 ms typical:
  - Active-Low $\overline{\text{RESET}}$ Output (LM3722)
  - Active-High RESET Output (LM3723)
  - Active-Low $\overline{\text{RESET}}$ Open Drain Output (LM3724)
- Guaranteed $\overline{\text{RESET}}$ Output valid for $V_{CC} \geq 1V$
- Low Supply Current, 6µA typical
- Power supply transient immunity
- Compatible with MAX811/812 applications

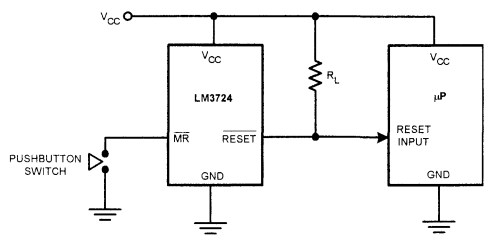
Applications

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment

Typical Application Circuits



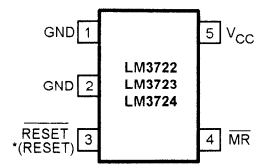
20014401



20014437

Connection Diagram

SOT23-5



20014402

*( ) are for LM3723

Ordering Information

Industrial Temperature Range (−40˚C to +85˚C):

Reset Threshold (V)	LM3722 Supplied as 1000 units, tape & reel	LM3722 Supplied as 3000 units, tape & reel	Package Top Mark	Package Type	NSC Package
4.63	LM3722IM5-4.63	LM3722IM5X-4.63	R43B	SOT23-5	MF05A
3.08	LM3722IM5-3.08	LM3722IM5X-3.08	R41B		
2.32	LM3722IM5-2.32	LM3722IM5X-2.32	R34B		
Reset Threshold (V)	**LM3723 Supplied as 1000 units, tape & reel**	**LM3723 Supplied as 3000 units, tape & reel**	**Package Top Mark**	**Package Type**	**NSC Package**
4.63	LM3723IM5-4.63	LM3723IM5X-4.63	R13B	SOT23-5	MF05A
3.08	LM3723IM5-3.08	LM3723IM5X-3.08	R11B		
2.32	LM3723IM5-2.32	LM3723IM5X-2.32	R46B		
Reset Threshold (V)	**LM3724 Supplied as 1000 units, tape & reel**	**LM3724 Supplied as 3000 units, tape & reel**	**Package Top Mark**	**Package Type**	**NSC Package**
4.63	LM3724IM5-4.63	LM3724IM5X-4.63	R55B	SOT23-5	MF05A
3.08	LM3724IM5-3.08	LM3724IM5X-3.08	R53B		
2.32	LM3724IM5-2.32	LM3724IM5X-2.32	R50B		

Extended Temperature Range (−40˚C to +125˚C):

Reset Threshold (V)	LM3722 Supplied as 1000 units, tape & reel	LM3722 Supplied as 3000 units, tape & reel	Package Top Mark	Package Type	NSC Package
4.63	LM3722EM5-4.63	LM3722EM5X-4.63	R56B	SOT23-5	MF05A
3.08	LM3722EM5-3.08	LM3722EM5X-3.08	R57B		
2.32	LM3722EM5-2.32	LM3722EM5X-2.32	R58B		
Reset Threshold (V)	**LM3723 Supplied as 1000 units, tape & reel**	**LM3723 Supplied as 3000 units, tape & reel**	**Package Top Mark**	**Package Type**	**NSC Package**
4.63	LM3723EM5-4.63	LM3723EM5X-4.63	R59B	SOT23-5	MF05A
3.08	LM3723EM5-3.08	LM3723EM5X-3.08	R60		
2.32	LM3723EM5-2.32	LM3723EM5X-2.32	R61B		
Reset Threshold (V)	**LM3724 Supplied as 1000 units, tape & reel**	**LM3724 Supplied as 3000 units, tape & reel**	**Package Top Mark**	**Package Type**	**NSC Package**
4.63	LM3724EM5-4.63	LM3724EM5X-4.63	R62B	SOT23-5	MF05A
3.08	LM3724EM5-3.08	LM3724EM5X-3.08	R63B		
2.32	LM3724EM5-2.32	LM3724EM5X-2.32	R64B		

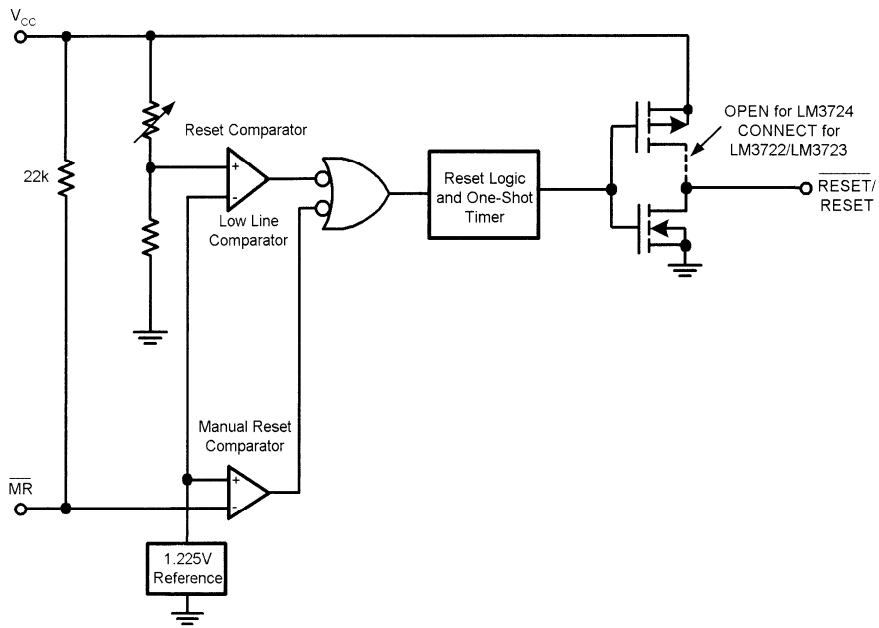
Custom voltages and improved accuracies are available, subject to minimum orders. Contact your local National Semiconductor Sales Office for information.

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground reference
2	GND	Ground reference, device substrate, connect to ground.
3	$\overline{\text{RESET}}$ LM3722/LM3724	Active-low output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold voltage, and for 190 ms after V_{CC} rises above the reset threshold voltage.
	RESET LM3723	Active-high output. RESET remains high while V_{CC} is below the reset threshold, and for 190 ms after V_{CC} rises above the reset threshold.
4	$\overline{\text{MR}}$	Active-low input. Reset is asserted whenever this pin is pulled low and remains asserted for 190 ms after the $\overline{\text{MR}}$ pin goes high. May be left open.
5	V_{CC}	Supply Voltage (+5V, +3.3V, or +2.5V, nominal)

Block Diagram

LM3722/LM3723/LM3724 Block Diagram



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National Semiconductor

LM3812/LM3813
Precision Current Gauge IC with Ultra Low Loss Sense Element and PWM Output

General Description

The LM3812/LM3813 Current Gauges provide easy to use precision current measurement with virtually zero insertion loss (typically 0.004Ω). The LM3812 is used for high-side sensing and the LM3813 is used for low-side sensing.

A Delta Sigma analog to digital converter is incorporated to precisely measure the current and to provide a current averaging function. Current is averaged over 50 msec time periods in order to provide immunity to current spikes. The ICs have a pulse-width modulated (PWM) output which indicates the current magnitude and direction. The shutdown pin can be used to inhibit false triggering during start-up, or to enter a low quiescent current mode.

The LM3812 and LM3813 are factory-set in two different current options. The sense range is −1A to +1A or −7A to +7A. The sampling interval for these parts is 50ms. If faster sampling is desired, please refer to the data sheets for the part numbers LM3814 and LM3815.

Key Specifications

- Ultra low insertion loss (typically 0.004Ω)
- 2V to 5.25V supply range
- ±2% accuracy at room temperature (includes accuracy of the internal sense element) (LM3812-1.0, LM3813-1.0)
- Low quiescent current in shutdown mode (typically 2.5 μA)
- 50 msec sampling interval

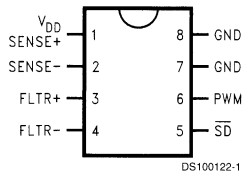
Features

- No external sense element required
- PWM output indicates the current magnitude and direction
- PWM output can be interfaced with microprocessors
- Precision ΔΣ current-sense technique
- Low temperature sensitivity
- Internal filtering rejects false trips
- Internal Power-On-Reset (POR)

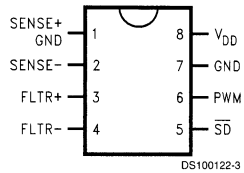
Applications

- Battery charge/discharge gauge
- Motion control diagnostics
- Power supply load monitoring and management
- Resettable smart fuse

Connection Diagrams



Top View
LM3812
for High-Side Sensing



Top View
LM3813
for Low-Side Sensing

Ordering Information

Order No.[#]	Sense Range	Sampling Interval[*]	Sensing Method	NS Package Number[‡]	Package Type	Supplied As:
LM3812M-1.0	±1A	50 ms	High-side	M08A	SO-8	95 units in Rails
LM3812MX-1.0	±1A	50 ms	High-side	M08A	SO-8	2.5k units on Tape and Reel
LM3812M-7.0	±7A	50 ms	High-side	M08A	SO-8	95 units in Rails
LM3812MX-7.0	±7A	50 ms	High-side	M08A	SO-8	2.5k units on Tape and Reel
LM3813M-1.0	±1A	50 ms	Low-side	M08A	SO-8	95 units in Rails
LM3813MX-1.0	±1A	50 ms	Low-side	M08A	SO-8	2.5k units on Tape and Reel
LM3813M-7.0	±7A	50 ms	Low-side	M08A	SO-8	95 units in Rails
LM3813MX-7.0	±7A	50 ms	Low-side	M08A	SO-8	2.5k units on Tape and Reel

[#] Suffix M indicates that the part is available in Surface Mount package. Suffix X indicates that the part is available in 2.5k units on Tape and Reel.

[*] Current is sampled over a fixed interval. The average current during this interval is indicated by the duty cycle of the PWM output during next interval.

[‡] The Package code M08A is internal to National Semiconductor and indicates an 8-lead surface mount package, SO-8.

Pin Description (High-Side, LM3812)

Pin	Name	Function
1	SENSE+, V_{DD}	High side of internal current sense, also supply voltage.
2	SENSE–	Low side of internal current sense.
3	FLTR+	Filter input — provides anti-aliasing for delta sigma modulator.
4	FLTR–	Filter input.
5	$\overline{SD}$	Shutdown pin. Connected to V_{DD} through a pull up resistor for normal operation. When low, the IC goes into a low current mode (typically 3 µA).
6	PWM	PWM output indicates the current magnitude and direction.
7	GND	Ground
8	GND	Ground

Pin Description (Low-Side, LM3813)

Pin	Name	Function
1	SENSE+, GND	High side of internal current sense, also ground.
2	SENSE–	Low side of internal current sense.
3	FLTR+	Filter input – provides anti-aliasing for delta sigma modulator.
4	FLTR–	Filter input.
5	$\overline{SD}$	Shutdown pin. Connected to V_{DD} through a pull up resistor for normal operation. When low, the IC goes into a low current mode (typically 3 µA).
6	PWM	PWM output indicates the current magnitude and direction.
7	GND	Ground
8	V_{DD}	V_{DD} (supply)

National Semiconductor

LM3814/LM3815
Fast Current Gauge IC with Ultra Low Loss Sense Element and PWM Output

General Description

The LM3814/LM3815 Current Gauges provide easy to use precision current measurement with virtually zero insertion loss (typically 0.004Ω). The LM3814 is used for high-side sensing and the LM3815 is used for low-side sensing.

A Delta Sigma analog to digital converter is incorporated to precisely measure the current and to provide a current averaging function. Current is averaged over 6 msec time periods in order to provide immunity to current spikes. The ICs have a pulse-width modulated (PWM) output which indicates the current magnitude and direction. The shutdown pin can be used to inhibit false triggering during start-up, or to enter a low quiescent current mode.

The LM3814 and LM3815 are factory-set in two different current options. The sense range is −1A to +1A or −7A to +7A. The user specifies a particular part number to match the current range for a given application. The sampling interval for these parts is 6ms. If larger sampling interval is desired for better accuracy, please refer to the data sheets for the part numbers LM3812 and LM3813.

Key Specifications

- Ultra low insertion loss (typically 0.004Ω)
- 2V to 5.25V supply range
- ±3.5% accuracy at room temperature (includes accuracy of the internal sense element) (LM3814-1.0, LM3815-1.0)
- Low quiescent current in shutdown mode (typically 2.5 μA)
- 6 msec sampling interval

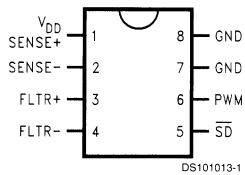
Features

- No external sense element required
- PWM output indicates the current magnitude and direction
- PWM output can be interfaced with microprocessors
- Precision ΔΣ current-sense technique
- Low temperature sensitivity
- Internal filtering rejects false trips
- Internal Power-On-Reset (POR)

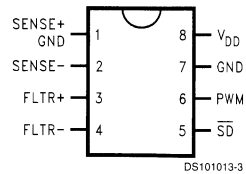
Applications

- Battery charge/discharge gauge
- Motion control diagnostics
- Power supply load monitoring and management
- Resettable smart fuse

Connection Diagrams



Top View
LM3814
for High-Side Sensing



Top View
LM3815
for Low-Side Sensing

Ordering Information

Order No.[#]	Sense Range	Sampling Interval[*]	Sensing Method	NS Package Number[‡]	Package Type	Supplied As:
LM3814M-1.0	±1A	6 ms	High-side	M08A	SO-8	95 units in Rails
LM3814MX-1.0	±1A	6 ms	High-side	M08A	SO-8	2.5k units on Tape and Reel
LM3814M-7.0	±7A	6 ms	High-side	M08A	SO-8	95 units in Rails
LM3814MX-7.0	±7A	6 ms	High-side	M08A	SO-8	2.5k units on Tape and Reel
LM3815M-1.0	±1A	6 ms	Low-side	M08A	SO-8	95 units in Rails
LM3815MX-1.0	±1A	6 ms	Low-side	M08A	SO-8	2.5k units on Tape and Reel
LM3815M-7.0	±7A	6 ms	Low-side	M08A	SO-8	95 units in Rails
LM3815MX-7.0	±7A	6 ms	Low-side	M08A	SO-8	2.5k units on Tape and Reel

[#] Suffix M indicates that the part is available in Surface Mount package. Suffix X indicates that the part is available in 2.5k units on Tape and Reel.

[*] Current is sampled over a fixed interval. The average current during this interval is indicated by the duty cycle of the PWM output during next interval.

[‡] The Package code M08A is internal to National Semiconductor and indicates an 8-lead surface mount package, SO-8.

Pin Description (High-Side, LM3814)

Pin	Name	Function
1	SENSE+, V_{DD}	High side of internal current sense, also supply voltage.
2	SENSE–	Low side of internal current sense.
3	FLTR+	Filter input — provides anti-aliasing for delta sigma modulator.
4	FLTR–	Filter input.
5	$\overline{SD}$	Shutdown pin. Connected to V_{DD} through a pull up resistor for normal operation. When low, the IC goes into a low current mode (typically 3 µA).
6	PWM	PWM output indicates the current magnitude and direction.
7	GND	Ground
8	GND	Ground

Pin Description (Low-Side, LM3815)

Pin	Name	Function
1	SENSE+, GND	High side of internal current sense, also ground.
2	SENSE–	Low side of internal current sense.
3	FLTR+	Filter input – provides anti-aliasing for delta sigma modulator.
4	FLTR–	Filter input.
5	$\overline{SD}$	Shutdown pin. Connected to V_{DD} through a pull up resistor for normal operation. When low, the IC goes into a low current mode (typically 3 µA).
6	PWM	PWM output indicates the current magnitude and direction.
7	GND	Ground
8	V_{DD}	V_{DD} (supply)

National Semiconductor

LM3822
Precision Current Gauge IC with Internal Zero Ohm Sense Element and PWM Output

General Description

The LM3822 Current Gauge provides easy to use precision current measurement with virtually zero insertion loss (typically 0.003Ω). The LM3822 is used for high-side sensing.

A Delta Sigma analog to digital converter is incorporated to precisely measure the current and to provide a current averaging function. Current is averaged over 50 msec time periods in order to provide immunity to current spikes. The ICs have a pulse-width modulated (PWM) output which indicates the current magnitude and direction. The shutdown pin can be used to inhibit false triggering during start-up, or to enter a low quiescent current mode.

The LM3822 is factory-set in two different current options. The sense range is −1.0A to +1.0A or −2.0A to +2.0A. The sampling interval for this part is 50ms. If faster sampling is desired, please refer to the data sheet for the part number LM3824.

Key Specifications

- Ultra low insertion loss (typically 0.003Ω)
- 2V to 5.5V supply range
- ±2% accuracy at room temperature for the 1A device (includes accuracy of the internal sense element)
- Low quiescent current in shutdown mode (typically 1.8 µA)
- 50 msec sampling interval
- In MSOP-8 Package

Features

- No external sense element required
- PWM output indicates the current magnitude and direction
- PWM output is easily interfaced with microprocessors and controllers
- Precision ΔΣ current-sense technique
- Low temperature sensitivity
- Internal filtering rejects false trips
- Internal Power-On-Reset (POR)
- DC Offset is less than 1 mA for 1A part

Applications

- Battery charge/discharge gauge
- Motion control diagnostics
- Power supply load monitoring and management
- Resettable smart fuse

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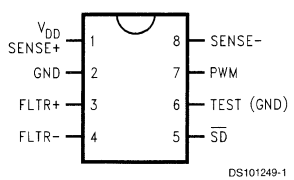
Connection Diagram



Top View
LM3822 for High-Side Sensing

Ordering Information

Order No.*	Sense Range	Sampling Interval*	Sensing Method	NS Package Number	Package Type	Supplied As:
LM3822MM-1.0	±1.0A	50 ms	High-side	MUA08A	MSOP-8	Tape and Reel (1000 units/reel)
LM3822MMX-1.0	±1.0A	50 ms	High-side	MUA08A	MSOP-8	Tape and Reel (3500 units/reel)
LM3822MM-2.0	±2.0A	50 ms	High-side	MUA08A	MSOP-8	Tape and Reel (1000 units/reel)
LM3822MMX-2.0	±2.0A	50 ms	High-side	MUA08A	MSOP-8	Tape and Reel (3500 units/reel)

* Current is sampled over a fixed interval. The average current during this interval is indicated by the duty cycle of the PWM output during next interval.

Pin Description (High-Side, LM3822)

Pin	Name	Function
1	SENSE+, V_{DD}	High side of internal current sense, also supply voltage.
2	GND	Supply Ground.
3	FLTR+	Filter input — provides anti-aliasing for delta sigma modulator.
4	FLTR–	Filter input.
5	$\overline{SD}$	Shutdown input. Connected to V_{DD} through a pull-up resistor for normal operation. When low, the LM3822 is put into a low current mode.
6	TEST	Connect to GND for normal operation.
7	PWM	Digital output indicates the current magnitude and direction.
8	SENSE–	Low side of internal current sense.

National Semiconductor

LM3824
Precision Current Gauge IC with Internal Zero Ohm Sense Element and PWM Output

General Description

The LM3824 Current Gauge provides easy to use precision current measurement with virtually zero insertion loss (typically 0.003Ω). The LM3824 is used for high-side sensing.

A Delta Sigma analog to digital converter is incorporated to precisely measure the current and to provide a current averaging function. Current is averaged over 6 msec time periods in order to provide immunity to current spikes. The ICs have a pulse-width modulated (PWM) output which indicates the current magnitude and direction. The shutdown pin can be used to inhibit false triggering during start-up, or to enter a low quiescent current mode.

The LM3824 is factory-set in two different current options. The sense range is −1.0A to +1.0A or −2.0A to +2.0A. The sampling interval for this part is 6ms. If a more precise measurement is required, please refer to LM3822 datasheet.

Key Specifications

- Ultra low insertion loss (0.003Ω)
- 2V to 5.5V supply range
- ±3% accuracy at room temperature for the 1A device (includes accuracy of the internal sense element)
- Low quiescent current in shutdown mode (typically 1.8 µA)
- 6 msec sampling interval
- In MSOP-8 Package

Features

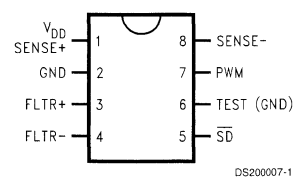
- No external sense element required
- PWM output indicates the current magnitude and direction
- PWM output is easily interfaced with microprocessors and controllers
- Precision ΔΣ current-sense technique
- Low temperature sensitivity
- Internal filtering rejects false trips
- Internal Power-On-Reset (POR)
- DC Offset is less than 8 mA for 1A part

Applications

- Battery charge/discharge gauge
- Motion control diagnostics
- Power supply load monitoring and management
- Resettable smart fuse

12

Connection Diagram



Top View
LM3824 for High-Side Sensing

Ordering Information

Order No.*	Sense Range	Sampling Interval*	Sensing Method	NS Package Number	Package Type	Supplied As:
LM3824MM-1.0	±1.0A	6 ms	High-side	MUA08A	MSOP-8	Tape and Reel (1000 units/reel)
LM3824MMX-1.0	±1.0A	6 ms	High-side	MUA08A	MSOP-8	Tape and Reel (3500 units/reel)
LM3824MM-2.0	±2.0A	6 ms	High-side	MUA08A	MSOP-8	Tape and Reel (1000 units/reel)
LM3824MMX-2.0	±2.0A	6 ms	High-side	MUA08A	MSOP-8	Tape and Reel (3500 units/reel)

* Current is sampled over a fixed interval. The average current during this interval is indicated by the duty cycle of the PWM output during next interval.

Pin Description (High-Side, LM3824)

Pin	Name	Function
1	SENSE+, V_{DD}	High side of internal current sense, also supply voltage.
2	GND	Supply Ground.
3	FLTR+	Filter input — provides anti-aliasing for delta sigma modulator.
4	FLTR–	Filter input.
5	$\overline{SD}$	Shutdown input. Connected to V_{DD} through a pull-up resistor for normal operation. When low, the LM3824 is put into a low current mode.
6	TEST	Connect to GND for normal operation.
7	PWM	Digital output indicates the current magnitude and direction.
8	SENSE–	Low side of internal current sense.

National Semiconductor

LM809/LM810
3-Pin Microprocessor Reset Circuits

General Description

The LM809/810 microprocessor supervisory circuits can be used to monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down and brown-out conditions.

The function of the LM809/810 is to monitor the V_{CC} supply voltage, and assert a reset signal whenever this voltage declines below the factory-programmed reset threshold. The reset signal remains asserted for 240ms after V_{CC} rises above the threshold. The LM809 has an active-low $\overline{\text{RESET}}$ output, while the LM810 has an active-high RESET output.

Seven standard reset voltage options are available, suitable for monitoring 5V, 3.3V, and 3V supply voltages.

With a low supply current of only 15µA, the LM809/810 are ideal for use in portable equipment. The LM809/LM810 are available in the 3-pin SOT23 package.

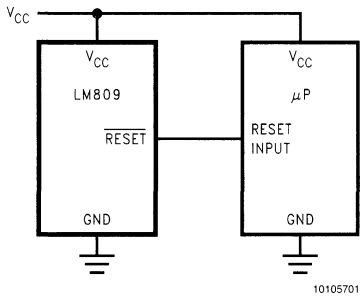
Features

- Precise monitoring of 3V, 3.3V, and 5V supply voltages
- Superior upgrade to MAX809/810
- Fully specified over temperature
- 140ms min. Power-On Reset pulse width, 240ms typical
  Active-low $\overline{\text{RESET}}$ Output (LM809)
  Active-high RESET Output (LM810)
- Guaranteed RESET Output valid for $V_{CC} \geq 1V$
- Low Supply Current, 15µA typ.
- Power supply transient immunity

Applications

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment
- Automotive

Typical Application Circuit



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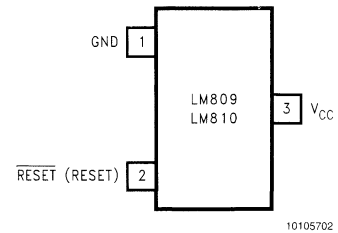
Connection Diagram



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( ) are for LM810

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Ordering Information

Reset Threshold (V)	LM809 Supplied as 1000 units, tape & reel	LM809 Supplied as 3000 units, tape & reel	Package Top Mark	Package Type	NSC Package
4.63	LM809M3-4.63	LM809M3X-4.63	S8B	SOT23-3	M03B
4.38	LM809M3-4.38	LM809M3X-4.38	S7B		
4.00	LM809M3-4.00	LM809M3X-4.00	S6B		
3.08	LM809M3-3.08	LM809M3X-3.08	S5B		
2.93	LM809M3-2.93	LM809M3X-2.93	S4B		
2.63	LM809M3-2.63	LM809M3X-2.63	S3B		
2.45	LM809M3-2.45	LM809M3X-2.45	SFB		

Reset Threshold (V)	LM810 Supplied as 1000 units, tape & reel	LM810 Supplied as 3000 units, tape & reel	Package Top Mark	Package Type	NSC Package
4.63	LM810M3-4.63	LM810M3X-4.63	SEB	SOT23-3	M03B
4.38	LM810M3-4.38	LM810M3X-4.38	SDB		
4.00	LM810M3-4.00	LM810M3X-4.00	SCB		
3.08	LM810M3-3.08	LM810M3X-3.08	SBB		
2.93	LM810M3-2.93	LM810M3X-2.93	SAB		
2.63	LM810M3-2.63	LM810M3X-2.63	S9B		

Custom voltages and improved accuracies are available, subject to minimum orders. Contact your local National Semiconductor Sales Office for information.

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground reference
2	$\overline{\text{RESET}}$ (LM809)	Active-low output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
	RESET (LM810)	Active-high output. RESET remains high while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
3	V_{CC}	Supply Voltage (+5V, +3.3V, or +3.0V)

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

General Description

The LMC6953 is a voltage supervisory chip designed to meet PCI (Peripheral Component Interconnect) Specifications Revision 2.1. It monitors 5V and 3.3V power supplies. In cases of power-up, power-down, brown-out, power failure and manual reset interrupt, the LMC6953 provides an active low reset. $\overline{\text{RESET}}$ holds low for 100 ms after both 5V and 3.3V powers recover, or after manual reset signal returns to high state. The external capacitor on pin 8 adjusts the reset delay.

This part is ideal on PCI motherboards or add-in cards to ensure the integrity of the entire system when there is a fault condition. The active low reset sets the microprocessor or local device in a known state.

The LMC6953 has a built-in bandgap reference that accurately determines all the threshold voltages. The internal reset delay circuitry eliminates additional discrete components.

Features

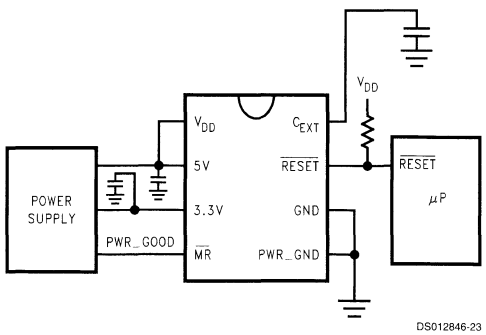
- Compliant to PCI specifications revision 2.1.
- Under and over voltage detectors for 5V and 3.3V
- Power failure detection (5V falling under 3.3V by 300 mV max)
- Manual reset input pin
- Guaranteed $\overline{\text{RESET}}$ assertion at V_{DD} = 1.5V
- Integrated reset delay circuitry
- Open drain output
- Adjustable reset delay
- Response time for over and under voltage detection: 490 ns Max
- Power failure response time: 90 ns Max
- Requires minimal external components

Applications

- Desktop PCs
- PCI-Based Systems
- Network servers

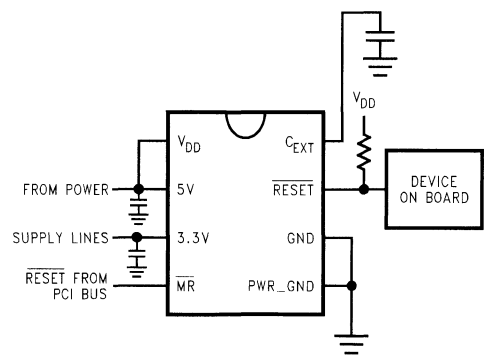
Typical Application Circuits

On Mother Board



DS012846-23

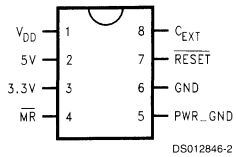
On Add-in Cards



DS012846-24

Connection Diagram

8–Pin SO



Top View

Ordering Information

Package	Industrial Temp Range −40°C to +85°C	NSC Drawing	Supplied As
8-Pin Small Outline	LMC6953CM	M08A	Rails
	LMC6953CMX		2.5k Tape and Reel

National Semiconductor

LP3470
Tiny Power On Reset Circuit

General Description

The LP3470 is a micropower CMOS voltage supervisory circuit designed to monitor power supplies in microprocessor (µP) and other digital systems. It provides maximum adjustability for power-on-reset (POR) and supervisory functions. It is available in the following six standard reset threshold voltage (V_{RTH}) options: 2.63V, 2.93V, 3.08V, 3.65V, 4.00V, 4.38V, and 4.63V. If other voltage options between 2.4V and 5.0V are desired please contact your National Semiconductor representative.

The LP3470 asserts a reset signal whenever the V_{CC} supply voltage falls below a reset threshold. The reset time-out period is adjustable using an external capacitor. Reset remains asserted for an interval (programmed by an external capacitor) after V_{CC} has risen above the threshold voltage.

The device is available in the tiny SOT23-5 package.

Key Specifications

- ±1% Reset Threshold Accuracy Over Temperature
- Standard Reset Threshold Voltages: 2.63V, 2.93V, 3.08V, 3.65V, 4.00V, 4.38V, and 4.63V
- Custom Reset Threshold Voltages: For other voltages between 2.4V and 5.0V contact your National Semiconductor representative
- Very Low Quiescent Current (16 µA typical)
- Guaranteed $\overline{\text{Reset}}$ valid down to V_{CC}=0.5V

Features

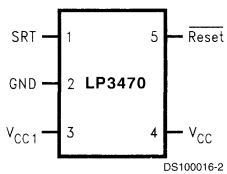
- Tiny SOT23-5 Package
- Open Drain $\overline{\text{Reset}}$ Output
- Programmable Reset Timeout Period Using an External Capacitor
- Immune to Short V_{CC} Transients

Applications

- Critical µP and µC Power Monitoring
- Intelligent Instruments
- Computers
- Portable/Battery-Powered Equipments

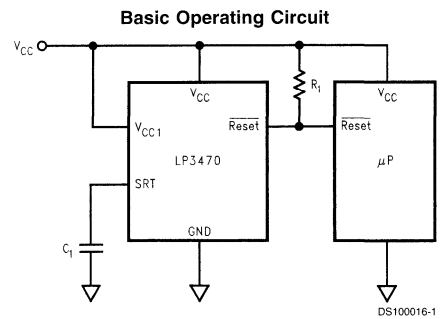
Pin Configuration and Basic Operating Circuit

Pin Configuration



Top View
See NS Package Number MF05A

Basic Operating Circuit



Ordering Information

Operating Temperature Range	Order Number	Nominal V_{RTH} (V)	Package Marking	Package Type	Supplied As
−20°C to +85°C	LP3470M5-2.63	2.63	D25B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-2.63	2.63	D25B	SOT23-5	3000 Units on Tape and Reel
	LP3470M5-2.93	2.93	D26B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-2.93	2.93	D26B	SOT23-5	3000 Units on Tape and Reel
	LP3470M5-3.08	3.08	D28B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-3.08	3.08	D28B	SOT23-5	3000 Units on Tape and Reel
	LP3470M5-3.65	3.65	D37B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-3.65	3.65	D37B	SOT23-5	3000 Units on Tape and Reel
	LP3470M5-4.00	4.00	D29B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-4.00	4.00	D29B	SOT23-5	3000 Units on Tape and Reel
	LP3470M5-4.38	4.38	D30B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-4.38	4.38	D30B	SOT23-5	3000 Units on Tape and Reel
	LP3470M5-4.63	4.63	D31B	SOT23-5	1000 Units on Tape and Reel
	LP3470M5X-4.63	4.63	D31B	SOT23-5	3000 Units on Tape and Reel
−40°C to +85°C	LP3470IM5-2.63	2.63	D25C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-2.63	2.63	D25C	SOT23-5	3000 Units on Tape and Reel
	LP3470IM5-2.93	2.93	D26C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-2.93	2.93	D26C	SOT23-5	3000 Units on Tape and Reel
	LP3470IM5-3.08	3.08	D28C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-3.08	3.08	D28C	SOT23-5	3000 Units on Tape and Reel
	LP3470IM5-3.65	3.65	D37C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-3.65	3.65	D37C	SOT23-5	3000 Units on Tape and Reel
	LP3470IM5-4.00	4.00	D29C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-4.00	4.00	D29C	SOT23-5	3000 Units on Tape and Reel
	LP3470IM5-4.38	4.38	D30C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-4.38	4.38	D30C	SOT23-5	3000 Units on Tape and Reel
	LP3470IM5-4.63	4.63	D31C	SOT23-5	1000 Units on Tape and Reel
	LP3470IM5X-4.63	4.63	D31C	SOT23-5	3000 Units on Tape and Reel

National Semiconductor

MCP809/MCP810
3-Pin Microprocessor Reset Circuits

General Description

The MCP809/810 microprocessor supervisory circuits can be used to monitor the power supplies in microprocessor and digital systems. They provide a reset to the microprocessor during power-up, power-down and brown-out conditions.

The function of the MCP809/810 is to monitor the V_{CC} supply voltage, and assert a reset signal whenever this voltage declines below the factory-programmed reset threshold. The reset signal remains asserted for 240ms after V_{CC} rises above the threshold. The MCP809 has an active-low $\overline{\text{RESET}}$ output, while the MCP810 has an active-high RESET output.

Seven standard reset voltage options are available, suitable for monitoring 5V, 3.3V, and 3V supply voltages.

With a low supply current of only 15µA, the MCP809/810 are ideal for use in portable equipment. The MCP809/MCP810 are available in the 3-pin SOT23 package.

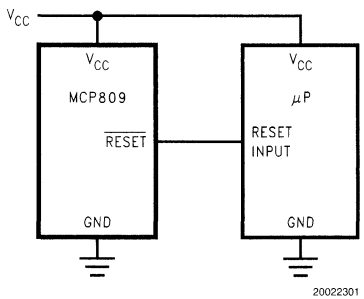
Features

- Precise monitoring of 3V, 3.3V, and 5V supply voltages
- Fully specified over temperature
- 140ms min. Power-On Reset pulse width, 240ms typical
  Active-low $\overline{\text{RESET}}$ Output (MCP809)
  Active-high RESET Output (MCP810)
- Guaranteed RESET Output valid for $V_{CC} \geq 1V$
- Low Supply Current, 15µA typ.
- Power supply transient immunity

Applications

- Microprocessor Systems
- Computers
- Controllers
- Intelligent Instruments
- Portable/Battery-Powered Equipment
- Automotive

Typical Application Circuit



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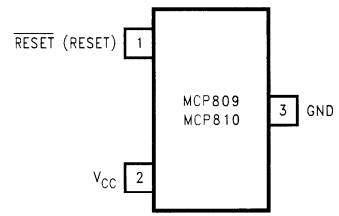
Connection Diagram



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( ) are for MCP810

Ordering Information

Reset Threshold (V)	MCP809 Supplied as 1000 units, tape & reel	MCP809 Supplied as 3000 units, tape & reel	Package Top Mark	Package Type	NSC Package
4.63	MCP809M3-4.63	MCP809M3X-4.63	SVB	SOT23-3	MF03A
4.38	MCP809M3-4.38	MCP809M3X-4.38	SUB		
4.00	MCP809M3-4.00	MCP809M3X-4.00	STB		
3.08	MCP809M3-3.08	MCP809M3X-3.08	SSB		
2.93	MCP809M3-2.93	MCP809M3X-2.93	SRB		
2.63	MCP809M3-2.63	MCP809M3X-2.63	SPB		

Reset Threshold (V)	MCP810 Supplied as 1000 units, tape & reel	MCP810 Supplied as 3000 units, tape & reel	Package Top Mark	Package Type	NSC Package
4.63	MCP810M3-4.63	MCP810M3X-4.63	SNB	SOT23-3	MF03A
4.38	MCP810M3-4.38	MCP810M3X-4.38	SLB		
4.00	MCP810M3-4.00	MCP810M3X-4.00	SKB		
3.08	MCP810M3-3.08	MCP810M3X-3.08	SJB		
2.93	MCP810M3-2.93	MCP810M3X-2.93	SHB		
2.63	MCP810M3-2.63	MCP810M3X-2.63	SGB		

Custom voltages and improved accuracies are available, subject to minimum orders. Contact your local National Semiconductor Sales Office for information.

Pin Description

PIN	NAME	FUNCTION
3	GND	Ground reference
1	$\overline{\text{RESET}}$ (MCP809)	Active-low output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
	RESET (MCP810)	Active-high output. RESET remains high while V_{CC} is below the reset threshold, and for 240ms after V_{CC} rises above the reset threshold.
2	V_{CC}	Supply Voltage (+5V, +3.3V, or +3.0V)

Section 13

Temperature Sensors and System Hardware Monitors

Section 13 Contents

National Semiconductor

Temperature Sensor Selection Guide

Device	Description	Output Type	Operating Temp Range	Accuracy (max)	Accuracy (typ)	Sensor Gain	Supply Voltage	Quiescent Current (max)
Analog Output Temperature Sensors								
LM19C	TO-92 Precision Celsius Temperature Sensor	Analog	−55°C to +130°C	±3.8°C		−11.7 mV/°C	+2.4V to +5.5V	10 µA
LM20B	SC-70 Precision Celsius Temperature Sensor	Analog	−55°C to +130°C	±2.5°C		−11.7 mV/°C	+2.4V to +5.5V	10 µA
LM20C	SC-70 Precision Celsius Temperature Sensor	Analog	−55°C to +130°C	±5.0°C		−11.7 mV/°C	+2.4V to +5.5V	10 µA
LM20S	micro SMD Precision Celsius Temperature Sensor	Analog	−40°C to +125°C	±3.5°C		−11.7 mV/°C	+2.4V to +5.5V	10 µA
LM34A	Precision Farenheit Temperature Sensor	Analog	−50°F to +300°F	±2.0°F	±0.8°F	10 mV/°F	+5V to +30V	163 µA
LM34	Precision Farenheit Temperature Sensor	Analog	−50°F to +300°F	±3.0°F	±01.6°F	10 mV/°F	+5V to +30V	181 µA
LM34CA	Precision Farenheit Temperature Sensor	Analog	−40°F to +230°F	±3.0°F	±0.8°F	10 mV/°F	+5V to +30V	142 µA
LM34C	Precision Farenheit Temperature Sensor	Analog	−40°F to +230°F	±4.0°F	±1.6°F	10 mV/°F	+5V to +30V	159 µA
LM34D	Precision Farenheit Temperature Sensor	Analog	−32°F to +212°F	±4.0°F	±1.8°F	10 mV/°F	+5V to +30V	159 µA
LM35A	Precision Celsius Temperature Sensor	Analog	−55°C to +150°C	±1.0°C	±0.4°C	10 mV/°C	+4V to +30V	133 µA
LM35	Precision Celsius Temperature Sensor	Analog	−55°C to +150°C	±1.5°C	±0.8°C	10 mV/°C	+4V to +30V	161 µA
LM35CA	Precision Celsius Temperature Sensor	Analog	−40°C to +110°C	±1.5°C	±0.4°C	10 mV/°C	+4V to +30V	116 µA
LM35C	Precision Celsius Temperature Sensor	Analog	−40°C to +110°C	±2.0°C	±0.8°C	10 mV/°C	+4V to +30V	141 µA
LM35D	Precision Celsius Temperature Sensor	Analog	0°C to +100°C	±2.0°C	±0.9°C	10 mV/°C	+4V to +30V	141 µA
LM45B	SOT-23, Celsius Temperature Sensor	Analog	−40°C to +125°C	±3.0°C −20°C to +100°C		10 mV/°C	+4V to +10V	160 µA
LM45C	SOT-23, Celsius Temperature Sensor	Analog	−40°C to +125°C	±4.0°C −20°C to +100°C		10 mV/°C	+4V to +10V	160 µA
LM50B	SOT-23, Celsius Temperature Sensor	Analog	−40°C to +150°C	±3.0°C −25°C to +100°		10 mV/°C	+4.5V to +10V	180 µA
LM50C	SOT-23, Celsius Temperature Sensor	Analog	−40°C to +150°C	±4.0°C −40°C to +125°C		10 mV/°C	+4.5V to +10V	180 µA
LM60B	2.7V,SOT-23 Celsius Temperature Sensor	Analog	−25°C to +125°C	±3.0°C		6.25 mV/°C	+2.7V to +10V	125 µA
LM60C	2.7V,SOT-23 Celsius Temperature Sensor	Analog	−40°C to +125°C	±4.0°C		6.25 mV/°C	+2.7V to +10V	125 µA
LM61B	2.7V,SOT-23 Celsius Temperature Sensor	Analog	−25°C to +85°C	±3.0°C		10 mV/°C	+2.7V to +10V	155 µA
LM61C	2.7V,SOT-23 Celsius Temperature Sensor	Analog	−30°C to +100°C	±4.0°C		10 mV/°C	+2.7V to +10V	155 µA
LM62B	2.7V,SOT-23 Celsius Temperature Sensor	Analog	0°C to +90°C	+2.5/−2°C		15.6 mV/°C	+2.7V to +10V	165 µA
LM62C	2.7V,SOT-23 Celsius Temperature Sensor	Analog	0°C to +90°C	+4/-3°C		15.6 mV/°C	+2.7V to +10V	165 µA
LM135A	Precision Shunt Celsius Temperature Sensor	Analog	−55°C to +150°C	±2.7°C	±1.3°C	10 mV/°K	Shunt Ref	0.4 mA to 5mA

Device	Description	Output Type	Operating Temp Range	Accuracy (max)	Accuracy (typ)	Sensor Gain	Supply Voltage	Quiescent Current (max)
LM135	Precision Shunt Celsius Temperature Sensor	Analog	−55°C to +150°C	±5.0°C	±2.0°C	10 mV/°K	Shunt Ref	0.4 mA to 5mA
LM235A	Precision Shunt Celsius Temperature Sensor	Analog	−40°C to +125°C	±2.7°C	±1.3°C	10 mV/°K	Shunt Ref	0.4 mA to 5mA
LM235	Precision Shunt Celsius Temperature Sensor	Analog	−40°C to +125°C	±5.0°C	±2.0°C	10 mV/°K	Shunt Ref	0.4 mA to 5mA
LM335A	Precision Shunt Celsius Temperature Sensor	Analog	−40°C to +100°C	±5.0°C	±2.0°C	10 mV/°K	Shunt Ref	0.4 mA to 5mA
LM335	Precision Shunt Celsius Temperature Sensor	Analog	−40°C to +100°C	±9.0°C	±4.0°C	10 mV/°K	Shunt Ref	0.4 mA to 5mA
Digital Output Temperature Sensor								
LM26	SOT-23, Low Power, Factory Preset Thermostat	Thermo-stat/ Analog	−55°C to +120°C	±3.0°C −55°C to +110°C		-10.82 mV/°C	+2.7V to +5.5V	10µA
LM56B	Low Power Dual Output Thermostat	Thermo-stat/ Analog	−40°C to +125°C	±2.0°C −25°C to +85°C		6.2 mV/°C	+2.7V to +10V	230 µA
LM56C	Low Power Dual Output Thermostat	Thermo-stat/ Analog	−40°C to +125°C	±3.0°C −25°C to +85°C		6.2 mV/°C	+2.7V to +10V	230 µA
LM66	Dual Output Thermostat, Preset at +73°C and +82°C	Thermo-stat/ Analog	−40°C to +125°C	±3.0°C −25°C to +85°C		6.2 mV/°C	+2.7V to +10V	250 µA
LM70	SPI/MICROWIRE, 10-Bit Plus Sign Temperature Sensor	3-Wire Serial	−55°C to +150°C	+1.5/−2.0°C −10°C to 60°C		0.25°C /LSB	+2.65V to +5.5V	490 µA
LM74	SPI/MICROWIRE, 12-Bit Plus Sign Temperature Sensor	3-Wire Serial	−40°C to +125°C	±1.25°C		0.0625°C /LSB	+3.0V to +5.5V	520 µA
LM75	8-bit Plus Sign, Temperature Sensor	2-Wire Serial*, $\overline{OS}$	−55°C to +125°C	±3.0°C		0.5°C /LSB	+3.0V to +5.5V	1 mA
LM76CNM	12-Bit Plus Sign, ACPI Temperature Sensor	2-Wire Serial*, $\overline{T\_CRIT\_A}$, $\overline{INT}$	−55°C to +150°C	±1.0°C +70°C to +100°C		0.0625°C /LSB	+3.0V to +3.6V	500 µA
LM76CHM	12-Bit Plus Sign, ACPI Temperature Sensor	2-Wire Serial*, $\overline{T\_CRIT\_A}$, $\overline{INT}$	−55°C to +150°C	±1.0°C −10°C to +45°C		0.0625°C /LSB	+4.5V to +5.5V	450 µA
LM77	12-Bit Plus Sign, ACPI Temperature Sensor	2-Wire Serial*, $\overline{T\_CRIT\_A}$, $\overline{INT}$	−55°C to +125°C	±1.5°C −10°C to +65°C		0.5°C /LSB	+3.0V to +5.5V	500 µA
LM82	7-Bit Plus Sign, Remote Diode Temperature Sensor	2-Wire Serial*, $\overline{T\_CRIT\_A}$, $\overline{INT}$	−40°C to +125°C	±3.0°C +25°C to +100°C		1°C /LSB	+3.0V to +3.6V	800 µA
LM83	7-Bit Plus Sign, Triple Remote Diode Temperature Sensor	2-Wire Serial*, $\overline{T\_CRIT\_A}$, $\overline{INT}$	−40°C to +125°C	±3.0°C +25°C to +100°C		1°C /LSB	+3.0V to +3.6V	800 µA
LM84	7-Bit Plus Sign, Remote Diode Temperature Sensor	2-Wire Serial*, $\overline{INT}$	0°C to +125°C	±4.0°C +60°C to +100°C		1°C /LSB	+3.0V to +3.6V	1 mA
LM86	10-Bit Plus Sign, Remote Diode Temperature Sensor	2-Wire Serial*, $\overline{ALERT}$, $\overline{T\_CRIT\_A}$	0°C to +85°C	±1.0°C +60°C to +100°C		0.125°C /LSB	+3.0V to +3.6V	0.78 mA (typ)
LM88	Factory Programmable Dual Remote-Diode Thermostat	Thermostat	0°C to +125°C	±3.0°C +60°C to +100°C			2.8V to 3.8V	1.5 mA
LM90	10-Bit Plus Sign, Remote Diode Temperature Sensor	2-Wire Serial*, $\overline{ALERT}$, $\overline{T\_CRIT\_A}$	0°C to +85°C	±3.0°C +60°C to +100°C		0.125°C /LSB	+3.0V to +3.6V	0.78 mA (typ)
LM91	7-Bit Plus Sign, Remote Diode Temperature Sensor	2-Wire Serial*, $\overline{INT}$	0°C to +125°C	±4.0°C +60°C to +100°C		1°C /LSB	+3.0V to +3.6V	1 mA

Device	Description	Output Type	Operating Temp Range	Accuracy		Sensor Gain	Supply Voltage	Quiescent Current (max)
				(max)	(typ)			
LM92CIM	12-Bit Plus Sign Temperature Sensor	2-Wire Serial*, $\overline{T\_CRIT\_A}$, $\overline{INT}$	−55°C to +150°C	±0.33°C at +30°C		0.0625°C /LSB	+2.7V to +5.5V	625 µA

* - SMBus or I^2C compatible

National Semiconductor

System Hardware Monitor Selection Guide

Device	Description	Operating Temp Range	Voltage Monitoring Accuracy (max)	Temperature Sensor Accuracy (max)	Sensor Gain	Supply Voltage (V)	Quiescent Current (mA)
LM78	ISA Bus/2 Wire Serial System Hardware Monitor (Not Recommended for New Designs)	−40°C to +125°C	±1%	±3.0°C	1°C/LSB	+4.25V to 5.75V	2 mA
LM79	ISA Bus/2 Wire Serial System Hardware Monitor (Not Recommended for New Designs)	−40°C to +125°C	±1%	±3.0°C	1°C/LSB	+4.25V to 5.75V	2 mA
LM80	2 Wire Serial System Hardware Monitor	−25°C to +125°C	±1%	±3.0°C	0.0625°C /LSB	+2.8V to +5.75V	1.5 mA
LM81B	SMBus System Hardware Monitor (D/A Output and Input Scaling Resistors)	−40°C to +125°C	±1.2%	±3.0°C	0.0625°C /LSB	+2.8V to +3.8V	1.4 mA
LM87	SMBus Remote Diode System Hardware Monitor (with D/A Output and Input Scaling Resistors)	−40°C to +125°C	±2%	±3.0°C (internal) ±4 (remote diode)	1°C/LSB	+2.8V to +3.8V	2.0 mA

National Semiconductor

LM19
2.4V, 10µA, TO-92 Temperature Sensor

General Description

The LM19 is a precision analog output CMOS integrated-circuit temperature sensor that operates over a −55˚C to +130˚C temperature range. The power supply operating range is +2.4 V to +5.5 V. The transfer function of LM19 is predominately linear, yet has a slight predictable parabolic curvature. The accuracy of the LM19 when specified to a parabolic transfer function is ±2.5˚C at an ambient temperature of +30˚C. The temperature error increases linearly and reaches a maximum of ±3.8˚C at the temperature range extremes. The temperature range is affected by the power supply voltage. At a power supply voltage of 2.7 V to 5.5 V the temperature range extremes are +130˚C and −55˚C. Decreasing the power supply voltage to 2.4 V changes the negative extreme to −30˚C, while the positive remains at +130˚C.

The LM19's quiescent current is less than 10 µA. Therefore, self-heating is less than 0.02˚C in still air. Shutdown capability for the LM19 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates or does not necessitate shutdown at all.

Applications

- Cellular Phones
- Computers
- Power Supply Modules
- Battery Management
- FAX Machines
- Printers
- HVAC
- Disk Drives
- Appliances

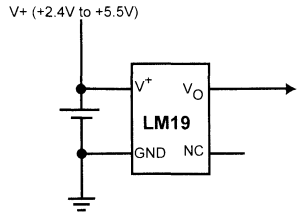
Features

- Rated for full −55˚C to +130˚C range
- Available in a TO-92 package
- Predictable curvature error
- Suitable for remote applications

Key Specifications

■ Accuracy at +30˚C	±2.5 ˚C (max)
■ Accuracy at +130˚C & −55˚C	±3.5 to ±3.8 ˚C (max)
■ Power Supply Voltage Range	+2.4V to +5.5V
■ Current Drain	10 µA (max)
■ Nonlinearity	±0.4 % (typ)
■ Output Impedance	160 Ω (max)
■ Load Regulation	
0 µA < I_L < +16 µA	−2.5 mV (max)

Typical Application



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$$V_O = (-3.88 \times 10^{-6} \times T^2) + (-1.15 \times 10^{-2} \times T) + 1.8639$$

or

$$T = -1481.96 + \sqrt{2.1962 \times 10^{6} + \frac{(1.8639 - V_O)}{3.88 \times 10^{-6}}}$$

where:

T is temperature, and V_O is the measured output voltage of the LM19.

Output Voltage vs Temperature

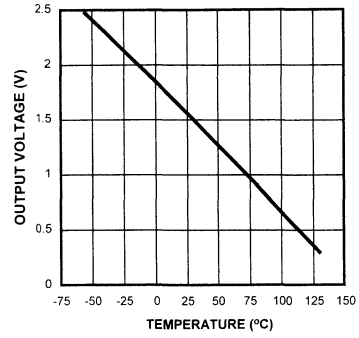

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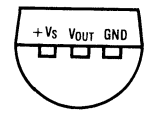
FIGURE 1. Full-Range Celsius (Centigrade) Temperature Sensor (−55˚C to +130˚C) Operating from a Single Li-Ion Battery Cell

Typical Application (Continued)

Temperature (T)	Typical V_O
+130˚C	+303 mV
+100˚C	+675 mV
+80˚C	+919 mV
+30˚C	+1515 mV
+25˚C	+1574 mV
0˚C	+1863.9 mV
−30˚C	+2205 mV
−40˚C	+2318 mV
−55˚C	+2485 mV

Connection Diagram

TO-92



BOTTOM VIEW

20004001

See NS Package Number Z03A

Ordering Information

Order Number	Temperature Accuracy	Temperature Range	NS Package Number	Device Marking	Transport Media
LM19CIZ	±3.8˚C	−55˚C to +130˚C	Z03A	LM19CIZ	Bulk

National Semiconductor

LM20
2.4V, 10µA, SC70, micro SMD Temperature Sensor

General Description

The LM20 is a precision analog output CMOS integrated-circuit temperature sensor that operates over a −55˚C to +130˚C temperature range. The power supply operating range is +2.4 V to +5.5 V. The transfer function of LM20 is predominately linear, yet has a slight predictable parabolic curvature. The accuracy of the LM20 when specified to a parabolic transfer function is ±1.5˚C at an ambient temperature of +30˚C. The temperature error increases linearly and reaches a maximum of ±2.5˚C at the temperature range extremes. The temperature range is affected by the power supply voltage. At a power supply voltage of 2.7 V to 5.5 V the temperature range extremes are +130˚C and −55˚C. Decreasing the power supply voltage to 2.4 V changes the negative extreme to −30˚C, while the positive remains at +130˚C.

The LM20's quiescent current is less than 10 µA. Therefore, self-heating is less than 0.02˚C in still air. Shutdown capability for the LM20 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates or does not necessitate shutdown at all.

Applications

- Cellular Phones
- Computers
- Power Supply Modules
- Battery Management
- FAX Machines
- Printers
- HVAC
- Disk Drives
- Appliances

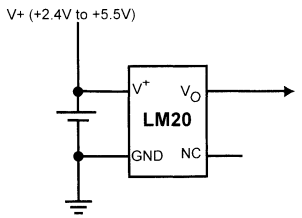
Features

- Rated for full −55˚C to +130˚C range
- Available in an SC70 and a micro SMD package
- Predictable curvature error
- Suitable for remote applications

Key Specifications

■ Accuracy at +30˚C	±1.5 to ±4 ˚C (max)
■ Accuracy at +130˚C & −55˚C	±2.5 to ±5 ˚C (max)
■ Power Supply Voltage Range	+2.4V to +5.5V
■ Current Drain	10 µA (max)
■ Nonlinearity	±0.4 % (typ)
■ Output Impedance	160 Ω (max)
■ Load Regulation 0 µA < I_L < +16 µA	−2.5 mV (max)

Typical Application



DS100908-2

$$V_O = (-3.88x10^{-6}xT^2) + (-1.15x10^{-2}xT) + 1.8639$$

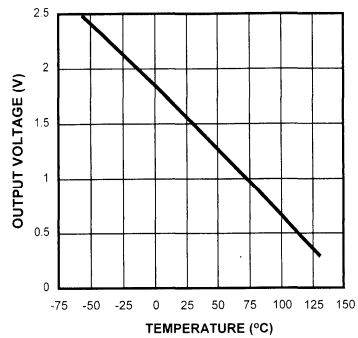
or

$$T = -1481.96 + \sqrt{2.1962 \times 10^{6} + \frac{(1.8639 - V_O)}{3.88 \times 10^{-6}}}$$

where:

T is temperature, and V_O is the measured output voltage of the LM20.

Output Voltage vs Temperature



DS100908-24

Full-Range Celsius (Centigrade) Temperature Sensor (−55˚C to +130˚C) Operating from a Single Li-Ion Battery Cell

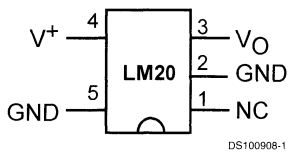
Typical Application (Continued)

Temperature (T)	Typical V_O
+130˚C	+303 mV
+100˚C	+675 mV
+80˚C	+919 mV
+30˚C	+1515 mV

Temperature (T)	Typical V_O
+25˚C	+1574 mV
0˚C	+1863.9 mV
−30˚C	+2205 mV
−40˚C	+2318 mV
−55˚C	+2485 mV

Connection Diagrams

SC70-5



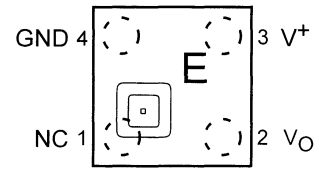
DS100908-1

Note:

- GND (pin 2) may be grounded or left floating. For optimum thermal conductivity to the pc board ground plane pin 2 should be grounded.
- NC (pin 1) should be left floating or grounded. Other signal traces should not be connected to this pin.

Top View
See NS Package Number MAA05A

micro SMD



DS100908-32

Note:

- Pin numbers are referenced to the package marking text orientation.
- Reference JEDEC Registration MO-211, variation BA
- The actual physical placement of package marking will vary slightly from part to part. The package marking will designate the date code and will vary considerably. Package marking does not correlate to device type in any way.

Top View
See NS Package Number BPA04DDC

Ordering Information

Order Number	Temperature Accuracy	Temperature Range	NS Package Number	Device Marking	Transport Media
LM20BIM7	±2.5˚C	−55˚C to +130˚C	MAA05A	T2B	1000 Units on Tape and Reel
LM20BIM7X	±2.5˚C	−55˚C to +130˚C	MAA05A	T2B	3000 Units on Tape and Reel
LM20CIM7	±5˚C	−55˚C to +130˚C	MAA05A	T2C	1000 Units on Tape and Reel
LM20CIM7X	±5˚C	−55˚C to +130˚C	MAA05A	T2C	3000 Units on Tape and Reel
LM20SIBP	±3.5˚C	−40˚C to +125˚C	BPA04DDC	Date Code	250 Units on Tape and Reel
LM20SIBPX	±3.5˚C	−40˚C to +125˚C	BPA04DDC	Date Code	3000 Units on Tape and Reel

National Semiconductor

LM26
SOT-23, ±3°C Accurate, Factory Preset Thermostat

General Description

The LM26 is a precision, single digital-output, low-power thermostat comprised of an internal reference, DAC, temperature sensor and comparator. Utilizing factory programming, it can be manufactured with different trip points as well as different digital output functionality. The trip point (T_{OS}) can be preset at the factory to any temperature in the range of −55°C to +110°C in 1°C increments. The LM26 has one digital output (OS/$\overline{OS}$/US/$\overline{US}$), one digital input (HYST) and one analog output (V_{TEMP}). The digital output stage can be preset as either open-drain or push-pull. In addition, it can be factory programmed to be active HIGH or LOW. The digital output can be factory programmed to indicate an over temperature shutdown event (OS or $\overline{OS}$) or an under temperature shutdown event (US or $\overline{US}$). When preset as an overtemperature shutdown ($\overline{OS}$) it will go LOW to indicate that the die temperature is over the internally preset T_{OS} and go HIGH when the temperature goes below (T_{OS}−T_{HYST}). Similarly, when preprogrammed as an undertemperature shutdown (US) it will go HIGH to indicate that the temperature is below T_{US} and go LOW when the temperature is above (T_{US}+T_{HYST}). The typical hysteresis, T_{HYST}, can be set to 2°C or 10°C and is controlled by the state of the HYST pin. A V_{TEMP} analog output provides a voltage that is proportional to temperature and has a −10.82mV/°C output slope.

Available parts are detailed in the ordering information. For other part options, contact a National Semiconductor Distributor or Sales Representative for information on minimum order qualification. The LM26 is currently available in a 5-lead SOT-23 package.

Applications

- Microprocessor Thermal Management
- Appliances
- Portable Battery Powered Systems
- Fan Control
- Industrial Process Control
- HVAC Systems
- Remote Temperature Sensing
- Electronic System Protection

Features

- Internal comparator with pin programmable 2°C or 10°C hysteresis
- No external components required
- Open Drain or push-pull digital output; supports CMOS logic levels
- Internal temperature sensor with V_{TEMP} output pin
- V_{TEMP} output allows after-assembly system testing
- Internal voltage reference and DAC for trip-point setting
- Currently available in 5-pin SOT-23 plastic package
- Excellent power supply noise rejection

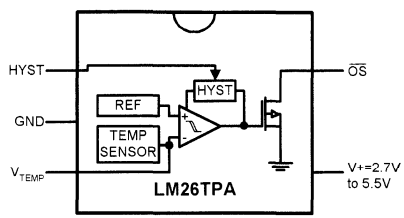
Key Specifications

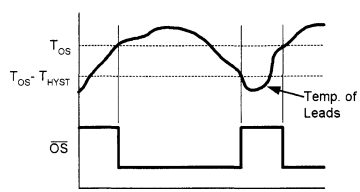
■ Power Supply Voltage	2.7V to 5.5V
■ Power Supply Current	40µA (max)
	20µA (typ)
■ Hysteresis Temperature	2°C or 10°C (typ)

Temperature Trip Point Accuracy

Temperature Range	LM26CIM
−55°C to +110°C	±3°C (max)
+120°C	±4°C (max)

LM26CIM5-TPA Simplified Block Diagram and Connection Diagram





HYST=GND for 10°C Hysteresis
HYST=V+ for 2°C Hysteresis
V_{TEMP}=(-3.479x10^{-6}x(T-30)^2)+(-1.082x10^{-2}x(T-30))+1.8015V

10132301

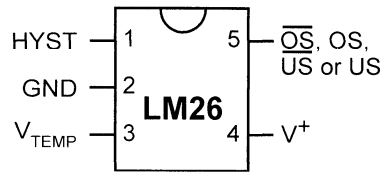
The LM26CIM5-TPA has a fixed trip point of 85°C.
For other trip point and output function availability, please see ordering information or contact National Semiconductor.

Ordering Information

For more detailed information on the suffix meaning see the part number template at the end of the Electrical Characteristics Section. Contact National Semiconductor for other set points and output options.

Order Number			NS Package		
Bulk Rail	3000 Units in Tape & Reel	Top Mark	Number	Trip Point Setting	Output Function
LM26CIM5-KLA	LM26CIM5X-KLA	TKLA	MA05B	23˚C	Open Drain $\overline{OS}$
LM26CIM5-NPA	LM26CIM5X-NPA	TNPA	MA05B	45˚C	Open Drain $\overline{OS}$
LM26CIM5-RPA	LM26CIM5X-RPA	TRPA	MA05B	65˚C	Open Drain $\overline{OS}$
LM26CIM5-TPA	LM26CIM5X-TPA	TTPA	MA05B	85˚C	Open Drain $\overline{OS}$
LM26CIM5-VHA	LM26CIM5X-VHA	TVHA	MA05B	90˚C	Open Drain $\overline{OS}$
LM26CIM5-VPA	LM26CIM5X-VPA	TVPA	MA05B	95˚C	Open Drain $\overline{OS}$
LM26CIM5-XHA	LM26CIM5X-XHA	TXHA	MA05B	100˚C	Open Drain $\overline{OS}$
LM26CIM5-XPA	LM26CIM5X-XPA	TXPA	MA05B	105˚C	Open Drain $\overline{OS}$
LM26CIM5-YHA	LM26CIM5X-YHA	TYHA	MA05B	110˚C	Open Drain $\overline{OS}$
LM26CIM5-YPA	LM26CIM5X-YPA	TYPA	MA05B	115˚C	Open Drain $\overline{OS}$
LM26CIM5-ZHA	LM26CIM5X-ZHA	TZHA	MA05B	120˚C	Open Drain $\overline{OS}$

Connection Diagram



10132302

Pin Description

Pin Number	Pin Name	Function	Connection
1	HYST	Hysteresis control, digital input	GND for 10˚C or V^+ for 2˚C
2	GND	Ground, connected to the back side of the die through lead frame.	System GND
3	V_{TEMP}	Analog output voltage proportional to temperature	Leave floating or connect to a high impedance node.
4	V^+	Supply input	2.7V to 5.5V with a 0.1µF bypass capacitor. For PSRR information see *Section Titled NOISE CONSIDERATIONS.*
5	$\overline{OS}$	Overtemperature Shutdown open-drain active low thermostat digital output	Controller interrupt, system or power supply shutdown; pull-up resistor ≥ 10kΩ
	OS	Overtemperature Shutdown totem-pull active high thermostat digital output	Controller interrupt, system or power supply shutdown
	$\overline{US}$	Undertemperature Shutdown open-drain active low thermostat digital output	System or power supply shutdown; pull-up resistor ≥ 10kΩ
	US	Undertemperature Shutdown totem-pull active high thermostat digital output	System or power supply shutdown

Note: pin 5 functionality and trip point setting are programmed during LM26 manufacture.

National Semiconductor

LM34
Precision Fahrenheit Temperature Sensors

General Description

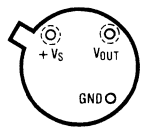
The LM34 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Fahrenheit temperature. The LM34 thus has an advantage over linear temperature sensors calibrated in degrees Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Fahrenheit scaling. The LM34 does not require any external calibration or trimming to provide typical accuracies of ±½°F at room temperature and ±1½°F over a full −50 to +300°F temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM34's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies or with plus and minus supplies. As it draws only 75 µA from its supply, it has very low self-heating, less than 0.2°F in still air. The LM34 is rated to operate over a −50° to +300°F temperature range, while the LM34C is rated for a −40° to +230°F range (0°F with improved accuracy). The LM34 series is available packaged in hermetic TO-46 transistor packages, while the LM34C, LM34CA and LM34D are also available in the plastic TO-92 transistor package. The LM34D is also available in an 8-lead surface mount small outline package. The LM34 is a complement to the LM35 (Centigrade) temperature sensor.

Features

- Calibrated directly in degrees Fahrenheit
- Linear +10.0 mV/°F scale factor
- 1.0°F accuracy guaranteed (at +77°F)
- Rated for full −50° to +300°F range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 5 to 30 volts
- Less than 90 µA current drain
- Low self-heating, 0.18°F in still air
- Nonlinearity only ±0.5°F typical
- Low-impedance output, 0.4Ω for 1 mA load

Connection Diagrams

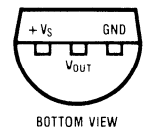
TO-46
Metal Can Package
(Note 1)



DS006685-1

Order Numbers LM34H, LM34AH, LM34CH, LM34CAH or LM34DH
See NS Package Number H03H

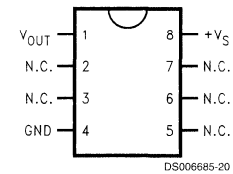
TO-92
Plastic Package



BOTTOM VIEW
DS006685-2

Order Number LM34CZ, LM34CAZ or LM34DZ
See NS Package Number Z03A

SO-8
Small Outline
Molded Package



DS006685-20

N.C. = No Connection

Top View
Order Number LM34DM
See NS Package Number M08A

Note 1: Case is connected to negative pin (GND).

Typical Applications

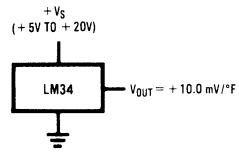


FIGURE 1. Basic Fahrenheit Temperature Sensor (+5° to +300°F)

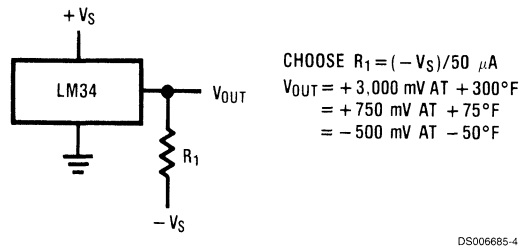


FIGURE 2. Full-Range Fahrenheit Temperature Sensor

National Semiconductor

LM35
Precision Centigrade Temperature Sensors

General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 µA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-220 package.

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 µA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

Typical Applications

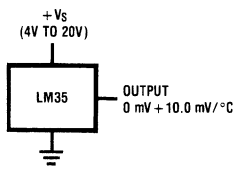
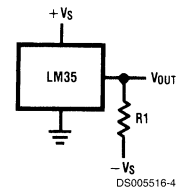


FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)



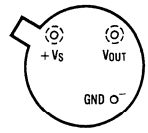
Choose $R_1 = -V_S/50\ \mu A$
V_{OUT} = +1,500 mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

FIGURE 2. Full-Range Centigrade Temperature Sensor

13

Connection Diagrams

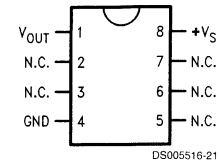
TO-46
Metal Can Package*



*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

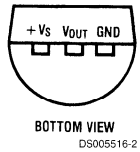
SO-8
Small Outline Molded Package



N.C. = No Connection

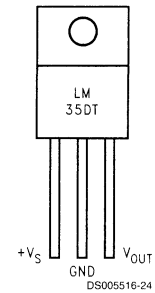
Top View
Order Number LM35DM
See NS Package Number M08A

TO-92
Plastic Package



Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

TO-220
Plastic Package*



*Tab is connected to the negative pin (GND).
Note: The LM35DT pinout is different than the discontinued LM35DP.

Order Number LM35DT
See NS Package Number TA03F

National Semiconductor

LM45
SOT-23 Precision Centigrade Temperature Sensors

General Description

The LM45 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM45 does not require any external calibration or trimming to provide accuracies of ±2°C at room temperature and ±3°C over a full −20 to +100°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM45's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with a single power supply, or with plus and minus supplies. As it draws only 120 µA from its supply, it has very low self-heating, less than 0.2°C in still air. The LM45 is rated to operate over a −20° to +100°C temperature range.

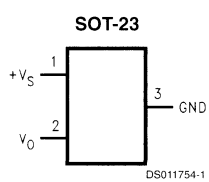
Applications

- Battery Management
- FAX Machines
- Printers
- Portable Medical Instruments
- HVAC
- Power Supply Modules
- Disk Drives
- Computers
- Automotive

Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- ±3°C accuracy guaranteed
- Rated for full −20° to +100°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4.0V to 10V
- Less than 120 µA current drain
- Low self-heating, 0.20°C in still air
- Nonlinearity only ±0.8°C max over temp
- Low impedance output, 20Ω for 1 mA load

Connection Diagram



Top View
See NS Package Number MA03B

Order Number	SOT-23 Device Marking	Supplied As
LM45BIM3	T4B	1000 Units on Tape and Reel
LM45BIM3X	T4B	3000 Units on Tape and Reel
LM45CIM3	T4C	1000 Units on Tape and Reel
LM45CIM3X	T4C	3000 Units on Tape and Reel

Typical Applications

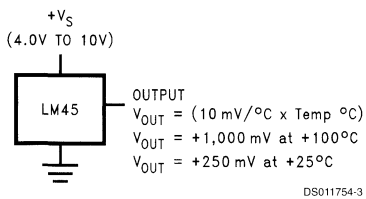
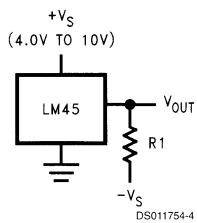


FIGURE 1. Basic Centigrade Temperature Sensor (+2.5°C to +100°C)



Choose $R_1 = -V_S/50\ \mu A$
V_{OUT}= (10 mV/°C x Temp °C)
V_{OUT} = +1,000 mV at +100°C
= +250 mV at +25°C
= −200 mV at −20°C

FIGURE 2. Full-Range Centigrade Temperature Sensor (−20°C to +100°C)

National Semiconductor

LM50
SOT-23 Single-Supply Centigrade Temperature Sensor

General Description

The LM50 is a precision integrated-circuit temperature sensor that can sense a −40°C to +125°C temperature range using a single positive supply. The LM50's output voltage is linearly proportional to Celsius (Centigrade) temperature (+10 mV/°C) and has a DC offset of +500 mV. The offset allows reading negative temperatures without the need for a negative supply. The ideal output voltage of the LM50 ranges from +100 mV to +1.75V for a −40°C to +125°C temperature range. The LM50 does not require any external calibration or trimming to provide accuracies of ±3°C at room temperature and ±4°C over the full −40°C to +125°C temperature range. Trimming and calibration of the LM50 at the wafer level assure low cost and high accuracy. The LM50's linear output, +500 mV offset, and factory calibration simplify circuitry required in a single supply environment where reading negative temperatures is required. Because the LM50's quiescent current is less than 130 µA, self-heating is limited to a very low 0.2°C in still air.

Applications

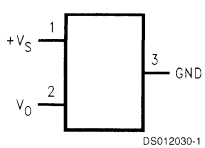
- Computers
- Disk Drives
- Battery Management
- Automotive
- FAX Machines
- Printers
- Portable Medical Instruments
- HVAC
- Power Supply Modules

Features

- Calibrated directly in degree Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- ±2°C accuracy guaranteed at +25°C
- Specified for full −40° to +125°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4.5V to 10V
- Less than 130 µA current drain
- Low self-heating, less than 0.2°C in still air
- Nonlinearity less than 0.8°C over temp

Connection Diagram

SOT-23



Top View
See NS Package Number MA03B

Order Number	SOT-23 Device Marking	Supplied As
LM50BIM3	T5B	1000 Units on Tape and Reel
LM50CIM3	T5C	1000 Units on Tape and Reel
LM50BIM3X	T5B	3000 Units on Tape and Reel
LM50CIM3X	T5C	3000 Units on Tape and Reel

Typical Application

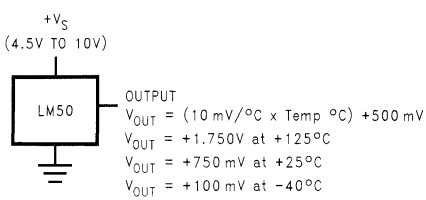


FIGURE 1. Full-Range Centigrade Temperature Sensor (−40°C to +125°C)

National Semiconductor

LM56
Dual Output Low Power Thermostat

General Description

The LM56 is a precision low power thermostat. Two stable temperature trip points (V_{T1} and V_{T2}) are generated by dividing down the LM56 1.250V bandgap voltage reference using 3 external resistors. The LM56 has two digital outputs. OUT1 goes LOW when the temperature exceeds T1 and goes HIGH when the the temperature goes below ($T1-T_{HYST}$). Similarly, OUT2 goes LOW when the temperature exceeds T2 and goes HIGH when the temperature goes below ($T2-T_{HYST}$). T_{HYST} is an internally set 5°C typical hysteresis.

The LM56 is available in an 8-lead Mini-SO8 surface mount package and an 8-lead small outline package.

Applications

- Microprocessor Thermal Management
- Appliances
- Portable Battery Powered 3.0V or 5V Systems
- Fan Control
- Industrial Process Control
- HVAC Systems
- Remote Temperature Sensing
- Electronic System Protection

Features

- Digital outputs support TTL logic levels
- Internal temperature sensor
- 2 internal comparators with hysteresis
- Internal voltage reference
- Currently available in 8-pin SO plastic package
- Future availability in the 8-pin Mini-SO8 package

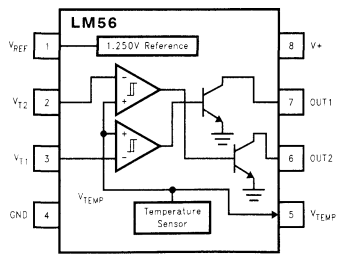
Key Specifications

- Power Supply Voltage 2.7V–10V
- Power Supply Current 230 µA (max)
- V_{REF} 1.250V ±1% (max)
- Hysteresis Temperature 5°C
- Internal Temperature Sensor Output Voltage (+6.20 mV/°C x T) +395 mV

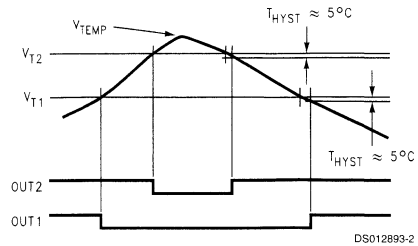
Temperature Trip Point Accuracy:

	LM56BIM	LM56CIM
+25°C	±2°C (max)	±3°C (max)
+25°C to +85°C	±2°C (max)	±3°C (max)
−40°C to +125°C	±3°C (max)	±4°C (max)

Simplified Block Diagram and Connection Diagram



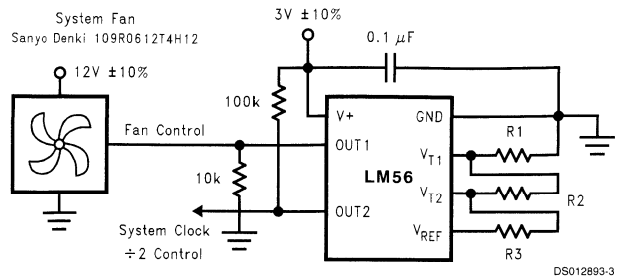
DS012893-1



DS012893-2

Order Number	LM56BIM	LM56BIMX	LM56CIM	LM56CIMX	LM56BIMM	LM56BIMMX	LM56CIMM	LM56CIMMX
NS Package Number	M08A	M08A	M08A	M08A	MUA08A	MUA08A	MUA08A	MUA08A
	SOP-8	SOP-8	SOP-8	SOP-8	MSOP-8	MSOP-8	MSOP-8	MSOP-8
Transport Media	Rail	2500 Units Tape & Reel	Rail	2500 Units Tape & Reel	Rail	3500 Units Tape & Reel	Rail	3500 Units Tape & Reel
Package Marking	LM56BIM	LM56BIM	LM56CIM	LM56CIM	T02B	T02B	T02C	T02C

Typical Application



V_{T1} = 1.250V x (R1)/(R1 + R2 + R3)
V_{T2} = 1.250V x (R1 + R2)/(R1 + R2 + R3)
where:
(R1 + R2 + R3) = 27 kΩ and
$V_{T1\ or\ T2}$ = [6.20 mV/°C x T] + 395 mV therefore:
R1 = V_{T1}/(1.25V) x 27 kΩ
R2 = (V_{T2}/(1.25V) x 27 kΩ) − R1
R3 = 27 kΩ − R1 − R2

FIGURE 1. Microprocessor Thermal Management

National Semiconductor

LM60
2.7V, SOT-23 or TO-92 Temperature Sensor

General Description

The LM60 is a precision integrated-circuit temperature sensor that can sense a −40˚C to +125˚C temperature range while operating from a single +2.7V supply. The LM60's output voltage is linearly proportional to Celsius (Centigrade) temperature (+6.25 mV/˚C) and has a DC offset of +424 mV. The offset allows reading negative temperatures without the need for a negative supply. The nominal output voltage of the LM60 ranges from +174 mV to +1205 mV for a −40˚C to +125˚C temperature range. The LM60 is calibrated to provide accuracies of ±2.0˚C at room temperature and ±3˚C over the full −25˚C to +125˚C temperature range.

The LM60's linear output, +424 mV offset, and factory calibration simplify external circuitry required in a single supply environment where reading negative temperatures is required. Because the LM60's quiescent current is less than 110 µA, self-heating is limited to a very low 0.1˚C in still air in the SOT-23 package. Shutdown capability for the LM60 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates.

Features

- Calibrated linear scale factor of +6.25 mV/˚C
- Rated for full −40˚ to +125˚C range
- Suitable for remote applications
- Available in SOT-23 and TO-92 packages

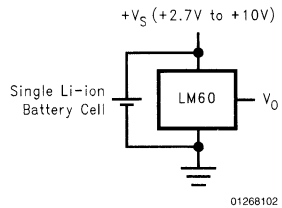
Applications

- Cellular Phones
- Computers
- Power Supply Modules
- Battery Management
- FAX Machines
- Printers
- HVAC
- Disk Drives
- Appliances

Key Specifications

- Accuracy at 25˚C: ±2.0 and ±3.0˚C (max)
- Accuracy for −40˚C to +125˚C: ±4.0˚C (max)
- Accuracy for −25˚C to +125˚C: ±3.0˚C (max)
- Temperature Slope: +6.25mV/˚C
- Power Supply Voltage Range: +2.7V to +10V
- Current Drain @ 25˚C: 110µA (max)
- Nonlinearity: ±0.8˚C (max)
- Output Impedance: 800Ω (max)

Typical Application



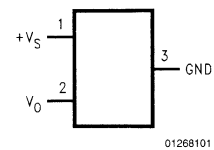
V_O = (+6.25 mV/˚C x T ˚C) + 424 mV

Temperature (T)	Typical V_O
+125˚C	+1205 mV
+100˚C	+1049 mV
+25˚C	+580 mV
0˚C	+424 mV
−25˚C	+268 mV
−40˚C	+174 mV

FIGURE 1. Full-Range Centigrade Temperature Sensor (−40˚C to +125˚C) Operating from a Single Li-Ion Battery Cell

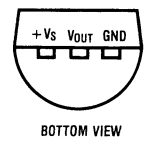
Connection Diagrams

SOT-23



Top View
See NS Package Number MA03B

TO-92



See NS Package Number Z03A

Ordering Information

Order Number	Device Marking	Supplied In	Accuracy Over Specified Temperature Range	Specified Temperature Range	Package Type
LM60BIM3	T6B	1000 Units on Tape and Reel	±3	$-25^{\circ}C \leq T_A \leq +125^{\circ}C$	SOT-23
LM60BIM3X	T6B	3000 Units on Tape and Reel			
LM60CIM3	T6C	1000 Units on Tape and Reel	±4	$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	
LM60CIM3X	T6C	3000 Units on Tape and Reel			
LM60BIZ	LM60BIZ	Bulk	±3	$-25^{\circ}C \leq T_A \leq +125^{\circ}C$	TO-92
LM60CIZ	LM60CIZ	Bulk	±4	$-40^{\circ}C \leq T_A \leq +125^{\circ}C$	

National Semiconductor

LM61
2.7V, SOT-23 or TO-92 Temperature Sensor

General Description

The LM61 is a precision integrated-circuit temperature sensor that can sense a −30˚C to +100˚C temperature range while operating from a single +2.7V supply. The LM61's output voltage is linearly proportional to Celsius (Centigrade) temperature (+10 mV/˚C) and has a DC offset of +600 mV. The offset allows reading negative temperatures without the need for a negative supply. The nominal output voltage of the LM61 ranges from +300 mV to +1600 mV for a −30˚C to +100˚C temperature range. The LM61 is calibrated to provide accuracies of ±2.0˚C at room temperature and ±3˚C over the full −25˚C to +85˚C temperature range.

The LM61's linear output, +600 mV offset, and factory calibration simplify external circuitry required in a single supply environment where reading negative temperatures is required. Because the LM61's quiescent current is less than 125 µA, self-heating is limited to a very low 0.2˚C in still air. Shutdown capability for the LM61 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates.

Features

- Calibrated linear scale factor of +10 mV/˚C
- Rated for full −30˚ to +100˚C range
- Suitable for remote applications

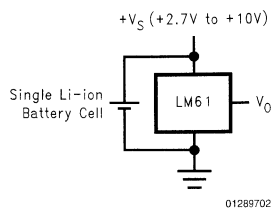
Applications

- Cellular Phones
- Computers
- Power Supply Modules
- Battery Management
- FAX Machines
- Printers
- HVAC
- Disk Drives
- Appliances

Key Specifications

■ Accuracy at 25˚C	±2.0 or ±3.0˚C (max)
■ Accuracy for −30˚C to +100˚C	±4.0˚C (max)
■ Accuracy for −25˚C to +85˚C	±3.0˚C (max)
■ Temperature Slope	+10 mV/˚C
■ Power Supply Voltage Range	+2.7V to +10V
■ Current Drain @ 25˚C	125 µA (max)
■ Nonlinearity	±0.8˚C (max)
■ Output Impedance	800 Ω (max)

Typical Application



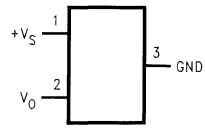
V_O = (+10 mV/˚C x T ˚C) + 600 mV

Temperature (T)	Typical V_O
+100˚C	+1600 mV
+85˚C	+1450 mV
+25˚C	+850 mV
0˚C	+600 mV
−25˚C	+350 mV
−30˚C	+300 mV

FIGURE 1. Full-Range Centigrade Temperature Sensor (−30˚C to +100˚C) Operating from a Single Li-Ion Battery Cell

Connection Diagrams

SOT-23



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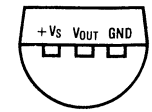
Top View
See NS Package Number MA03B

TO-92



BOTTOM VIEW

01289725

See NS Package Number Z03A

Ordering Information

Order Number	Device Marking	Supplied In	Accuracy Over Specified Temperature Range (°C)	Specified Temperature Range	Package Type
LM61BIM3	T1B	1000 Units on Tape and Reel	± 3	−25°C to +85°C	SOT-23
LM61BIM3X	T1B	3000 Units on Tape and Reel			
LM61CIM3	T1C	1000 Units on Tape and Reel	± 4	−30°C to +100°C	
LM61CIM3X	T1C	3000 Units on Tape and Reel			
LM61BIZ	LM61BIZ	Bulk	± 3	−25°C to +85°C	TO-92
LM61CIZ	LM61CIZ	Bulk	± 4	−30°C to +100°C	

National Semiconductor

LM62
2.7V, 15.6 mV/°C SOT-23 Temperature Sensor

General Description

The LM62 is a precision integrated-circuit temperature sensor that can sense a 0°C to +90°C temperature range while operating from a single +3.0V supply. The LM62's output voltage is linearly proportional to Celsius (Centigrade) temperature (+15.6 mV/°C) and has a DC offset of +480 mV. The offset allows reading temperatures down to 0°C without the need for a negative supply. The nominal output voltage of the LM62 ranges from +480 mV to +1884 mV for a 0°C to +90°C temperature range. The LM62 is calibrated to provide accuracies of ±2.0°C at room temperature and +2.5°C/−2.0°C over the full 0°C to +90°C temperature range.

The LM62's linear output, +480 mV offset, and factory calibration simplify external circuitry required in a single supply environment where reading temperatures down to 0°C is required. Because the LM62's quiescent current is less than 130 µA, self-heating is limited to a very low 0.2°C in still air. Shutdown capability for the LM62 is intrinsic because its inherent low power consumption allows it to be powered directly from the output of many logic gates.

Features

- Calibrated linear scale factor of +15.6 mV/°C
- Rated for full 0°C to +90°C range with 3.0V supply
- Suitable for remote applications

Applications

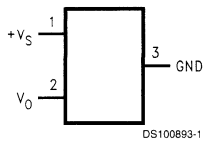
- Cellular Phones
- Computers
- Power Supply Modules
- Battery Management
- FAX Machines
- Printers
- HVAC
- Disk Drives
- Appliances

Key Specifications

Accuracy at 25°C	±2.0 or ±3.0°C (max)
Temperature Slope	+15.6 mV/°C
Power Supply Voltage Range	+2.7V to +10V
Current Drain @ 25°C	130 µA (max)
Nonlinearity	±0.8°C (max)
Output Impedance	4.7 kΩ (max)

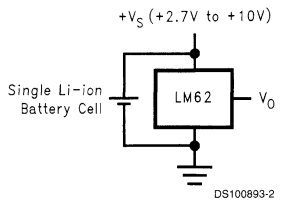
Connection Diagram

SOT-23



Top View
See NS Package Number MA03B

Typical Application



V_O = (+15.6 mV/°C x T°C) + 480 mV

Temperature (T)	Typical V_O
+90°C	+1884 mV
+70°C	+1572 mV
+25°C	870 mV
0°C	+480 mV

FIGURE 1. Full-Range Centigrade Temperature Sensor (0°C to +90°C) Stabilizing a Crystal Oscillator

Ordering Information

Order Number	SOT-23 Device Marking	Supplied As
LM62BIM3	T7B	1000 Units on Tape and Reel
LM62BIM3X	T7B	3000 Units on Tape and Reel
LM62CIM3	T7C	1000 Units on Tape and Reel
LM62CIM3X	T7C	3000 Units on Tape and Reel

National Semiconductor

LM66
Dual Output Internally Preset Thermostat

General Description

The LM66 is a precision low power thermostat. Two stable temperature trip points (V_{T1} and V_{T2}) are generated by dividing down the LM66 1.250V bandgap voltage reference using a resistors divider network. The LM66 has two digital outputs. OUT1 goes LOW when the temperature exceeds T1 and goes HIGH when the the temperature goes below ($T1-T_{HYST}$). Similarly, OUT2 goes LOW when the temperature exceeds T2 and goes HIGH when the temperature goes below ($T2-T_{HYST}$). T_{HYST} is an internally set 5°C typical hysteresis.

The LM66 is currently available in an 8-lead small outline package.

Applications

- Microprocessor Thermal Management
- Appliances
- Portable Battery Powered 3.0V or 5V Systems
- Fan Control
- Industrial Process Control
- HVAC Systems
- Remote Temperature Sensing
- Electronic System Protection

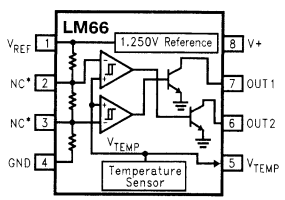
Features

- Digital outputs support TTL logic levels
- Internal temperature sensor
- 2 internal comparators with hysteresis
- Internal voltage reference
- Currently available in 8-pin SO plastic package

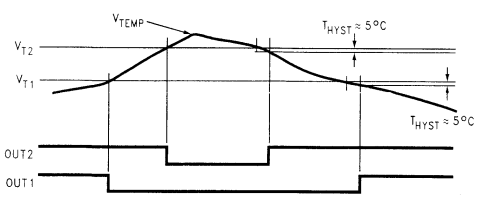
Key Specifications

■ Power Supply Voltage	2.7V to 10V
■ Power Supply Current	250 µA (max)
■ V_{REF}	1.250V ±1.4% (max)
■ Hysteresis Temperature	5°C
■ Internal Temperature Sensor Output Voltage	(+6.20 mV/°C x T) +400mV
■ Temperature Trip Point Accuracy	±3°C (max)
■ T1 set point	+73°C
■ T2 set point	+82°C

Simplified Block Diagram and Connection Diagram



DS100854-1



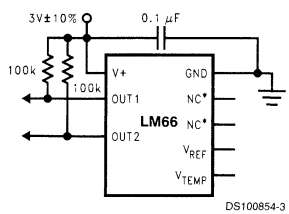
DS100854-2

Ordering Information

TABLE 1.

Order Number	LM66CIM-RLSKB	LM66CIMX-RLSKB
NS Package Number	M08A	M08A
Transport Media	Bulk Rail	2500 Units Tape & Reel

Typical Application



DS100854-3

National Semiconductor

LM70
SPI/MICROWIRE™ 10-Bit plus Sign Digital Temperature Sensor

General Description

The LM70 is a temperature sensor, Delta-Sigma analog-to-digital converter with an SPI and MICROWIRE compatible interface available in LLP and MSOP 8-pin packages. The host can query the LM70 at any time to read temperature. A shutdown mode decreases power consumption to less than 10 µA. This mode is useful in systems where low average power consumption is critical.

The LM70 has 10-bit plus sign temperature resolution (0.25°C per LSB) while operating over a temperature range of −55°C to +150°C.

The LM70's 2.65V to 5.5V supply voltage range, low supply current and simple SPI interface make it ideal for a wide range of applications. These include thermal management and protection applications in hard disk drives, printers, electronic test equipment, and office electronics.

Applications

- System Thermal Management
- Personal Computers
- Disk Drives
- Office Electronics
- Electronic Test Equipment

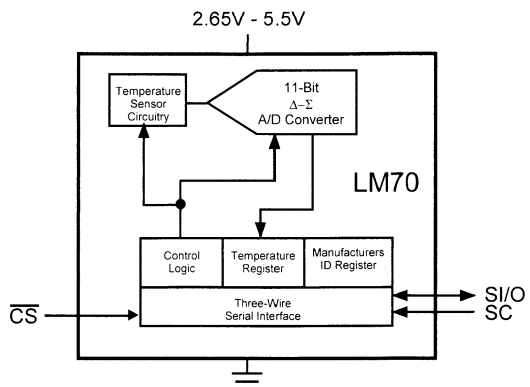
Features

- 0.25°C temperature resolution.
- Shutdown mode conserves power between temperature reading
- SPI and MICROWIRE Bus interface
- MSOP-8 and LLP-8 packages save space

Key Specifications

■ Supply Voltage		2.65V to 5.5V
■ Supply Current	operating	260µA (typ)
		490µA (max)
	shutdown	12µA (typ)
■ Temperature Accuracy	−40°C to 85°C	±2°C(max)
	−10°C to 65°C	+1.5/−2°C(max)
	−55°C to 125°C	+3/−2°C(max)
	−55°C to 150°C	+3.5/−2°C(max)

Simplified Block Diagram



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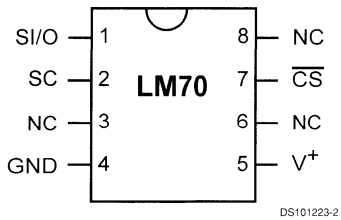
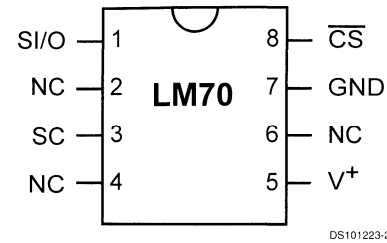
Connection Diagrams

MSOP-8



TOP VIEW
NS Package Number MUA08A

LLP-8



TOP VIEW
NS Package Number LDA08A

Ordering Information

Order Number	Package Marking	NS Package Number	Supply Voltage	Transport Media
LM70CILD-3	T33	LLP-8, LDA08A	2.65V to 3.6V	_ Units in Rail
LM70CILDX-3	T33	LLP-8, LDA08A	2.65V to 3.6V	_ Units in Rail
LM70CILD-5	T35	LLP-8, LDA08A	4.5V to 5.5V	_ Units in Tape and Reel
LM70CILDX-5	T35	LLP-8, LDA08A	4.5V to 5.5V	_ Units in Tape and Reel
LM70CIMM-3	T04C	MSOP-8, MUA08A	2.65V to 3.6V	250 Units in Rail
LM70CIMMX-3	T04C	MSOP-8, MUA08A	2.65V to 3.6V	3500 Units in Tape and Reel
LM70CIMM-5	T03C	MSOP-8, MUA08A	4.5V to 5.5V	250 Units in Rail
LM70CIMMX-5	T03C	MSOP-8, MUA08A	4.5V to 5.5V	3500 Units in Tape and Reel

Pin Descriptions

Label	SOP-8 Pin #	LLP-8 Pin #	Function	Typical Connection
SI/O	1	1	Input/Output - Serial bus bi-directional data line. Schmitt trigger input.	From and to Controller
SC	2	3	Clock - Serial bus clock Schmitt trigger input line.	From Controller
GND	4	7	Power Supply Ground	Ground
V^+	5	5	Positive Supply Voltage Input	DC Voltage from 2.65V to 5.5V. Bypass with a 0.1 µF ceramic capacitor.
$\overline{CS}$	7	8	Chip Select input.	From Controller
NC	3, 6, 8	2, 4, 6	No Connect	These pins are not connected to the LM70 die in any way.

Typical Application

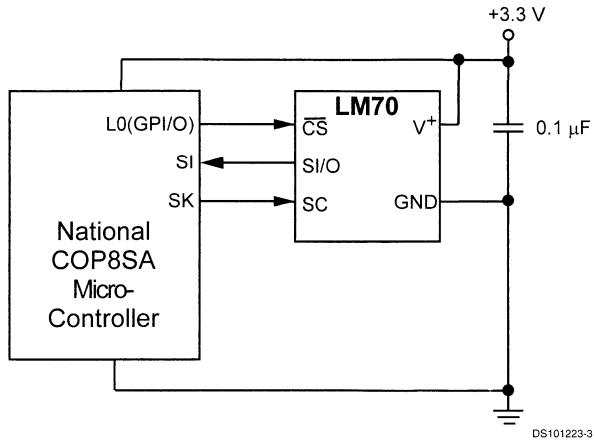


FIGURE 1. COP Microcontroller Interface

National Semiconductor

LM74
SPI/MICROWIRE™ 12-Bit Plus Sign Temperature Sensor

General Description

The LM74 is a temperature sensor, Delta-Sigma analog-to-digital converter with an SPI and MICROWIRE compatible interface. The host can query the LM74 at any time to read temperature. A shutdown mode decreases power consumption to less than 10 µA. This mode is useful in systems where low average power consumption is critical.

The LM74 has 12-bit plus sign temperature resolution (0.0625°C per LSB) while operating over a temperature range of −55°C to +150°C.

The LM74's 3.0V to 5.5V supply voltage range, low supply current and simple SPI interface make it ideal for a wide range of applications. These include thermal management and protection applications in hard disk drives, printers, electronic test equipment, and office electronics. The LM74 is available in the SO-8 package as well as an 5-Bump micro SMD package.

Applications

- System Thermal Management
- Personal Computers
- Disk Drives
- Office Electronics
- Electronic Test Equipment

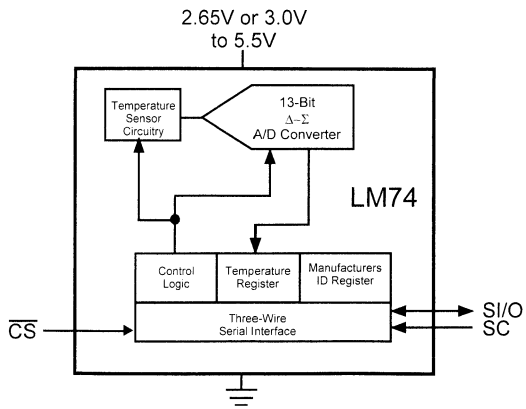
Features

- 0.0625°C temperature resolution.
- Shutdown mode conserves power between temperature reading
- SPI and MICROWIRE Bus interface
- 5-Bump micro SMD package saves space

Key Specifications

■ Supply Voltage		3.0V or 2.65V to 5.5V
■ Supply Current	operating	265µA (typ)
		520µA (max)
	shutdown	3µA (typ)
■ Temperature Accuracy	−10°C to 65°C	±1.25°C(max)
	−25°C to 110°C	±2.1°C(max)
	−55°C to 125°C	±3°C(max)

Simplified Block Diagram



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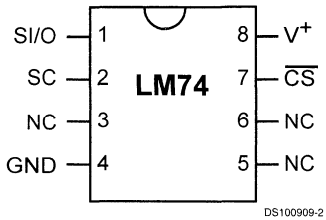
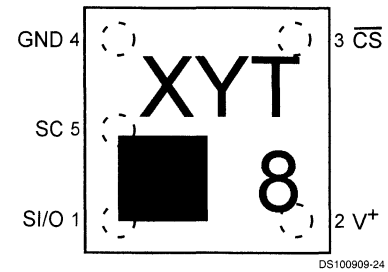
Connection Diagram

SO-8



TOP VIEW
NS Package Number M08A

5-Bump micro SMD



Note:

- Pin numbers are referenced to the package marking text orientation. Pin 1 is designated by the square.
- Reference JEDEC Registration MO-211, variation BC
- The top 4 characters designate the date code. The bottom 3 characters designate the device type (see ordering information).

TOP VIEW
NS Package Number BPD05MPB

Ordering Information

Order Number	Package Marking	NS Package Number	Supply Voltage	Transport Media
LM74CIM-3	LM74CIM-3	SO-8, M08A	3.0V to 3.6V	95 Units in Rail
LM74CIMX-3	LM74CIM-3	SO-8, M08A	3.0V to 3.6V	2500 Units in Tape and Reel
LM74CIM-5	LM74CIM-5	SO-8, M08A	4.5V to 5.5V	95 Units in Rail
LM74CIMX-5	LM74CIM-5	SO-8, M08A	4.5V to 5.5V	2500 Units in Tape and Reel
LM74CIBP-3	T8	micro SMD, BPD05MPB	2.65V to 3.6V	250 Units in Tape and Reel
LM74CIBPX-3	T8	micro SMD, BPD05MPB	2.65V to 3.6V	3000 Units in Tape and Reel
LM74CIBP-5	T9	micro SMD, BPD05MPB	4.5V to 5.5V	250 Units in Tape and Reel
LM74CIBPX-5	T9	micro SMD, BPD05MPB	4.5V to 5.5V	3000 Units in Tape and Reel

Pin Descriptions

Label	SO-8 Pin #	micro SMD Pin #	Function	Typical Connection
SI/O	1	1	Slave Input/Output - Serial bus bi-directional data line. Shmitt trigger input.	From and to Controller
SC	2	5	Slave Clock - Serial bus clock Shmitt trigger input line.	From Controller
NC	3		No Connection	No Connection
GND	4	4	Power Supply Ground	Ground
NC	5		No Connection	No Connection
NC	6		No Connection	No Connection
$\overline{CS}$	7	3	Chip Select input.	From Controller
V^+	8	2	Positive Supply Voltage Input	DC Voltage from 3.0V to 5.5V for the LM74CIM and 2.65V to 5.5V for the LM74CIBP. Bypass with a 0.1 µF ceramic capacitor.

Typical Application

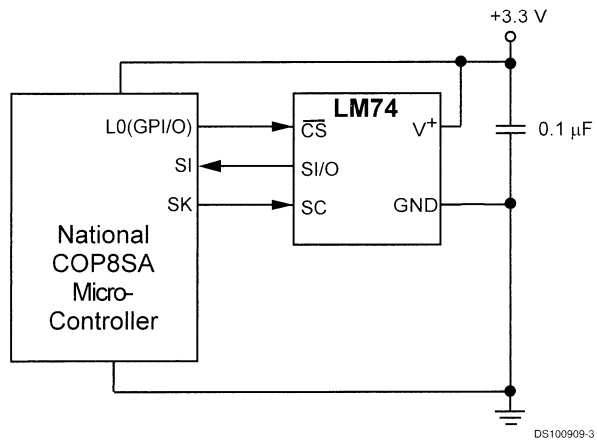


FIGURE 1. COP Microcontroller Interface

National Semiconductor

LM75
Digital Temperature Sensor and Thermal watchdog with Two-Wire Interface

General Description

The LM75 is a temperature sensor, Delta-Sigma analog-to-digital converter, and digital over-temperature detector with I²C® interface. The host can query the LM75 at any time to read temperature. The open-drain Overtemperature Shutdown (O.S.) output becomes active when the temperature exceeds a programmable limit. This pin can operate in either "Comparator" or "Interrupt" mode.

The host can program both the temperature alarm threshold (T_{OS}) and the temperature at which the alarm condition goes away (T_{HYST}). In addition, the host can read back the contents of the LM75's T_{OS} and T_{HYST} registers. Three pins (A0, A1, A2) are available for address selection. The sensor powers up in Comparator mode with default thresholds of 80°C T_{OS} and 75°C T_{HYST}.

The LM75's 3.0V to 5.5V supply voltage range, low supply current and I²C interface make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, and office electronics.

Features

- SOP-8 and Mini SOP-8 (MSOP) packages save space
- I²C Bus interface
- Separate open-drain output pin operates as interrupt or comparator/thermostat output
- Register readback capability
- Power up defaults permit stand-alone operation as thermostat
- Shutdown mode to minimize power consumption
- Up to 8 LM75s can be connected to a single bus

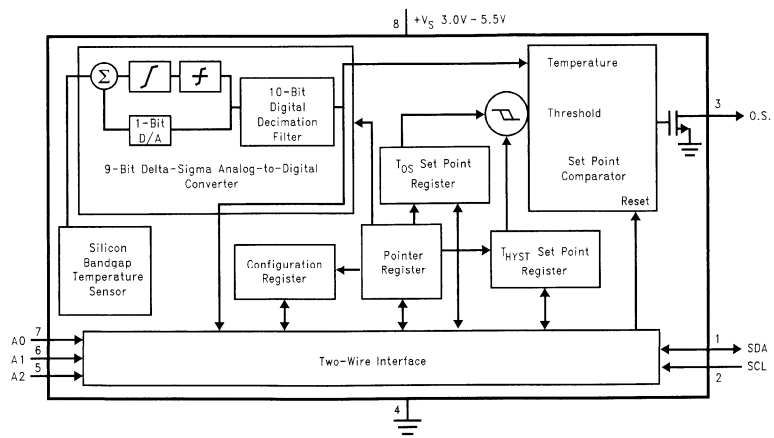
Key Specifications

■ Supply Voltage		3.0V to 5.5V
■ Supply Current	operating	250 µA (typ)
		1 mA (max)
	shutdown	4 µA (typ)
■ Temperature Accuracy	−25°C to 100°C	±2°C(max)
	−55°C to 125°C	±3°C(max)

Applications

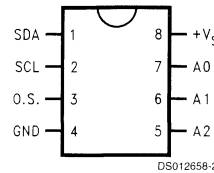
- System Thermal Management
- Personal Computers
- Office Electronics
- Electronic Test Equipment

Simplified Block Diagram



Connection Diagram

SOP-8 and Mini SOP-8



Ordering Information

Order Number	Package Marking	NS Package Number	Supply Voltage	Transport Media
LM75CIM-3	LM75CIM-3	M08A (SOP-8)	3.3V	
LM75CIMX-3	LM75CIM-3	M08A (SOP-8)	3.3V	2500 Units on Tape and Reel
LM75CIMM-3	T01C	MUA08A (MSOP-8)	3.3V	250 Units in Rail
LM75CIMMX-3	T01C	MUA08A (MSOP-8)	3.3V	3500 Units on Tape and Reel
LM75CIM-5	LM75CIM-5	M08A (SOP-8)	5V	
LM75CIMX-5	LM75CIM-5	M08A (SOP-8)	5V	2500 Units on Tape and Reel
LM75CIMM-5	T00C	MUA08A (MSOP-8)	5V	250 Units in Rail
LM75CIMMX-5	T00C	MUA08A (MSOP-8)	5V	3500 Units on Tape and Reel

Pin Description

Label	Pin #	Function	Typical Connection
SDA	1	I^2C Serial Bi-Directional Data Line. Open Drain.	From Controller, tied to a pull-up
SCL	2	I^2C Clock Input	From Controller
O.S.	3	Overtemperature Shutdown Open Drain Output	Pull Up Resistor, Controller Interrupt Line
GND	4	Power Supply Ground	Ground
$+V_S$	8	Positive Supply Voltage Input	DC Voltage from 3V to 5.5V
A0–A2	7,6,5	User-Set I^2C Address Inputs	Ground (Low, "0") or $+V_S$ (High, "1")

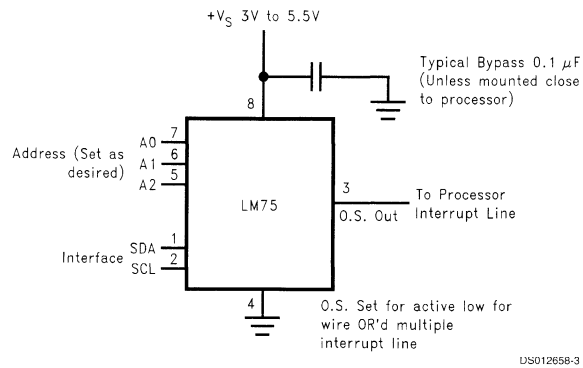


FIGURE 1. Typical Application

National Semiconductor

LM76
±0.5°C, ±1°C, 12-Bit + Sign Digital Temperature Sensor and Thermal Window Comparator with Two-Wire Interface

General Description

The LM76 is a digital temperature sensor and thermal window comparator with an I²C™ Serial Bus interface with an accuracy of ±1°C. This accuracy for the LM76CHM is specified for a −10°C to 45°C temperature range, while for the LM76CNM the temperature range is 70°C to 100°C. The LM76CHM is specified with an accuracy ±0.5°C at 25°C. The window-comparator architecture of the LM76 eases the design of temperature control systems conforming to the ACPI (Advanced Configuration and Power Interface) specification for personal computers. The open-drain Interrupt (INT) output becomes active whenever temperature goes outside a programmable window, while a separate Critical Temperature Alarm (T_CRIT_A) output becomes active when the temperature exceeds a programmable critical limit. The INT output can operate in either a comparator or event mode, while the T_CRIT_A output operates in comparator mode only.

The host can program both the upper and lower limits of the window as well as the critical temperature limit. Programmable hysterisis as well as a fault queue are available to minimize false tripping. Two pins (A0, A1) are available for address selection. The sensor powers up with default thresholds of 2°C T_{HYST}, 10°C T_{LOW}, 64°C T_{HIGH}, and 80°C T_CRIT.

The LM76's 3.3V and 5.0V supply voltage, Serial Bus interface, 12-bit + sign output, and full-scale range of over 127°C make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, office electronics and bio-medical applications.

Features

- Window comparison simplifies design of ACPI compatible temperature monitoring and control.
- Serial Bus interface
- Separate open-drain outputs for Interrupt and Critical Temperature shutdown
- Shutdown mode to minimize power consumption
- Up to 4 LM76s can be connected to a single bus
- 12-bit + sign output; full-scale reading of over 127°C

Key Specifications

■ Supply Voltage		3.3V or 5.0V
■ Supply Current	operating	250 µA (typ)
		450 µA (max)
	shutdown	8 µA (max)
■ Temperature Accuracy	+25°C	±0.5°C(max)
	−10°C to +45°C	±1.0°C(max)
	70°C to 100°C	±1.0°C(max)
■ Resolution		0.0625°C

Applications

- System Thermal Management
- Personal Computers
- Office Electronics
- HVAC

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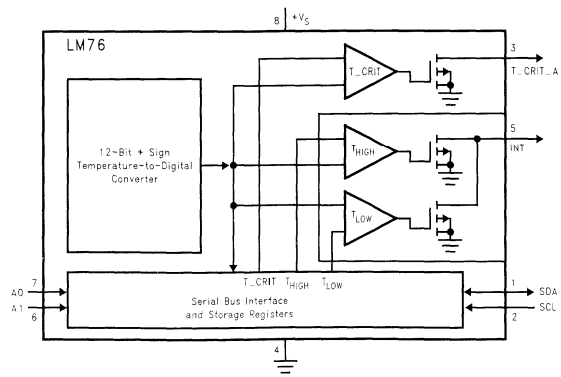
Simplified Block Diagram



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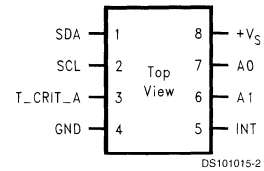
Connection Diagram

SO-8



LM76 See NS Package Number M08A

Ordering Information

Order Number	Supply Voltage	Acurracy	Temperature Range for Accuracy	Transport Media
LM76CHM-5	5.0V	±0.5°C ±1.0°C	25°C −10°C to 45°C	95 units in Rail
LM76CHMX-5	5.0V	±0.5°C ±1.0°C	25°C −10°C to 45°C	2500 Units on Tape and Reel
LM76CNM-3	3.3V	±1°C	70°C to 100°C	95 units in Rail
LM76CNMX-3	3.3V	±1°C	70°C to 100°C	2500 Units on Tape and Reel

Pin Description

Label	Pin #	Function	Typical Connection
SDA	1	Serial Bi-Directional Data Line, Open Drain Output, CMOS Logic Level	Pull Up Resistor, Controller I^2C Data Line
SCL	2	Serial Bus Clock Input, CMOS Logic Level	From Controller I^2C Clock Line
T_CRIT_A	3	Critical Temperature Alarm, Open Drain Output	Pull Up Resistor, Controller Interrupt Line or System Hardware Shutdown
GND	4	Power Supply Ground	Ground
INT	5	Interrupt, Open Drain Output	Pull Up Resistor, Controller Interrupt Line
$+V_S$	8	Positive Supply Voltage Input	DC Voltage from 3.3V power supply or 5V.
A0–A1	7,6	User-Set Address Inputs, TTL Logic Level	Ground (Low, "0") or $+V_S$ (High, "1")

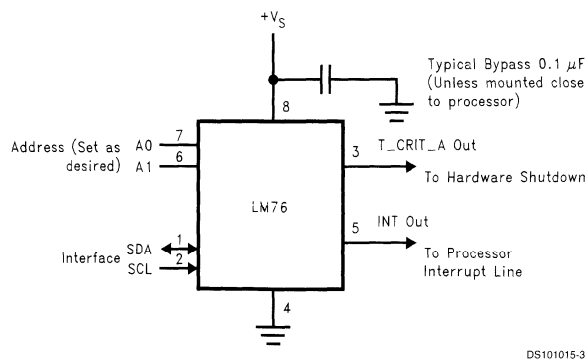


FIGURE 1. Typical Application

National Semiconductor

LM77
9-Bit + Sign Digital Temperature Sensor and Thermal Window Comparator with Two-Wire Interface

General Description

The LM77 is a digital temperature sensor and thermal window comparator with an I²C™ Serial Bus interface. The window-comparator architecture of the LM77 eases the design of temperature control systems conforming to the ACPI (Advanced Configuration and Power Interface) specification for personal computers. The open-drain Interrupt (INT) output becomes active whenever temperature goes outside a programmable window, while a separate Critical Temperature Alarm (T_CRIT_A) output becomes active when the temperature exceeds a programmable critical limit. The INT output can operate in either a comparator or event mode, while the T_CRIT_A output operates in comparator mode only.

The host can program both the upper and lower limits of the window as well as the critical temperature limit. Programmable hysterisis as well as a fault queue are available to minimize false tripping. Two pins (A0, A1) are available for address selection. The sensor powers up with default thresholds of 2°C T_{HYST}, 10°C T_{LOW}, 64°C T_{HIGH}, and 80°C T_CRIT.

The LM77's 3.0V to 5.5V supply voltage range, Serial Bus interface, 9-bit + sign output, and full-scale range of over 128°C make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, office electronics, automotive, and HVAC applications.

Features

- Window comparison simplifies design of ACPI compatible temperature monitoring and control.
- Serial Bus interface
- Separate open-drain outputs for Interrupt and Critical Temperature shutdown
- Shutdown mode to minimize power consumption
- Up to 4 LM77s can be connected to a single bus
- 9-bit + sign output; full-scale reading of over 128°C
- SOP and MSOP 8-lead packages

Key Specifications

■ Supply Voltage		3.0V to 5.5V
■ Supply Current	operating	250 µA (typ)
		500 µA (max)
	shutdown	5 µA (typ)
■ Temperature Accuracy	−10°C to 65°C	±1.5°C(max)
	−25°C to 100°C	±2°C(max)
	−55°C to 125°C	±3°C(max)

Applications

- System Thermal Management
- Personal Computers
- Office Electronics
- Electronic Test Equipment
- Automotive
- HVAC

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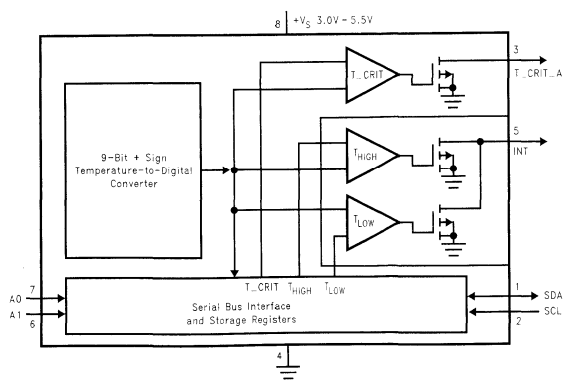
Simplified Block Diagram



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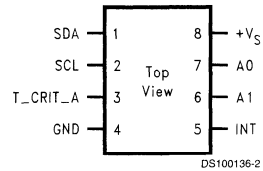
Connection Diagram

SOP8 or MSOP



DS100136-2

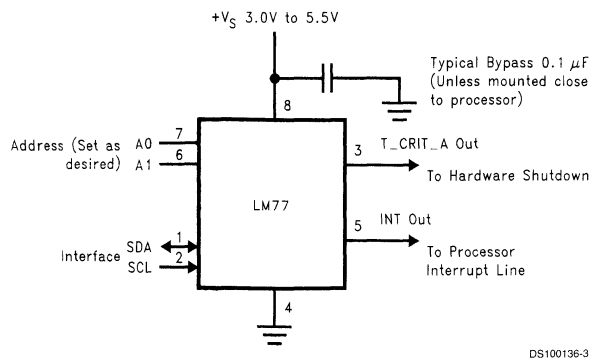
LM77 See NS Package Number M08A or MM08A

Ordering Information

Order Number	Supply Voltage	Package	Supplied In
LM77CIM-3	3.3V	SOP8, M08A	Rail
LM77CIMX-3	3.3V	SOP8, M08A	2500 Units on Tape and Reel
LM77CIM-5	5V	SOP8, M08A	Rail
LM77CIMX-5	5V	SOP8, M08A	2500 Units on Tape and Reel
LM77CIMM-3	3.3V	MSOP8, MUA08A	Rail
LM77CIMMX-3	3.3V	MSOP8, MUA08A	3500 Units on Tape and Reel
LM77CIMM-5	5V	MSOP8, MUA08A	Rail
LM77CIMMX-5	5V	MSOP8, MUA08A	3500 Units on Tape and Reel

Pin Description

Label	Pin #	Function	Typical Connection
SDA	1	Serial Bi-Directional Data Line. Open Drain Output	From Controller
SCL	2	Serial Bus Clock Input	From Controller
T_CRIT_A	3	Critical Temperature Alarm Open Drain Output	Pull Up Resistor, Controller Interrupt Line or System Hardware Shutdown
GND	4	Power Supply Ground	Ground
INT	5	Interrupt Open Drain Output	Pull Up Resistor, Controller Interrupt Line
$+V_S$	8	Positive Supply Voltage Input	DC Voltage from 3V to 5.5V
A0–A1	7,6	User-Set Address Inputs	Ground (Low, "0") or $+V_S$ (High, "1")



DS100136-3

FIGURE 1. Typical Application

National Semiconductor

LM80
Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor

General Description

The LM80 provides 7 positive voltage inputs, temperature measurement, fan speed measurement, and hardware monitoring on an I²C™ interface. The LM80 performs WATCHDOG comparisons of all measured values and an open-drain interrupt output becomes active when any values exceed programmed limits. A Chassis Intrusion input is provided to monitor and reset an external circuit designed to latch a chassis intrusion event.

The LM80 is especially suited to interface to both linear and digital temperature sensors. The 10 mV LSB and 2.56 volt input range is ideal for accepting inputs from a linear sensor such as the LM50. The $\overline{BTI}$ is used as an input from either digital or thermostat sensors such as LM75 and LM56.

The LM80's 2.8V to 5.75V supply voltage range, low supply current, and I²C interface make it ideal for a wide range of applications. These include hardware monitoring and protection applications in personal computers, electronic test equipment, and office electronics.

Features

- Temperature sensing
- 7 positive voltage inputs
- 2 programmable fan speed monitoring inputs
- 10 mV LSB and 2.56V input range accepts outputs from linear temperature sensors such as the LM50
- Chassis Intrusion Detector input
- WATCHDOG comparison of all monitored values
- Separate input to show status in Interrupt Status Register of additional external temperature sensors such as the LM56 or LM75
- I²C Serial Bus interface compatibility
- Shutdown mode to minimize power consumption
- Programmable $\overline{RST\_OUT}/\overline{OS}$ pin: $\overline{RST\_OUT}$ provides a Reset output; $\overline{OS}$ provides an Interrupt Output activated by an Overtemperature Shutdown event

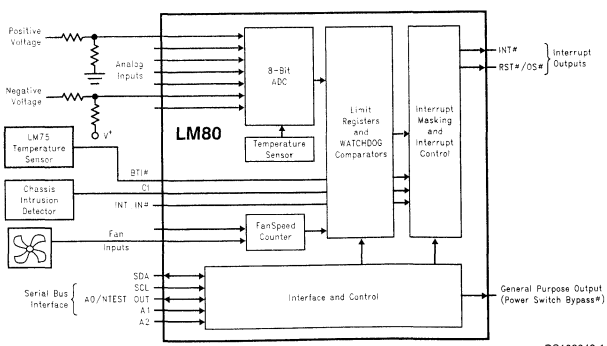
Key Specifications

■ Voltage monitoring Error		±1% (max)
■ Temperature Error −25°C to +125°C		± 3°C (max)
■ Supply Voltage Range		2.8V to 5.75V
■ Supply Current	Operating:	0.2 mA typ
	Shutdown:	15 µA typ
■ ADC Resolution		8 Bits
■ Temperature Resolution		0.5°C

Applications

- System Thermal and Hardware Monitoring for Servers and PCs
- Office Electronics
- Electronic Test Equipment and Instrumentation

Typical Application



# Indicates Active Low ("Not")

13

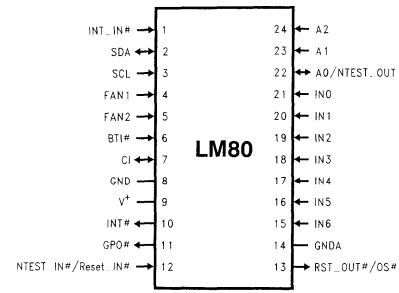
Ordering Information

Temperature Range $-25^{\circ}C \leq T_A \leq +125^{\circ}C$		NS Package Number	Specified Power Supply Voltage
Order Number	Device Marking		
LM80CIMT-3[1] LM80CIMTX-3[2]	LM80CIMT-3	MTC24B	3.3V
LM80CIMT-5[1] LM80CIMTX-5[2]	LM80CIMT-5	MTC24B	5.0V

Note: [1]-Rail transport media, 62 parts per rail

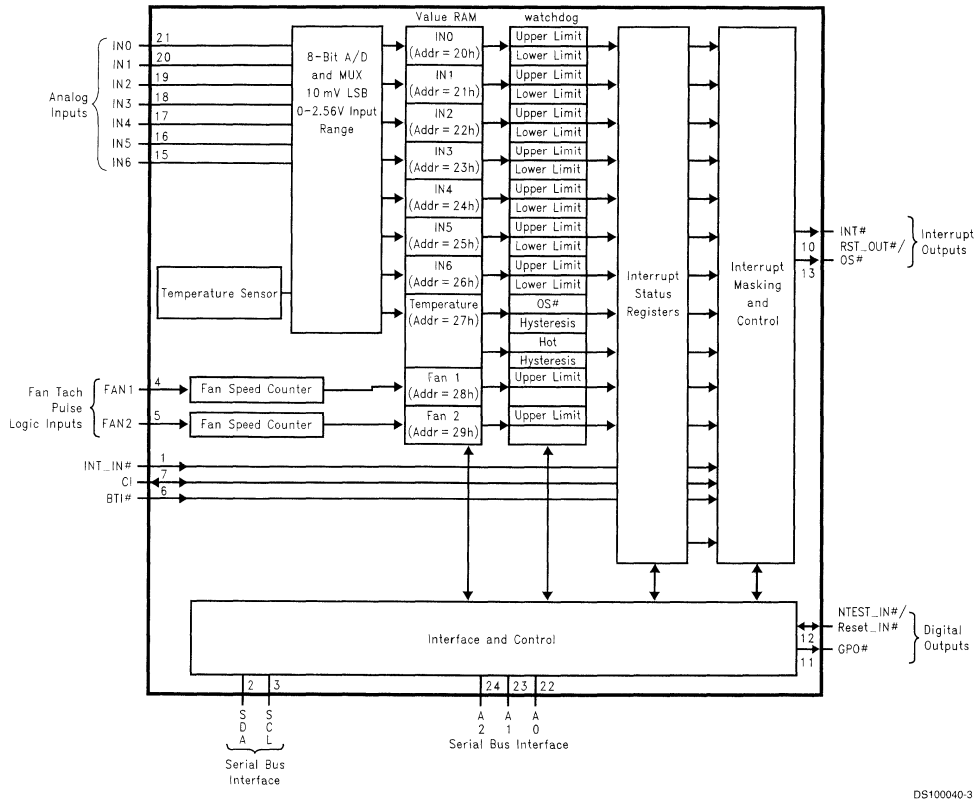
[2]-Tape and reel transport media, 3400 parts per reel

Connection Diagram



DS100040-2

Block Diagram



DS100040-3

Pin Descriptions

Pin Name(s)	Pin Number	Number of Pins	Type	Description
$\overline{\text{INT\_IN}}$	1	1	Digital Input	This is an active low input that propagates the $\overline{\text{INT\_IN}}$ signal to the $\overline{\text{INT}}$ output of the LM80 via Interrupt Mask Register 1 Bit 7 and $\overline{\text{INT}}$ enable Bit 1 of the Configuration Register.
SDA	2	1	Digital I/O	Serial Bus bidirectional Data. Open-drain output.
SCL	3	1	Digital Input	Serial Bus Clock.

Pin Descriptions (Continued)

Pin Name(s)	Pin Number	Number of Pins	Type	Description
FAN1-FAN2	4-5	2	Digital Inputs	0 to V^+ fan tachometer inputs.
$\overline{BTI}$	6	1	Digital Input	Board Temperature Interrupt driven by O.S. outputs of additional temperature sensors such as LM75. Provides internal pull-up of 10 kΩ.
CI (Chassis Intrusion)	7	1	Digital I/O	An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM80. The LM80 provides an internal open drain on this line, controlled by Bit 5 of the Configuration Register, to provide a minimum 10 ms reset of this line.
GND	8	1	GROUND	Internally connected to all of the digital circuitry.
V^+ (+2.8V to +5.75V)	9	1	POWER	+3.3V or +5V V^+ power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
$\overline{INT}$	10	1	Digital Output	Non-Maskable Interrupt (open source)/Interrupt Request (open drain). The mode is selected with Bit 5 of the Configuration Register and the output is enabled when Bit 1 of the Configuration Register is set to 1. The default state is disabled.
$\overline{GPO}$ ($\overline{Power\ Switch\ Bypass}$)	11	1	Digital Output	An active low open drain output intended to drive an external P-channel power MOSFET for software power control.
$\overline{NTEST\_IN}$/ $\overline{RESET\_IN}$	12	1	Digital Input	An active-low input that enables NAND Tree board-level connectivity testing. Refer to Section 10.0 on NAND Tree testing. Whenever NAND Tree connectivity is enabled the LM80 is also reset to its power on state.
$\overline{RST\_OUT}/\overline{OS}$	13	1	Digital Output	Master Reset, 5 mA driver (open drain), active low output with a 10 ms minimum pulse width. Available when enabled via Bit 4 in Configuration Register and Bit 7 of the Fan Divisor/$\overline{RST\_OUT}/\overline{OS}$ Register. Bit 6 of the Fan Divisor/$\overline{RST\_OUT}/\overline{OS}$ Register enables this output as an active low Overtemperature Shutdown ($\overline{OS}$).
GNDA	14	1	GROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs. This pin needs to be taken to a low noise analog ground plane for optimum performance.
IN6-IN0	15-21	7	Analog Inputs	0V to 2.56V full scale range Analog Inputs.
A0/NTEST_OUT	22	1	Digital I/O	The lowest order bit of the Serial Bus Address. This pin functions as an output when doing a NAND Tree test.
A1-A2	23-24	2	Digital Inputs	The two highest order bits of the Serial Bus Address.
TOTAL PINS		**24**		

National Semiconductor

LM81
Serial Interface ACPI-Compatible Microprocessor System Hardware Monitor

General Description

The LM81 is a highly integrated data acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor-based system. In a PC, the LM81 can be used to monitor power supply voltages, temperatures, and fan speeds. Actual values for these inputs can be read at any time. Programmable WATCHDOG limits in the LM81 activate a fully programmable and maskable interrupt system with two outputs ($\overline{INT}$ and $\overline{T\_CRIT\_}$).

The LM81 has an on-chip digital output temperature sensor with 9-bit or 12-bit resolution, a 6 analog input ADC with 8-bit resolution and an 8-bit DAC. Two fan tachometer outputs can be measured with the LM81's FAN1 and FAN2 inputs. The DAC, with a 0 to 1.25V output voltage range, can be used for fan speed control. Additional inputs are provided for Chassis Intrusion detection circuits, and VID monitor inputs. The LM81 has a Serial Bus interface that is compatible with SMBus™.

Features

- Temperature sensing
- 6 positive voltage inputs with scaling resistors to monitor +5V, +12V, +3.3V, +2.5V, Vccp power supplies directly
- 8-bit DAC output for controlling fan speed
- 2 fan speed monitoring inputs
- Chassis Intrusion detector input
- WATCHDOG comparison of all monitored values
- SMBus 1.0 (LM81C) and 1.1 (LM81B) Serial Bus interface compatibility
- LM81B has improved voltage monitoring accuracy
- VID0-VID4 monitoring inputs

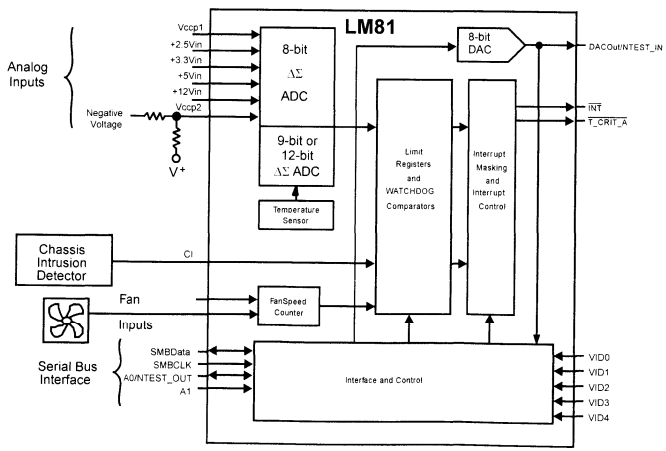
Key Specifications

■ Voltage Monitoring Error	+2% or ±1.2% (max)
■ Temperature Error −40°C to +125°C	± 3°C (max)
■ Supply Voltage Range	2.8V to 3.8V
■ Supply Current	0.4 mA (typ)
■ ADC and DAC Resolution	8 Bits
■ Temperature Resolution	0.5°C

Applications

- System Thermal and Hardware Monitoring for Servers and PCs
- Office Electronics
- Electronic Test Equipment and Instrumentation

Typical Application



# Indicates Active Low ("Not")

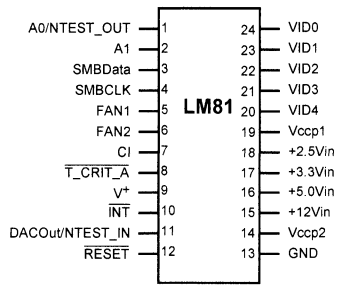
Ordering Information

Temperature Range $-40^{\circ}C \le T_A \le +125^{\circ}C$		NS Package Number	SMBus Revision Level	Voltage Monitoring Error
Order Number	Device Marking			
LM81BIMT-3[1]	LM81BIMT-3	MTC24B	1.1	±1.2%
LM81BIMTX-3[2]	LM81BIMT-3	MTC24B	1.1	±1.2%
LM81CIMT-3[1]	LM81CIMT-3	MTC24B	1.0	+2%
LM81CIMTX-3[2]	LM81CIMT-3	MTC24B	1.0	+2%

Note: [1]-Rail transport media, 62 parts per rail

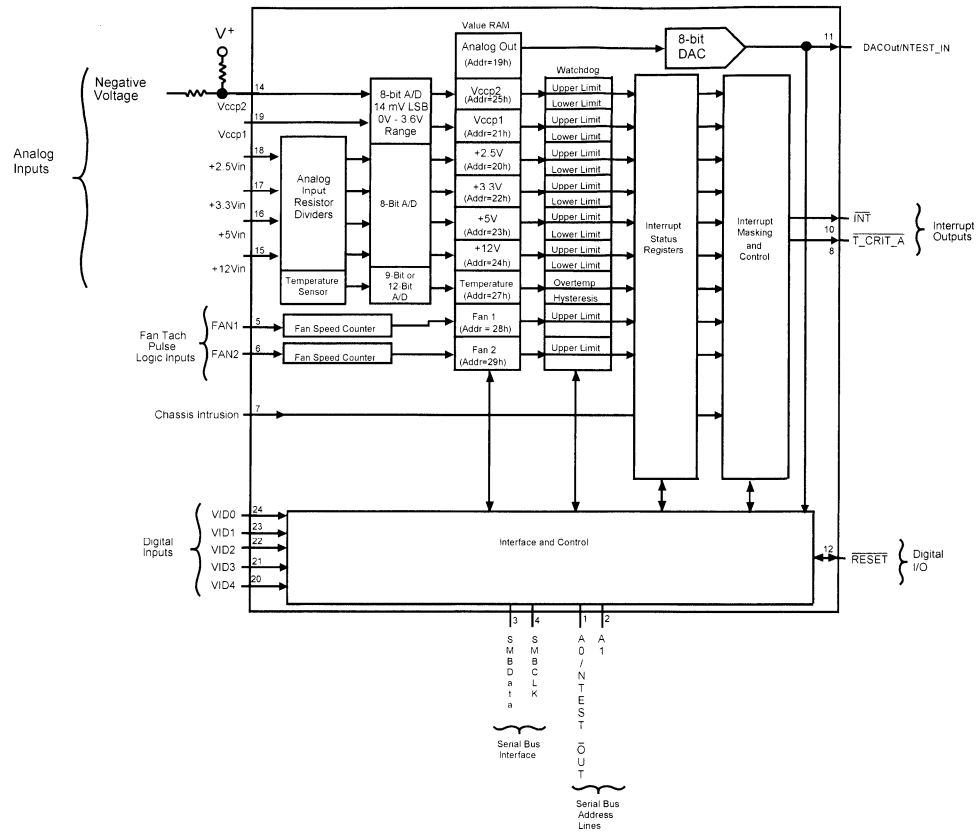
[2]-Tape and reel transport media, 3400 parts per reel

Connection Diagram



DS100072-3

Block Diagram



Pin Description

Pin Name(s)	Pin Number	Number of Pins	Type	Description
A0/NTEST_OUT	1	1	Digital I/0	The lowest order programmable bit of the serial bus address. This pin functions as an output during NAND Tree tests (board-level connectivity testing). Refer to *SECTION 11* on NAND Tree testing.
A1	2	1	Digital Input	The highest order programmable bit of the serial bus address.
SMBData	3	1	Digital I/O	Serial Bus bidirectional Data. Open-drain output.
SMBCLK	4	1	Digital Input	Serial Bus Clock.
FAN1-FAN2	5-6	2	Digital Inputs	Schmitt Trigger fan tachometer inputs.
CI	7	1	Digital I/O	An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM81. There is also an internal open-drain output on this line, controlled by Bit 6 of the Configuration Register (40h) or Bit 7 CI Clear Register (46h), to provide a minimum 20 ms reset pulse. See *Section 3.3* and *Section 9.0*.
$\overline{\text{T\_CRIT\_A}}$	8	1	Digital Output	Critical Temperature Alarm active low open-drain output. This pin can be grounded when not used.
V^+ (+2.8V to +3.8V)	9	1	POWER	+3.3V V^+ power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.

Pin Description (Continued)

Pin Name(s)	Pin Number	Number of Pins	Type	Description
$\overline{\text{INT}}$	10	1	Digital Output	Interrupt active low open-drain output. This output is enabled when Bit 1 in the Configuration Register is set to 1. The default state is disabled.
DACOut/NTEST_IN	11	1	Analog Output/Digital Input	0V to +1.25V amplitude 8-bit DAC output. When forced high by an external voltage the NAND Tree Test mode is enabled which provides board-level connectivity testing. Refer to Section 11.0 on NAND Tree testing.
$\overline{\text{RESET}}$	12	1	Digital I/O	Master Reset, 5 mA driver (open-drain), active low output with a 20 ms minimum pulse width. Available when enabled via Bit 4 in the Configuration register. It acts as an active low power on RESET input.
GND	13	1	GROUND	Internally connected to all circuitry. The ground reference for all analog inputs and the DAC output. This pin needs to be connected to a low noise analog ground plane for optimum performance of the DAC output.
Vccp2	14	1	Analog Input	Analog input for monitoring −12V or Vccp2. Selectable by choosing the appropriate external resistor divider values such that the input to the LM81 is scaled to +2.5V. See *Section 4.0.*
+12Vin	15	1	Analog Input	Analog input for monitoring +12V.
+5Vin	16	1	Analog Input	Analog input for monitoring +5V.
+3.3Vin	17	1	Analog Input	Analog input for monitoring +3.3V.
+2.5Vin	18	1	Analog Input	Analog input for monitoring +2.5V.
Vccp1	19	1	Analog Input	Analog input for monitoring Vccp, a processor voltage that is nominally at +2.5V.
VID4-VID0	20-24	5	Digital Inputs	Supply Voltage readouts from the Pentium/PRO power supplies that indicate the operating voltage or the processor (e.g. 1.5V to 2.9V). The values are read in the VID/Fan Divisor Register and the VID4 Register.
TOTAL PINS		**24**		

National Semiconductor

LM82
Remote Diode and Local Digital Temperature Sensor with Two-Wire Interface

General Description

The LM82 is a digital temperature sensor with a 2 wire serial interface that senses the voltage and thus the temperature of a remote diode using a Delta-Sigma analog-to-digital converter with a digital over-temperature detector. The LM82 accurately senses its own temperature as well as the temperature of external devices, such as Pentium II® Processors or diode connected 2N3904s. The temperature of any ASIC can be detected using the LM82 as long as a dedicated diode (semiconductor junction) is available on the die. Using the SMBus interface a host can access the LM82's registers at any time. Activation of a $\overline{\text{T\_CRIT\_A}}$ output occurs when any temperature is greater than a programmable comparator limit, T_CRIT. Activation of an $\overline{\text{INT}}$ output occurs when any temperature is greater than its corresponding programmable comparator HIGH limit.

The host can program as well as read back the state of the T_CRIT register and the 2 T_HIGH registers. Three state logic inputs allow two pins (ADD0, ADD1) to select up to 9 SMBus address locations for the LM82. The sensor powers up with default thresholds of 127°C for T_CRIT and all T_HIGHs. The LM82 is pin for pin and register compatible with the LM84, Maxim MAX1617 and Analog Devices ADM1021.

Features

- Accurately senses die temperature of remote ICs, or diode junctions
- On-board local temperature sensing
- SMBus and I^2C compatible interface, supports SMBus 1.1 TIMEOUT
- Two interrupt outputs: $\overline{\text{INT}}$ and $\overline{\text{T\_CRIT\_A}}$
- Register readback capability
- 7 bit plus sign temperature data format, 1 °C resolution
- 2 address select pins allow connection of 9 LM82s on a single bus

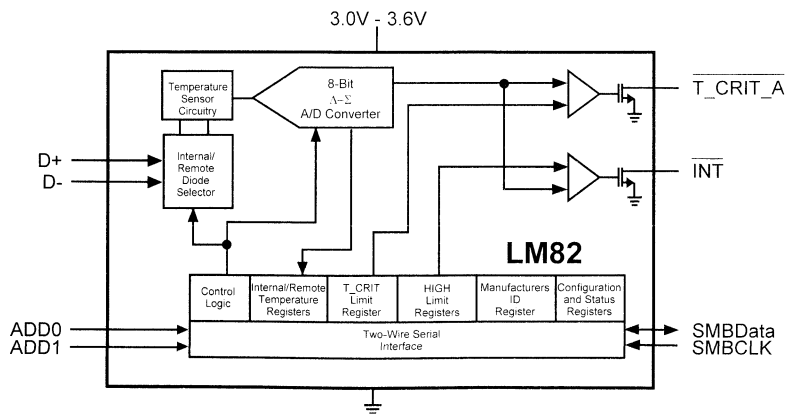
Key Specifications

- Supply Voltage 3.0V to 3.6V
- Supply Current 0.8mA (max)
- Local Temp Accuracy (includes quantization error)
  0°C to +85°C ±3.0°C (max)
- Remote Diode Temp Accuracy (includes quantization error)
  +25°C to +100°C ±3°C (max)
  0°C to +125°C ±4°C (max)

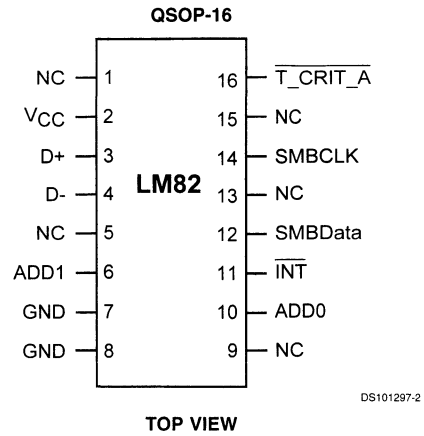
Applications

- System Thermal Management
- Computers
- Electronic Test Equipment
- Office Electronics
- HVAC

Simplified Block Diagram



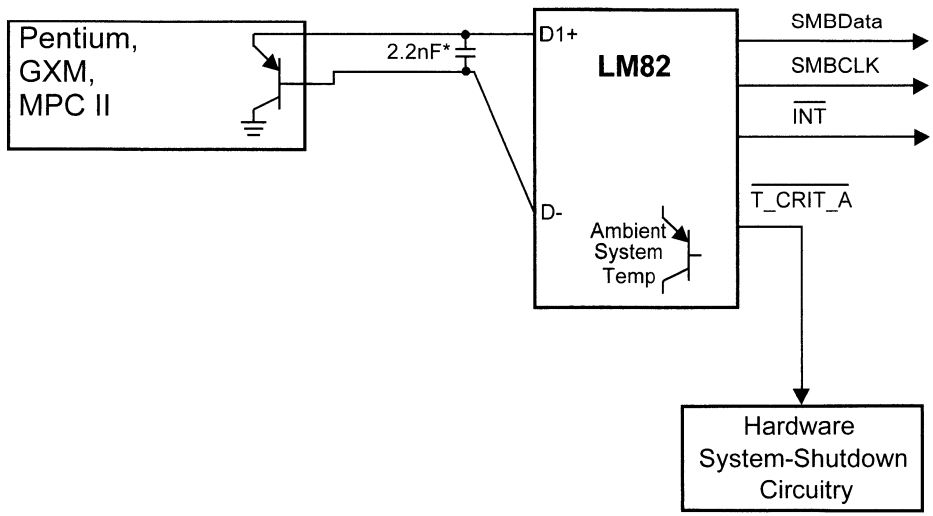
Connection Diagram



Ordering Information

Order Number	NS Package Number	Transport Media
LM82CIMQA	MQA16A (QSOP-16)	95 Units in Rail
LM82CIMQAX	MQA16A (QSOP-16)	2500 Units on Tape and Reel

Typical Application



*Note: 2.2nF Capacitors must be placed as close as possilbe to D+ and D- pins of the LM82.

DS101297-3

Pin Description

Label	Pin #	Function	Typical Connection
NC	1, 5	floating, unconnected	Left floating. PC board traces may be routed through the pads for these pins. No restrictions applied.
V_{CC}	2	Positive Supply Voltage Input	DC Voltage from 3.0 V to 3.6 V
D+	3	Diode Current Source	To Diode Anode. Connected to remote discrete diode junction or to the diode junction on a remote IC whose die temperature is being sensed. When not used they should be left floating.
D−	4	Diode Return Current Sink	To Diode Cathode. Must float when not used.
ADD0–ADD1	10, 6	User-Set SMBus (I^2C) Address Inputs	Ground (Low, "0"), V_{CC} (High, "1") or open ("TRI-LEVEL")
GND	7, 8	Power Supply Ground	Ground
NC	9, 13, 15	Manufacturing test pins.	Left floating. PC board traces may be routed through the pads for these pins, although the components that drive these traces should share the same supply as the LM82 so that the Absolute Maximum Rating, Voltage at Any Pin, is not violated.
$\overline{INT}$	11	Interrupt Output, open-drain	Pull Up Resistor, Controller Interrupt or Alert Line
SMBData	12	SMBus (I^2C) Serial Bi-Directional Data Line, open-drain output	From and to Controller, Pull-Up Resistor
SMBCLK	14	SMBus (I^2C) Clock Input	From Controller, Pull-Up Resistor
$\overline{T\_CRIT\_A}$	16	Critical Temperature Alarm, open-drain output	Pull Up Resistor, Controller Interrupt Line or System Shutdown

National Semiconductor

LM83
Triple-Diode Input and Local Digital Temperature Sensor with Two-Wire Interface

General Description

The LM83 is a digital temperature sensor with a 2 wire serial interface that senses the voltage and thus the temperature of three remote diodes using a Delta-Sigma analog-to-digital converter with a digital over-temperature detector. The LM83 accurately senses its own temperature as well as the temperature of three external devices, such as Pentium II® Processors or diode connected 2N3904s. The temperature of any ASIC can be detected using the LM83 as long as a dedicated diode (semiconductor junction) is available on the die. Using the SMBus interface a host can access the LM83's registers at any time. Activation of a $\overline{\text{T\_CRIT\_A}}$ output occurs when any temperature is greater than a programmable comparator limit, T_CRIT. Activation of an $\overline{\text{INT}}$ output occurs when any temperature is greater than its corresponding programmable comparator HIGH limit.

The host can program as well as read back the state of the T_CRIT register and the four T_HIGH registers. Three state logic inputs allow two pins (ADD0, ADD1) to select up to 9 SMBus address locations for the LM83. The sensor powers up with default thresholds of 127°C for T_CRIT and all T_HIGHs. The LM83 is pin for pin and register compatible with the LM84 as well as the Maxim MAX1617 and the Analog Devices ADM1021.

Features

- Accurately senses die temperature of 3 remote ICs, or diode junctions
- On-board local temperature sensing
- SMBus and I^2C compatible interface, supports SMBus 1.1 TIMEOUT
- Two interrupt outputs: $\overline{\text{INT}}$ and $\overline{\text{T\_CRIT\_A}}$
- Register readback capability
- 7 bit plus sign temperature data format, 1 °C resolution
- 2 address select pins allow connection of 9 LM83s on a single bus

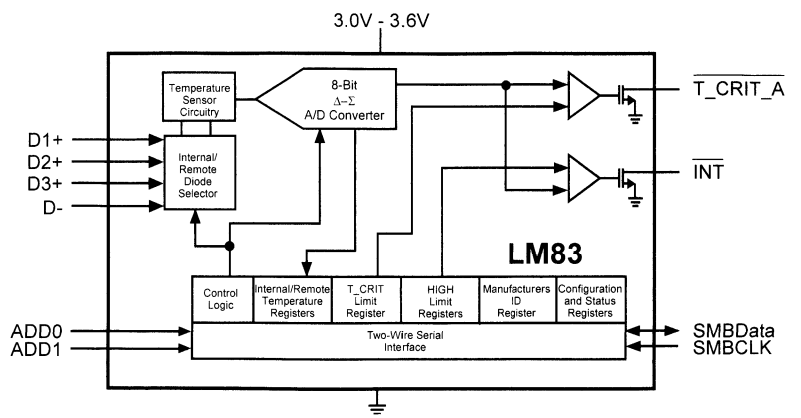
Key Specifications

- Supply Voltage 3.0V to 3.6V
- Supply Current 0.8mA (max)
- Local Temp Accuracy (includes quantization error)
  0°C to +85°C ±3.0°C (max)
- Remote Diode Temp Accuracy (includes quantization error)
  +25°C to +100°C ±3°C (max)
  0°C to +125°C ±4°C (max)

Applications

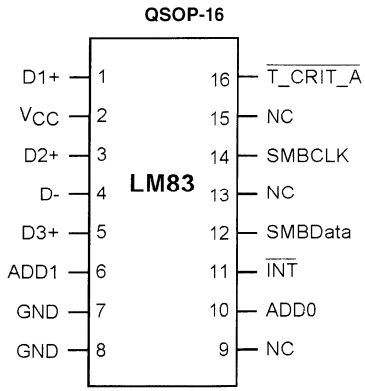
- System Thermal Management
- Computers
- Electronic Test Equipment
- Office Electronics
- HVAC

Simplified Block Diagram



DS101058-1

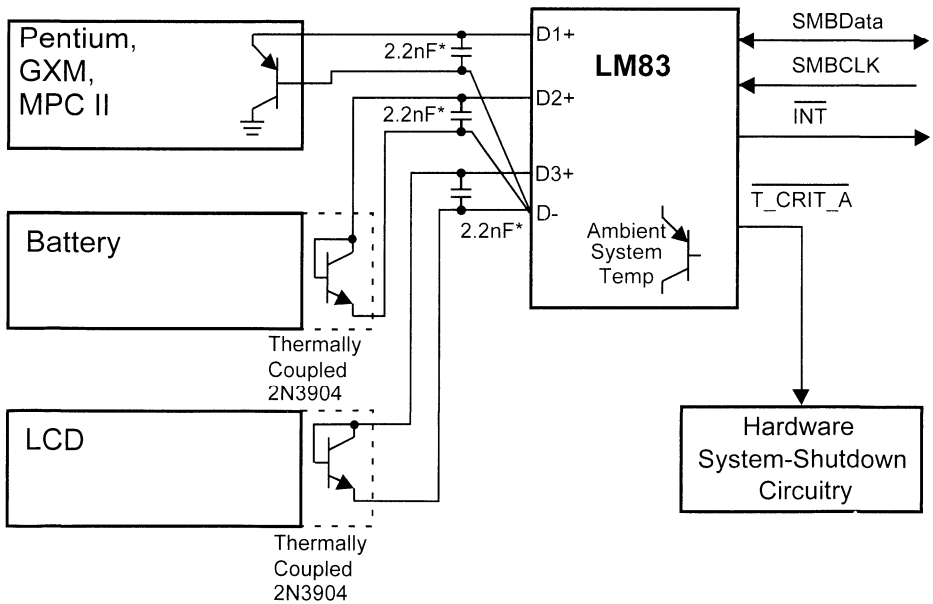
Connection Diagram



Ordering Information

Order Number	NS Package Number	Transport Media
LM83CIMQA	MQA16A (QSOP-16)	95 Units in Rail
LM83CIMQAX	MQA16A (QSOP-16)	2500 Units on Tape and Reel

Typical Application



*Note: 2.2nF Capacitors must be placed as close as possilbe to D+ and D- pins of the LM83.

DS101058-3

Pin Description

Label	Pin #	Function	Typical Connection
D1+, D2+, D3+	1, 3, 5	Diode Current Source	To Diode Anode. Connected to remote discrete diode junction or to the diode junction on a remote IC whose die temperature is being sensed. When not used they should be left floating.
V_{CC}	2	Positive Supply Voltage Input	DC Voltage from 3.0 V to 3.6 V

Pin Description (Continued)

Label	Pin #	Function	Typical Connection
D−	4	Diode Return Current Sink	To all Diode Junction Cathodes using a star connection to pin. Must float when not used.
ADD0–ADD1	10, 6	User-Set SMBus (I^2C) Address Inputs	Ground (Low, "0"), V_{CC} (High, "1") or open ("TRI-LEVEL")
GND	7, 8	Power Supply Ground	Ground
NC	9, 13, 15	Manufacturing test pins.	Left floating. PC board traces may be routed through the pads for these pins, although the components that drive these traces should share the same supply as the LM83 so that the Absolute Maximum Rating, Voltage at Any Pin, is not violated.
$\overline{INT}$	11	Interrupt Output, open-drain	Pull Up Resistor, Controller Interrupt or Alert Line
SMBData	12	SMBus (I^2C) Serial Bi-Directional Data Line, open-drain output	From and to Controller, Pull-Up Resistor
SMBCLK	14	SMBus (I^2C) Clock Input	From Controller, Pull-Up Resistor
$\overline{T\_CRIT\_A}$	16	Critical Temperature Alarm, open-drain output	Pull Up Resistor, Controller Interrupt Line or System Shutdown

National Semiconductor

LM84
Diode Input Digital Temperature Sensor with Two-Wire Interface

General Description

The LM84 is a remote diode temperature sensor, Delta-Sigma analog-to-digital converter, and digital over-temperature detector with an SMBus™ interface. The LM84 senses its own temperature as well as the temperature of a target IC with a diode junction, such as a Pentium® II processor or a diode connected 2N3904. A diode junction (semiconductor junction) is required on the target IC's die. A host can query the LM84 at any time to read the temperature of this diode as well as the temperature state of the LM84 itself. A $\overline{\text{T\_CRIT\_A}}$ interrupt output becomes active when the temperature is greater than a programmable comparator limit, T_CRIT.

The host can program as well as read back the state of the T_CRIT register. Three state logic inputs allow two pins (ADD0, ADD1) to select up to 9 SMBus address locations for the LM84. The sensor powers up with default thresholds of 127°C for T_CRIT.

Features

- Directly senses die temperature of remote ICs
- Senses temperature of remote diodes
- SMBus compatible interface, supports SMBus Timeout
- Register readback capability
- 7 bit plus sign temperature data format
- 2 address select lines enable 9 LM84s to be connected to a single bus

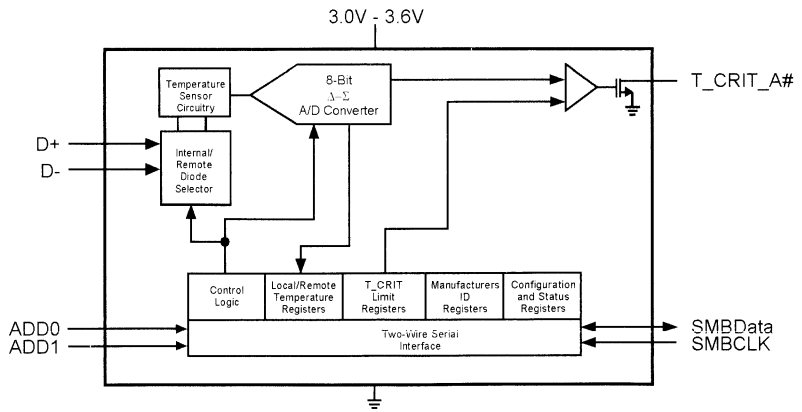
Key Specifications

■ Supply Voltage	3.0V - 3.6V
■ Supply Current	1 mA (max)
■ Local Temperature Accuracy	±1.0°C (typ)
■ Remote Diode Temperature Accuracy	
+60°C to +100°C	±3°C (max)
0°C to +125°C	±5°C (max)

Applications

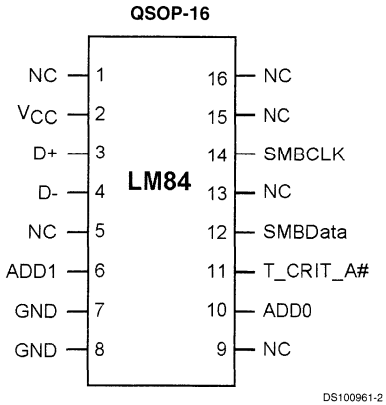
- System Thermal Management
- Personal Computers
- Electronic Test Equipment
- Office Electronics
- HVAC

Simplified Block Diagram



# Indicates Active Low ("NOT")

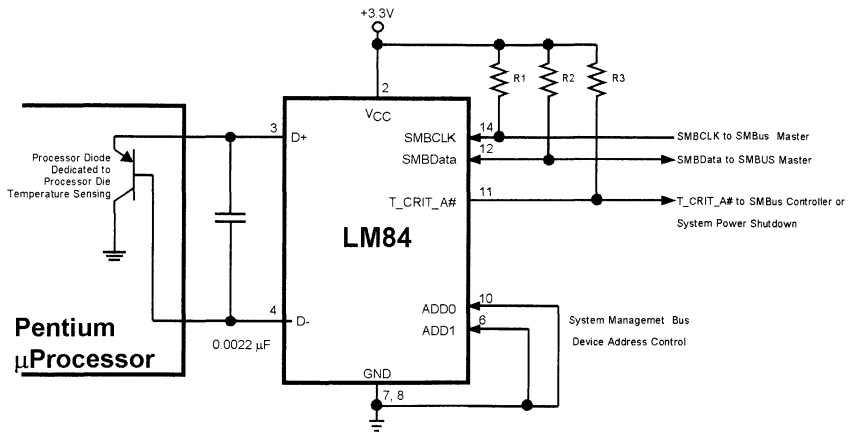
Connection Diagram



Ordering Information

Order Number	NS Package Number	Transport Media	SMBus Revision Level	Noise Filter on SMBCLK
LM84BIMQA	MQA16A (QSOP-16)	95 Units in Rail	1.1	20MHz
LM84BIMQAX	MQA16A (QSOP-16)	2500 Units on Tape and Reel	1.1	20MHz
LM84CIMQA	MQA16A (QSOP-16)	95 Units in Rail	1.0	Not Available
LM84CIMQAX	MQA16A (QSOP-16)	2500 Units on Tape and Reel	1.0	Not Available

Typical Application



Pin Descriptions

Label	Pin #	Function	Typical Connection
NC	1, 5, 9, 13, 16	Manufacturing test pins.	Left floating. PC board traces may be routed through the pads for these pins. Although, the components that drive these traces should share the same supply as the LM84 so that the Absolute Maximum Voltage at any Pin rating is not violated.
V_{CC}	2	Positive Supply Voltage Input	DC Voltage from 3.0V to 3.6V
D+	3	Diode Current Source	To Diode Anode. Connected to remote discrete diode or to the diode on the external IC whose die temperature is being sensed.
D−	4	Diode Return Current Sink	To Diode Cathode. Must be grounded when not used.
ADD0–ADD1	10, 6	User-Set SMBus (I^2C) Address Inputs	Ground (Low, "0"), V_{CC} (High, "1") or open ("TRI-LEVEL")
GND	7, 8	Power Supply Ground	Ground
$\overline{\text{T\_CRIT\_A}}$	11	Critical Temperature Alarm, open-drain output	Pull Up Resistor, Controller Interrupt Line or System Shutdown
SMBData	12	SMBus (I^2C) Serial Bi-Directional Data Line, open-drain output	From and to Controller, Pull Up Resistor
SMBCLK	14	SMBus (I^2C) Clock Input	From Controller
NC	15	No Connection	Left floating. PC board traces may be routed through the pads for this pin.

National Semiconductor

PRELIMINARY

LM86
±1°C Accurate, Remote Diode and Local Digital Temperature Sensor with Two-Wire Interface

General Description

The LM86 is an 11-bit digital temperature sensor with a 2-wire System Management Bus (SMBus) serial interface. This temperature sensor measures the voltage and thus the temperature of a remote diode using a Delta-Sigma analog-to-digital converter with a digital window comparator. The LM86 accurately measures its own temperature as well as the temperature of an external device, such as Pentium® III Processor or diode connected 2N3904. The remote diode temperature sensor is targeted for the non-ideality factor of 1.008. The temperature of any ASIC can be determined using the LM86 as long as a dedicated diode (semiconductor junction) is available on the die. The SMBus master can access the LM86's registers at any time. Activation of the $\overline{\text{ALERT}}$ output occurs when any temperature goes outside a preprogrammed interval set by the HIGH and LOW temperature limit registers or exceeds the T_CRIT temperature limit. Activation of the $\overline{\text{T\_CRIT\_A}}$ occurs when any temperature goes above the T_CRIT programmed limit.

The host can program as well as read back all the LOW, HIGH and T_CRIT registers. The sensor powers up with default values for all the LOW, HIGH and T_CRIT registers. The LM86 is pin and register compatible with the the Analog Devices ADM1032 and Maxim MAX6657/8.

Features

- Accurately senses die temperature of remote ICs or diode junctions
- On-board local temperature sensing
- 10 bit plus sign remote diode temperature data format, 0.125 °C resolution
- $\overline{\text{T\_CRIT\_A}}$ output useful for system shutdown
- $\overline{\text{ALERT}}$ output supports SMBus 2.0 protocol
- SMBus 2.0 compatible interface, supports TIMEOUT
- Register readback capability
- 8-pin MSOP and SOIC packages

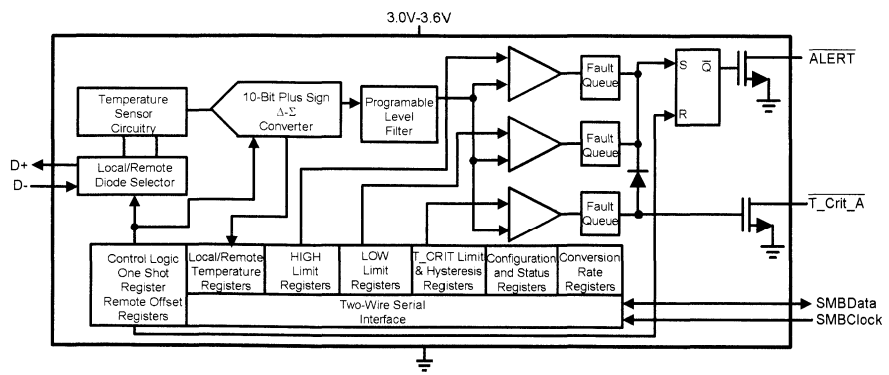
Key Specifications

- Supply Voltage 3.0V to 3.6V
- Supply Current 0.8mA (typ)
- Local Temp Accuracy (includes quantization error)
  T_A=25°C to 125°C ±3.0°C (max)
- Remote Diode Temp Accuracy (includes quantization error)
  T_A=30°C to 50°C, T_D=60°C to 100°C ±1.0°C (max)
  T_A=0°C to 85°C, T_D=25°C to 125°C ±3.0°C (max)

Applications

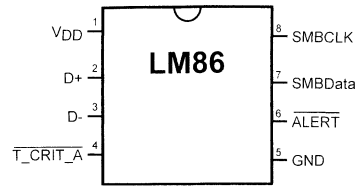
- System Thermal Management
- Computers
- Electronic Test Equipment
- Office Electronics
- HVAC

Simplified Block Diagram



Connection Diagram

MSOP-8 or SOIC-8



TOP VIEW

Ordering Information

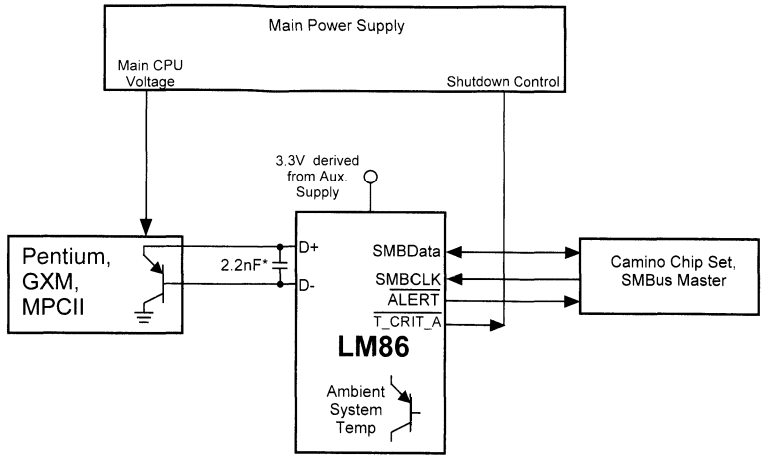
	Package Marking	NS Package Number	Transport Media	Remote Diode η, non_ideality Target*	Typical Processor Types*
LM86CIMM	T10C	MUA08A (MSOP-8)	1000 Units on Tape and Reel	1.008	Pentium III processor CPUID 68h/ PGA370Socket/Celeron®/ AMD Athlon® MP model 6
LM86CIMMX	T10C	MUA08A (MSOP-8)	3500 Units on Tape and Reel		
LM86CIM	LM86CIM	M08A (SOIC-8)	95 Units in Rail		
LM86CIMX	LM86CIM	M08A (SOIC-8)	2500 Units on Tape and Reel		

* - This is not meant to be an exhaustive list of possible processors. Any processor/transistor with a non_ideality as listed will yeild an accuracy as specied in the Electrical Characteristics. See *Section* 4.1.1 Diode Non-Ideality Factor Effect on Accuracy for a detailed explanation.

Pin Descriptions

Label	Pin #	Function	Typical Connection
V_{DD}	1	Positive Supply Voltage Input	DC Voltage from 3.0 V to 3.6 V
D+	2	Diode Current Source	To Diode Anode. Connected to remote discrete diode conected transistor junction or to the diode connected transistor junction on a remote IC whose die temperature is being sensed.
D–	3	Diode Return Current Sink	To Diode Cathode.
$\overline{\text{T\_CRIT\_A}}$	4	T_CRIT Alarm Output, Open-Drain, Active-Low	Pull-Up Resistor, Controller Interrupt or Power Supply Shutdown Control
GND	5	Power Supply Ground	Ground
$\overline{\text{ALERT}}$	6	Interrupt Output, Open-Drain, Active-Low	Pull-Up Resistor, Controller Interrupt or Alert Line
SMBData	7	SMBus Bi-Directional Data Line, Open-Drain Output	From and to Controller, Pull-Up Resistor
SMBCLK	8	SMBus Input	From Controller, Pull-Up Resistor

Typical Application



*Note: 2.2nF Capacitor must be placed as close as possible to D+ and D- pins of the LM86.

10130303

National Semiconductor

LM87
Serial Interface System Hardware Monitor with Remote Diode Temperature Sensing

General Description

The LM87 is a highly integrated data acquisition system for hardware monitoring of servers, Personal Computers, or virtually any microprocessor-based system. In a PC, the LM87 can be used to monitor power supply voltages, motherboard and processor temperatures, and fan speeds. Actual values for these inputs can be read at any time. Programmable WATCHDOG limits in the LM87 activate a fully programmable and maskable interrupt system with two outputs (INT# and THERM#).

The LM87 has an on-chip digital output temperature sensor with 8-bit resolution as well as the capability of monitoring 2 external diode temperatures to 8-bit resolution, an 8 channel analog input ADC with 8-bit resolution and an 8-bit DAC. A channel on the ADC measures the supply voltage applied to the LM87, nominally 3.3 V. Two of the ADC inputs can be redirected to a counter that can measure the speed of up to 2 fans. A slow speed ΣΔ ADC architecture allows stable measurement of signals in an extremely noisy environment. The DAC, with a 0 to 2.5 V output voltage range, can be used for fan speed control. Additional inputs are provided for Chassis Intrusion detection circuits, and VID monitor inputs. The VID monitor inputs can also be used as IRQ inputs if VID monitoring is not required. The LM87 has a Serial Bus interface that is compatible with SMBus™ and I²C™.

Features

- Remote diode temperature sensing (2 channels)
- 8 positive voltage inputs with scaling resistors for monitoring +5 V, +12 V, +3.3 V, +2.5 V, Vccp power supplies directly
- 2 inputs selectable for fan speed or voltage monitoring
- 8-bit DAC output for controlling fan speed
- Chassis Intrusion Detector input
- WATCHDOG comparison of all monitored values
- SMBus or I²C Serial Bus interface compatibility
- VID0-VID4 or IRQ0-IRQ4 monitoring inputs
- On chip temperature sensor

Key Specifications

■ Voltage Monitoring Error	±2 % (max)
■ External Temperature Error	±4 °C (max)
■ Internal Temperature Error	
−40 °C to +125 °C	± 3 °C (typ)
■ Supply Voltage Range	2.8 to 3.8 V
■ Supply Current	0.7 mA (typ)
■ ADC and DAC Resolution	8 Bits
■ Temperature Resolution	1.0 °C

Applications

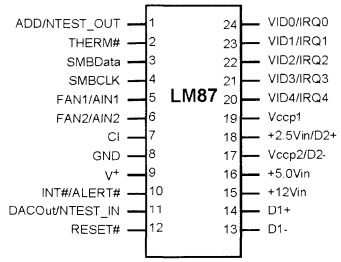
- System Thermal and Hardware Monitoring for Servers, Workstations and PCs
- Networking and Telecom Equipment
- Office Electronics
- Electronic Test Equipment and Instrumentation

Ordering Information

Temperature Range $-40\ ^\circ C \le T_A \le +125\ ^\circ C$		NS Package Number
Order Number	Device Marking	
LM87CIMT[1]	LM87CIMT	MTC24B
LM87CIMTX[2]	LM87CIMT	MTC24B

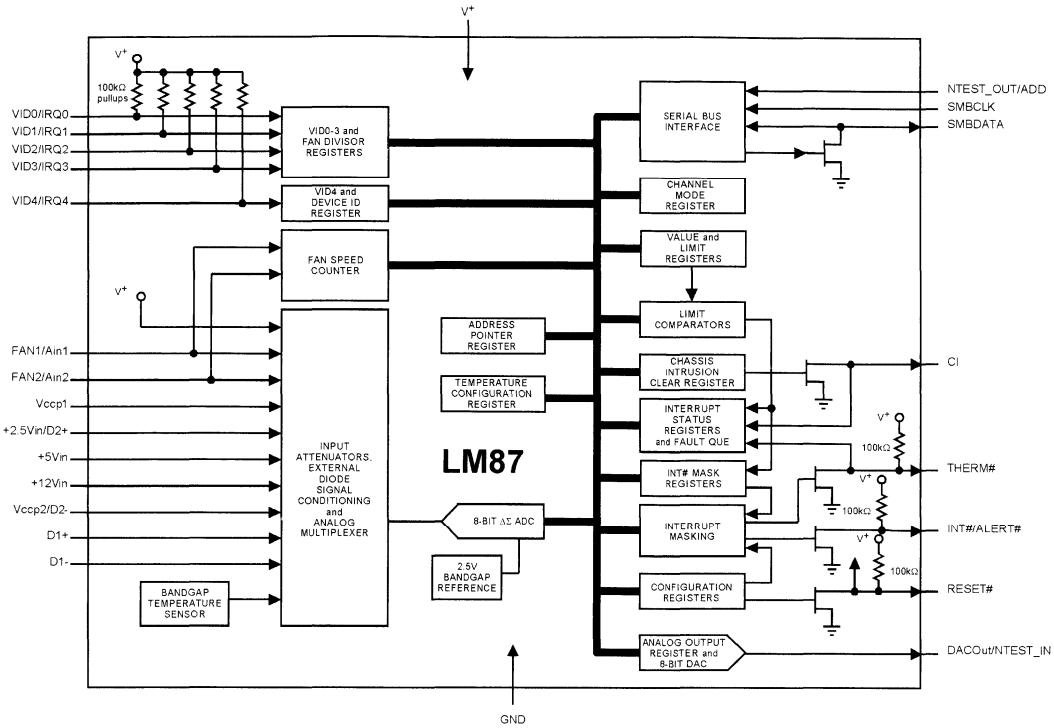
Note: [1]-Rail transport media, 61 parts per rail
[2]-Tape and reel transport media, 2500 parts per reel

Connection Diagram



10099503

Block Diagram



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Pin Description

Pin Name(s)	Pin Number	Number of Pins	Type	Description
ADD/NTEST_OUT	1	1	Digital I/0	This pin normally functions as a three-state input that controls the two LSBs of the Serial Bus Address. When this pin is tied to V_{CC} the two LSBs are 01. When tied to Ground, the two LSBs are 10. If this pin is not connected, the two LSBs are 00. This pin also functions as an output during NAND Tree tests (board-level connectivity testing). To ensure proper NAND tree function, this pin should not be tied directly to V_{CC} or Ground. Instead, a series 5 kΩ resistor should be used to allow the test output function to work. Refer to *SECTION 11* on NAND Tree testing.
THERM#	2	1	Digital I/O	This pin functions as an open-drain interrupt output for temperature interrupts only, or as an interrupt input for fan control. It has an on-chip 100 kΩ pullup resistor.
SMBData	3	1	Digital I/O	Serial Bus bidirectional Data. Open-drain output.
SMBCLK	4	1	Digital Input	Serial Bus Clock.
FAN1/AIN1-FAN2/AIN2	5-6	2	Analog/Digital Inputs	Programmable as analog inputs (0 to 2.5V) or digital Schmitt Trigger fan tachometer inputs.
CI	7	1	Digital I/O	An active high input from an external circuit which latches a Chassis Intrusion event. This line can go high without any clamping action regardless of the powered state of the LM87. There is also an internal open-drain output on this line, controlled by Bit 7 of the CI Clear Register (46h), to provide a minimum 20 ms reset pulse.

Pin Description (Continued)

Pin Name(s)	Pin Number	Number of Pins	Type	Description
GND	8	1	GROUND	The system ground pin. Internally connected to all circuitry. The ground reference for all analog inputs and the DAC output. This pin needs to be connected to a low noise analog ground plane for optimum performance of the DAC output.
V^+ (+2.8 V to +3.8 V)	9	1	POWER	+3.3 V V^+ power. Bypass with the parallel combination of 10 µF (electrolytic or tantalum) and 0.1 µF (ceramic) bypass capacitors.
INT# /ALERT#	10	1	Digital Output	Interrupt active low open-drain output. This output is enabled when Bit 1 in the Configuration Register is set to 1. The default state is disabled. It has an on-chip 100 kΩ pullup resistor. Alternately used as an active low output to signal SMBus Alert Response Protocol.
DACOut/NTEST_IN	11	1	Analog Output/Digital Input	0 V to +2.5 V amplitude 8-bit DAC output. When forced high on power up by an external voltage the NAND Tree Test mode is enabled which provides board-level connectivity testing.
RESET#	12	1	Digital I/O	Master Reset, 5 mA driver (open-drain), active low output with a 45 ms minimum pulse width. Available when enabled via Bit 4 in the Configuration register. It also acts as an active low power on RESET input. It has an on-chip 100 kΩ pullup resistor.
D1–	13	1	Analog Input	Analog input for monitoring the cathode of the first external temperature sensing diode.
D1+	14	1	Analog Input	Analog input for monitoring the anode of the first external temperature sensing diode.
+12Vin	15	1	Analog Input	Analog input for monitoring +12 V.
+5Vin	16	1	Analog Input	Analog input for monitoring +5 V.
Vccp2/D2–	17	1	Analog Input	Digitally programmable analog input for monitoring Vccp2 (0 to 3.6 V input range) or the cathode of the second external temperature sensing diode.
+2.5Vin/D2+	18	1	Analog Input	Digitally programmable analog input for monitoring +2.5 V or the anode of the second external temperature sensing diode.
Vccp1	19	1	Analog Input	Analog input (0 to 3.6 V input range) for monitoring Vccp1, the core voltage of processore 1.
VID4/IRQ4-VID0/IRQ0	20-24	5	Digital Inputs	Digitally programmable dual function digital inputs. Can be programmed to monitor the VID pins of the Pentium/PRO and Pentium II processors, that indicate the operating voltage of the processor, or as interrupt inputs. The values are read in the VID/Fan Divisor Register and the VID4 Register. These inputs have on-chip 100 kΩ pullup resistors.
TOTAL PINS		**24**		

# Indicates Active Low ("Not")

National Semiconductor

LM88
Factory Programmable Dual Remote-Diode Thermostat

General Description

The LM88 is a dual remote-diode temperature sensor with 3 digital comparators. The LM88 has 3 open-drain outputs ($\overline{O\_SP0}$, $\overline{O\_SP1}$ and $\overline{O\_CRIT}$) that can be used as interrupts or to signal system shutdown. The digital comparators can be factory programmed to make a greater than or less than comparison. When programmed for a greater than comparison outputs:

$\overline{O\_SP0}$ and $\overline{O\_SP1}$ activate when the temperatures measured by D0 or D1 exceed the associated setpoints of T_SP0 or T_SP1.

$\overline{O\_CRIT}$ activates when the temperature measured by either D0 or D1 exceeds setpoint T_CRIT.

T_CRIT can be set at 1°C intervals from −40°C to +125°C. T_SP0 and T_SP1 can be set at 4°C intervals in the range of T_CRIT +127°C/−128°C. Hysteresis for all comparators is set to 1°C. $\overline{O\_CRIT}$, in conjunction with T_CRIT, could be used to prevent catastrophic damage to key subsystems such as notebook Card Bus cards while $\overline{O\_SP0}$ and $\overline{O\_SP1}$, in conjunction with T_SP0 and T_SP1, can warn of an impending failure.

The LM88 is available in an 8-lead mini-small-outline package.

Applications

- Microprocessor Thermal Management
- Appliances
- Portable Battery Powered Systems
- Fan Control
- Industrial Process Control
- HVAC Systems
- Remote Temperature Sensing
- Electronic System Protection

Features

- 2 external remote diode input channels
- 3 digital comparator outputs, 1 per remote diode and one T_CRIT common to both
- Factory programmable greater than or less than comparisons
- 1°C comparator hysteresis
- 2 setpoints, T_SP0 and T_SP1, factory programmable in 4°C intervals
- 1 setpoint, T_CRIT, factory programmable in 1°C intervals
- Active Low open-drain digital outputs
- 8-pin mini-SO plastic package

Key Specifications

■ Power Supply Voltage	2.8V–3.8V
■ Power Supply Current	1.5 mA (max)
■ LM88 Temperature Range	−40°C to +85°C
■ Diode Setpoint Temperature Range	0°C to +125°C

Temperature Trip Point Accuracy:

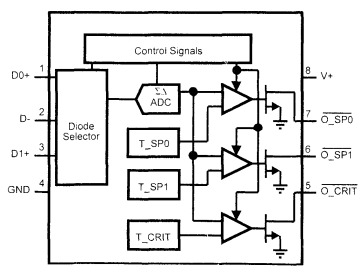
Diode Junction Temperature (T_{DJ})	LM88CIM Accuracy	LM88CIM Temperature Range
+45°C to +85°C	±3°C (max)	−40°C to +85°C
+60°C to +100°C	±3°C (max)	−40°C to +85°C

Note: These are sample ranges. Contact factory for other ranges.

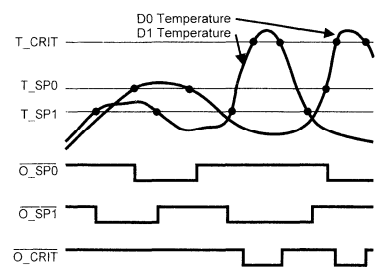
13

Simplified Block Diagram and Connection Diagram

MSOP-8/MUA08A Package



Top View



For simplicity, the effects of the hysteresis are not shown in the temperature response diagram.

Simplified Block Diagram and Connection Diagram (Continued)

Order Number	Device Marking	NS Package Number	Transport Media	T_SP0 (°C)	T_SP1 (°C)	T_CRIT (°C)	Setpoint Accuracy (°C)
LM88CIMM-A	T08A	MUA08A or MSOP-8	Rail	61	49	80	±3
LM88CIMMX-A			Tape and Real				
LM88CIMM-B	T08A	MUA08A or MSOP-8	Rail	41	49	60	±3
LM88CIMMX-B			Tape and Real				

For other setpoints please contact the factory. Performance is dependent on temperature range.

Typical Application

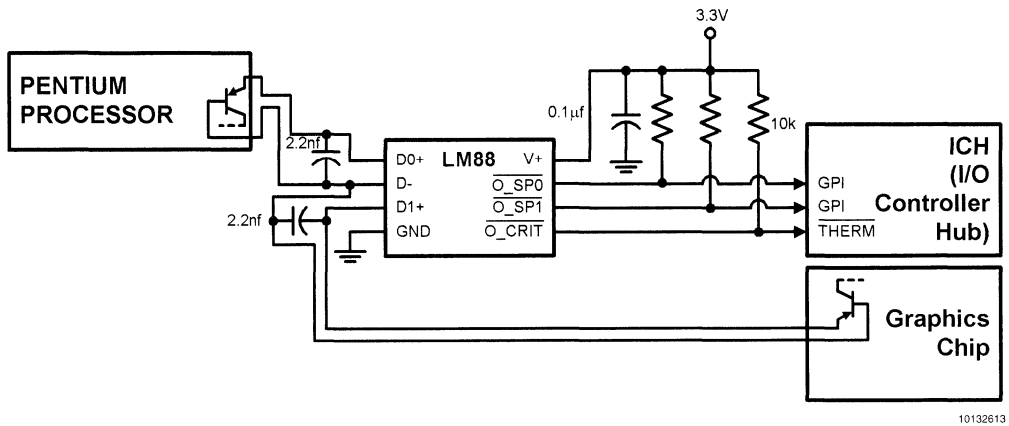


FIGURE 1. Thermal Protection for Pentium® Processor and Graphics Chip

National Semiconductor

LM91
Diode Input Digital Temperature Sensor with Two-Wire Interface

General Description

The LM91 is a remote diode temperature sensor, Delta-Sigma analog-to-digital converter, and digital over-temperature detector with an SMBus™ interface. The LM91 senses its own temperature as well as the temperature of a target IC with a diode junction, such as a Pentium® II processor or a diode connected 2N3904. A diode junction (semiconductor junction) is required on the target IC's die. A host can query the LM91 at any time to read the temperature of this diode as well as the temperature state of the LM91 itself. A $\overline{\text{T\_CRIT\_A}}$ interrupt output becomes active when the temperature is greater than a programmable comparator limit, T_CRIT.

The host can program as well as read back the state of the T_CRIT register. Power up default values for T_CRIT are as shown in the ordering information table. Three state logic inputs allow two pins (ADD0, ADD1) to select up to 9 SMBus address locations for the LM91.

Features

- Directly senses die temperature of remote ICs
- Senses temperature of remote diodes
- SMBus compatible interface, supports SMBus Timeout
- Register readback capability
- 7 bit plus sign temperature data format
- 2 address select lines enable 9 LM91s to be connected to a single bus

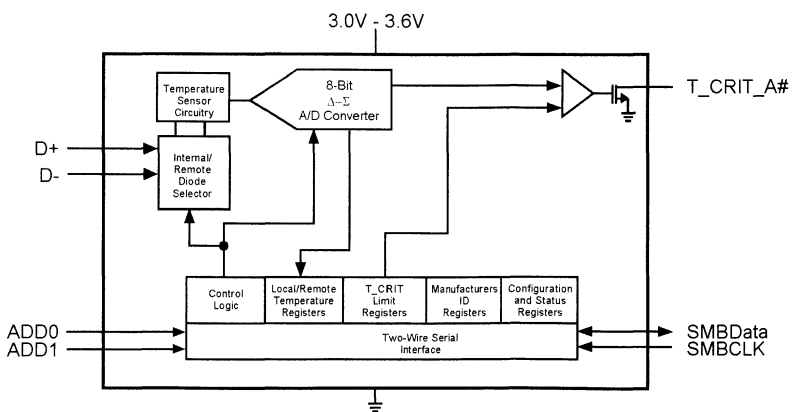
Key Specifications

■ Supply Voltage	3.0V - 3.6V
■ Supply Current	1 mA (max)
■ Local Temperature Accuracy	±1.0˚C (typ)
■ Remote Diode Temperature Accuracy	
+60˚C to +100˚C	±4˚C (max)
0˚C to +125˚C	±6˚C (max)

Applications

- System Thermal Management
- Personal Computers
- Electronic Test Equipment
- Office Electronics
- HVAC

Simplified Block Diagram

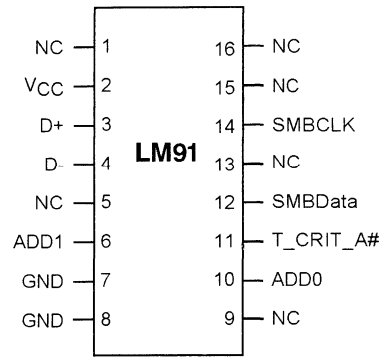


20034301

# Indicates Active Low ("NOT")

Connection Diagram

QSOP-16



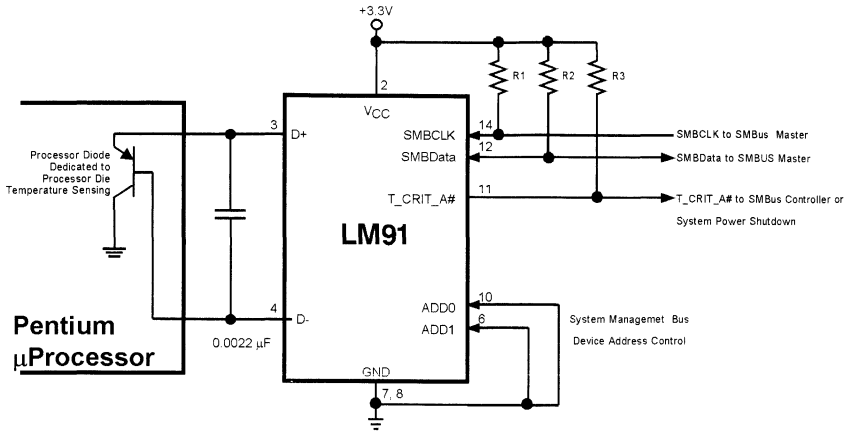
20034302

TOP VIEW

Ordering Information

Order Number	NS Package Number	Transport Media	SMBus Revision Level	Noise Filter on SMBCLK	Remote Diode Accuracy	Local T_CRIT Default	Remote T_CRIT Default
LM91DIMQA	MQA16A (QSOP-16)	95 Units in Rail	1.1	20MHz	±4°C	127°C	95°C
LM91DIMQAX	MQA16A (QSOP-16)	2500 Units on Tape and Reel	1.1	20MHz	±4°C	127°C	95°C

Typical Application



20034303

Pin Descriptions

Label	Pin #	Function	Typical Connection
NC	1, 5, 9, 13, 16	Manufacturing test pins.	Left floating. PC board traces may be routed through the pads for these pins. Although, the components that drive these traces should share the same supply as the LM91 so that the Absolute Maximum Voltage at any Pin rating is not violated.
V_{CC}	2	Positive Supply Voltage Input	DC Voltage from 3.0V to 3.6V
D+	3	Diode Current Source	To Diode Anode. Connected to remote discrete diode or to the diode on the external IC whose die temperature is being sensed.
D–	4	Diode Return Current Sink	To Diode Cathode. Must be grounded when not used.
ADD0–ADD1	10, 6	User-Set SMBus (I^2C) Address Inputs	Ground (Low, "0"), V_{CC} (High, "1") or open ("TRI-LEVEL")
GND	7, 8	Power Supply Ground	Ground
$\overline{\text{T\_CRIT\_A}}$	11	Critical Temperature Alarm, open-drain output	Pull Up Resistor, Controller Interrupt Line or System Shutdown
SMBData	12	SMBus (I^2C) Serial Bi-Directional Data Line, open-drain output	From and to Controller, Pull Up Resistor
SMBCLK	14	SMBus (I^2C) Clock Input	From Controller
NC	15	No Connection	Left floating. PC board traces may be routed through the pads for this pin.

National Semiconductor

LM92
±0.33°C Accurate, 12-Bit + Sign Temperature Sensor and Thermal Window Comparator with Two-Wire Interface

General Description

The LM92 is a digital temperature sensor and thermal window comparator with an I²C™ Serial Bus interface and an accuracy of ±0.33°C. The window-comparator architecture of the LM92 eases the design of temperature control systems. The open-drain Interrupt (INT) output becomes active whenever temperature goes outside a programmable window, while a separate Critical Temperature Alarm (T_CRIT_A) output becomes active when the temperature exceeds a programmable critical limit. The INT output can operate in either a comparator or event mode, while the T_CRIT_A output operates in comparator mode only.

The host can program both the upper and lower limits of the window as well as the critical temperature limit. Programmable hysterisis as well as a fault queue are available to minimize false tripping. Two pins (A0, A1) are available for address selection. The sensor powers up with default thresholds of 2°C T_{HYST}, 10°C T_{LOW}, 64°C T_{HIGH}, and 80°C T_CRIT.

The LM92's 2.7V to 5.5V supply voltage range, Serial Bus interface, 12-bit + sign output, and full-scale range of over 128°C make it ideal for a wide range of applications. These include thermal management and protection applications in personal computers, electronic test equipment, office electronics, automotive, medical and HVAC applications.

Features

- Window comparison simplifies design of ACPI compatible temperature monitoring and control.
- Serial Bus interface
- Separate open-drain outputs for Interrupt and Critical Temperature shutdown
- Shutdown mode to minimize power consumption
- Up to 4 LM92s can be connected to a single bus
- 12-bit + sign output
- Operation up to 150°C

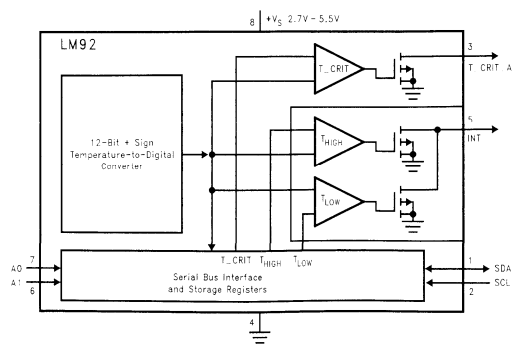
Key Specifications

■ Supply Voltage		2.7V to 5.5V
■ Supply Current	operating	350µA (typ)
		625µA (max)
	shutdown	5µA (typ)
■ Temperature	30°C	±0.33°C(max)
Accuracy	10°C to 50°C	±0.50°C(max)
	−10°C to 85°C	±1.0°C(max)
	125°C	±1.25°C(max)
	−25°C to 150°C	±1.5°C(max)
■ Linearity		±0.5°C(max)
■ Resolution		0.0625°C

Applications

- HVAC
- Medical Electronics
- Electronic Test Equipment
- System Thermal Management
- Personal Computers
- Office Electronics
- Automotive

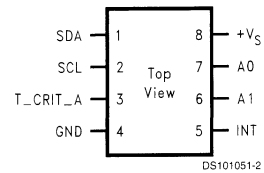
Simplified Block Diagram



DS101051-1

Connection Diagram

SO-8



LM92
See NS Package Number M08A

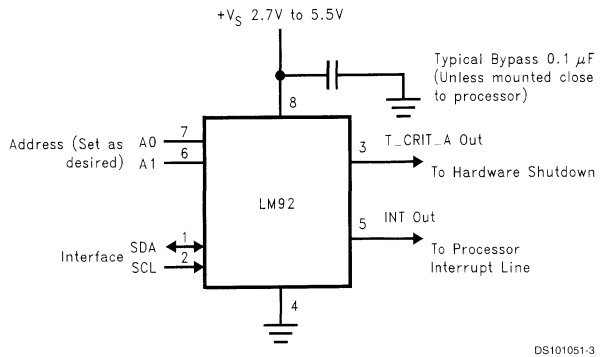
Ordering Information

Order Number	Supply Voltage	Supplied As
LM92CIM	2.7V to 5.5V	
LM92CIMX	2.7V to 5.5V	2500 Units on Tape and Reel

Pin Descriptions

Label	Pin #	Function	Typical Connection
SDA	1	Serial Bi-Directional Data Line. Open Drain Output	From Controller
SCL	2	Serial Bus Clock Input	From Controller
T_CRIT_A	3	Critical Temperature Alarm Open Drain Output	Pull Up Resistor, Controller Interrupt Line or System Hardware Shutdown
GND	4	Power Supply Ground	Ground
INT	5	Interrupt Open Drain Output	Pull Up Resistor, Controller Interrupt Line
$+V_S$	8	Positive Supply Voltage Input	DC Voltage from 2.7V to 5.5V
A0–A1	7,6	User-Set Address Inputs	Ground (Low, "0") or $+V_S$ (High, "1")

Typical Application



National Semiconductor

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM234-3 and LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

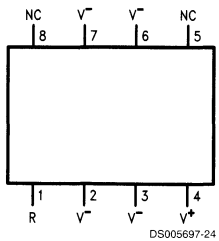
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic, TO-92 and SO-8 plastic packages.

Features

- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1μA to 10mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

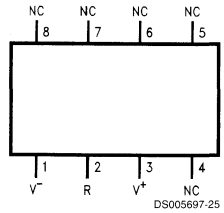
Connection Diagrams

SO-8
Surface Mount Package



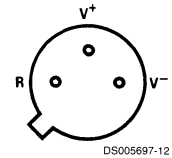
Order Number LM334M or LM334MX
See NS Package Number M08A

SO-8 Alternative Pinout
Surface Mount Package



Order Number LM334SM or LM334SMX
See NS Package Number M08A

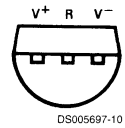
TO-46
Metal Can Package



V⁻ Pin is electrically connected to case.

Bottom View
Order Number LM134H, LM234H or LM334H
See NS Package Number H03H

TO-92 Plastic Package



Bottom View
Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package Number Z03A

National Semiconductor

LM135/LM235/LM335, LM135A/LM235A/LM335A Precision Temperature Sensors

General Description

The LM135 series are precision, easily-calibrated, integrated circuit temperature sensors. Operating as a 2-terminal zener, the LM135 has a breakdown voltage directly proportional to absolute temperature at +10 mV/°K. With less than 1Ω dynamic impedance the device operates over a current range of 400 μA to 5 mA with virtually no change in performance. When calibrated at 25°C the LM135 has typically less than 1°C error over a 100°C temperature range. Unlike other sensors the LM135 has a linear output.

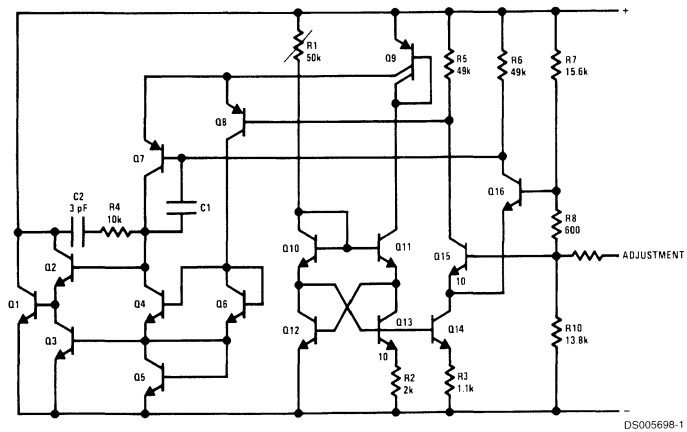
Applications for the LM135 include almost any type of temperature sensing over a −55°C to +150°C temperature range. The low impedance and linear output make interfacing to readout or control circuitry especially easy.

The LM135 operates over a −55°C to +150°C temperature range while the LM235 operates over a −40°C to +125°C temperature range. The LM335 operates from −40°C to +100°C. The LM135/LM235/LM335 are available packaged in hermetic TO-46 transistor packages while the LM335 is also available in plastic TO-92 packages.

Features

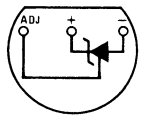
- Directly calibrated in °Kelvin
- 1°C initial accuracy available
- Operates from 400 μA to 5 mA
- Less than 1Ω dynamic impedance
- Easily calibrated
- Wide operating temperature range
- 200°C overrange
- Low cost

Schematic Diagram



Connection Diagrams

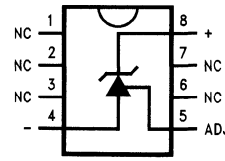
TO-92
Plastic Package



DS005698-8

Bottom View
Order Number LM335Z
or LM335AZ
See NS Package
Number Z03A

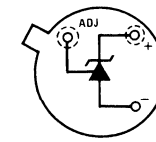
SO-8
Surface Mount Package



DS005698-25

Order Number LM335M
See NS Package
Number M08A

TO-46
Metal Can Package*



DS005698-26

*Case is connected to negative pin

Bottom View
Order Number LM135H,
LM135H-MIL, LM235H,
LM335H, LM135AH,
LM235AH or LM335AH
See NS Package
Number H03H

Section 14
Voltage References

Section 14 Contents

National Semiconductor

Voltage Reference Selection Guide

Low Dropout Voltage References

Output Voltage	Device	Voltage Tolerance Max, T_A= 25°C	Temperature Drift		Load Reg. %/mA	Output Current	Quiescent Current (µA)
			ppm/°C (Max)	Over Range			
0.2 (Adj)	‡LM10B	±2.5%	20 typ	−25°C to +85°C	0.01%	0mA	0.27
	‡LM10C	±5.0%	30 typ	0°C to +70°C	0.01%	0mA	0.30
1.024	LM4140A-1.0	0.1%	3	0°C to 70°C	1	8mA	230
	LM4140B-1.0	0.1%	6	0°C to 70°C	1	8mA	230
	LM4140C-1.0	0.1%	10	0°C to 70°C	1	8mA	230
1.250	LM4121AI-1.2	0.2%	50	−40°C to +85°C	0.01	±5mA	160
	LM4121I-1.2	0.5%	50	−40°C to +85°C	0.01	±5mA	160
	LM4140A-1.2	0.1%	3	0°C to 70°C	1	8mA	230
	LM4140B-1.2	0.1%	6	0°C to 70°C	1	8mA	230
	LM4140C-1.2	0.1%	10	0°C to 70°C	1	8mA	230
1.250 (Adj.)	LM4121AI-ADJ	0.2%	50	−40°C to +85°C	0.01	±5mA	160
	LM4121I-ADJ	0.5%	50	−40°C to +85°C	0.01	±5mA	160
1.800	LM4120AI-1.8	0.2%	50	−40°C to +85°C	0.04	±5mA	160
	LM4120I-1.8	0.5%	50	−40°C to +85°C	0.04	±5mA	160
2.048	LM4120AI-2.0	0.2%	50	−40°C to +85°C	0.04	±5mA	160
	LM4120I-2.0	0.5%	50	−40°C to +85°C	0.04	±5mA	160
	LM4130AI-2.0	0.05%	10	−40°C to +85°C	32	20mA	50
	LM4130BI-2.0	0.2%	10	−40°C to +85°C	32	20mA	50
	LM4130CI-2.0	0.1%	20	−40°C to +85°C	32	20mA	50
	LM4130DI-2.0	0.4%	20	−40°C to +85°C	32	20mA	50
	LM4130EI-2.0	0.5%	30	−40°C to +85°C	32	20mA	50
	LM4140A-2.0	0.1%	3	0°C to 70°C	1	8mA	230
	LM4140B-2.0	0.1%	6	0°C to 70°C	1	8mA	230
	LM4140C-2.0	0.1%	10	0°C to 70°C	1	8mA	230
2.50	LM4120AI-2.5	0.2%	50	−40°C to +85°C	0.04	±5mA	50
	LM4120I-2.5	0.5%	50	−40°C to +85°C	0.04	±5mA	50
	LM4130AI-2.5	0.05%	10	−40°C to +85°C	25	20mA	50
	LM4130BI-2.5	0.2%	10	−40°C to +85°C	25	20mA	50
	LM4130CI-2.5	0.1%	20	−40°C to +85°C	25	20mA	50
	LM4130DI-2.5	0.4%	20	−40°C to +85°C	25	20mA	50
	LM4130EI-2.5	0.5%	30	−40°C to +85°C	25	20mA	50
	LM4140A-2.5	0.1%	3	0°C to 70°C	1	8mA	230
	LM4140B-2.5	0.1%	6	0°C to 70°C	1	8mA	230
	LM4140C-2.5	0.1%	10	0°C to 70°C	1	8mA	230
3.0	LM4120AI-3.0	0.2%	50	−40°C to +85°C	0.04	±5mA	160
	LM4120I-3.0	0.5%	50	−40°C to +85°C	0.04	±5mA	160
3.3	LM4120AI-3.3	0.2%	50	−40°C to +85°C	0.04	±5mA	160
	LM4120I-3.3	0.5%	50	−40°C to +85°C	0.04	±5mA	160

Low Dropout Voltage References (Continued)

Output Voltage	Device	Voltage Tolerance Max, T_A= 25°C	Temperature Drift		Load Reg. %/mA	Output Current	Quiescent Current (µA)
			ppm/°C (Max)	Over Range			
4.096	LM4120AI-4.1	0.2%	50	−40°C to +85°C	0.04	±5mA	160
	LM4120I-4.1	0.5%	50	−40°C to +85°C	0.04	±5mA	160
	LM4130AI-4.1	0.05%	10	−40°C to +85°C	16	20mA	50
	LM4130BI-4.1	0.2%	10	−40°C to +85°C	16	20mA	50
	LM4130CI-4.1	0.1%	20	−40°C to +85°C	16	20mA	50
	LM4130DI-4.1	0.4%	20	−40°C to +85°C	16	20mA	50
	LM4130EI-4.1	0.5%	30	−40°C to +85°C	16	20mA	50
	LM4140A-4.1	0.1%	3	0°C to 70°C	5	8mA	230
	LM4140B-4.1	0.1%	6	0°C to 70°C	5	8mA	230
	LM4140C-4.1	0.1%	10	0°C to 70°C	5	8mA	230
5.0	LM4120AI-5.0	0.2%	50	−40°C to +85°C	0.04	±5mA	160
	LM4120AI-5.0	0.5%	50	−40°C to +85°C	0.04	±5mA	160

‡Reference has on-board Op Amp.

Shunt References

Reverse Breakdown Voltage (V_R)	Device	Voltage Tolerance Max, T_A= 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance Ω (Typ)
			ppm/°C (Max)	Over Range		
1.225*	LM4041AI-1.2	± 0.1%	100	−40°C to +85°C	60µA to 12mA	1.5 Max
	LM4041BI-1.2	± 0.2%	100	−40°C to +85°C	60µA to 12mA	1.5 Max
	LM4041CI-1.2	± 0.5%	100	−40°C to +85°C	60µA to 12mA	1.5 Max
	LM4041DI-1.2	± 1.0%	150	−40°C to +85°C	65µA to 12mA	2.0 Max
	LM4041EI-1.2	± 2.0%	150	−40°C to +85°C	65µA to 12mA	2.0 Max
	LM4041CE-1.2	± 0.5%	100	−40°C to +125°C	60µA to 12mA	1.5 Max
	LM4041DE-1.2	± 1.0%	150	−40°C to +125°C	60µA to 12mA	1.5 Max
	LM4041EE-1.2	± 2.0%	150	−40°C to +125°C	65µA to 12mA	2.0 Max
	LM4051AI-1.2	± 0.1%	50	−40°C to +85°C	60µA to 12mA	0.3
	LM4051BI-1.2	± 0.1%	50	−40°C to +85°C	60µA to 12mA	0.3
	LM4051CI-1.2	± 0.1%	50	−40°C to +85°C	60µA to 12mA	0.3
1.22	LM113-2	± 1%	100 (Typ)	−55°C to +125°C	500µA to 20mA	1.0 Max
	LM113-1	± 2%	100 (Typ)	−55°C to +125°C	500µA to 20mA	1.0 Max
	LM113	± 5%	100 (Typ)	−55°C to +125°C	500µA to 20mA	1.0 Max
	LM313	± 5%	100 (Typ)	0°C to +70°C	500µA to 20mA	1.0 Max

Shunt References (Continued)

Reverse Breakdown Voltage (V_R)	Device	Voltage Tolerance Max, T_A= 25˚C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance Ω (Typ)
			ppm/˚C (Max)	Over Range		
1.235	LM185BX-1.2	± 1%	30	−55˚C to +125˚C	10µA to 20mA	1
	LM185BY-1.2	± 1%	50	−55˚C to +125˚C	10µA to 20mA	1
	LM185-1.2	± 1%	150	−55˚C to +125˚C	10µA to 20mA	1
	LM285BX-1.2	± 1%	30	−40˚C to +85˚C	10µA to 20mA	1
	LM285BY-1.2	± 1%	50	−40˚C to +85˚C	10µA to 20mA	1
	LM285-1.2	± 1%	150	−40˚C to +85˚C	10µA to 20mA	1
	LM385BX-1.2	± 1%	30	0˚C to +70˚C	15µA to 20mA	1
	LM385BY-1.2	± 1%	50	0˚C to +70˚C	15µA to 20mA	1
	LM385B-1.2	± 1%	150	0˚C to +70˚C	15µA to 20mA	1
	LM385M3-1.2*	+ 2%, −2.4%	150	0˚C to +70˚C	10µA to 20mA	1
	LM385-1.2	+ 2%, −2.4%	150	0˚C to +70˚C	15µA to 20mA	1
1.24 to 5.3 (Adj.)	LM185B	± 1%	150	−55˚C to +125˚C	10µA to 20mA	0.3
	LM185BX	± 1%	30	−55˚C to +125˚C	10µA to 20mA	0.3
	LM185BY	± 1%	50	−55˚C to +125˚C	10µA to 20mA	0.3
	LM285BX	± 1%	30	−40˚C to +85˚C	10µA to 20mA	0.3
	LM285BY	± 1%	50	−40˚C to +85˚C	10µA to 20mA	0.3
	LM285	± 2%	150	−40˚C to +85˚C	10µA to 20mA	0.3
	LM385BX	± 1%	30	0˚C to +70˚C	13µA to 20mA	0.4
	LM385BY	± 1%	50	0˚C to +70˚C	13µA to 20mA	0.4
	LM385	± 2%	150	0˚C to +70˚C	13µA to 20mA	0.4
1.225 to 10V (Adj.)	LM4041DE-ADJ	± 1%	150	−40˚C to +125˚C	60µA to 12mA	2.0
	LM4041DI-ADJ	± 1%	150	−40˚C to +85˚C	60µA to 12mA	2.0
	LM4041CE-ADJ	± 0.5%	100	−40˚C to +125˚C	60µA to 12mA	2.0
	LM4041CI-ADJ	± 0.5%	100	−40˚C to +85˚C	60µA to 12mA	2.0
	LM4051AI-ADJ	± 0.1%	50	−40˚C to +85˚C	60µA to 12mA	2.0
	LM4051BI-ADJ	± 0.1%	50	−40˚C to +85˚C	60µA to 12mA	2.0
	LM4051CI-ADJ	± 0.1%	50	−40˚C to +85˚C	60µA to 12mA	2.0
1.24 to 30V (Adj.)*	LMV431AI	± 1%	129	−40˚C to +85˚C	80 µA to 20mA	0.25
	LMV431AC	± 1%	129	0˚C to +70˚C	80 µA to 20mA	0.25
	LMV431I	± 1.5%	129	−40˚C to +85˚C	80 µA to 20mA	0.25
	LMV431C	± 1.5%	129	0˚C to +70˚C	80 µA to 20mA	0.25
1.24 to 6.3 (Adj.)	†LM611IM	± 0.6%	150	−55˚C to +125˚C	16µA to 10mA	0.2
	LM611C	± 2.0%	150	0˚C to +70˚C	16µA to 10mA	0.2
	††LM613AM	± 0.6%	80	−55˚C to +125˚C	16µA to 10mA	0.2
	††LM613M	± 2.0%	150	−55˚C to +125˚C	16µA to 10mA	0.2
	LM613AI	± 0.6%	80	−40˚C to +85˚C	16µA to 10mA	0.2
	LM613I	± 2.0%	150	−40˚C to +85˚C	16µA to 10mA	0.2
	LM613C	± 2.0%	150	0˚C to +70˚C	16µA to 10mA	0.2
	‡LM614M	± 2.0%	150	−55˚C to +125˚C	16µA to 10mA	0.2
	LM614I	± 2.0%	150	−40˚C to +85˚C	16µA to 10mA	0.2
	LM614C	± 2.0%	150	0˚C to +70˚C	16µA to 10mA	0.2
2.49	LM136A	± 1%	72	−55˚C to +125˚C	400µA to 10mA	0.4
	LM136	± 2%	72	−55˚C to +125˚C	400µA to 10mA	0.4
	LM236A	± 1%	72	−25˚C to +85˚C	400µA to 10mA	0.4
	LM236	± 2%	72	−25˚C to +85˚C	400µA to 10mA	0.4
	LM336	± 4%	54	0˚C to +70˚C	400µA to 10mA	0.4
	LM336B	± 2%	54	0˚C to +70˚C	400µA to 10mA	0.4

Shunt References (Continued)

Reverse Breakdown Voltage (V_R)	Device	Voltage Tolerance Max, T_A= 25°C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance Ω (Typ)
			ppm/°C (Max)	Over Range		
2.5*	LM4040AI-2.5	± 0.1%	100	−40°C to +85°C	65µA to 15mA	0.8 Max
	LM4040BI-2.5	± 0.2%	100	−40°C to +85°C	65µA to 15mA	0.8 Max
	LM4040CI-2.5	± 0.5%	100	−40°C to +85°C	65µA to 15mA	0.8 Max
	LM4040DI-2.5	± 1.0%	150	−40°C to +85°C	65µA to 15mA	0.9 Max
	LM4040EI-2.5	± 2.0%	150	−40°C to +85°C	65µA to 15mA	1.1 Max
	LM4040CE-2.5	± 0.5%	100	−40°C to +125°C	65µA to 15mA	0.8 Max
	LM4040DE-2.5	± 1.0%	150	−40°C to +125°C	65µA to 15mA	0.9 Max
	LM4040EE-2.5	± 2.0%	150	−40°C to +125°C	65µA to 15mA	1.1 Max
	LM4050A-2.5	± 0.1%	50	−40°C to +85°C	60µA to 15mA	0.3
	LM4050B-2.5	± 0.2%	50	−40°C to +85°C	60µA to 15mA	0.3
	LM4050C-2.5	± 0.5%	50	−40°C to +85°C	60µA to 15mA	0.3
	LM4431-2.5	± 2.0%	30 Typ.	0°C to +70°C	45µA to 15mA	1.0
2.5	LM185BX-2.5	± 1.5%	30	−55°C to +125°C	20µA to 20mA	1
	LM185BY-2.5	± 1.5%	50	−55°C to +125°C	20µA to 20mA	1
	LM185B-2.5	± 1.5%	150	−55°C to +125°C	20µA to 20mA	1
	LM285BX-2.5	± 1.5%	30	−40°C to +85°C	20µA to 20mA	1
	LM285BY-2.5	± 1.5%	50	−40°C to +85°C	20µA to 20mA	1
	LM285-2.5	± 1.5%	150	−40°C to +85°C	20µA to 20mA	1
	LM385BX-2.5	± 1.5%	30	0°C to +70°C	20µA to 20mA	1
	LM385BY-2.5	± 1.5%	50	0°C to +70°C	20µA to 20mA	1
	LM385B-2.5	± 1.5%	150	0°C to +70°C	20µA to 20mA	1
	LM432	± 2%	13 Typ.	−40°C to +85°C	200µA to 1mA	0.2
	LM433	± 3%	13 Typ.	−40°C to +85°C	200µA to 1mA	0.2
	LM385M3-2.5*	± 3%	150	0°C to +70°C	15µA to 20mA	1
	LM385-2.5	± 3%	150	0°C to +70°C	20µA to 20mA	1
2.5 to 36 (Adj)	LM431CI	± 0.5%	55	−40°C to +85°C	1mA to 100mA	0.5
	LM431CC	± 0.5%	55	0°C to +70°C	1mA to 100mA	0.5
	LM431BI	± 1%	55	−40°C to +85°C	1mA to 100mA	0.5
	LM431BC	± 1%	55	0°C to +70°C	1mA to 100mA	0.5
	LM431AI	± 2%	55	−40°C to +85°C	1mA to 100mA	0.75
	LM431AC	± 2%	55	0°C to +70°C	1mA to 100mA	0.75
4.096*	LM4040A-4.1	± 0.1%	100	−40°C to +85°C	68µA to 15mA	1.0 Max
	LM4040B-4.1	± 0.2%	100	−40°C to +85°C	68µA to 15mA	1.0 Max
	LM4040C-4.1	± 0.5%	100	−40°C to +85°C	68µA to 15mA	1.0 Max
	LM4040D-4.1	± 1.0%	150	−40°C to +85°C	73µA to 15mA	1.3 Max
	LM4050A-4.1	± 0.1%	50	−40°C to +85°C	68µA to 15mA	0.5
	LM4050B-4.1	± 0.2%	50	−40°C to +85°C	68µA to 15mA	0.5
	LM4050C-4.1	± 0.5%	50	−40°C to +85°C	68µA to 15mA	0.5
5.0	LM136A	± 1%	72	−55°C to +125°C	400µA to 10mA	1.0 Max
	LM136	± 2%	72	−55°C to +125°C	400µA to 10mA	1.0 Max
	LM236A	± 1%	72	−25°C to +85°C	400µA to 10mA	1.0 Max
	LM236	± 2%	72	−25°C to +85°C	400µA to 10mA	1.0 Max
	LM336B	± 2%	54	0°C to +70°C	400µA to 10mA	1.4 Max
	LM336	± 4%	54	0°C to +70°C	400µA to 10mA	1.4 Max

Shunt References (Continued)

Reverse Breakdown Voltage (V_R)	Device	Voltage Tolerance Max, T_A= 25˚C	Temperature Drift		Operating Current Range, I_R	Output Dynamic Impedance Ω (Typ)
			ppm/˚C (Max)	Over Range		
5.0*	LM4040AI-5.0	± 0.1%	100	−40˚C to +85˚C	74µA to 15mA	1.1 Max
	LM4040BI-5.0	± 0.2%	100	−40˚C to +85˚C	74µA to 15mA	1.1 Max
	LM4040CE-5.0	± 0.5%	100	−40˚C to +125˚C	74µA to 15mA	1.1 Max
	LM4040CI-5.0	± 0.5%	100	−40˚C to +85˚C	74µA to 15mA	1.1 Max
	LM4040DE-5.0	± 1.0%	150	−40˚C to +125˚C	74µA to 15mA	1.1 Max
	LM4040DI-5.0	± 1.0%	150	−40˚C to +85˚C	74µA to 15mA	1.5 Max
	LM4050A-5.0	± 0.1%	50	−40˚C to +85˚C	74µA to 15mA	0.5
	LM4050B-5.0	± 0.2%	50	−40˚C to +85˚C	74µA to 15mA	0.5
	LM4050C-5.0	± 0.5%	50	−40˚C to +85˚C	74µA to 15mA	0.5
6.9	LM129A	+ 3%, −2%	10	−55˚C to +125˚C	600µA to 15mA	0.6
	LM129B	+ 3%, −2%	20	−55˚C to +125˚C	600µA to 15mA	0.6
	LM129C	+ 3%, −2%	50	−55˚C to +125˚C	600µA to 15mA	0.6
	LM329A	± 5%	50	0˚C to +70˚C	600µA to 15mA	0.8
	LM329B	± 5%	50	0˚C to +70˚C	600µA to 15mA	0.8
	LM329C	± 5%	20	0˚C to +70˚C	600µA to 15mA	0.8
	LM329D	± 5%	100	0˚C to +70˚C	600µA to 15mA	0.8
6.95	LM199A	± 2%	0.5	−55˚C to +125˚C	500µA to 10mA	0.5
	LM299	± 2%	1	−25˚C to +85˚C	500µA to 10mA	0.5
	LM399A	± 5%	1	0˚C to +70˚C	500µA to 10mA	0.5
	LM399	± 5%	2	0˚C to +70˚C	500µA to 10mA	0.5
8.192*	LM4040A-8.2	± 0.1%	100	−40˚C to +85˚C	91µA to 15mA	1.5 Max
	LM4040B-8.2	± 0.2%	100	−40˚C to +85˚C	91µA to 15mA	1.5 Max
	LM4040C-8.2	±0.5%	100	−40˚C to +85˚C	91µA to 15mA	1.5 Max
	LM4040D-8.2	± 1.0%	150	−40˚C to +85˚C	96µA to 15mA	1.9 Max
	LM4050A-8.2	± 0.1%	50	−40˚C to +85˚C	91µA to 15mA	0.6
	LM4050B-8.2	± 0.2%	50	−40˚C to +85˚C	91µA to 15mA	0.6
	LM4050C-8.2	±0.5%	50	−40˚C to +85˚C	91µA to 15mA	0.6
10.0*	LM4040A-10.0	± 0.1%	100	−40˚C to +85˚C	100µA to 15mA	1.7 Max
	LM4040B-10.0	± 0.2%	100	−40˚C to +85˚C	100µA to 15mA	1.7 Max
	LM4040C-10.0	± 0.5%	100	−40˚C to +85˚C	100µA to 15mA	1.7 Max
	LM4040D-10.0	± 1.0%	150	−40˚C to +85˚C	110µA to 15mA	2.3 Max
	LM4050A-10.0	± 0.1%	50	−40˚C to +85˚C	91µA to 15mA	0.7
	LM4050B-10.0	± 0.2%	50	−40˚C to +85˚C	91µA to 15mA	0.7
	LM4050C-10.0	± 0.5%	50	−40˚C to +85˚C	91µA to 15mA	0.7

*Available in SOT23-3 or SSOT23-3 Package.
†LM611 has on-board Op Amp.
††LM613 has on-board Dual Op Amp and Dual Comparator.
‡LM614 has on-board Quad Op Amp.

Current References

All have an output current range of 2µA to 10mA, and an operating voltage range of 1V to 40V.

Device	Operating Temperature Range	Set Current Error			Set Current Temperature Dependence*
		2µA to 10µA	10µA to 1mA	1mA to 5mA	
LM134	−55˚C to +125˚C	±8%	±3%	±5%	0.96T to 0.104T
LM234	−25˚C to +100˚C	±8%	±3%	±5%	0.96T to 0.104T
LM234-3	−25˚C to +100˚C	N/A	±1%	N/A	0.98T to 0.102T
LM234-6	−25˚C to +100˚C	N/A	±2%	N/A	0.97T to 0.103T

Current References (Continued)

All have an output current range of 2µA to 10mA, and an operating voltage range of 1V to 40V.

Device	Operating Temperature Range	Set Current Error			Set Current Temperature Dependence*
		2µA to 10µA	10µA to 1mA	1mA to 5mA	
LM334	0°C to +70°C	±12%	±6%	±8%	0.96T to 0.104T

* Set current changes linearly with temperature at a rate of 0.33%/°C.

"Reference Grade" Voltage Regulators

Please refer to the Low Dropout Regulators Selection Guide for many voltage regulators having a maximum voltage tolerance (at T_A= 25°C) of between ±0.5% and ±1.5%.

National Semiconductor

LM10
Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270µA. A complementary output stage swings within 15 mV of the supply terminals or will deliver ±20 mA output current with ±0.4V saturation. Reference output can be as low as 200 mV.

The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

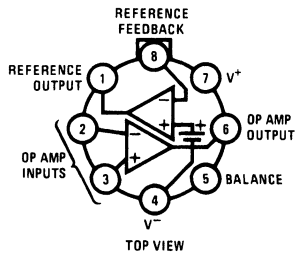
This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Features

- input offset voltage: 2.0 mV (max)
- input offset current: 0.7 nA (max)
- input bias current: 20 nA (max)
- reference regulation: 0.1% (max)
- offset voltage drift: 2µV/°C
- reference drift: 0.002%/°C

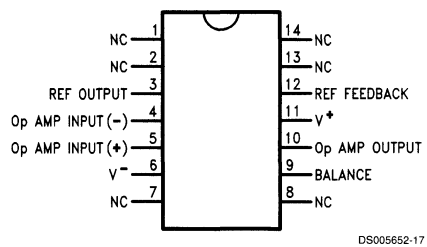
Connection and Functional Diagrams

Metal Can Package (H)



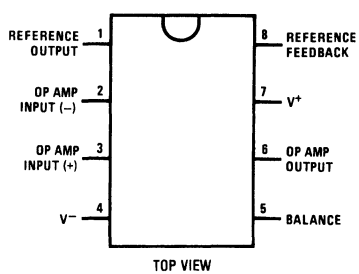
Order Number LM10BH, LM10CH, LM10CLH or LM10H/883
available per SMA# 5962-8760401
See NS Package Number H08A

Small Outline Package (WM)

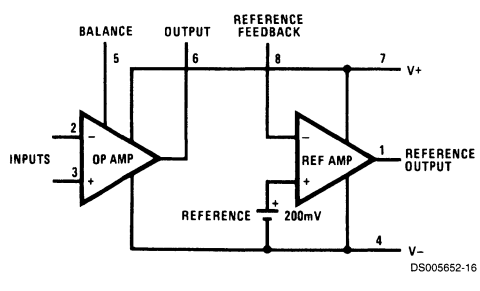


Order Number LM10CWM or LM10CWMX
See NS Package Number M14B

Dual-In-Line Package (N)



Order Number LM10CN or LM10CLN
See NS Package Number N08E



National Semiconductor

LM129/LM329
Precision Reference

General Description

The LM129 and LM329 family are precision multi-current temperature-compensated 6.9V zener references with dynamic impedances a factor of 10 to 100 less than discrete diodes. Constructed in a single silicon chip, the LM129 uses active circuitry to buffer the internal zener allowing the device to operate over a 0.5 mA to 15 mA range with virtually no change in performance. The LM129 and LM329 are available with selected temperature coefficients of 0.001, 0.002, 0.005 and 0.01%/°C. These references also have excellent long term stability and low noise.

A new subsurface breakdown zener used in the LM129 gives lower noise and better long-term stability than conventional IC zeners. Further the zener and temperature compensating transistor are made by a planar process so they are immune to problems that plague ordinary zeners. For example, there is virtually no voltage shift in zener voltage due to temperature cycling and the device is insensitive to stress on the leads.

The LM129 can be used in place of conventional zeners with improved performance. The low dynamic impedance simplifies biasing and the wide operating current allows the replacement of many zener types.

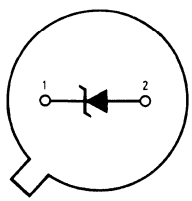
The LM129 is packaged in a 2-lead TO-46 package and is rated for operation over a −55°C to +125°C temperature range. The LM329 for operation over 0°C to 70°C is available in both a hermetic TO-46 package and a TO-92 epoxy package.

Features

- 0.6 mA to 15 mA operating current
- 0.6Ω dynamic impedance at any current
- Available with temperature coefficients of 0.001%/°C
- 7μV wideband noise
- 5% initial tolerance
- 0.002% long term stability
- Low cost
- Subsurface zener

Connection Diagrams

Metal Can Package (T0–46)

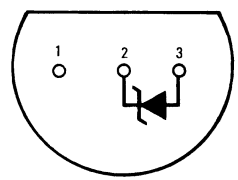


DS005714-6

Pin 2 is electrically connected to case

Bottom View
Order Number LM129AH, LM129AH/883, LM129BH, LM129BH/883, LM129CH, LM329AH, LM329BH, LM329CH or LM329DH
See NS Package H02A

Plastic Package (TO-92)

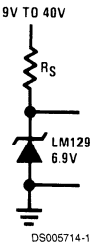


DS005714-4

Bottom View
Order Number LM329BZ, LM329CZ or LM329DZ
See NS Package Z03A

Typical Applications

Simple Reference



DS005714-1

National Semiconductor

LM199/LM299/LM399/LM3999 Precision Reference

General Description

The LM199 series are precision, temperature-stabilized monolithic zeners offering temperature coefficients a factor of ten better than high quality reference zeners. Constructed on a single monolithic chip is a temperature stabilizer circuit and an active reference zener. The active circuitry reduces the dynamic impedance of the zener to about 0.5Ω and allows the zener to operate over 0.5 mA to 10 mA current range with essentially no change in voltage or temperature coefficient. Further, a new subsurface zener structure gives low noise and excellent long term stability compared to ordinary monolithic zeners. The package is supplied with a thermal shield to minimize heater power and improve temperature regulation.

The LM199 series references are exceptionally easy to use and free of the problems that are often experienced with ordinary zeners. There is virtually no hysteresis in reference voltage with temperature cycling. Also, the LM199 is free of voltage shifts due to stress on the leads. Finally, since the unit is temperature stabilized, warm up time is fast.

The LM199 can be used in almost any application in place of ordinary zeners with improved performance. Some ideal applications are analog to digital converters, calibration standards, precision voltage or current sources or precision power supplies. Further in many cases the LM199 can replace references in existing equipment with a minimum of wiring changes.

The LM199 series devices are packaged in a standard hermetic TO-46 package inside a thermal shield. The LM199 is rated for operation from −55°C to +125°C while the LM299 is rated for operation from −25°C to +85°C and the LM399 is rated from 0°C to +70°C.

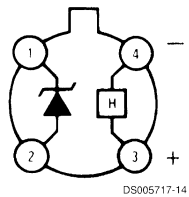
The LM3999 is packaged in a standard TO-92 package and is rated from 0°C to +70°C

Features

- Guaranteed 0.0001%/°C temperature coefficient
- Low dynamic impedance — 0.5Ω
- Initial tolerance on breakdown voltage — 2%
- Sharp breakdown at 400 µA
- Wide operating current — 500 µA to 10 mA
- Wide supply range for temperature stabilizer
- Guaranteed low noise
- Low power for stabilization — 300 mW at 25°C
- Long term stability — 20 ppm
- Proven reliability, low-stress packaging in TO-46 integrated-circuit hermetic package, for low hysteresis after thermal cycling. 33 million hours MTBF at T_A = +25°C (T_J = +86°C)
- Certified long term stability available
- MIL-STD-883 compliant

Connection Diagrams

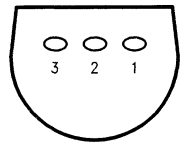
Metal Can Package (TO-46)



DS005717-14

Top View
LM199/LM299/LM399 (See Table on fourth page)
NS Package Number H04D

Plastic Package TO-92

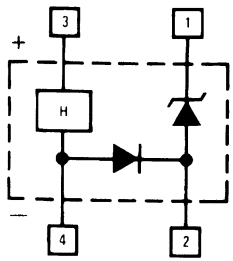


DS005717-10

Bottom View
LM3999 (See Table on fourth page)
NS Package Number Z03A

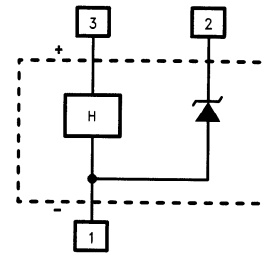
Functional Block Diagrams

LM199/LM299/LM399



DS005717-15

LM3999



DS005717-11

National Semiconductor

LM134/LM234/LM334
3-Terminal Adjustable Current Sources

General Description

The LM134/LM234/LM334 are 3-terminal adjustable current sources featuring 10,000:1 range in operating current, excellent current regulation and a wide dynamic voltage range of 1V to 40V. Current is established with one external resistor and no other parts are required. Initial current accuracy is ±3%. The LM134/LM234/LM334 are true floating current sources with no separate power supply connections. In addition, reverse applied voltages of up to 20V will draw only a few dozen microamperes of current, allowing the devices to act as both a rectifier and current source in AC applications.

The sense voltage used to establish operating current in the LM134 is 64mV at 25°C and is directly proportional to absolute temperature (°K). The simplest one external resistor connection, then, generates a current with ≈+0.33%/°C temperature dependence. Zero drift operation can be obtained by adding one extra resistor and a diode.

Applications for the current sources include bias networks, surge protection, low power reference, ramp generation, LED driver, and temperature sensing. The LM234-3 and LM234-6 are specified as true temperature sensors with guaranteed initial accuracy of ±3°C and ±6°C, respectively. These devices are ideal in remote sense applications because series resistance in long wire runs does not affect accuracy. In addition, only 2 wires are required.

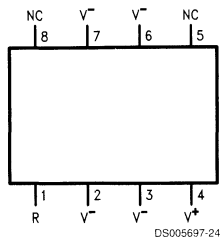
The LM134 is guaranteed over a temperature range of −55°C to +125°C, the LM234 from −25°C to +100°C and the LM334 from 0°C to +70°C. These devices are available in TO-46 hermetic, TO-92 and SO-8 plastic packages.

Features

- Operates from 1V to 40V
- 0.02%/V current regulation
- Programmable from 1μA to 10mA
- True 2-terminal operation
- Available as fully specified temperature sensor
- ±3% initial accuracy

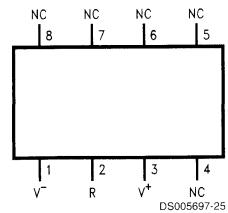
Connection Diagrams

SO-8
Surface Mount Package



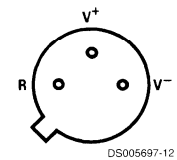
Order Number LM334M or LM334MX
See NS Package Number M08A

SO-8 Alternative Pinout
Surface Mount Package



Order Number LM334SM or LM334SMX
See NS Package Number M08A

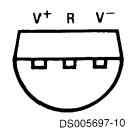
TO-46
Metal Can Package



V⁻ Pin is electrically connected to case.

Bottom View
Order Number LM134H, LM234H or LM334H
See NS Package Number H03H

TO-92 Plastic Package



Bottom View
Order Number LM334Z, LM234Z-3 or LM234Z-6
See NS Package Number Z03A

National Semiconductor

LM136-2.5/LM236-2.5/LM336-2.5V Reference Diode

General Description

The LM136-2.5/LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low-temperature-coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-2.5 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

The LM136-2.5 is rated for operation over −55°C to +125°C while the LM236-2.5 is rated over a −25°C to +85°C temperature range.

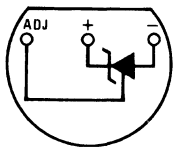
The LM336-2.5 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages.

Features

- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

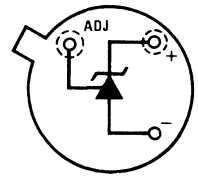
TO-92
Plastic Package



DS005715-8

Bottom View
Order Number LM236Z-2.5,
LM236AZ-2.5, LM336Z-2.5 or LM336BZ-2.5
See NS Package Number Z03A

TO-46
Metal Can Package

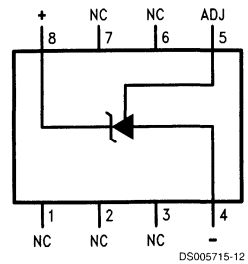


DS005715-20

Bottom View
Order Number LM136H-2.5,
LM136H-2.5/883, LM236H-2.5,
LM136AH-2.5, LM136AH-2.5/883
or LM236AH-2.5
See NS Package Number H03H

Connection Diagrams (Continued)

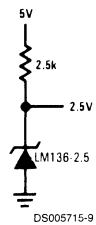
SO Package



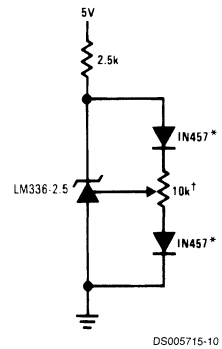
Top View
Order Number LM236M-2.5, LM236AM-2.5, LM336M-2.5 or LM336BM-2.5
See NS Package Number M08A

Typical Applications

2.5V Reference

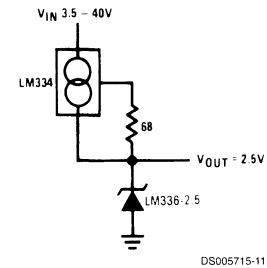


2.5V Reference with Minimum Temperature Coefficient



†Adjust to 2.490V
*Any silicon signal diode

Wide Input Range Reference



National Semiconductor

LM136-5.0/LM236-5.0/LM336-5.0
5.0V Reference Diode

General Description

The LM136-5.0/LM236-5.0/LM336-5.0 integrated circuits are precision 5.0V shunt regulator diodes. These monolithic IC voltage references operate as a low temperature coefficient 5.0V zener with 0.6Ω dynamic impedance. A third terminal on the LM136-5.0 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-5.0 series is useful as a precision 5.0V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 5.0V makes it convenient to obtain a stable reference from low voltage supplies. Further, since the LM136-5.0 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

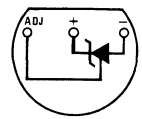
The LM136-5.0 is rated for operation over −55°C to +125°C while the LM236-5.0 is rated over a −25°C to +85°C temperature range. The LM336-5.0 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages. For applications requiring 2.5V see LM136-2.5.

Features

- Adjustable 4V to 6V
- Low temperature coefficient
- Wide operating current of 600 µA to 10 mA
- 0.6Ω dynamic impedance
- ± 1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

Connection Diagrams

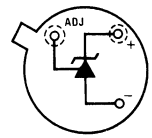
TO-92
Plastic Package



DS005716-4

Bottom View
Order Number LM236AZ-5.0, LM336Z-5.0 or LM336BZ-5.0
See NS Package Number Z03A

TO-46
Metal Can Package

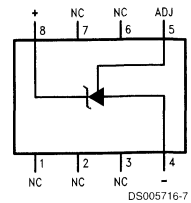


DS005716-5

Bottom View
Order Number LM136H-5.0,
LM136H-5.0/883, LM236H-5.0,
LM136AH-5.0, LM136AH-5.0/883,
or LM236AH-5.0
See NS Package Number H03H

Connection Diagrams (Continued)

SO Package

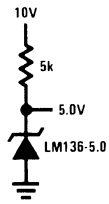


DS005716-7

Order Number LM336M-5.0 or LM336BM-5.0
See NS Package Number M08A

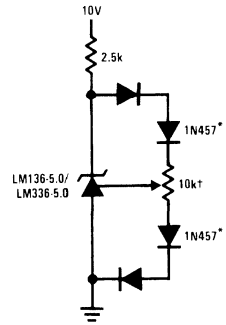
Typical Applications

5.0V Reference



DS005716-1

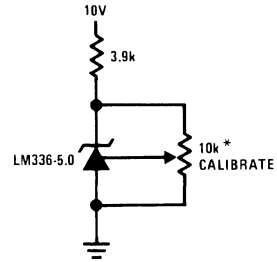
5.0V Reference with Minimum Temperature Coefficient



DS005716-15

† Adjust to 5.00V
* Any silicon signal diode

Trimmed 4V to 6V Reference with Temperature Coefficient Independent of Breakdown Voltage



DS005716-3

* Does not affect temperature coefficient

National Semiconductor

LM185/LM285/LM385
Adjustable Micropower Voltage References

General Description

The LM185/LM285/LM385 are micropower 3-terminal adjustable band-gap voltage reference diodes. Operating from 1.24 to 5.3V and over a 10μA to 20mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185 band-gap reference uses only transistors and resistors, low noise and good long-term stability result.

Careful design of the LM185 has made the device tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part.

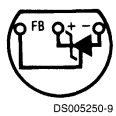
The LM185 is rated for operation over a −55°C to 125°C temperature range, while the LM285 is rated −40°C to 85°C and the LM385 0°C to 70°C. The LM185 is available in a hermetic TO-46 package and a leadless chip carrier package, while the LM285/LM385 are available in a low-cost TO-92 molded package, as well as S.O.

Features

- Adjustable from 1.24V to 5.30V
- Operating current of 10μA to 20mA
- 1% and 2% initial tolerance
- 1Ω dynamic impedance
- Low temperature coefficient

Connection Diagrams

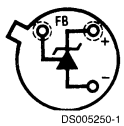
TO-92
Plastic Package



DS005250-9

Bottom View

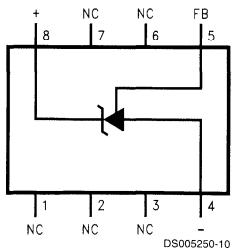
TO-46
Metal Can Package



DS005250-1

Bottom View

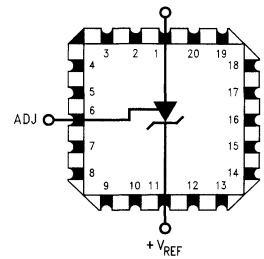
SOIC Package



DS005250-10

Top View

20-Leadless Chip Carrier



DS005250-15

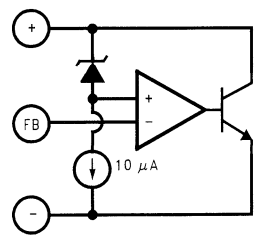
Top View

14

Ordering Information

Package	Temperature Range			NSC Drawing
	−55°C to 125°C	−40°C to 85°C	0°C to 70°C	
TO-46	LM185BH			H03H
	LM185BH/883			
	LM185BYH			
	LM185BYH/883			
TO-92		LM285BXZ	LM385BXZ	Z03A
		LM285BYZ	LM385BYZ	
		LM285Z	LM385BZ	
			LM385Z	
8-Pin SOIC		LM285M	LM385M	M08A
		LM285BYM	LM385BM	
20-Leadless Chip Carrier	LM185BE/883			E20A

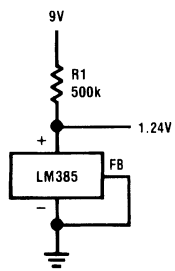
Block Diagram



DS005250-13

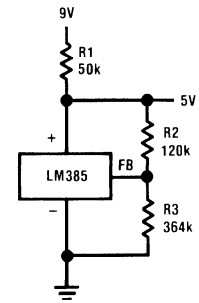
Typical Applications

1.2V Reference



DS005250-14

5.0V Reference



DS005250-2

$$V_{OUT} = 1.24\left(\frac{R3}{R2} + 1\right)$$

National Semiconductor

LM185-1.2/LM285-1.2/LM385-1.2
Micropower Voltage Reference Diode

General Description

The LM185-1.2/LM285-1.2/LM385-1.2 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 10 µA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM185-1.2 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-1.2 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-1.2 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life.

Further, the wide operating current allows it to replace older references with a tighter tolerance part.

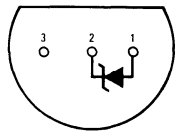
The LM185-1.2 is rated for operation over a −55˚C to 125˚C temperature range while the LM285-1.2 is rated −40˚C to 85˚C and the LM385-1.2 0˚C to 70˚C. The LM185-1.2/LM285-1.2 are available in a hermetic TO-46 package and the LM285-1.2/LM385-1.2 are also available in a low-cost TO-92 molded package, as well as SO and SOT-23. The LM185-1.2 is also available in a hermetic leadless chip carrier package.

Features

- ±4 mV (±0.3%) max. initial tolerance (A grade)
- Operating current of 10 µA to 20 mA
- 0.6Ω max dynamic impedance (A grade)
- Low temperature coefficient
- Low voltage reference—1.235V
- 2.5V device and adjustable device also available
- LM185-2.5 series and LM185 series, respectively

Connection Diagrams

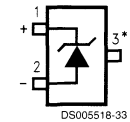
TO-92
Plastic Package (Z)



DS005518-10

Bottom View
Order Number LM285Z-1.2,
LM285BXZ-1.2, LM285BYZ-1.2
LM385Z-1.2, LM385BZ-1.2
LM385BXZ-1.2 or LM385BYZ-1.2
See NS Package Number Z03A

SOT23



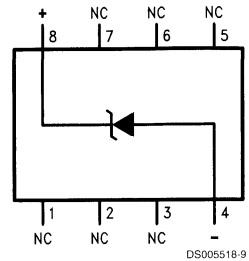
DS005518-33

* Pin 3 is attached to the Die Attach Pad (DAP) and should be connected to Pin 2 or left floating.

Order Number LM385M3-1.2
See NS Package Number MA03B

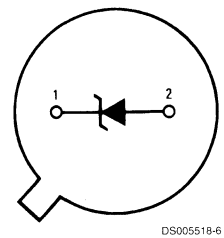
Connection Diagrams (Continued)

SO Package



Order Number LM285M-1.2,
LM285BXM-1.2, LM285BYM-1.2
LM385M-1.2, LM385BM-1.2
LM385BXM-1.2 or LM385BYM-1.2
See NS Package Number M08A

TO-46
Metal Can Package (H)



Bottom View
Order Number LM185H-1.2, LM185H-1.2/883,
LM185BXH-1.2, LM185BYH-1.2
LM285H-1.2 or LM285BXH-1.2
See NS Package Number H02A

National Semiconductor

LM185-2.5/LM285-2.5/LM385-2.5
Micropower Voltage Reference Diode

General Description

The LM185-2.5/LM285-2.5/LM385-2.5 are micropower 2-terminal band-gap voltage regulator diodes. Operating over a 20 µA to 20 mA current range, they feature exceptionally low dynamic impedance and good temperature stability. On-chip trimming is used to provide tight voltage tolerance. Since the LM-185-2.5 band-gap reference uses only transistors and resistors, low noise and good long term stability result.

Careful design of the LM185-2.5 has made the device exceptionally tolerant of capacitive loading, making it easy to use in almost any reference application. The wide dynamic operating range allows its use with widely varying supplies with excellent regulation.

The extremely low power drain of the LM185-2.5 makes it useful for micropower circuitry. This voltage reference can be used to make portable meters, regulators or general purpose analog circuitry with battery life approaching shelf life. Further, the wide operating current allows it to replace older references with a tighter tolerance part. For applications requiring 1.2V see LM185-1.2.

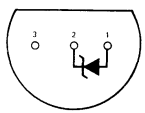
The LM185-2.5 is rated for operation over a −55˚C to 125˚C temperature range while the LM285-2.5 is rated −40˚C to 85˚C and the LM385-2.5 0˚C to 70˚C. The LM185-2.5/LM285-2.5 are available in a hermetic TO-46 package and the LM285-2.5/LM385-2.5 are also available in a low-cost TO-92 molded package, as well as S.O. and SOT-23. The LM185-2.5 is also available in a hermetic leadless chip carrier package.

Features

- ±20 mV (±0.8%) max. initial tolerance (A grade)
- Operating current of 20 µA to 20 mA
- 0.6Ω dynamic impedance (A grade)
- Low temperature coefficient
- Low voltage reference—2.5V
- 1.2V device and adjustable device also available—LM185-1.2 series and LM185 series, respectively

Connection Diagrams

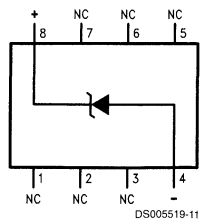
TO-92
Plastic Package



DS005519-8

Bottom View
Order Number LM285Z-2.5,
LM285BXZ-2.5, LM285BYZ-2.5
LM385Z-2.5, LM385AXZ-2.5
LM385AYZ-2.5, LM385BZ-2.5,
LM385BXZ-2.5 or LM385BYZ-2.5
See NS Package Number Z03A

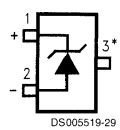
SO Package



DS005519-11

Order Number LM285M-2.5,
LM285BXM-2.5, LM285BYM-2.5
LM385M-2.5, LM385BM-2.5
LM385BXM-2.5 or LM385BYM-2.5
See NS Package Number M08A

SOT-23



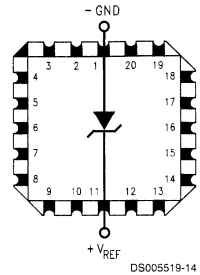
DS005519-29

* Pin 3 is attached to the Die Attach Pad (DAP) and should be connected to Pin 2 or left floating.

Order Number LM385M3-2.5
See NS Package Number MA03B

Connection Diagrams (Continued)

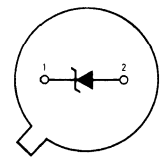
LCC
Leadless Chip Carrier



DS005519-14

Order Number LM185E-2.5/883
See NS Package Number E20A

TO-46
Metal Can Package



DS005519-13

Bottom View
Order Number LM185H-2.5,
LM185H-2.5/883, LM185BXH-2.5,
LM185BXH-2.5/883, LM185BYH-2.5,
LM185BYH2.5/883, LM285H-2.5,
or LM285BYH-2.5
See NS Package Number H02A

National Semiconductor

LM4040
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4040 precision voltage reference is available in the sub-miniature SC70 and SOT-23 surface-mount package. The LM4040's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4040 easy to use. Further reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 µA for the LM4040-2.5 to 100 µA for the LM4040-10.0. All versions have a maximum operating current of 15 mA.

The LM4040 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Also available is the LM4041 with two reverse breakdown voltage versions: adjustable and 1.2V. Please see the LM4041 data sheet.

Features

- Small packages: SOT-23, TO-92 and SC70
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V

Key Specifications (LM4040-2.5)

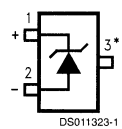
■ Output voltage tolerance (A grade, 25°C)	±0.1% (max)
■ Low output noise (10 Hz to 10 kHz)	35 μV_{rms}(typ)
■ Wide operating current range	60 µA to 15 mA
■ Industrial temperature range	−40°C to +85°C
■ Extended temperature range	−40°C to +125°C
■ Low temperature coefficient	100 ppm/°C (max)

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams

SOT-23

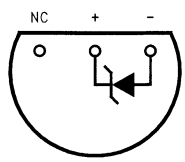


DS011323-1

*This pin must be left floating or connected to pin 2.

Top View
See NS Package Number MF03A
(JEDEC Registration TO-236AB)

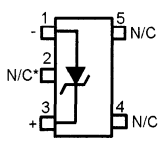
TO-92



DS011323-3

Bottom View
See NS Package Number Z03A

SC70



DS011323-30

*This pin must be left floating or connected to pin 1.

Top View
See NS Package Number MAA05A

Ordering Information
Industrial Temperature Range (−40°C to +85°C)

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package					NS Package Number
	M3 (SOT-23)		M7 (SC70)		Z (TO-92)	
	Supplied as 1000 Units Tape and Reel	Supplied as 3000 Units tape and Reel	Supplied as 1000 Units Tape and Reel	Supplied as 3000 Units Tape and Reel		
±0.1%, 100 ppm/°C max (A grade)	LM4040AIM3-2.5 LM4040AIM3-4.1 LM4040AIM3-5.0 LM4040AIM3-8.2 LM4040AIM3-10.0	LM4040AIM3X-2.5 LM4040AIM3X-4.1 LM4040AIM3X-5.0 LM4040AIM3X-8.2 LM4040AIM3X-10.0			LM4040AIZ-2.5 LM4040AIZ-4.1 LM4040AIZ-5.0 LM4040AIZ-8.2 LM4040AIZ-10.0	MF03A, Z03A
±0.2%, 100 ppm/°C max (B grade)	LM4040BIM3-2.5 LM4040BIM3-4.1 LM4040BIM3-5.0 LM4040BIM3-8.2 LM4040BIM3-10.0	LM4040BIM3X-2.5 LM4040BIM3X-4.1 LM4040BIM3X-5.0 LM4040BIM3X-8.2 LM4040BIM3X-10.0	LM4040BIM7-2.5 LM4040BIM7-4.1 LM4040BIM7-5.0	LM4040BIM7X-2.5 LM4040BIM7X-4.1 LM4040BIM7X-5.0	LM4040BIZ-2.5 LM4040BIZ-4.1 LM4040BIZ-5.0 LM4040BIZ-8.2 LM4040BIZ-10.0	MF03A, Z03A, MAA05A
±0.5%, 100 ppm/°C max (C grade)	LM4040CIM3-2.5 LM4040CIM3-4.1 LM4040CIM3-5.0 LM4040CIM3-8.2 LM4040CIM3-10.0	LM4040CIM3X-2.5 LM4040CIM3X-4.1 LM4040CIM3X-5.0 LM4040CIM3X-8.2 LM4040CIM3X-10.0	LM4040CIM7-2.5 LM4040CIM7-4.1 LM4040CIM7-5.0	LM4040CIM7X-2.5 LM4040CIM7X-4.1 LM4040CIM7X-5.0	LM4040CIZ-2.5 LM4040CIZ-4.1 LM4040CIZ-5.0 LM4040CIZ-8.2 LM4040CIZ-10.0	MF03A, Z03A, MAA05A
±1.0%, 150 ppm/°C max (D grade)	LM4040DIM3-2.5 LM4040DIM3-4.1 LM4040DIM3-5.0 LM4040DIM3-8.2 LM4040DIM3-10.0	LM4040DIM3X-2.5 LM4040DIM3X-4.1 LM4040DIM3X-5.0 LM4040DIM3X-8.2 LM4040DIM3X-10.0	LM4040DIM7-2.5 LM4040DIM7-4.1 LM4040DIM7-5.0	LM4040DIM7X-2.5 LM4040DIM7X-4.1 LM4040DIM7X-5.0	LM4040DIZ-2.5 LM4040DIZ-4.1 LM4040DIZ-5.0 LM4040DIZ-8.2 LM4040DIZ-10.0	MF03A, Z03A, MAA05A
±2.0%, 150 ppm/°C max (E grade)	LM4040EIM3-2.5	LM4040EIM3X-2.5	LM4040EIM7-2.5	LM4040EIM7X-2.5	LM4040EIZ-2.5	MF03A, Z03A, MAA05A

Extended Temperature Range (−40 °C to +125 °C)

Reverse Breakdown Voltage Tolerance at 25 °C and Average Reverse Breakdown Voltage Temperature Coefficient	Package
	M3 (SOT-23) See NS Package Number MF03A
±0.5%, 100 ppm/°C max (C grade)	LM4040CEM3-2.5, LM4040CEM3-5.0
±1.0%, 150 ppm/°C max (D grade)	LM4040DEM3-2.5, LM4040DEM3-5.0
±2.0%, 150 ppm/°C max (E grade)	LM4040EEM3-2.5

SOT-23 AND SC70 Package Marking Information

Only three fields of marking are possible on the SOT-23's and SC70's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
R2A SOT-23 only R4A SOT-23 only R5A SOT-23 only R8A SOT-23 only R0A SOT-23 only R2B	First Field: R = Reference Second Field: 2 = 2.500V Voltage Option 4 = 4.096V Voltage Option 5 = 5.000V Voltage Option

SOT-23 AND SC70 Package Marking Information (Continued)

Part Marking	Field Definition
R4B	8 = 8.192V Voltage Option
R5B	0 = 10.000V Voltage Option
R8B SOT-23 only	
R0B SOT-23 only	Third Field:
R2C	A–E = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance
R4C	A = ±0.1%, B = ±0.2%, C = +0.5%, D = ±1.0%, E = ±2.0%
R5C	
R8C SOT-23 only	
R0C SOT-23 only	
R2D	
R4D	
R5D	
R8D SOT-23 only	
R0D SOT-23 only	
R2E	

National Semiconductor

LM4041
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4041 precision voltage reference is available in the sub-miniature SC70 and SOT-23 surface-mount packages. The LM4041's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4041 easy to use. Further reducing design effort is the availability of a fixed (1.225V) and adjustable reverse breakdown voltage. The minimum operating current is 60 µA for the LM4041-1.2 and the LM4041-ADJ. Both versions have a maximum operating current of 12 mA.

The LM4041 utilizes fuse and zener-zap reverse breakdown or reference voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features

- Small packages: SOT-23, TO-92, and SC70
- No output capacitor required
- Tolerates capacitive loads
- Reverse breakdown voltage options of 1.225V and adjustable

Key Specifications (LM4041-1.2)

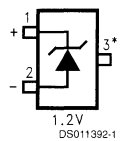
- Output voltage tolerance (A grade, 25°C) ±0.1%(max)
- Low output noise (10 Hz to 10kHz) $20\mu V_{rms}$
- Wide operating current range 60µA to 12mA
- Industrial temperature range −40°C to +85°C
- Extended temperature range −40°C to +125°C
- Low temperature coefficient 100 ppm/°C (max)

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Automotive
- Precision Audio Components

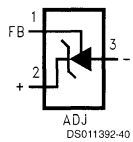
Connection Diagrams

SOT-23



DS011392-1

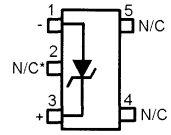
*This pin must be left floating or connected to pin 2.



DS011392-40

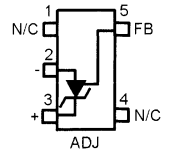
Top View
See NS Package Number MF03A
(JEDEC Registration TO-236AB)

SC-70



DS011392-46

*This pin must be left floating or connected to pin 1.

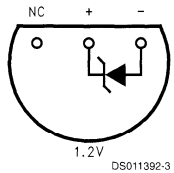


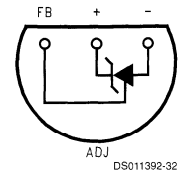
DS011392-47

Top View
See NS Package Number MAA05A

Connection Diagrams (Continued)

TO-92





Bottom View
See NS Package Number Z03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	Package					NS Package Number
	M3 (SOT-23)		M7 (SC70)		Z (TO-92)	
	Supplied as 1000 Units Tape and Reel	Supplied as 3000 Units Tape and Reel	Supplied as 1000 Units Tape and Reel	Supplied as 3000 Units Tape and Reel		
±0.1%, 100 ppm/°C max (A grade)	LM4041AIM3-1.2	LM4041AIM3X-1.2			LM4041AIZ-1.2	MF03A, Z03A
±0.2%, 100 ppm/°C max (B grade)	LM4041BIM3-1.2	LM4041BIM3X-1.2	LM4041BIM7-1.2	LM4041BIM7X-1.2	LM4041BIZ-1.2	MF03A, Z03A, MAA05A
±0.5%, 100 ppm/°C max (C grade)	LM4041CEM3-1.2 LM4041CIM3-1.2 LM4041CEM3-ADJ LM4041CIM3-ADJ	LM4041CEM3X-1.2 LM4041CIM3X-1.2 LM4041CEM3X-ADJ LM4041CIM3X-ADJ	LM4041CIM7-1.2 LM4041CIM7-ADJ	LM4041CIM7X-1.2 LM4041CIM7X-ADJ	LM4041CIZ-1.2 LM4041CIZ-ADJ	MF03A, Z03A, MAA05A
±1.0%, 150 ppm/°C max (D grade)	LM4041DEM3-1.2 LM4041DIM3-1.2 LM4041DEM3-ADJ LM4041DIM3-ADJ	LM4041DEM3X-1.2 LM4041DIM3X-1.2 LM4041DEM3X-ADJ LM4041DIM3X-ADJ	LM4041DIM7-1.2 LM4041DIM7-ADJ	LM4041DIM7X-1.2 LM4041DIM7X-ADJ	LM4041DIZ-1.2 LM4041DIZ-ADJ	MF03A, Z03A, MAA05A
±2.0%, 150 ppm/°C max (E grade)	LM4041EEM3-1.2 LM4041EIM3-1.2	LM4041EEM3X-1.2 LM4041EIM3X-1.2	LM4041EIM7-1.2	LM4041EIM7X-1.2	LM4041EIZ-1.2	MF03A, Z03A, MAA05A

SOT-23 and SC70 Package Marking Information

Only three fields of marking are possible on the SOT-23's and SC70's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
R1A (SOT-23 Only) R1B R1C R1D R1E	First Field: R = Reference Second Field: 1 = 1.225V Voltage Option A = Adjustable Third Field:
RAC RAD	A–E = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance A = ±0.1%, B = ±0.2%, C = ±0.5%, D = ±1.0%, E = ±2.0%

National Semiconductor

LM4050
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4050 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SSOT-23 surface-mount package. The LM4050's design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4050 easy to use. Further reducing design effort is the availability of several fixed reverse breakdown voltages: 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V. The minimum operating current increases from 60 µA for the LM4050-2.5 to 100 µA for the LM4050-10.0. All versions have a maximum operating current of 15 mA.

The LM4050 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

All grades and voltage options of the LM4050 operate between −40°C and +85°C. Selected parts can operate in the extended temperature range, from −40°C and +125°C.

Features

- Small packages: SSOT-23
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltages of 2.500V, 4.096V, 5.000V, 8.192V, and 10.000V

Key Specifications (LM4050-2.5)

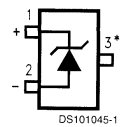
■ Output voltage tolerance (A grade, 25°C)	±0.1% (max)
■ Low output noise (10 Hz to 10 kHz)	41 μV_{rms}(typ)
■ Wide operating current range	60 µA to 15 mA
■ Industrial temperature range	−40°C to +85°C
■ Extended temperature range	−40°C to +125°C
■ Low temperature coefficient	50 ppm/°C (max)

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Automotive
- Precision Audio Components

Connection Diagrams

SSOT-23



*This pin must be left floating or connected to pin 2.

Top View
See NS Package Number MF03A

Ordering Information

Industrial Temperature Range (−40 °C to +85 °C)

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	LM4050 Supplied as 1000 Units, Tape and Reel	LM4050 Supplied as 3000 Units, Tape and Reel
±0.1%, 50 ppm/°C max (A grade)	LM4050AIM3-2.5	LM4050AIM3X-2.5
	LM4050AIM3-4.1	LM4050AIM3X-4.1
	LM4050AIM3-5.0	LM4050AIM3X-5.0
	LM4050AIM3-8.2	LM4050AIM3X-8.2
	LM4050AIM3-10	LM4050AIM3X-10
±0.2%, 50 ppm/°C max (B grade)	LM4050BIM3-2.5	LM4050BIM3X-2.5
	LM4050BIM3-4.1	LM4050BIM3X-4.1
	LM4050BIM3-5.0	LM4050BIM3X-5.0
	LM4050BIM3-8.2	LM4050BIM3X-8.2
	LM4050BIM3-10	LM4050BIM3X-10
±0.5%, 50 ppm/°C max (C grade)	LM4050CIM3-2.5	LM4050CIM3X-2.5
	LM4050CIM3-4.1	LM4050CIM3X-4.1
	LM4050CIM3-5.0	LM4050CIM3X-5.0
	LM4050CIM3-8.2	LM4050CIM3X-8.2
	LM4050CIM3-10	LM4050CIM3X-10

Extended Temperature Range (−40 °C to +125 °C)

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	LM4050 Supplied as 1000 Units, Tape and Reel	LM4050 Supplied as 3000 Units, Tape and Reel
±0.5%, 50 ppm/°C max (C grade)	LM4050CEM3-2.5	LM4050CEM3X-2.5

SSOT-23 Package Marking Information

Only three fields of marking are possible on the SSOT-23's small surface. This table gives the meaning of the three fields.

Part Marking	Field Definition
RCA RDA REA RFA RGA RCB RDB REB RFB RGB RCC RDC REC RFC RGC	First Field: R = Reference Second Field: C = 2.500V Voltage Option D = 4.096V Voltage Option E = 5.000V Voltage Option F = 8.192V Voltage Option G = 10.000V Voltage Option Third Field: A–C = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance A = ±0.1%, B = ±0.2%, C = +0.5%,

National Semiconductor

LM4051
Precision Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4051 precision voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SSOT-23 surface-mount package. The LM4051's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4051 easy to use. Further reducing design effort is the availability of a fixed (1.225V) and adjustable reverse breakdown voltage. The minimum operating current is 60 µA for the LM4051-1.2 and the LM4051-ADJ. Both versions have a maximum operating current of 12 mA.

The LM4051 comes in three grades (A, B, and C). The best grade devices (A) have an initial accuracy of 0.1%, while the B-grade have 0.2% and the C-grade 0.5%, all with a tempco of 50 ppm/°C guaranteed from −40°C to 125°C.

The LM4051 utilizes fuse and zener-zap trim of reference voltage during wafer sort to ensure that the prime parts have an accuracy of better than ±0.1% (A grade) at 25°C.

Features

- Small packages: SSOT-23
- No output capacitor required
- Tolerates capacitive loads
- Reverse breakdown voltage options of 1.225V and adjustable

Key Specifications (LM4051-1.2)

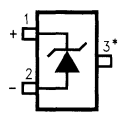
- Output voltage tolerance (A grade, 25°C) ±0.1%(max)
- Low output noise (10 Hz to 10kHz) $20\mu V_{rms}$
- Wide operating current range 60µA to 12mA
- Industrial temperature range (tempco guaranteed from −40°C to +125°C) −40°C to +85°C
- Low temperature coefficient 50 ppm/°C (max)

Applications

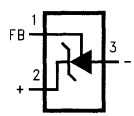
- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Automotive and Industrial
- Precision Audio Components
- Base Stations
- Battery Chargers
- Medical Equipment
- Communication

Connection Diagrams

SSOT-23



DS101222-1



DS101222-40

*This pin must be left floating or connected to pin 2.

Top View
See NS Package Number MF03A

Ordering Information

Reverse Breakdown Voltage Tolerance at 25°C and Average Reverse Breakdown Voltage Temperature Coefficient	LM4051 Supplied as 1000 Units, Tape and Reel	LM4051 Supplied as 3000 Units, Tape and Reel	Part Marking
±0.1%, 50 ppm/°C max (A grade)	LM4051AIM3-1.2	LM4051AIM3X-1.2	RHA
	LM4051AIM3-ADJ	LM4051AIM3X-ADJ	RIA
±0.2%, 50 ppm/°C max (B grade)	LM4051BIM3-1.2	LM4051BIM3X-1.2	RHB
	LM4051BIM3-ADJ	LM4051BIM3X-ADJ	RIB
±0.5%, 50 ppm/°C max (C grade)	LM4051CIM3-1.2	LM4051CIM3X-1.2	RHC
	LM4051CIM3-ADJ	LM4051CIM3X-ADJ	RIC

SOT-23 Package Marking Information

Only three fields of marking are possible on the SSOT-23's small surface. This table gives the meaning of the three fields.

Field Definition
First Field:
R = Reference
Second Field:
H = 1.225V Voltage Option
I = Adjustable
Third Field:
A–C = Initial Reverse Breakdown Voltage or Reference Voltage Tolerance
A = ±0.1%, B = ±0.2%, C = ±0.5%

National Semiconductor

LM4120
Precision Micropower Low Dropout Voltage Reference

General Description

The LM4120 is a precision low power low dropout bandgap voltage reference with up to 5 mA output current source and sink capability.

This series reference operates with input voltages as low as 2V and up to 12V consuming 160 µA (Typ.) supply current. In power down mode, device current drops to less than 2 µA.

The LM4120 comes in two grades (A and Standard) and seven voltage options for greater flexibility. The best grade devices (A) have an initial accuracy of 0.2%, while the standard have an initial accuracy of 0.5%, both with a tempco of 50ppm/°C guaranteed from −40°C to +125°C.

The very low dropout voltage, low supply current and power-down capability of the LM4120 makes this product an ideal choice for battery powered and portable applications.

The device performance is guaranteed over the industrial temperature range (−40°C to +85°C), while certain specs are guaranteed over the extended temperature range (−40°C to +125°C). Please contact National for full specifications over the extended temperature range. The LM4120 is available in a standard 5-pin SOT-23 package.

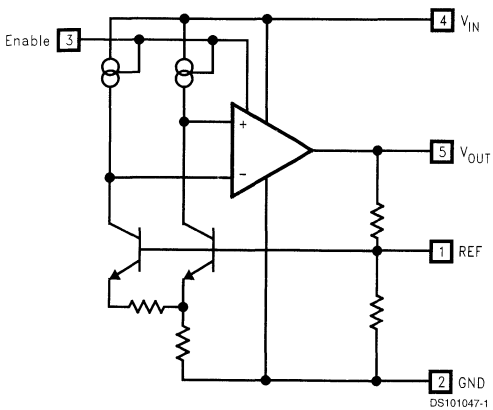
Features

- Small SOT23-5 package
- Low dropout voltage: 120 mV Typ @ 1 mA
- High output voltage accuracy: 0.2%
- Source and Sink current output: ±5 mA
- Supply current: 160 µA Typ.
- Low Temperature Coefficient: 50 ppm/°C
- Enable pin
- Fixed output voltages: 1.8, 2.048, 2.5, 3.0, 3.3, 4.096 and 5.0V
- Industrial temperature Range: −40°C to +85°C
- (For extended temperature range, −40°C to 125°C, contact National Semiconductor)

Applications

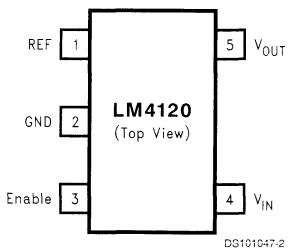
- Portable, battery powered equipment
- Instrumentation and process control
- Automotive & Industrial
- Test equipment
- Data acquisition systems
- Precision regulators
- Battery chargers
- Base stations
- Communications
- Medical equipment

Functional Block Diagram



DS101047-1

Connection Diagram



DS101047-2

Refer to the Ordering Information Table in this Data Sheet for Specific Part Number

SOT23-5 Surface Mount Package

Ordering Information

Industrial Temperature Range (−40°C to + 85°C)

Initial Output Voltage Accuracy at 25°C And Temperature Coefficient	LM4120 Supplied as 1000 Units, Tape and Reel	LM4120 Supplied as 3000 Units, Tape and Reel	Top Marking
0.2%, 50 ppm/°C max (A grade)	LM4120AIM5-1.8	LM4120AIM5X-1.8	R21A
	LM4120AIM5-2.0	LM4120AIM5X-2.0	R14A
	LM4120AIM5-2.5	LM4120AIM5X-2.5	R08A
	LM4120AIM5-3.0	LM4120AIM5X-3.0	R15A
	LM4120AIM5-3.3	LM4120AIM5X-3.3	R16A
	LM4120AIM5-4.1	LM4120AIM5X-4.1	R17A
	LM4120AIM5-5.0	LM4120AIM5X-5.0	R18A
0.5%, 50 ppm/°C max	LM4120IM5-1.8	LM4120IM5X-1.8	R21B
	LM4120IM5-2.0	LM4120IM5X-2.0	R14B
	LM4120IM5-2.5	LM4120IM5X-2.5	R08B
	LM4120IM5-3.0	LM4120IM5X-3.0	R15B
	LM4120IM5-3.3	LM4120IM5X-3.3	R16B
	LM4120IM5-4.1	LM4120IM5X-4.1	R17B
	LM4120IM5-5.0	LM4120IM5X-5.0	R18B

SOT-23 Package Marking Information

Only four fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the four fields.

Field Information
First Field:
R = Reference
Second and third Field:
21 = 1.800V Voltage Option
14 = 2.048V Voltage Option
08 = 2.500V Voltage Option
15 = 3.000V Voltage Option
16 = 3.300V Voltage Option
17 = 4.096V Voltage Option
18 = 5.000V Voltage Option
Fourth Field:
A-B = Initial Reference Voltage Tolerance
A = ±0.2%
B = ±0.5%

National Semiconductor

LM4121
Precision Micropower Low Dropout Voltage Reference

General Description

The LM4121 is a precision bandgap voltage reference available in a fixed 1.25V and adjustable version with up to 5 mA current source and sink capability.

This series reference operates with input voltages as low as 1.8V and up to 12V consuming 160 µA (Typ.) supply current. In power down mode, device current drops to less than 2 µA.

The LM4121 comes in two grades A and Standard. The best grade devices (A) have an initial accuracy of 0.2%, while the standard have an initial accuracy of 0.5%, both with a tempco of 50ppm/°C guaranteed from −40°C to +125°C.

The very low operating voltage, low supply current and power-down capability of the LM4121 makes this product an ideal choice for battery powered and portable applications.

The device performance is guaranteed over the industrial temperature range (−40°C to +85°C), while certain specs are guaranteed over the extended temperature range (−40°C to +125°C). Please contact National for full specifications over the extended temperature range. The LM4121 is available in a standard 5-pin SOT-23 package.

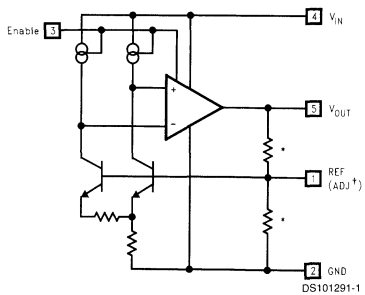
Features (LM4121-1.2)

- Small SOT23-5 package
- Low voltage operation
- High output voltage accuracy: 0.2%
- Source and Sink current output: ±5 mA
- Supply current: 160 µA Typ.
- Low Temperature Coefficient: 50 ppm/°C
- Enable pin
- Output voltages: 1.25V and Adjustable
- Industrial temperature Range: −40°C to +85°C
- (For extended temperature range, −40°C to 125°C, contact National Semiconductor)

Applications

- Portable, battery powered equipment
- Instrumentation and process control
- Automotive & Industrial
- Test equipment
- Data acquisition systems
- Precision regulators
- Battery chargers
- Base stations
- Communications
- Medical equipment

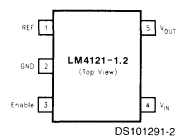
Block Diagram



* Resistors are removed on the LM4121-ADJ
†LM4121-ADJ only

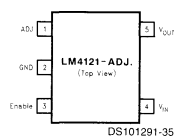
LM4121-1.2 Block Diagram

Connection Diagrams



Refer to the Ordering Information Table in this Data Sheet for Specific Part Number

SOT23-5 Surface Mount Package



Ordering Information

Industrial Temperature Range (−40˚C to + 85˚C)

Initial Output Voltage Accuracy at 25˚C And Temperature Coefficient	LM4121 Supplied as 1000 Units, Tape and Reel	LM4121 Supplied as 3000 Units, Tape and Reel	Top Marking
0.2%, 50 ppm/˚C max (A grade)	LM4121AIM5-1.2	LM4121AIM5X-1.2	R19A
	LM4121AIM5-ADJ	LM4121AIM5X-ADJ	R20A
0.5%, 50 ppm/˚C max	LM4121IM5-1.2	LM4121IM5X-1.2	R19B
	LM4121IM5-ADJ	LM4121IM5X-ADJ	R20B

SOT-23 Package Marking Information

Only four fields of marking are possible on the SOT-23's small surface. This table gives the meaning of the four fields.

Field Information
First Field:
R = Reference
Second and third Field:
19 = 1.250V Voltage Option
20 = Adjustable
Fourth Field:
A-B = Initial Reference Voltage Tolerance
A = ±0.2%
B = ±0.5%

National Semiconductor

LM4130
Precision Micropower Low Dropout Voltage Reference

General Description

The LM4130 family of precision voltage references performs comparable to the best laser-trimmed bipolar references, but in cost effective CMOS technology. Key to this break through is the use of EEPROM registers for correction of curvature, tempco, and accuracy on a CMOS bandgap architecture that allows package level programming to overcome assembly shift. The shifts in voltage accuracy and tempco during assembly of die into plastic packages limit the accuracy of references trimmed with laser techniques.

Unlike other LDO references, the LM4130 requires no output capacitor. Neither is a buffer amplifier required, even with loads up to 20mA. These advantages and the SOT23 packaging are important for cost-critical and space-critical applications.

Series references provide lower power consumption than shunt references, since they don't have to idle the maximum possible load current under no load conditions. This advantage, the low quiescent current (75μA), and the low dropout voltage(275mV) make the LM4130 ideal for battery-powered solutions.

The LM4130 is available in five grades (A, B, C, D and E) for greater flexibility. The best grade devices (A) have an initial accuracy of 0.05% with guaranteed temperature coefficient of 10ppm/°C or less, while the lowest grade parts (E) have an initial accuracy of 0.5% and a tempco of 30ppm/°C.

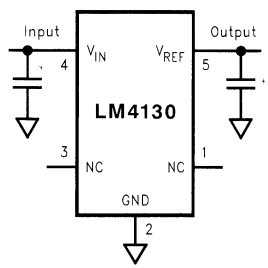
Features

- Small SOT23-5 package
- High output voltage accuracy 0.05%
- Low Temperature Coefficient 10 ppm/°C
- Stable with capacitive loads to 100μF
- Low dropout voltage ≤275 mV @ 10 mA
- Supply Current ≤75 μA
- Full accuracy −40°C to 85°C
- Extended operation to 125°C
- Excellent load and line regulation
- Output current 20 mA
- Output impedance < 1Ω
- Voltage options: 2.048V, 2.500V, and 4.096V

Applications Summary

- Portable, battery powered equipment
- Instrumentation and process control
- Automotive & Industrial
- Test equipment
- Data acquisition systems
- Precision regulators
- Battery chargers
- Base stations
- Communications
- Medical equipment
- Servo systems

Connection Diagram and Pin Configuration



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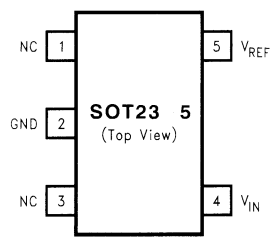
*Optional, Recommended for improved transient response and input noise reduction.
(See Application Information)



DS101046-2

Refer to the Ordering Information Table in this Data Sheet for Specific Part Number

SOT23-5 Surface Mount Package

Ordering Information

Industrial Temperature Range (−40°C to + 85°C)

Initial Output Voltage Accuracy at 25°C And Temperature Coefficient	LM4130 Supplied as 1000 Units, Tape and Reel	LM4130 Supplied as 3000 Units, Tape and Reel	Part Marking
0.05%, 10 ppm/°C max (A grade)	LM4130AIM5-2.0	LM4130AIM5X-2.0	R02A
	LM4130AIM5-2.5	LM4130AIM5X-2.5	R03A
	LM4130AIM5-4.1	LM4130AIM5X-4.1	R04A
0.2%, 10 ppm/°C max (B grade)	LM4130BIM5-2.0	LM4130BIM5X-2.0	R02B
	LM4130BIM5-2.5	LM4130BIM5X-2.5	R03B
	LM4130BIM5-4.1	LM4130BIM5X-4.1	R04B
0.1%, 20 ppm/°C max (C grade)	LM4130CIM5-2.0	LM4130CIM5X-2.0	R02C
	LM4130CIM5-2.5	LM4130CIM5X-2.5	R03C
	LM4130CIM5-4.1	LM4130CIM5X-4.1	R04C
0.4%, 20 ppm/°C max (D grade)	LM4130DIM5-2.0	LM4130DIM5X-2.0	R02D
	LM4130DIM5-2.5	LM4130DIM5X-2.5	R03D
	LM4130DIM5-4.1	LM4130DIM5X-4.1	R04D
0.5%, 30 ppm/°C max (E grade)	LM4130EIM5-2.0	LM4130EIM5X-2.0	R02E
	LM4130EIM5-2.5	LM4130EIM5X-2.5	R03E
	LM4130EIM5-4.1	LM4130EIM5X-4.1	R04E

SOT23-5 Package Marking Information

Only four fields of marking are possible on the SOT23-5's small surface. This table gives the meaning of the four fields.

Field Information
First Field:
R = Reference
Second and Third Field:
02 = 2.048V Voltage Option
03 = 2.50V Voltage Option
04 = 4.096V Voltage Option
Fourth Field:
A-E = Initial Reference Voltage Tolerance and Temperature Coefficient
A = ±0.05%, 10ppm/°C
B = ±0.2%, 10ppm/°C
C = ±0.1%, 20ppm/°C
D = ±0.4%, 20ppm/°C
E = ±0.5%, 30ppm/°C

National Semiconductor

LM4140
High Precision Low Noise Low Dropout Voltage Reference

General Description

The LM4140 series of precision references are designed to combine high accuracy, low drift and noise with low power dissipation in a small package.

The LM4140 is the industry's first reference with output voltage options lower than the bandgap voltage.

The key to the advance performance of the LM4140 is the use of EEPROM registers and CMOS DACs for temperature coefficient curvature correction and trimming of the output voltage accuracy of the device during the final production testing.

The major advantage of this method is the much higher resolution available with DACs than is available economically with most methods utilized by other bandgap references.

The low input and dropout voltage, low supply current and output drive capability of the LM4140 makes this product an ideal choice for battery powered and portable applications.

The LM4140 is available in three grades (A, B, C) with 0.1% initial accuracy and 3, 6 and 10 ppm/°C temperature coefficients. For even lower Tempco, contact National Semiconductor.

The device performance is specified over the temperature range (0°C to +70°C) and is available in compact 8-pin SO package.

For other output voltage options from 0.5V to 4.5V, contact National Semiconductor.

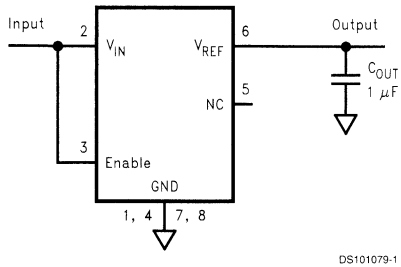
Features

- High initial accuracy: 0.1%
- Ultra low noise
- Low Temperature Coefficient: 3 ppm/°C (A grade)
- Low voltage operation: 1.8V
- SO-8 package
- Low dropout voltage: 20 mV (typ) @ 1mA
- Supply Current: 230 µA (typ), ≤ 1 µA disable mode
- Enable pin
- Output voltage options: 1.024V, 1.250V, 2.048V, 2.500V, and 4.096V
- Custom voltages from 0.5V to 4.5V
- Temperature range (0°C to 70°C)

Applications Summary

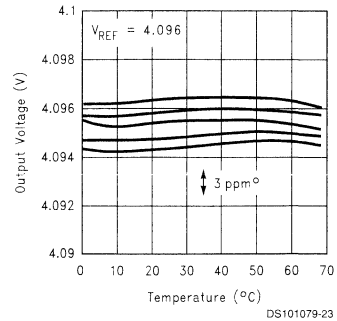
- Portable, battery powered equipment
- Instrumentation and test equipment
- Automotive
- Industrial process control
- Data acquisition systems
- Medical equipment
- Precision scales
- Servo systems
- Battery charging

Typical Application



C_{OUT}, Output bypass capacitor. See text for selection detail.

Typical Temperature Coefficient (Sample of 5 Parts)



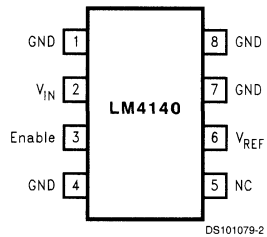
Refer to the Ordering Information Table in this Data Sheet for Specific Part Number

Ordering Information Temperature Range (0°C to 70°C)

Initial Output Voltage Accuracy @ 25°C and Temperature Coefficient	LM4140 Supplied as 95 Units, Tape and Reel	LM4140 Supplied as 2500 Units, Tape and Reel
0.1%, 3 ppm/°C max (A grade)	LM4140ACM-1.0	LM4140ACMX-1.0
	LM4140ACM-1.2	LM4140ACMX-1.2
	LM4140ACM-2.0	LM4140ACMX-2.0
	LM4140ACM-2.5	LM4140ACMX-2.5
	LM4140ACM-4.1	LM4140ACMX-4.1
0.1%, 6 ppm/°C max (B grade)	LM4140BCM-1.0	LM4140BCMX-1.0
	LM4140BCM-1.2	LM4140BCMX-1.2
	LM4140BCM-2.0	LM4140BCMX-2.0
	LM4140BCM-2.5	LM4140BCMX-2.5
	LM4140BCM-4.1	LM4140BCMX-4.1
0.1%, 10 ppm/°C max (C grade)	LM4140CCM-1.0	LM4140CCMX-1.0
	LM4140CCM-1.2	LM4140CCMX-1.2
	LM4140CCM-2.0	LM4140CCMX-2.0
	LM4140CCM-2.5	LM4140CCMX-2.5
	LM4140CCM-4.1	LM4140CCMX-4.1

Connection Diagram

8-Lead Surface Mount (M)



Top View
See NS Package Number M08A

Pin Functions

V_{ref} (Pin 6): Reference Output. Capable of sourcing up to 8mA.

Input (Pin 2): Positive Supply.

Ground (Pins 1, 4, 7, 8): Negative Supply or Ground Connection. These pins must be connected to ground.

Enable (Pin 3): Pulled to input for normal operation. Forcing this pin to ground will turn-off the output.

NC (Pin 5): This pin must be left open.

National Semiconductor

LM431
Adjustable Precision Zener Shunt Regulator

General Description

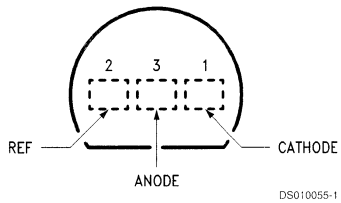
The LM431 is a 3-terminal adjustable shunt regulator with guaranteed temperature stability over the entire temperature range of operation. It is now available in a chip sized package (4-Bump micro SMD) using National's micro SMD package technology. The output voltage may be set at any level greater than 2.5V (V_{REF}) up to 36V merely by selecting two external resistors that act as a voltage divided network. Due to the sharp turn-on characteristics this device is an excellent replacement for many zener diode applications.

Features

- Average temperature coefficient 50 ppm/°C
- Temperature compensated for operation over the full temperature range
- Programmable output voltage
- Fast turn-on response
- Low output noise
- LM431 in micro SMD package
- See AN-1112 for micro SMD considerations

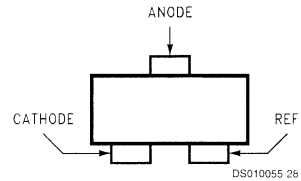
Connection Diagrams

TO-92: Plastic Package



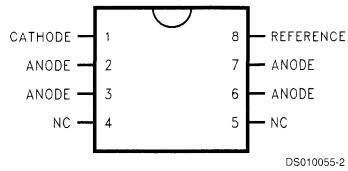
Top View

SOT-23: 3-Lead Small Outline



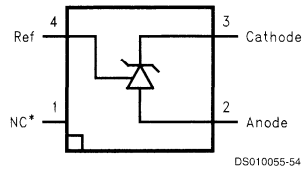
Top View

SO-8: 8-Pin Surface Mount



Top view

4-Bump micro SMD



Top View
(bump side down)

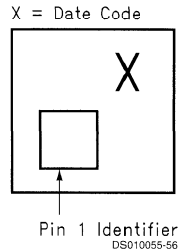
Note: *NC = Not internally connected. Must be electrically isolated from the rest of the circuit for the microSMD package.

Ordering Information

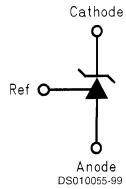
Package	Typical Accuracy Order Number/Package Marking			Temperature Range	Transport Media	NSC Drawing
	0.5%	1%	2%			
TO-92	LM431CCZ/ LM431CCZ	LM431BCZ/ LM431BCZ	LM431ACZ/ LM431ACZ	0°C to +70°C	Rails	Z03A
	LM431CIZ/ LM431CIZ	LM431BIZ/ LM431BIZ	LM431AIZ/ LM431AIZ	−40°C to +85°C		
SO-8	LM431CCM/ 431CCM	LM431BCM/ 431BCM	LM431ACM/ LM431ACM	0°C to +70°C	Rails and Tape &Reel	M08A
	LM431CIM/ 431CIM	LM431BIM/ 431BIM	LM431AIM/ LM431AIM	−40°C to +85°C		
SOT-23	LM431CCM3/ N1B	LM431BCM3/ N1D	LM431ACM3/ N1F	0°C to +70°C	Rails and Tape &Reel	MF03A
	LM431CIM3 N1A	LM431BIM3 N1C	LM431AIM3 N1E	−40°C to +85°C		
micro SMD	–	–	LM431AIBP LM431AIBPX(Note 1)	−40°C to +85°C	250 Units Tape and Reel 3k Units Tape and Reel	BPA04AFB

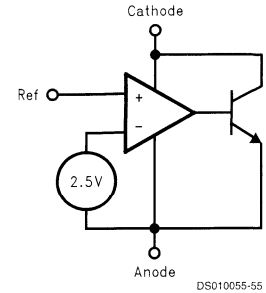
Note 1: The micro SMD package marking is a 1 digit manufacturing Date Code only

micro SMD Top View Marking Example



Symbol and Functional Diagrams





DC Test Circuits

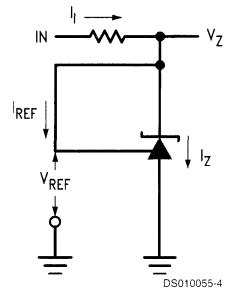
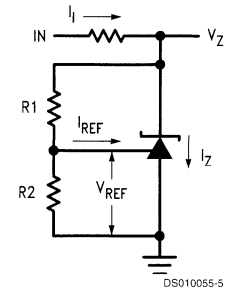


FIGURE 1. Test Circuit for $V_Z = V_{REF}$



Note: $V_Z = V_{REF} (1 + R1/R2) + I_{REF} \bullet R1$

FIGURE 2. Test Circuit for $V_Z > V_{REF}$

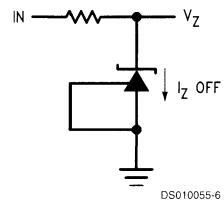


FIGURE 3. Test Circuit for Off-State Current

National Semiconductor

LM432
Dual Op Amp with On-Chip Fixed 2.5V Reference

General Description

The LM432 integrates two operational amplifiers and one 2.5V reference. The reference is based on the LMV431 adjustable shunt regulator with the output voltage adjusted to a fixed 2.5V. The Op Amps are similar to the LM358 with a common-mode input range that includes ground. Integrating the reference and Op Amps creates a solution for low cost charging applications.

Applications

- Low cost charging circuitry
- Power supplies and adapters

Features

Dual Op Amp Circuitry

(Typical for V_S= 5V)

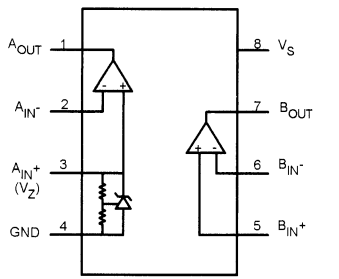
- Input offset voltage 0.6mV
- Input offset current 1nA
- Input bias current 3nA
- Common-mode input voltage range 0V to V_S–1V
- Power supply current 150µA

Reference Circuitry

- Reference voltage 2.5V
- Reference voltage deviation (–40˚C to 85˚C) 4mV
- Sink Current Capability 0.2mA to 10mA

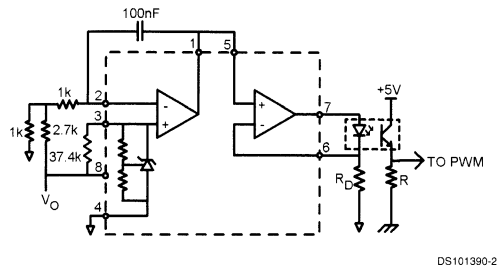
Connection Diagram

8-Pin SOIC



Top View

Application Circuit



Optocoupler Driver Circuit for Power Supply Isolation

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LM432MA	LM432MA	Rails	M08A
	LM432MAX	LM432MA	2.5k Unit Tape and Reel	

National Semiconductor

LM433
Dual Op Amp with On-Chip Fixed 2.5V Reference

General Description

The LM433 integrates two operational amplifiers and one 2.5V reference. The reference is based on the LMV431 adjustable shunt regulator with the output voltage adjusted to a fixed 2.5V. The Op Amps are similar to the LM358 with a common-mode input range that includes ground. Integrating the reference and Op Amps creates a solution for low cost charging applications.

Applications

- Low cost charging circuitry
- Power supplies and adapters

Features

Dual Op Amp Circuitry

(Typical for V_S = 5V)

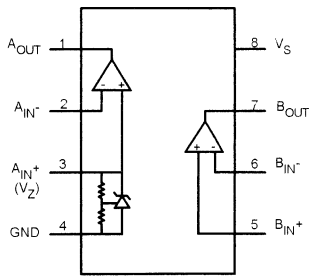
- Input offset voltage 0.6mV
- Input offset current 1nA
- Input bias current 3nA
- Common-mode input voltage range 0V to V_S−1V
- Power supply current 150µA

Reference Circuitry

- Reference voltage 2.5V
- Reference voltage deviation (−40˚C to 85˚C) 4mV
- Sink Current Capability 0.2mA to 10mA

Connection Diagram

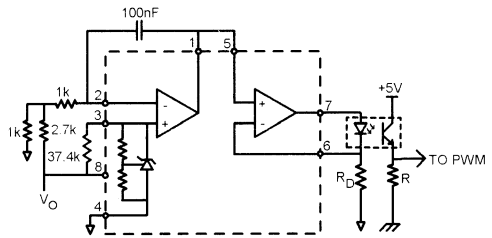
8-Pin SOIC



DS200039-1

Top View

Application Circuit



DS200039-2

Optocoupler Driver Circuit for Power Supply Isolation

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin SOIC	LM433MA	LM433MA	Rails	M08A
	LM433MAX	LM433MA	2.5k Unit Tape and Reel	

National Semiconductor

LM4431
Micropower Shunt Voltage Reference

General Description

Ideal for space critical applications, the LM4431 voltage reference is available in the sub-miniature (3 mm x 1.3 mm) SOT-23 surface-mount package. The LM4431's advanced design eliminates the need for an external stabilizing capacitor while ensuring stability with any capacitive load, thus making the LM4431 easy to use. The operating current range is 100 µA to 15 mA.

The LM4431 utilizes fuse and zener-zap reverse breakdown voltage trim during wafer sort to ensure that the parts have an accuracy of better than ±2.0% at 25°C. Bandgap reference temperature drift curvature correction and low dynamic impedance ensure stable reverse breakdown voltage accuracy over a wide range of operating temperatures and currents.

Features

- Small package: SOT-23
- No output capacitor required
- Tolerates capacitive loads
- Fixed reverse breakdown voltage of 2.50V

Key Specifications

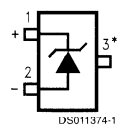
- Output voltage tolerance 25°C: ±2.0% (max)
- Low output noise (10 Hz to 10 kHz): 35 μV_{rms} (typ)
- Wide operating current range: 100 µA to 15 mA
- Commercial temperature range: 0°C to +70°C
- Low temperature coefficient: 30 ppm/°C (typ)

Applications

- Portable, Battery-Powered Equipment
- Data Acquisition Systems
- Instrumentation
- Process Control
- Energy Management
- Product Testing
- Power Supplies

Connection Diagram

SOT-23



DS011374-1

* This pin must be left floating or connected to pin 2.

Top View
Order Number LM4431M3-2.5
See NS Package Number MF03A
(JEDEC Registration TO-236AB)

SOT-23 Package Marking Information

Only three fields of marking are possible on the SOT-23's small surface. The following table gives the meaning of the three fields.

Part Marking	Field Definition
S2E	First Field: S = Reference Second Field: 2 = 2.500V Voltage Option Third Field: E = Initial Reverse Breakdown Voltage Tolerance of ±2.0%

National Semiconductor

LM611
Operational Amplifier and Adjustable Reference

General Description

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current: 300 µA (op amp)
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+–1.8V)
- Wide differential input voltage: ±36V
- Available in low cost 8-pin DIP
- Available in plastic package rated for Military Temperature Range Operation

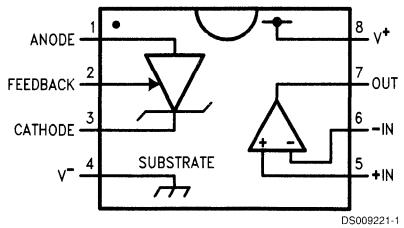
REFERENCE

- Adjustable output voltage: 1.2V to 6.3V
- Tight initial tolerance available: ±0.6%
- Wide operating current range: 17 µA to 20 mA
- Reference floats above ground
- Tolerant of load capacitance

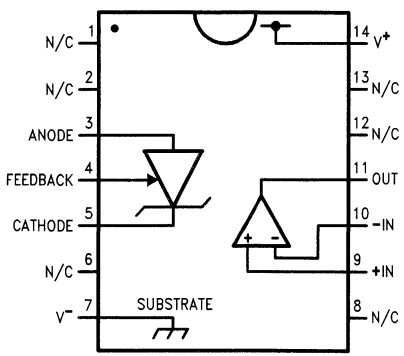
Applications

- Transducer bridge driver
- Process and Mass Flow Control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



DS009221-1



DS009221-2

National Semiconductor

LM613
Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

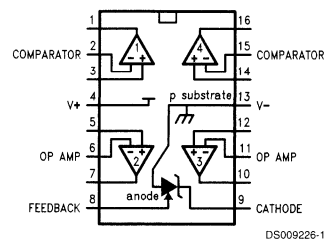
- Low operating current (Op Amp): 300 µA
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+ – 1.8V)
- Wide differential input voltage: ±36V
- Available in plastic package rated for Military Temp. Range Operation

REFERENCE

- Adjustable output voltage: 1.2V to 6.3V
- Tight initial tolerance available: ±0.6%
- Wide operating current range: 17 µA to 20 mA
- Tolerant of load capacitance

Applications

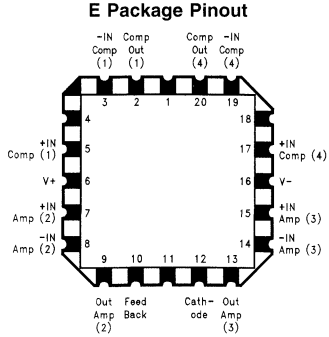
- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's



DS009226-1

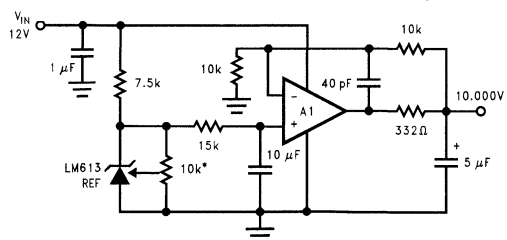
Top View

E Package Pinout



DS009226-48

Ultra Low Noise, 10.00V Reference.
Total output noise is typically 14 μV_{RMS}.



DS009226-43

*10k must be low t.c. trimpot

National Semiconductor

LM614
Quad Operational Amplifier and Adjustable Reference

General Description

The LM614 consists of four op-amps and a programmable voltage reference in a 16-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with four wide output swing op-amps makes the LM614 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), initial tolerance (2.0%), and the ability to be programmed from 1.2V to 5.0V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multichip solution, offering a high level of integration without sacrificing performance.

Features

Op Amp

- Low operating current: 450µA
- Wide supply voltage range: 4V to 36V
- Wide common-mode range: V^- to (V^+– 1.8V)
- Wide differential input voltage: ±36V

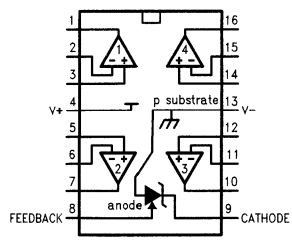
Reference

- Adjustable output voltage: 1.2V to 5.0V
- Initial tolerance: ±2.0%
- Wide operating current range: 17µA to 20mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver and signal processing
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagram



00932601

Ordering Information

Package	Temperature Range	Part Number	Package Marking	Transport Media	NSC Drawing
16-Pin Wide Body SOIC	0°C to 70°C	LM614CWM	LM614CWM	Rails	M16B
		LM614CWMX	LM614CWM	1k Units Tape and Reel	
	−40°C to 85°C	LM614IWM	LM614IWM	Rails	
		LM614IWMX	LM614IWM	1k Units Tape and Reel	

National Semiconductor

LMV431/LMV431A/LMV431B
Low-Voltage (1.24V) Adjustable Precision Shunt Regulators

General Description

The LMV431, LMV431A and LMV431B are precision 1.24V shunt regulators capable of adjustment to 30V. Negative feedback from the cathode to the adjust pin controls the cathode voltage, much like a non-inverting op amp configuration (Refer to Symbol and Functional diagrams). A two resistor voltage divider terminated at the adjust pin controls the gain of a 1.24V band-gap reference. Shorting the cathode to the adjust pin (voltage follower) provides a cathode voltage of a 1.24V.

The LMV431, LMV431A and LMV431B have respective initial tolerances of 1.5%, 1% and 0.5%. The LMV431 and LMV431A are available in commercial and Industrial temperature ranges. The LMV431B is only available in commercial temperature range.

The LMV431, LMV431A and LMV431B functionally lends themselves to several applications that require zener diode type performance at low voltages. Applications include a 3V to 2.7V low drop-out regulator, an error amplifier in a 3V off-line switching regulator and even as a voltage detector. These parts are typically stable with capacitive loads greater than 10nF and less than 50pF.

The LMV431, LMV431A and LMV431B provide performance at a competitive price.

Features

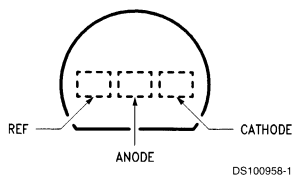
- Low Voltage Operation/Wide Adjust Range (1.24V/30V)
- 0.5% Initial Tolerance (LMV431B)
- Temperature Compensated for Industrial Temperature Range (39 PPM/°C for the LMV431AI)
- Low Operation Current (55µA)
- Low Output Impedance (0.25Ω)
- Fast Turn-On Response
- Low Cost

Applications

- Shunt Regulator
- Series Regulator
- Current Source or Sink
- Voltage Monitor
- Error Amplifier
- 3V Off-Line Switching Regulator
- Low Dropout N-Channel Series Regulator

Connection Diagrams

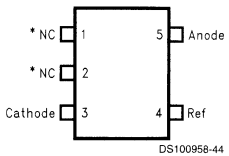
TO92: Plastic Package



DS100958-1

Top View

SOT23-5



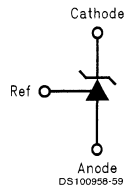
DS100958-44

*Pin 1 is not internally connected.

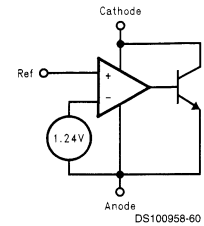
*Pin 2 is internally connected to Anode pin. Pin 2 should be either floating or connected to Anode pin.

Top View

Symbol and Functional Diagrams

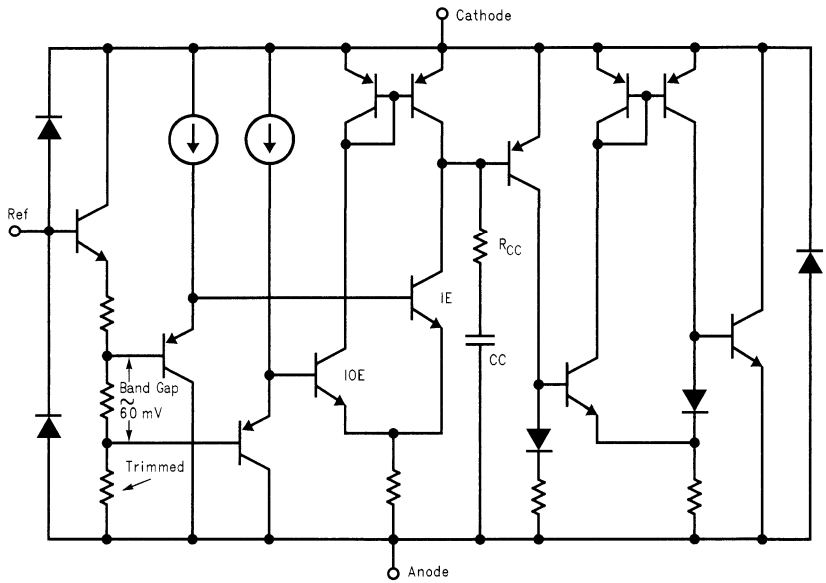


DS100958-59



DS100958-60

Simplified Schematic



DS100958-3

Ordering Information

Package	Temperature Range	Voltage Tolerance	Part Number	Package Marking	Drawing Number
TO92	Industrial Range −40°C to +85°C	1%	LMV431AIZ	LMV431AIZ	Z03A
		1.5%	LMV431IZ	LMV431IZ	
	Commerial Range 0°C to +70°C	0.5%	LMV431BCZ	LMV431BCZ	
		1%	LMV431ACZ	LMV431ACZ	
		1.5%	LMV431CZ	LMV431CZ	
SOT23-5	Industrial Range −40°C to +85°C	1%	LMV431AIM5	N08A	MF05A
		1%	LMV431AIM5X	N08A	
		1.5%	LMV431IM5	N08B	
		1.5%	LMV431IM5X	N08B	
	Commercial Range 0°C to +70°C	0.5%	LMV431BCM5	N09C	
		0.5%	LMV431BCM5X	N09C	
		1%	LMV431ACM5	N09A	
		1%	LMV431ACM5X	N09A	
		1.5%	LMV431CM5	N09B	
		1.5%	LMV431CM5X	N09B	

DC/AC Test Circuits for Table and Curves

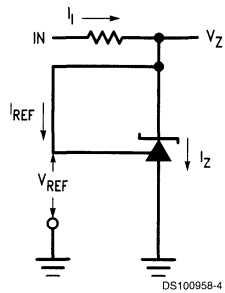
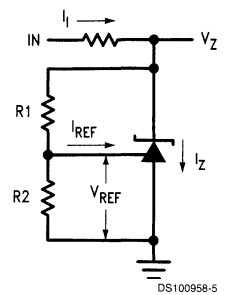


FIGURE 1. Test Circuit for $V_Z = V_{REF}$



Note: $V_Z = V_{REF} (1 + R1/R2) + I_{REF} * R1$

FIGURE 2. Test Circuit for $V_Z > V_{REF}$

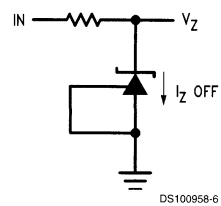


FIGURE 3. Test Circuit for Off-State Current

Section 15

Voltage Regulators - Linear

Section 15 Contents

National Semiconductor

Linear Voltage Regulators Selection Guide

Positive Regulators

Output Current (A)	Device	Output Voltage (V)	Quiescent Current or Min Load (mA) (Note 1)	Max Input Voltage (V)	Max Load Regulation %	Operating Temp Range (Note 3)	Package Availability (Note 4)	Additional Features
100mA	LM317L	Adj. (1.2 to 37)	5	40	1.5	Industrial	M, Z	
	LM78LXX	5, 6.2, 8.2, 9, 12, 15	5	35	1	Ext Commercial	M, Z	
180mA	LM9074	5	25	16.5	1	Industrial	M	Delayed Reset, Keep-Alive Logic
200mA	LM109	5	10	35	1	Military	H	
	LM309	5	10	35	1	Ext Commercial	H	
500mA	LM341	5, 12, 15	10	35	2	Industrial	T	
	LM78MXX	5, 12, 15	10	35	2	Industrial	H, T	
	LM117A	Adj. (1.2 to 37)	5	40	0.3	Military	H	
	LM317A	Adj. (1.2 to 37)	10	40	0.5	Industrial	H	
	LM317	Adj. (1.2 to 37)	10	40	0.5	Ext Commercial	H	
	LM117HV	Adj. (1.2 to 57)	12	60	0.5	Military	H	
	LM317HV	Adj. (1.2 to 57)	12	60	0.3	Ext Commercial	H	
1A	LM109K	5	10	35	1	Military	K	
	LM309K	5	10	35	1	Ext Commercial	K	
	LM317	Adj. (1.2 to 37)	10	40	0.5	Ext Commercial	MP	
	LM340	5, 12, 15	8	35	1	Commercial	K, S, T	
	LM340A	5, 12, 15	6	35	0.3	Commercial	T	
1.5A	LM117	Adj. (1.2 to 37)	10	35	0.3	Military	K, WG	
	LM317	Adj. (1.2 to 37)	10	35	0.5	Ext Commercial	K, MP, S, T	
	LM117HV	Adj. (1.2 to 57)	12	60	0.3	Military	K	
	LM317HV	Adj. (1.2 to 57)	12	60	0.5	Ext Commercial	K, T	
3A	LM123	5	20	20	1	Military	K	
	LM323A	5	20	20	2	Industrial	K	
	LM323	5	20	20	2	Ext Commercial	K	
	LM150	Adj. (1.2 to 33)	5	35	0.3	Military	K	
	LM350A	Adj. (1.2 to 33)	10	35	0.3	Industrial	K	
	LM350	Adj. (1.2 to 33)	10	35	0.5	Ext Commercial	K	
5A	LM138	Adj. (1.2 to 32)	5	40	0.3	Military	K	
	LM338	Adj. (1.2 to 32)	10	40	0.5	Ext Commercial	K, T	
Imax Set By	LM105	Adj. (4.5 to 40)	2	50	0.05	Military	H	45 mA Output w/o Pass
External	LM305A	Adj. (4.5 to 40)	2	50	0.2	Commercial	H	45 mA Output w/o Pass
Pass	LM305	Adj. (4.5 to 30)	2	40	0.2	Commercial	H	45 mA Output w/o Pass
Element	LM723	Adj. (2 to 37)	4	40	0.2	Military	H, J	Low Noise, High Quality Reference
	LM723C	Adj. (2 to 37)	4	40	0.3	Commercial	H, N	Low Noise, High Quality Reference

Negative Regulators

Output Current (A)	Device	Output Voltage (V)	Quiescent Current or Min Load (mA) (Note 1)	Max Input Voltage (V)	Max Load Regulation %	Operating Temp Range (Note 3)	Package Availability (Note 4)	Additional Features
100 mA	LM337L	Adj. (−1.2 to −37)	5	−40	1.5	Industrial	M, Z	
	LM320L	−5, −12, −15	6	−35	1	Commercial	M, Z	
	LM79Lxx	−5, −12, −15	6	−35	1	Ext Commercial	M, Z	
500 mA	LM137	Adj. (−1.2 to −37)	5	−40	1	Military	H	
	LM337	Adj. (−1.2 to −37)	10	−40	1.5	Ext Commecial	H	
	LM137HV	Adj. (−1.2 to −47)	5	−50	1	Military	H	
	LM337HV	Adj. (−1.2 to −47)	10	−50	1.5	Ext Commercial	H	
	LM79Mxx	−5, −12, −15	3	−35 (Note 2)	2	Ext Commercial	T	
1A	LM337	Adj. (−1.2 to −37)	10	−40	1.5	Ext Commercial	MP	
1.5A	LM120	−5, −12, −15	2	−35 (Note 2)	1	Military	K	
	LM320	−5, −12, −15	3	−35 (Note 2)	1	Ext Commercial	T	
	LM79xx	−5, −12, −15	3	−35 (Note 2)	1	Ext Commercial	T	
	LM137	Adj. (−1.2 to −37)	5	−40	1	Military	K	
	LM337	Adj. (−1.2 to −37)	10	−40	1.5	Ext Commercial	K, T	
	LM137HV	Adj. (−1.2 to −47)	5	−50	1	Military	K	
	LM337HV	Adj. (−1.2 to −47)	10	−50	1.5	Ext Commercial	K	
3A	LM133	Adj. (−1.2 to −32)	5	−35	0.5	Military	K	
	LM333	Adj. (−1.2 to −32)	5	−35	1	Industrial	K	

Note 1: Max quiescent current for fixed or minimum load for adjustables.

Note 2: Maximum input voltage is −25V for −5V version.

Note 3: Operating temp range:

Commercial = 0°C to +70°C

Ext Commercial = 0°C to +125°C

Industrial = −40°C to +125°C

Military = −55°C to +150°C

Note 4: Under Package Availability, the letter identifies the type of package.

H = Metal Can (TO-99)

J = Ceramic Dual-In-Line Package

K = Metal Can (TO-3)

N = Molded Dual-In-Line Package

M = SOIC

MP = SOT223 (3 Lead Surface Mount)

S = TO-263 (Power Surface Mount)

T = TO-220

WG = Ceramic SOIC

Z = TO-92

National Semiconductor

Voltage Regulators Definition Of Terms

Current-Limit Sense Voltage: The voltage across the current-limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

Dropout Voltage: The input-output voltage differential at which the circuit ceases to regulate against further reduction in input voltage.

Feedback Sense Voltage: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

Input Voltage Range: The range of dc input voltages over which the regulator will operate within specifications.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long term Stability: Output voltage stability under accelerated life-test conditions at 125°C with maximum rated voltages and power dissipation for 1000 hours.

Maximum Power Dissipation: The maximum total device dissipation for which the regulator will operate within specifications.

Output Input Voltage Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

Output Noise Voltage: The RMS ac voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Output Voltage Range: The range of regulated output voltages over which the specifications apply.

Output Voltage Scale Factor: The output voltage obtained for a unit value of resistance between the adjustment terminal and ground.

Quiescent Current: That part of the input current to the regulator that is not delivered to the load.

Ripple Rejection: The line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

Standby Current Drain: The part of the operating current of the regulator which does not contribute to the load current. (See Quiescent Current)

Temperature Stability: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Thermal Regulation: Percentage change in output voltage for a given change in power dissipation over a specified time period.

National Semiconductor

LM105/LM305/LM305A Voltage Regulators

General Description

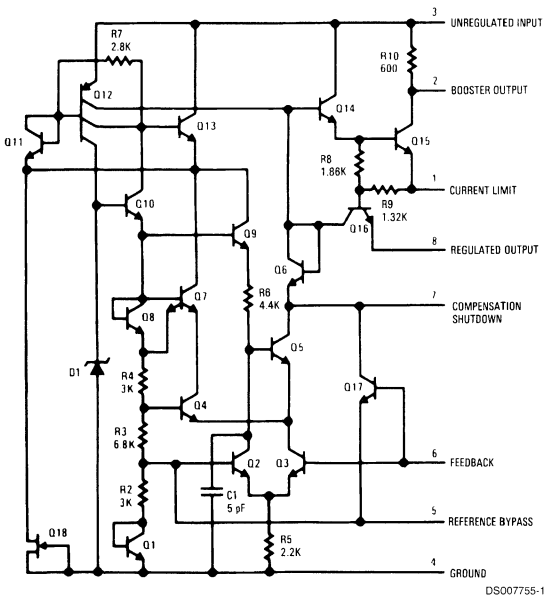
The LM105 series are positive voltage regulators similar to the LM100, except that an extra gain stage has been added for improved regulation. A redesign of the biasing circuitry removes any minimum load current requirement and at the same time reduces standby current drain, permitting higher voltage operation. They are direct, plug-in replacements for the LM100 in both linear and switching regulator circuits with output voltages greater than 4.5V. Important characteristics of the circuits are:

- Output voltage adjustable from 4.5V to 40V
- Output currents in excess of 10A possible by adding external transistors
- Load regulation better than 0.1%, full load with current limiting
- DC line regulation guaranteed at 0.03%/V
- Ripple rejection on 0.01%V
- 45 mA output current without external pass transistor (LM305A)

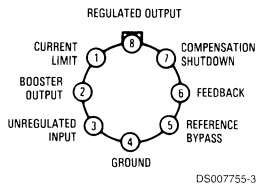
Like the LM100, they also feature fast response to both load and line transients, freedom from oscillations with varying resistive and reactive loads and the ability to start reliably on any load within rating. The circuits are built on a single silicon chip and are supplied in a TO-99 metal can.

The LM105 is specified for operation for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, and the LM305/LM305A is specified for $0^{\circ}C \leq T_A \leq +70^{\circ}C$.

Schematic and Connection Diagrams



Metal Can Package



Top View
Order Number LM105H, LM105H/883, SMD #5962-8958801, LM305H or LM305AH
See NS Package Number H08C

National Semiconductor

LM109/LM309
5-Volt Regulator

General Description

The LM109 series are complete 5V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems association with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

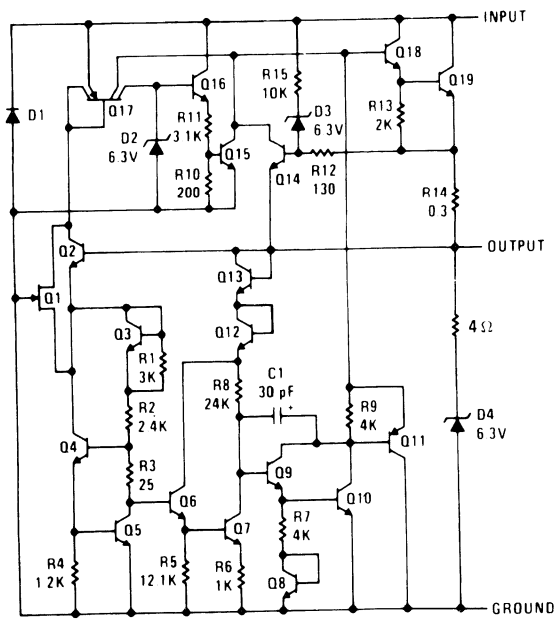
Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5V, as shown. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

Features

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

Schematic Diagram



DS007138-1

National Semiconductor

LM117/LM317A/LM317
3-Terminal Adjustable Regulator

General Description

The LM117 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 1.5A over a 1.2V to 37V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment pin and output, the LM117 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

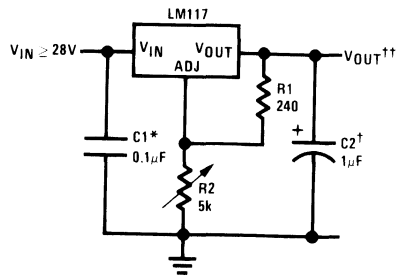
For applications requiring greater output current, see LM150 series (3A) and LM138 series (5A) data sheets. For the negative complement, see LM137 series data sheet.

Features

- Guaranteed 1% output voltage tolerance (LM317A)
- Guaranteed max. 0.01%/V line regulation (LM317A)
- Guaranteed max. 0.3% load regulation (LM117)
- Guaranteed 1.5A output current
- Adjustable output down to 1.2V
- Current limit constant with temperature
- P+ Product Enhancement tested
- 80 dB ripple rejection
- Output is short-circuit protected

Typical Applications

1.2V–25V Adjustable Regulator



00906301

Full output current not available at high input-output voltages

*Needed if device is more than 6 inches from filter capacitors.

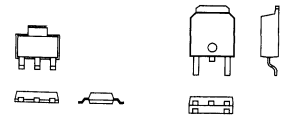
†Optional — improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}(R_2)$$

LM117 Series Packages

Part Number Suffix	Package	Design Load Current
K	TO-3	1.5A
H	**TO-39**	**0.5A**
T	TO-220	1.5A
E	**LCC**	**0.5A**
S	TO-263	1.5A
EMP	SOT-223	1A
MDT	**TO-252**	**0.5A**

SOT-223 vs D-Pak (TO-252) Packages



00906354

Scale 1:1

National Semiconductor

LM117HV/LM317HV
3-Terminal Adjustable Regulator

General Description

The LM117HV/LM317HV are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 1.5A over a 1.2V to 57V output range. They are exceptionally easy to use and require only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM117HV is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM117HV series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM117HV is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e. do not short the output to ground.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM117HV can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

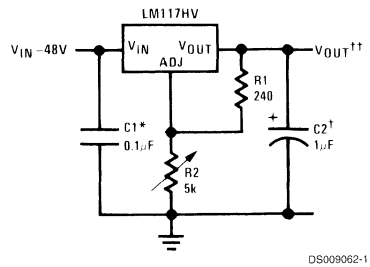
The LM117HVK STEEL and LM317HVK STEEL are packaged in standard TO-3 transistor packages, while the LM117HVH and LM317HVH are packaged in a solid Kovar base TO-39 transistor package. The LM317HVT uses a TO-220 plastic package. The LM117HV is rated for operation from −55°C to +150°C, and the LM317HV from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 1.5A output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- 100% electrical burn-in
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short-circuit protected
- P+ Product Enhancement tested

Typical Applications

1.2V-45V Adjustable Regulator



DS009062-1

Full output current not available at high input-output voltages

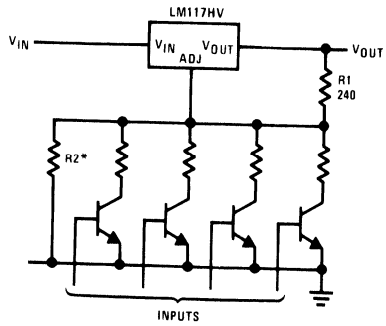
†Optional — improves transient response. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*Needed if device is more than 6 inches from filter capacitors.

$$\dagger\dagger V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right) + I_{ADJ}R_2$$

Typical Applications (Continued)

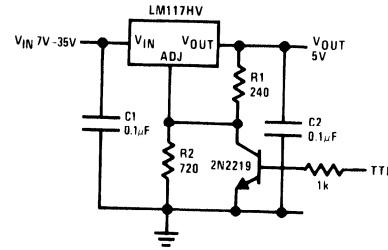
Digitally Selected Outputs



DS009062-2

*Sets maximum V_{OUT}

5V Logic Regulator with Electronic Shutdown*



DS009062-3

*Min. output ≈ 1.2V

National Semiconductor

LM123/LM323A/LM323
3-Amp, 5-Volt Positive Regulator

General Description

The LM123 is a three-terminal positive regulator with a preset 5V output and a load driving capability of 3 amps. New circuit design and processing techniques are used to provide the high output current without sacrificing the regulation characteristics of lower current devices.

The LM323A offers improved precision over the standard LM323. Parameters with tightened specifications include output voltage tolerance, line regulation, and load regulation.

The 3 amp regulator is virtually blowout proof. Current limiting, power limiting, and thermal shutdown provide the same high level of reliability obtained with these techniques in the LM109 1 amp regulator.

No external components are required for operation of the LM123. If the device is more than 4 inches from the filter capacitor, however, a 1 µF solid tantalum capacitor should be used on the input. A 0.1 µF or larger capacitor may be used on the output to reduce load transient spikes created by fast switching digital logic, or to swamp out stray load capacitance.

An overall worst case specification for the combined effects of input voltage, load currents, ambient temperature, and power dissipation ensure that the LM123 will perform satisfactorily as a system element.

For applications requiring other voltages, see LM150 series adjustable regulator data sheet.

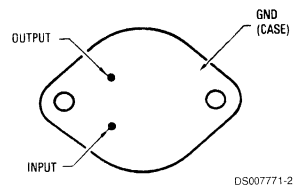
Operation is guaranteed over the junction temperature range −55°C to +150°C for LM123, −40°C to +125°C for LM323A, and 0°C to +125°C for LM323. A hermetic TO-3 package is used for high reliability and low thermal resistance.

Features

- Guaranteed 1% initial accuracy (A version)
- 3 amp output current
- Internal current and thermal limiting
- 0.01Ω typical output impedance
- 7.5V minimum input voltage
- 30W power dissipation
- P+ Product Enhancement tested

Connection Diagram

Metal Can Package

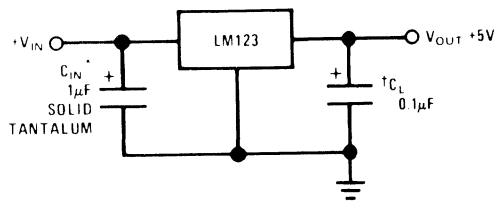


DS007771-2

Order Number LM123K STEEL, LM323AK STEEL or LM323K STEEL
See NS Package Number K02A
Order Number LM123K/883
See NS Package Number K02C

Typical Applications

Basic 3 Amp Regulator



DS007771-3

*Required if LM123 is more than 4" from filter capacitor.
†Regulator is stable with no load capacitor into resistive loads.

National Semiconductor

LM333
3-Ampere Adjustable Negative Regulator

General Description

The LM333 is an adjustable 3-terminal negative voltage regulator capable of supplying in excess of −3.0A over an output voltage range of −1.2V to −32V. This regulator is exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM333 features internal current limiting, thermal shutdown and safe-area compensation, making them substantially immune to failure from overloads.

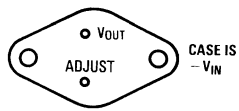
The LM333 serves a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM333 is an ideal complement to the LM150/LM350 adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −32V
- 3.0A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.2%
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- Standard 3-lead transistor package
- Output is short circuit protected

Connection Diagram

TO-3
Metal Can Package

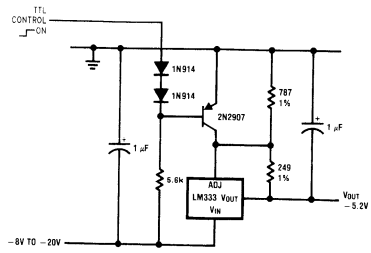


DS009065-1

Bottom View
Steel TO-3 Metal Can Package (K STEEL)
Order Number LM333K STEEL
See NS Package Number K02A

Typical Application

−5.2V Regulator with Electronic Shutdown



DS009065-6

National Semiconductor

LM137/LM337
3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM137/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM337 are ideal complements to the LM117/LM317 adjustable positive regulators.

Features

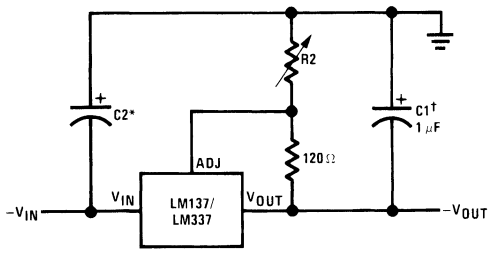
- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- P+ Product Enhancement tested
- Standard 3-lead transistor package
- Output is short circuit protected

LM137 Series Packages and Power Capability

Device	Package	Rated Power Dissipation	Design Load Current
LM137/337	TO-3 (K)	20W	1.5A
	TO-39 (H)	2W	0.5A
LM337	TO-220 (T)	15W	1.5A
LM337	SOT-223 (MP)	2W	1A

Typical Applications

Adjustable Negative Voltage Regulator



00906701

Full output current not available at high input-output voltages

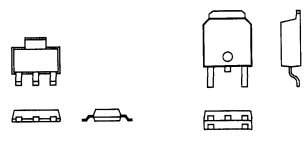
$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120}\right) + \left(-I_{ADJ} \times R2\right)$$

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients

Comparison between SOT-223 and D-Pak (TO-252) Packages



00906731

Scale 1:1

National Semiconductor

LM137HV/LM337HV
3-Terminal Adjustable Negative Regulators (High Voltage)

General Description

The LM137HV/LM337HV are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −47V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137HV series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

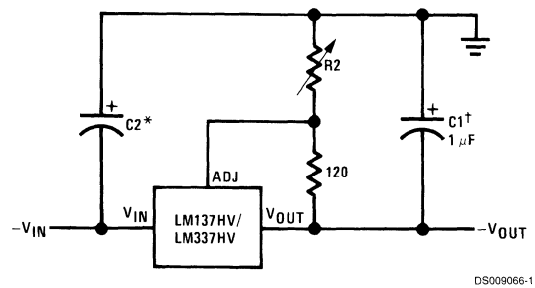
The LM137HV/LM337HV serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137HV/LM337HV are ideal complements to the LM117HV/LM317HV adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −47V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- P+ Product Enhancement tested
- Standard 3-lead transistor package
- Output short circuit protected

Typical Applications

Adjustable Negative Voltage Regulator



DS009066-1

$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right) + \left[-I_{Adj}(R_2)\right]$$

DS009066-25

†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability. Output capacitors in the range of 1 μF to 1000 μF of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor.

National Semiconductor

LM138/LM338
5-Amp Adjustable Regulators

General Description

The LM138 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 5A over a 1.2V to 32V output range. They are exceptionally easy to use and require only 2 resistors to set the output voltage. Careful circuit design has resulted in outstanding load and line regulation—comparable to many commercial power supplies. The LM138 family is supplied in a standard 3-lead transistor package.

A unique feature of the LM138 family is time-dependent current limiting. The current limit circuitry allows peak currents of up to 12A to be drawn from the regulator for short periods of time. This allows the LM138 to be used with heavy transient loads and speeds start-up under full-load conditions. Under sustained loading conditions, the current limit decreases to a safe value protecting the regulator. Also included on the chip are thermal overload protection and safe area protection for the power transistor. Overload protection remains functional even if the adjustment pin is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An output capacitor can be added to improve transient response, while bypassing the adjustment pin will increase the regulator's ripple rejection.

Besides replacing fixed regulators or discrete designs, the LM138 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., do not short-circuit output to ground. The part numbers in the LM138 series which have a K suffix are packaged in a standard Steel TO-3 package, while those with a T suffix are packaged in a TO-220 plastic package. The LM138 is rated for $-55^{\circ}C \leq T_J \leq +150^{\circ}C$, and the LM338 is rated for $0^{\circ}C \leq T_J \leq +125^{\circ}C$.

Features

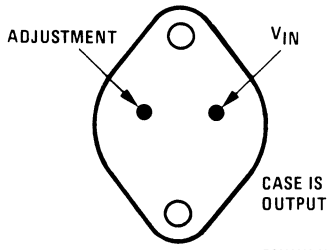
- Guaranteed 7A peak output current
- Guaranteed 5A output current
- Adjustable output down to 1.2V
- Guaranteed thermal regulation
- Current limit constant with temperature
- P^+ Product Enhancement tested
- Output is short-circuit protected

Applications

- Adjustable power supplies
- Constant current regulators
- Battery chargers

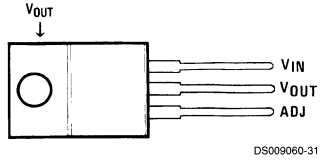
Connection Diagrams (See Physical Dimension section for further information)

(TO-3 STEEL)
Metal Can Package



Bottom View
Order Number LM138K STEEL or LM338K STEEL
See NS Package Number K02A

(TO-220)
Plastic Package



Front View
Order Number LM338T
See NS Package Number T03B

National Semiconductor

LM340/LM78XX Series
3-Terminal Positive Regulators

General Description

The LM140/LM340A/LM340/LM7800C monolithic 3-terminal positive voltage regulators employ internal current-limiting, thermal shutdown and safe-area compensation, making them essentially indestructible. If adequate heat sinking is provided, they can deliver over 1.0A output current. They are intended as fixed voltage regulators in a wide range of applications including local (on-card) regulation for elimination of noise and distribution problems associated with single-point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents.

Considerable effort was expended to make the entire series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

The 5V, 12V, and 15V regulator options are available in the steel TO-3 power package. The LM340A/LM340/LM7800C series is available in the TO-220 plastic power package, and the LM340-5.0 is available in the SOT-223 package, as well as the LM340-5.0 and LM340-12 in the surface-mount TO-263 package.

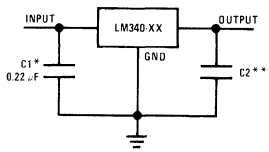
Features

- Complete specifications at 1A load
- Output voltage tolerances of ±2% at T_j = 25°C and ±4% over the temperature range (LM340A)
- Line regulation of 0.01% of V_{OUT}/V of ΔV_{IN} at 1A load (LM340A)
- Load regulation of 0.3% of V_{OUT}/A (LM340A)
- Internal thermal overload protection
- Internal short-circuit current limit
- Output transistor safe area protection
- P^+ Product Enhancement tested

Device	Output Voltages	Packages
LM140	5, 12, 15	TO-3 (K)
LM340A/LM340	5, 12, 15	TO-3 (K), TO-220 (T), SOT-223 (MP), TO-263 (S) (5V and 12V only)
LM7800C	5, 8, 12, 15	TO-220 (T)

Typical Applications

Fixed Output Regulator

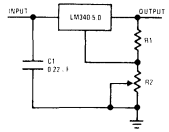


00778101

*Required if the regulator is located far from the power supply filter.

**Although no output capacitor is needed for stability, it does help transient response. (If needed, use 0.1 µF, ceramic disc).

Adjustable Output Regulator

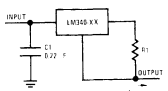


00778102

V_{OUT} = 5V + (5V/R1 + I_Q) R2 5V/R1 > 3 I_Q,

load regulation (L_f) ≈ [(R1 + R2)/R1] (L_f of LM340-5).

Current Regulator

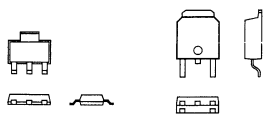


00778103

$$I_{OUT} = \frac{V2\text{-}3}{R1} + I_Q$$

ΔI_Q = 1.3 mA over line and load changes.

Comparison between SOT-223 and D-Pak (TO-252) Packages



00778138

Scale 1:1

National Semiconductor

LM150/LM350A/LM350
3-Amp Adjustable Regulators

General Description

The LM150 series of adjustable 3-terminal positive voltage regulators is capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An output capacitor can be added to improve transient response, while bypassing the adjustment pin will increase the regulator's ripple rejection.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded, i.e., avoid short-circuiting the output.

By connecting a fixed resistor between the adjustment pin and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

The part numbers in the LM150 series which have a K suffix are packaged in a standard Steel TO-3 package, while those with a T suffix are packaged in a TO-220 plastic package. The LM150 is rated for $-55^{\circ}C \leq T_J \leq +150^{\circ}C$, while the LM350A is rated for $-40^{\circ}C \leq T_J \leq +125^{\circ}C$, and the LM350 is rated for $0^{\circ}C \leq T_J \leq +125^{\circ}C$.

Features

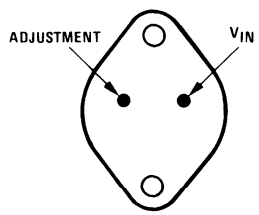
- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Guaranteed thermal regulation
- Output is short circuit protected
- Current limit constant with temperature
- P^+ Product Enhancement tested
- 86 dB ripple rejection
- Guaranteed 1% output voltage tolerance (LM350A)
- Guaranteed max. 0.01%/V line regulation (LM350A)
- Guaranteed max. 0.3% load regulation (LM350A)

Applications

- Adjustable power supplies
- Constant current regulators
- Battery chargers

Connection Diagrams

(TO-3 STEEL)
Metal Can Package

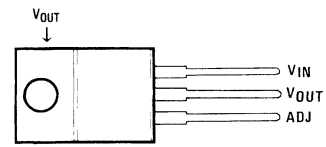


DS009061-4

Case is Output

Bottom View
Order Number LM150K STEEL
or LM350K STEEL
See NS Package Number K02A
Order Number LM150K/883
See NS Package Number K02C

(TO-220)
Plastic Package



DS009061-5

Front View
Order Number LM350AT or LM350T
See NS Package Number T03B

National Semiconductor

LM317L
3-Terminal Adjustable Regulator

General Description

The LM317L is an adjustable 3-terminal positive voltage regulator capable of supplying 100mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, both line and load regulation are better than standard fixed regulators. Also, the LM317L is available packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM317L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, no capacitors are needed unless the device is situated more than 6 inches from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM317L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

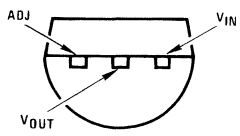
The LM317L is available in a standard TO-92 transistor package, the SO-8 package, and 6-Bump micro SMD package. The LM317L is rated for operation over a −25°C to 125°C range.

Features

- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Available in TO-92, SO-8, or 6-Bump micro SMD package
- Output is short circuit protected
- See AN-1112 for micro SMD considerations

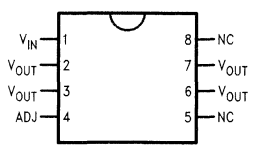
Connection Diagrams

TO-92 Plastic package



DS009064-4

8-Pin SOIC

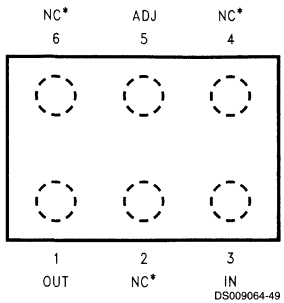


DS009064-5

Top View

Connection Diagrams (Continued)

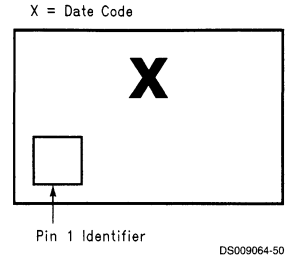
6-Bump micro SMD



*NC = Not Internally connected.

Top View
(Bump Side Down)

micro SMD Laser Mark



Package	Part Number	Package Marking	Media Transport	NSC Drawing
TO-92	LM317LZ	LM317LZ	1.8k Units per Box	Z03A
8-Pin SOIC	LM317LM	LM317LM	Rails	M08A
6-Bump micro SMD	* LM317LIBP	–	250 Units Tape and Reel	BPA06HPB
	* LM317LIBPX	–	3k Units Tape and Reel	

Note: The micro SMD package marking is a single digit manufacturing Date Code only.

National Semiconductor

LM320L/LM79LXXAC Series 3-Terminal Negative Regulators

General Description

The LM320L/LM79LXXAC dual marked series of 3-terminal negative voltage regulators features fixed output voltages of −5V, −12V, and −15V with output current capabilities in excess of 100mA. These devices were designed using the latest computer techniques for optimizing the packaged IC thermal/electrical performance. The LM79LXXAC series, even when combined with a minimum output compensation capacitor of 0.1µF, exhibits an excellent transient response, a maximum line regulation of 0.07% V_O/V, and a maximum load regulation of 0.01% V_O/mA.

The LM320L/LM79LXXAC series also includes, as self-protection circuitry: safe operating area circuitry for output transistor power dissipation limiting, a temperature independent short circuit current limit for peak output current limiting, and a thermal shutdown circuit to prevent excessive junction temperature. Although designed primarily as fixed voltage regulators, these devices may be combined with simple external circuitry for boosted and/or adjustable voltages and currents. The LM79LXXAC series is available in the 3-lead TO-92 package, and SO-8; 8 lead package. The LM320L series is available in the 3-lead TO-92 package.

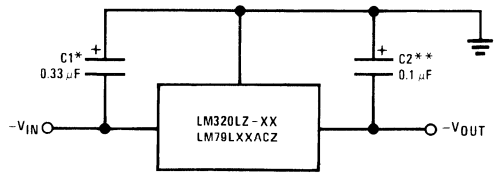
For output voltage other than −5V, −12V and −15V, the LM137L series provides an output voltage range from 1.2V to 47V.

Features

- Preset output voltage error is less than ±5% overload, line and temperature
- Specified at an output current of 100mA
- Easily compensated with a small 0.1µF output capacitor
- Internal short-circuit, thermal and safe operating area protection
- Easily adjustable to higher output voltages
- Maximum line regulation less than 0.07% V_{OUT}/V
- Maximum load regulation less than 0.01% V_{OUT}/mA

Typical Applications

Fixed Output Regulator

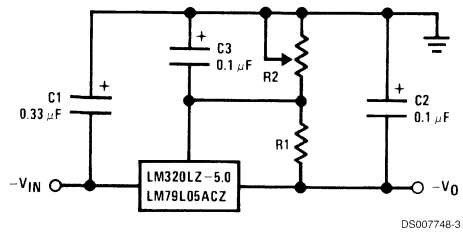


DS007748-1

*Required if the regulator is located far from the power supply filter. A 1µF aluminum electrolytic may be substituted.

**Required for stability. A 1µF aluminum electrolytic may be substituted.

Adjustable Output Regulator

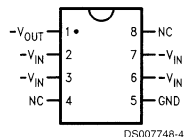


DS007748-3

$-V_O = -5V - (5V/R1 + I_Q) \bullet R2$,
$5V/R1 > 3\ I_Q$

Connection Diagrams

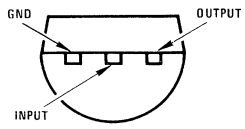
SO-8 Plastic (Narrow Body)



DS007748-4

Top View
Order Number LM79L05ACM, LM79L12ACM LM79L15ACM, LM79L05ACMX, LM79L12ACMX or LM79L15ACMX
See NS Package Number M08A

TO-92 Plastic Package (Z)



DS007748-2

Bottom View
Order Number LM320LZ-5.0, LM79L05ACZ, LM320LZ-12, LM79L12ACZ, LM320LZ-15 or LM79L15ACZ
See NS Package Number Z03A

National Semiconductor

LM330
3-Terminal Positive Regulator

General Description

The LM330 5V 3-terminal positive voltage regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Familiar regulator features such as current limit and thermal overload protection are also provided.

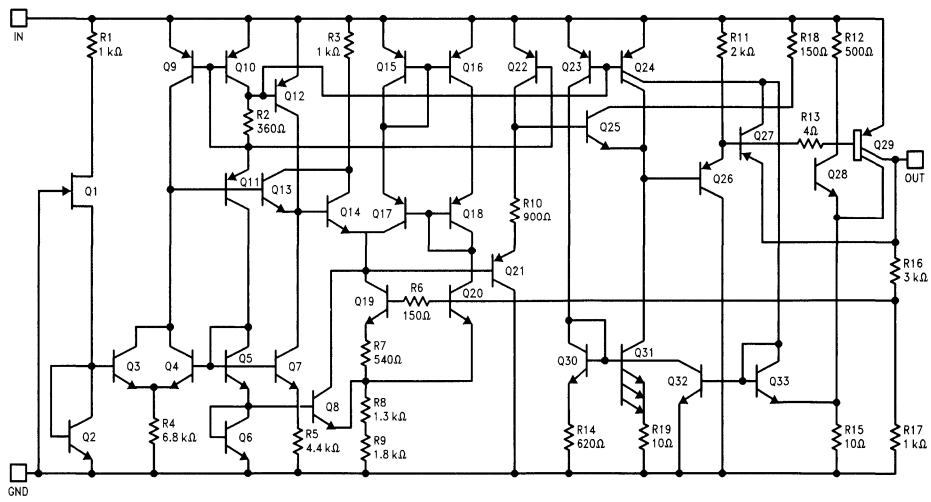
The low dropout voltage makes the LM330 useful for certain battery applications since this feature allows a longer battery discharge before the output falls out of regulation. For example, a battery supplying the regulator input voltage may discharge to 5.6V and still properly regulate the system and load voltage. Supporting this feature, the LM330 protects both itself and regulated systems from negative voltage inputs resulting from reverse installations of batteries.

Other protection features include line transient protection up to 26V, when the output actually shuts down to avoid damaging internal and external circuits. Also, the LM330 regulator cannot be harmed by a temporary mirror-image insertion.

Features

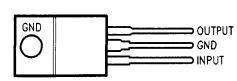
- Input-output differential less than 0.6V
- Output current of 150 mA
- Reverse battery protection
- Line transient protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- P^+ Product Enhancement tested

Schematic and Connection Diagrams



DS009306-1

(TO-220)
Plastic Package



DS009306-2

Front View
Order Number LM330T-5.0
See NS Package Number T03B

National Semiconductor

LM337L
3-Terminal Adjustable Regulator

General Description

The LM337L is an adjustable 3-terminal negative voltage regulator capable of supplying 100 mA over a 1.2V to 37V output range. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators. Also, the LM337L is packaged in a standard TO-92 transistor package which is easy to use.

In addition to higher performance than fixed regulators, the LM337L offers full overload protection. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is disconnected.

Normally, only a single 1 µF solid tantalum output capacitor is needed unless the device is situated more than 6 inches from the input filter capacitors, in which case an input bypass is needed. A larger output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejection ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators, the LM337L is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input-to-output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM337L can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

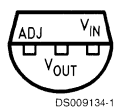
The LM337L is available in a standard TO-92 transistor package and a SO-8 surface mount package. The LM337L is rated for operation over a −25˚C to +125˚C range.

For applications requiring greater output current in excess of 0.5A and 1.5A, see LM137 series data sheets. For the positive complement, see series LM117 and LM317L data sheets.

Features

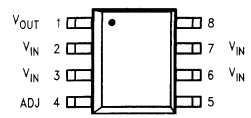
- Adjustable output down to 1.2V
- Guaranteed 100 mA output current
- Line regulation typically 0.01%/V
- Load regulation typically 0.1%
- Current limit constant with temperature
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 80 dB ripple rejection
- Output is short circuit protected

Connection Diagrams



DS009134-1

Bottom View



DS009134-2

Top View

Order Number LM337LM or LM337LZ
See NS Package Number M08A or Z03A

National Semiconductor

LM341/LM78MXX Series
3-Terminal Positive Voltage Regulators

General Description

The LM341 and LM78MXX series of three-terminal positive voltage regulators employ built-in current limiting, thermal shutdown, and safe-operating area protection which makes them virtually immune to damage from output overloads.

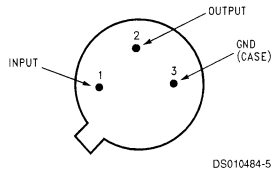
With adequate heatsinking, they can deliver in excess of 0.5A output current. Typical applications would include local (on-card) regulators which can eliminate the noise and degraded performance associated with single-point regulation.

Features

- Output current in excess of 0.5A
- No external components
- Internal thermal overload protection
- Internal short circuit current-limiting
- Output transistor safe-area compensation
- Available in TO-220, TO-39, and TO-252 D-PAK packages
- Output voltages of 5V, 12V, and 15V

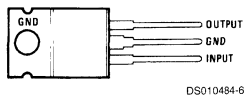
Connection Diagrams

TO-39 Metal Can Package (H)



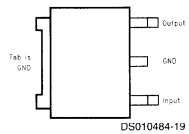
Bottom View
Order Number LM78M05CH, LM78M12CH or LM78M15CH
See NS Package Number H03A

TO-220 Power Package (T)



Top View
Order Number LM341T-5.0, LM341T-12, LM341T-15, LM78M05CT, LM78M12CT or LM78M15CT
See NS Package Number T03B

TO-252



Top View
Order Number LM78M05CDT
See NS Package Number TD03B

National Semiconductor

LM723/LM723C Voltage Regulator

General Description

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature controller.

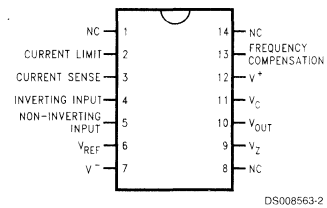
The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Features

- 150 mA output current without external pass transistor
- Output currents in excess of 10A possible by adding external transistors
- Input voltage 40V max
- Output voltage adjustable from 2V to 37V
- Can be used as either a linear or a switching regulator

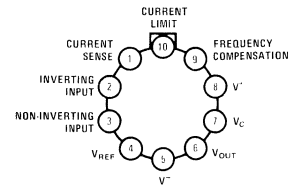
Connection Diagrams

Dual-In-Line Package



Top View
Order Number LM723J/883 or LM723CN
See NS Package J14A or N14A

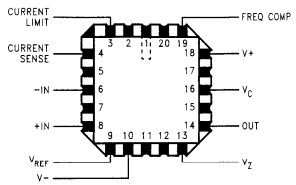
Metal Can Package



Note: Pin 5 connected to case.

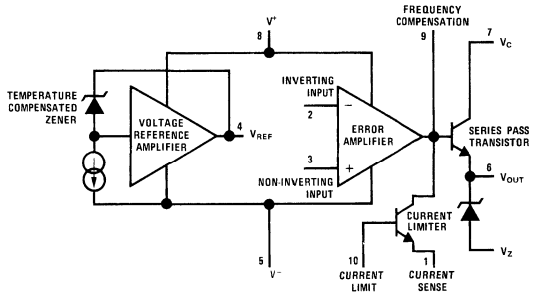
Top View
Order Number LM723H, LM723H/883 or LM723CH
See NS Package H10C

Connection Diagrams (Continued)



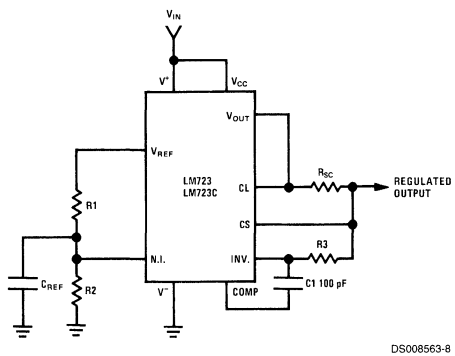
Top View
Order Number LM723E/883
See NS Package E20A

Equivalent Circuit*



*Pin numbers refer to metal can package.

Typical Application



Note: R3 = $\frac{R1\,R2}{R1 + R2}$

for minimum temperature drift.

Typical Performance

Regulated Output Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5mV
Load Regulation (ΔI_L = 50 mA)	1.5mV

FIGURE 1. Basic Low Voltage Regulator (V_{OUT} = 2 to 7 Volts)

National Semiconductor

LM78XX Series Voltage Regulators

General Description

The LM78XX series of three terminal regulators is available with several fixed output voltages making them useful in a wide range of applications. One of these is local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow these regulators to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment. Although designed primarily as fixed voltage regulators these devices can be used with external components to obtain adjustable voltages and currents.

The LM78XX series is available in an aluminum TO-3 package which will allow over 1.0A load current if adequate heat sinking is provided. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistor is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Considerable effort was expanded to make the LM78XX series of regulators easy to use and minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response. Input bypassing is needed only if the regulator is located far from the filter capacitor of the power supply.

For output voltage other than 5V, 12V and 15V the LM117 series provides an output voltage range from 1.2V to 57V.

Features

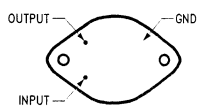
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required
- Output transistor safe area protection
- Internal short circuit current limit
- Available in the aluminum TO-3 package

Voltage Range

LM7805C	5V
LM7812C	12V
LM7815C	15V

Connection Diagrams

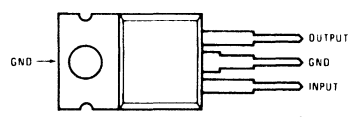
Metal Can Package
TO-3 (K)
Aluminum



DS007746-2

Bottom View
Order Number LM7805CK,
LM7812CK or LM7815CK
See NS Package Number KC02A

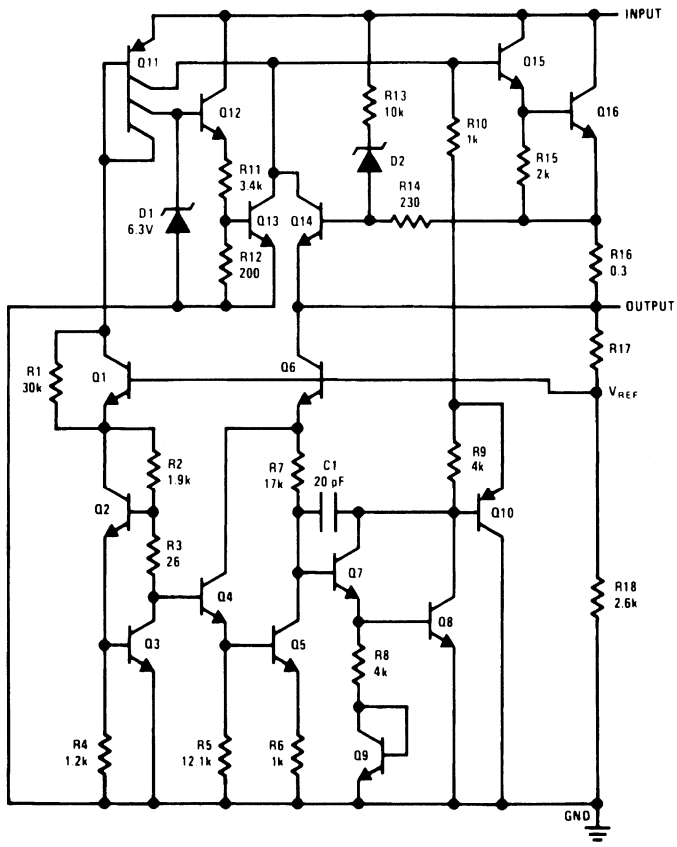
Plastic Package
TO-220 (T)



DS007746-3

Top View
Order Number LM7805CT,
LM7812CT or LM7815CT
See NS Package Number T03B

Schematic


INPUT
Q11
Q12
Q15
Q16
R13
10k
R10
1k
R15
2k
D2
R14
230
R11
3.4k
D1
6.3V
Q13
Q14
R12
200
R16
0.3
OUTPUT
R17
R1
30k
Q1
Q6
V_{REF}
R2
1.9k
R7
17k
C1
20 pF
R9
4k
Q2
Q10
R3
26
Q7
R18
2.6k
Q4
Q8
Q3
Q5
R8
4k
R4
1.2k
R5
12.1k
R6
1k
Q9
GND
DS007746-1

National Semiconductor

LM78LXX Series
3-Terminal Positive Regulators

General Description

The LM78LXX series of three terminal positive regulators is available with several fixed output voltages making them useful in a wide range of applications. When used as a zener diode/resistor combination replacement, the LM78LXX usually results in an effective output impedance improvement of two orders of magnitude, and lower quiescent current. These regulators can provide local on card regulation, eliminating the distribution problems associated with single point regulation. The voltages available allow the LM78LXX to be used in logic systems, instrumentation, HiFi, and other solid state electronic equipment.

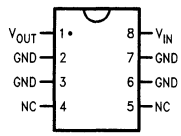
The LM78LXX is available in the plastic TO-92 (Z) package, the plastic SO-8 (M) package and a chip sized package (8-Bump micro SMD) using National's micro SMD package technology. With adequate heat sinking the regulator can deliver 100 mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation becomes too high for the heat sinking provided, the thermal shutdown circuit takes over preventing the IC from overheating.

Features

- LM78L05 in micro SMD package
- Output voltage tolerances of ±5% over the temperature range
- Output current of 100 mA
- Internal thermal overload protection
- Output transistor safe area protection
- Internal short circuit current limit
- Available in plastic TO-92 and plastic SO-8 low profile packages
- No external components
- Output voltages of 5.0V, 6.2V, 8.2V, 9.0V, 12V, 15V
- See AN-1112 for micro SMD considerations

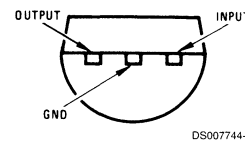
Connection Diagrams

SO-8 Plastic (M)
(Narrow Body)



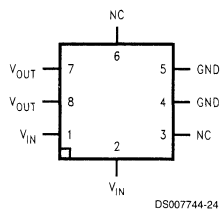
Top View

(TO-92)
Plastic Package (Z)



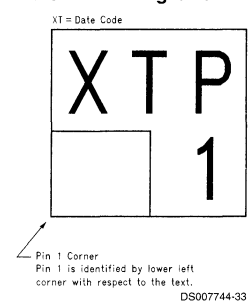
Bottom View

8-Bump micro SMD



Top View
(Bump Side Down)

micro SMD Marking Orientation



Top View

National Semiconductor

LM79XX Series
3-Terminal Negative Regulators

General Description

The LM79XX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79XX series is packaged in the TO-220 power package and is capable of supplying 1.5A of output current.

These regulators employ internal current limiting safe area protection and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79XX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current drain of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

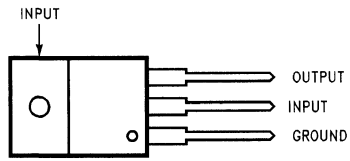
For applications requiring other voltages, see LM137 datasheet.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 1.5A output current
- 4% tolerance on preset output voltage

Connection Diagram

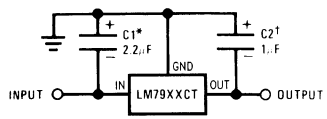
TO-220 Package



Front View
Order Number LM7905CT, LM7912CT or LM7915CT
See NS Package Number TO3B

Typical Applications

Fixed Regulator



*Required if regulator is separated from filter capacitor by more than 3". For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted.

†Required for stability. For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted. Values given may be increased without limit.

For output capacitance in excess of 100µF, a high current diode from input to output (1N4001, etc.) will protect the regulator from momentary input shorts.

National Semiconductor

LM79MXX Series
3-Terminal Negative Regulators

General Description

The LM79MXX series of 3-terminal regulators is available with fixed output voltages of −5V, −12V, and −15V. These devices need only one external component—a compensation capacitor at the output. The LM79MXX series is packaged in the TO-220 power package, and is capable of supplying 0.5A of output current.

These regulators employ internal current limiting, safe area protection, and thermal shutdown for protection against virtually all overload conditions.

Low ground pin current of the LM79MXX series allows output voltage to be easily boosted above the preset value with a resistor divider. The low quiescent current of these devices with a specified maximum change with line and load ensures good regulation in the voltage boosted mode.

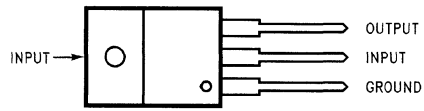
For output voltage other than −5V, −12V, and −15V the LM137 series provides an output voltage range from −1.2V to −57V.

Features

- Thermal, short circuit and safe area protection
- High ripple rejection
- 0.5A output current
- 4% tolerance on preset output voltage

Connection Diagram

TO-220 Plastic Package (T)



DS010483-7

Front View
Order Number LM79M05CT, LM79M12CT or LM79M15CT
See NS Package Number T03B

National Semiconductor

LM9074
System Voltage Regulator with Keep-Alive ON/OFF Control

General Description

The LM9074 is a 5V, 3% accurate, 180 mA NPN voltage regulator. The regulator features an active low delayed reset output flag which can be used to reset a microprocessor system on turn-ON and in the event that the regulator output falls out of regulation for any reason. An external capacitor programs a delay time interval before the reset output can return high.

Designed for automotive application the LM9074 contains a variety of protection features such as reverse battery, over-voltage shutdown, thermal shutdown, input transient protection and a wide operating temperature range.

A unique two-input logic control scheme is used to enable or disable the regulator output. An ON/OFF input can be provided by an ignition switch derived signal while a second, Keep-Alive input, is generated by a system controller. This allows for a system to remain ON after ignition has been switched OFF. The system controller can then execute a power-down routine and after which command the regulator OFF to a low quiescent current state (60 µA max).

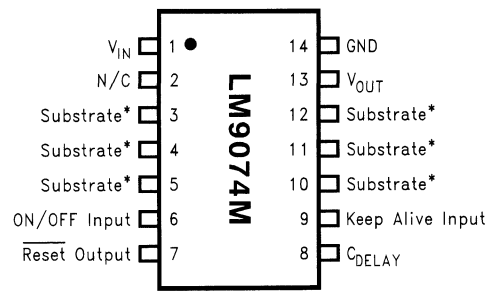
Design techniques have been employed to allow the regulator to remain operational and not generate false reset signals when subjected to high levels of RF energy (300V/m from 2 MHz to 400 MHz).

Features

- Automotive application reliability
- 3% output voltage tolerance
- Insensitive to radiated RFI
- Dropout voltage less than 2.5V with 180 mA output current
- Externally programmed reset delay interval
- Keep-alive feature with 2 logic control inputs
- 60V Load dump transient protection
- Thermal shutdown
- Short circuit protection and disable safety features
- Reverse battery protection
- Low OFF quiescent current, 60 µA maximum
- Wide operating temperature range −40°C to +125°C

Connection Diagram and Ordering Information (Top View)

14-Pin SO Package



* Substrate pins must be connected to Ground Pin

DS101305-2

Order Number LM9074M
See NS Package Number M14A

Section 16

Voltage Regulators - Low-Dropout

Section 16 Contents

National Semiconductor

Low Dropout Regulators Selection Guide

Output Current	Device	Output Voltage Accuracy (Note 1)	Output Voltage (V)				Dropout Voltage V (max) (Note 2)	Quiescent Current mA (max) (Note 3)	Max. Input Voltage
			3.0	3.3	5.0	Other Available Voltages			
50mA	LP2980A	0.5%	✓	✓	✓	2.5, 2.6, 2.7, 2.8, 2.9, 3.1, 3.2, 3.5, 3.6, 3.8, 4.0, 4.5, 4.7	0.15	0.095	16 (Note 4)
	LP2980LVA	0.5%				1.5, 1.8	(Note 5)	0.085	16
	LP2978A	1%				3.8	0.15	0.095	16
	LP2980	1%	✓	✓	✓	2.5, 2.6, 2.7, 2.8, 2.9, 3.1, 3.2, 3.5, 3.6, 3.8, 4.0, 4.5, 4.7	0.15	0.095	16
	LP2980LV	1%				1.5, 1.8	(Note 5)	0.085	16
	LP2980-ADJ	1%				Adjustable	0.15	0.095	16
	LP2982A	1%	✓	✓	✓	2.5, 2.75, 2.8, 3.6, 3.8, 4.0, 4.5, 4.7	0.15	0.095	16
	LP2978	1.5%				3.8	0.15	0.095	16
	LP2982	1.5%	✓	✓	✓	2.5, 2.75, 2.8, 3.6, 3.8, 4.0, 4.5, 4.7	0.15	0.095	16
	LM2936	3%F	✓	✓	✓		0.40F	<0.02F	40
80mA	LMS5213	4%	✓			2.8	0.6	0.01	6
100mA	LP2950AC	0.5%	✓	✓	✓		0.45	0.12	30
	LP2951AC	0.5%	✓	✓	✓	Adjustable (Note 6)	0.45	0.12	30
	LP2981A	0.75%	✓	✓	✓	2.5, 2.7, 2.8, 2.9, 3.1, 3.2, 3.6, 3.8, 4.0, 4.5, 4.7	0.25	0.095	16
	LP2981	1.25%	✓	✓	✓	2.5, 2.7, 2.8, 2.9, 3.1, 3.2, 3.6, 3.8, 4.0, 4.5, 4.7	0.25	0.095	16
	LP2951	1%			✓	Adjustable (Note 6)	0.45	0.12	30
	LP2951C	1%	✓	✓	✓	Adjustable (Note 6)	0.45	0.12	30
	LM2931A	4%			✓		0.6	1.0	26
	LM3480	4%		✓	✓	12, 15	1.1	4T	30
	LM3490	4%		✓	✓	12, 15	1.1	4T	30
	LM2931	5%			✓		0.6	1.0	26
	LM2931C	5%				Adjustable (Note 6)	0.6	1.0	26

Output Current	Device	Output Voltage Accuracy (Note 1)	Output Voltage (V)				Dropout Voltage V (max) (Note 2)	Quiescent Current mA (max) (Note 3)	Max. Input Voltage
			3.0	3.3	5.0	Other Available Voltages			
	LP2966 (2 outputs)	1%	✓	✓	✓	1.8, 2.5, 2.8, 3.6	0.195	0.45	7
	LP2967 (2 outputs)	1%		✓		2.5, 2.6, 2.8	0.22	0.34	16
	LP2983	1.5%				0.9, 1.0, 1.2		0.125	16
	LP2985A	1%	✓	✓	✓	2.8, 3.1, 3.2, 3.6, 3.8, 4.0, 4.7, 4.8	0.35	0.095	16
	LP2985	1.5%	✓	✓	✓	2.8, 3.1, 3.2, 3.6, 3.8, 4.0, 4.7, 4.8	0.35	0.095	16
	LP2985LV	1.5%				1.5, 1.8, 3.0		0.095	16
150mA	LP3962	±1.5%		✓	✓	1.8, 2.5	38	15	7
	LP3965	±1.5%		✓	✓	1.8, 2.5, Adjustable	38	15	7
	LP3984	2.0%	✓			1.5, 1.8, 2.0, 3.1	133	<1µA	6
	LP3985	2.5%	✓	✓	✓	2.5, 2.85, 2.9, 3.1, 3.2, 4.7	0.06	0.160	6.5
	LP3986	2.5%				28585, 2828	0.10	0.32	6
	LP3987	3.0%	✓	✓		2.4, 2.5, 2.7, 2.8, 2.85, 2.9, 3.1, 3.2, 4.7	100	<1µA	6
	LP3988	.30%	✓			2.5, 2.6, 2.85	150	<1.5µA	6
	LM2930	6%			✓	8	0.6	7	26
	LP2986A	0.5%	✓	✓	✓	Adjustable (Note 6)	0.23	0.12	16
	LP2987A	0.5%	✓	✓	✓	2.8, 3.2, 3.8	0.23	0.12	16
	LP2988A	0.5%	✓	✓	✓	2.8, 3.2, 3.8	0.23	0.12	16
200mA	LP2986	1%	✓	✓	✓	Adjustable (Note 6)	0.23	0.12	16
	LP2987	1%	✓	✓	✓	2.8, 3.2, 3.8	0.23	0.12	16
	LP2988	1%	✓	✓	✓	2.8, 3.2, 3.8	0.23	0.12	16
	LP2952A	0.5%		✓	✓	Adjustable (Note 6)	0.6	0.17	30
	LP2953A	0.5%		✓	✓	Adjustable (Note 6)	0.6	0.17	30
	LP2953AM	0.5%			✓	Adjustable (Note 6)	0.6	0.17	30
	LP2954A	0.5%			✓	Adjustable (Note 6)	0.6	0.15	30
	LP2956A	0.5%			✓	Adjustable (Note 6)	0.6	0.25	30
	LP2957A	0.5%			✓		0.6	0.20	30
250mA	LP2952	1%		✓	✓	Adjustable (Note 6)	0.6	0.17	30
	LP2953	1%		✓	✓	Adjustable (Note 6)	0.6	0.17	30
	LP2954	1%			✓	Adjustable (Note 6)	0.6	0.15	30
	LP2956	1%			✓	Adjustable (Note 6)	0.6	0.25	30
	LP2957	1%			✓		0.6	0.20	30
	LP2992	1.5%		✓	✓	1.5, 1.8, 2.5	0.25	0.125	16
	LM9070	3%F			✓		0.80F	4F	26
	LM9071	3%F			✓		0.80F	4F	26
300mA	LP3963	±1.5%		✓	✓	1.8, 2.5	80	15	7
	LP3966	±1.5%		✓	✓	1.8, 2.5, Adjustable	80	15	7
	LP3981					2.5, 2.8, 2.83, 3.03	132	<1µA	6
350mA	LM9072 (2 outputs)	2%F			✓		0.80F	15F	27

Output Current	Device	Output Voltage Accuracy (Note 1)	Output Voltage (V)				Dropout Voltage V (max) (Note 2)	Quiescent Current mA (max) (Note 3)	Max. Input Voltage
			3.0	3.3	5.0	Other Available Voltages			
500mA	LP2960A	0.8%		✓	✓	Adjustable (Note 6)	0.6	0.6	30
	LP2960	1.5%		✓	✓	Adjustable (Note 6)	0.6	0.6	30
	LP2989A	0.75%				2.5	425	<0.8	16
	LP2989	1.25%				2.5	425	<0.8	16
	LP2989LV	0.75%				1.8		<0.8	16
	LM2984 (3 outputs)	3%			✓		0.8	5T	26
	LM2937	3%		✓	✓	2.5, 8, 10, 12, 15	1.0F	10	26

Output Current	Device	Output Voltage Accuracy (Note 1)	Output Voltage (V)				Dropout Voltage V (max) (Note 2)	Quiescent Current mA (max) (Note 3)	Max. Input Voltage
			3.0	3.3	5.0	Other Available Voltages			
700mA	LM9073 (2 outputs)	2%F			✓		0.80F	15F	27
800mA	LM1117	1%		✓	✓	2.85, Adjustable	1.3F	10	20
	LP3961	±1.5%		✓	✓	1.8, 2.5	240	15	7
	LP3964	±1.5%		✓	✓	1.8, 2.5, Adjustable	240	15	7
1.0A	LM2990	2%				−5, −5.2, −12, −15	1.0T	5	−26
	LM2991	2%				Adjustable	1.0T	5	−26
	LM2940 (Mil)	3%			✓	8, 12, 15	0.7	15	26
	LM2940	3%			✓	8, 9, 10, 12	0.8	15	26
	LM2940C	3%			✓	9, 12, 15	0.8	15	26
	LM2941	3%				Adjustable	0.8	15	26
	LM2941C	3%				Adjustable	0.8	15	26
	LM3940	3%		✓			0.8	15	7.5
1.5A	LM1086	1%		✓	✓	2.85, Adjustable	1.5F	10	30
3A	LM1085	1%		✓	✓	12, Adjustable	1.5F	10	30
5A	LM1084	1%		✓	✓	12, Adjustable	1.5F	10	30
Controller	LM3411A (Note 7)	0.5%		✓	✓			0.125	
	LM3411 (Note 7)	1%		✓	✓			0.125	
	LP2975A	1.5%		✓	✓	12, Adjustable (Note 6)	—	0.24	24
	LP2975	2.5%		✓	✓	12, Adjustable (Note 6)	—	0.24	24
	LM3460	2.5%				1.2, 1.5	—	0.125	—

Note 1: 'F' denotes accuracy for full temperature range: otherwise, accuracy is at 25˚C.

Note 2: Dropout voltage is given for full load. 'F' denotes value for full temperature range, and 'T' denotes typical value; otherwise, values are maximum at 25˚C.

Note 3: Quiescent current is given for minimum load. 'F' denotes value for full temperature range, and 'T' denotes typical value; otherwise, values are maximum at 25˚C.

Note 4: 20V version available upon request.

Note 5: Minimum input voltage required to maintain regulation is 2.20V.

Note 6: Denotes products with fixed output voltages that also provide adjustment control of the output voltage.

Note 7: Refer to Voltage Control and Supervisor Products section for product data for the LM3411A/LM3411 regulator controller.

National Semiconductor

Low-Dropout Voltage Regulators Definition Of Terms

Dropout Voltage: The input-voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100 mV from the nominal value obtained at (V_{OUT} + 5V) input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

National Semiconductor

LM1084
5A Low Dropout Positive Regulators

General Description

The LM1084 is a series of low dropout voltage positive regulators with a maximum dropout of 1.5V at 5A of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1084 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in three fixed voltages: 3.3V, 5.0V and 12.0V. The fixed versions intergrate the adjust resistors.

The LM1084 circuit includes a zener trimmed bandgap reference, current limiting and thermal shutdown.

The LM1084 series is available in TO-220 and TO-263 packages. Refer to the LM1085 for the 3A version, and the LM1086 for the 1.5A version.

Features

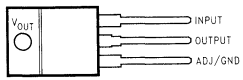
- Available in 3.3V, 5.0V, 12V and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 5A
- Industrial Temperature Range −40°C to 125°C
- Line Regulation 0.015% (typical)
- Load Regulation 0.1% (typical)

Applications

- Post Regulator for Switching DC/DC Conveter
- High Efficiency Linear Regulators
- Battery Charger

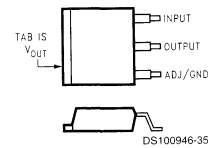
Connection Diagrams

TO-220



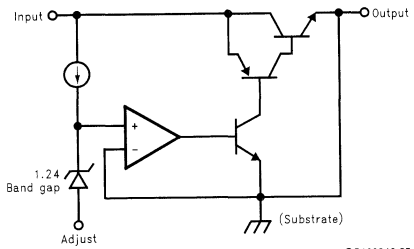
Top View

TO-263

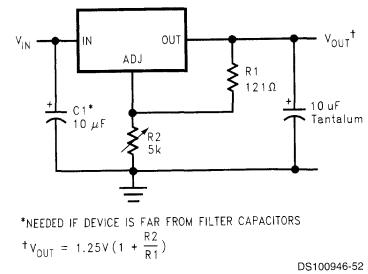


Top View

Basic Functional Diagram, Adjustable Version



Application Circuit



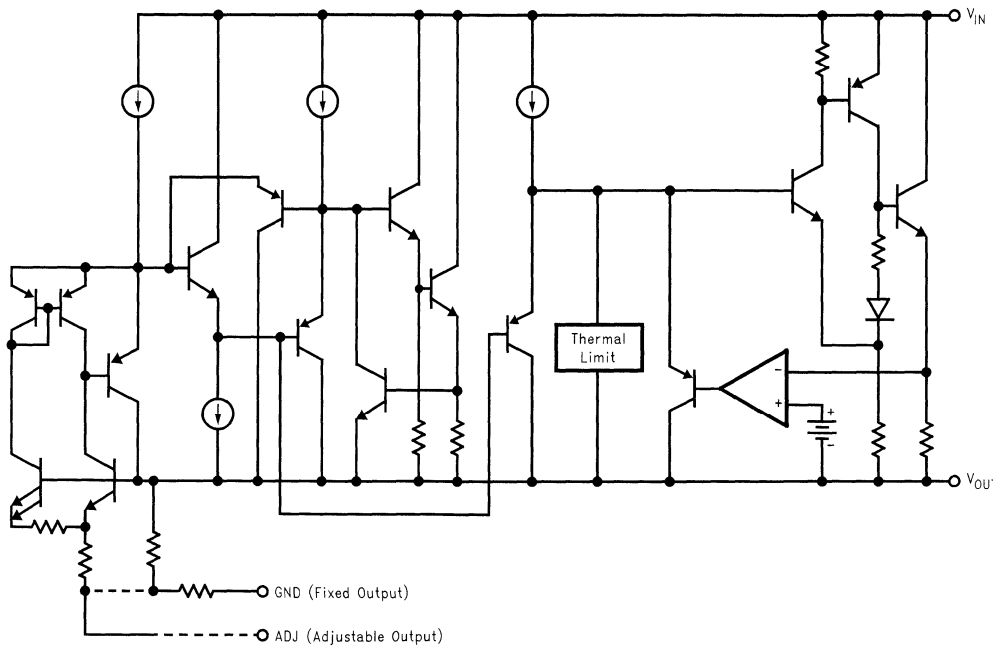
1.2V to 15V Adjustable Regulator

16

Ordering Information

Package	Temperature Range	Part Number	Transport Media	NSC Drawing
3-lead TO-263	−40°C to +125°C	LM1084IS-ADJ	Rails	TS3B
		LM1084ISX-ADJ	Tape and Reel	
		LM1084IS-12	Rails	
		LM1084ISX-12	Tape and Reel	
		LM1084IS-3.3	Rails	
		LM1084ISX-3.3	Tape and Reel	
		LM1084IS-5.0	Rails	
		LM1084ISX-5.0	Tape and Reel	
3-lead TO-220	−40°C to + 125°C	LM1084IT-ADJ	Rails	T03B
		LM1084IT-12	Rails	
		LM1084IT-3.3	Rails	
		LM1084IT-5.0	Rails	

Simplified Schematic



DS100946-34

National Semiconductor

LM1085
3A Low Dropout Positive Regulators

General Description

The LM1085 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 3A of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1085 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in three fixed voltages: 3.3V, 5.0V and 12.0V. The fixed versions integrate the adjust resistors.

The LM1085 circuit includes a zener trimmed bandgap reference, current limiting and thermal shutdown.

The LM1085 series is available in TO-220 and TO-263 packages. Refer to the LM1084 for the 5A version, and the LM1086 for the 1.5V version.

Features

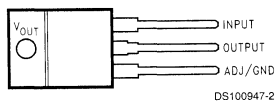
- Available in 3.3V, 5.0V, 12V and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 3A
- Line Regulation 0.015% (typical)
- Load Regulation 0.1% (typical)

Applications

- High Efficiency Linear Regulators
- Battery Charger
- Post Regulation for Switching Supplies
- Constant Current Regulator
- Microprocessor Supply

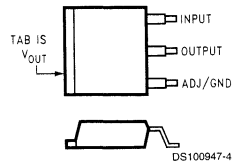
Connection Diagrams

TO-220



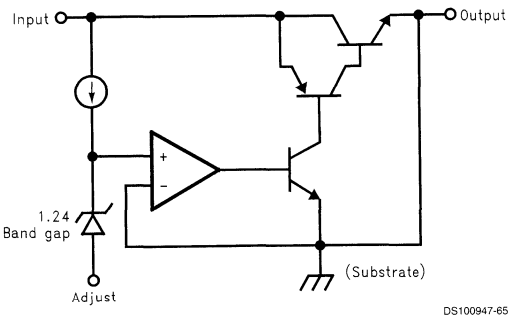
Top View

TO-263

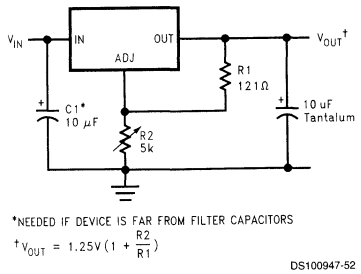


Top View

Basic Functional Diagram, Adjustable Version



Application Circuit



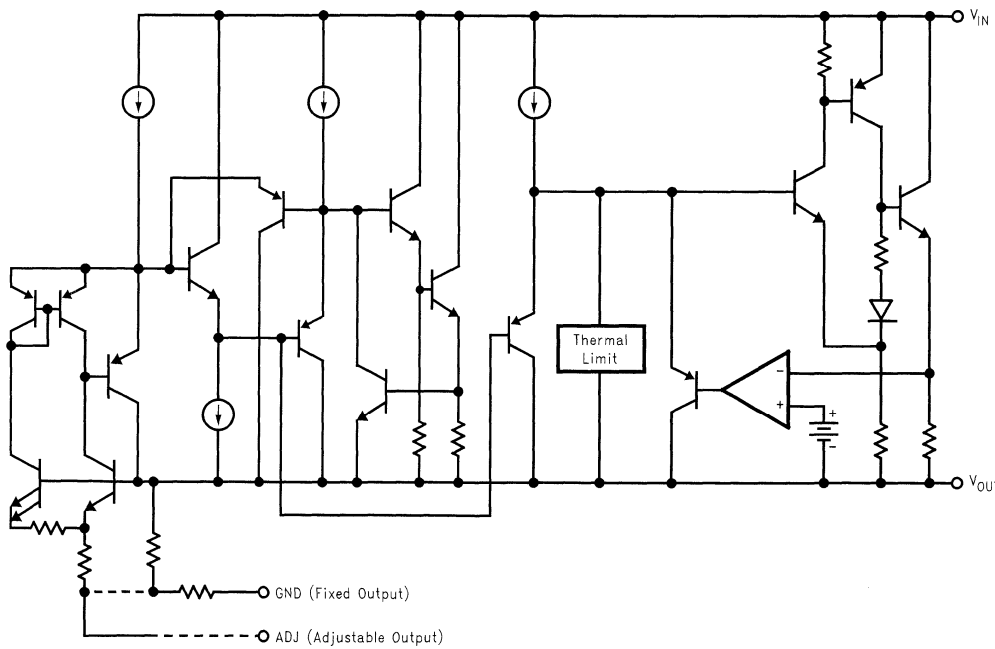
1.2V to 15V Adjustable Regulator

16

Ordering Information

Package	Temperature Range	Part Number	Transport Media	NSC Drawing
3-lead TO-263	−40°C to +125°C	LM1085IS-ADJ	Rails	TS3B
		LM1085ISX-ADJ	Tape and Reel	
		LM1085IS-12	Rails	
		LM1085ISX-12	Tape and Reel	
		LM1085IS-3.3	Rails	
		LM1085ISX-3.3	Tape and Reel	
		LM1085IS-5.0	Rails	
		LM1085ISX-5.0	Tape and Reel	
3-lead TO-220	−40°C to + 125°C	LM1085IT-ADJ	Rails	T03B
		LM1085IT-12	Rails	
		LM1085IT-3.3	Rails	
		LM1085IT-5.0	Rails	

Simplified Schematic



DS100947-34

National Semiconductor

LM1086
1.5A Low Dropout Positive Regulators

General Description

The LM1086 is a series of low dropout positive voltage regulators with a maximum dropout of 1.5V at 1.5A of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1086 is available in an adjustable version, which can set the output voltage with only two external resistors. It is also available in five fixed voltages: 2.5V, 2.85V, 3.3V, 3.45V and 5.0V. The fixed versions integrate the adjust resistors.

The LM1086 circuit includes a zener trimmed bandgap reference, current limiting and thermal shutdown.

The LM1086 series is available in TO-220 and TO-263 packages. Refer to the LM1084 for the 5A version, and the LM1085 for the 3A version.

Features

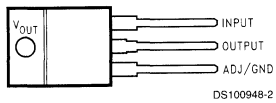
- Available in 2.5V, 2.85V, 3.3V, 3.45V, 5V and Adjustable Versions
- Current Limiting and Thermal Protection
- Output Current 1.5A
- Line Regulation 0.015% (typical)
- Load Regulation 0.1% (typical)

Applications

- SCSI-2 Active Terminator
- High Efficiency Linear Regulators
- Battery Charger
- Post Regulation for Switching Supplies
- Constant Current Regulator
- Microprocessor Supply

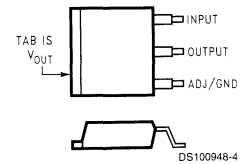
Connection Diagrams

TO-220



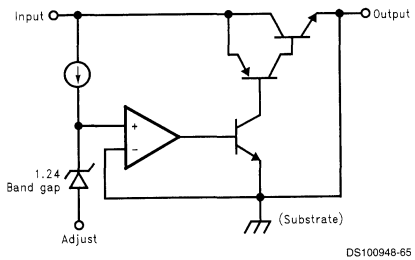
Top View

TO-263

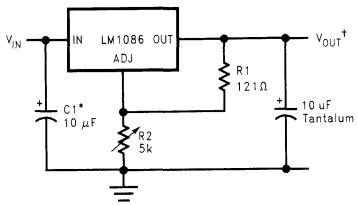


Top View

Basic Functional Diagram, Adjustable Version



Application Circuit



*NEEDED IF DEVICE IS FAR FROM FILTER CAPACITORS

† $V_{OUT} = 1.25V\left(1 + \frac{R2}{R1}\right)$

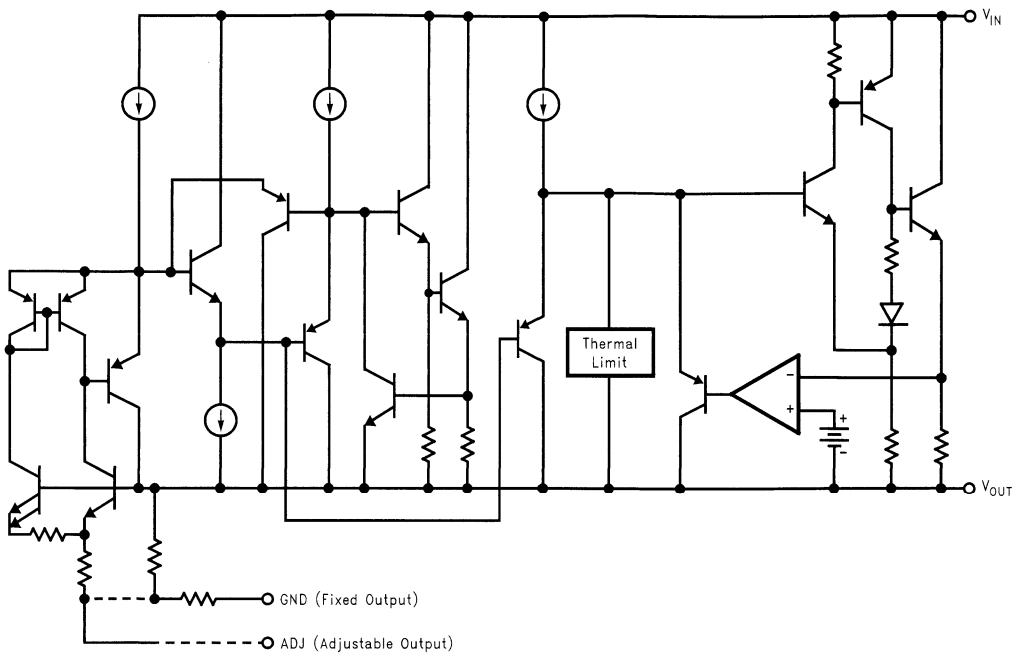
DS100948-52

1.2V to 15V Adjustable Regulator

Ordering Information

Package	Temperature Range	Part Number	Transport Media	NSC Drawing
3-lead TO-263	−40°C to +125°C	LM1086IS-ADJ	Rails	TS3B
		LM1086ISX-ADJ	Tape and Reel	
		LM1086IS-2.85	Rails	
		LM1086ISX-2.85	Tape and Reel	
		LM1086IS-3.3	Rails	
		LM1086ISX-3.3	Tape and Reel	
		LM1086IS-3.45	Rails	
		LM1086ISX-3.45	Tape and Reel	
		LM1086IS-5.0	Rails	
		LM1086ISX-5.0	Tape and Reel	
	0°C to +125°C	LM1086CS-ADJ	Rails	
		LM1086CSX-ADJ	Tape and Reel	
		LM1086CS-2.5	Rails	
		LM1086CSX-2.5	Tape and Reel	
		LM1086CS-2.85	Rails	
		LM1086CSX-2.85	Tape and Reel	
		LM1086CS-3.3	Rails	
		LM1086CSX-3.3	Tape and Reel	
		LM1086CS-5.0	Rails	
		LM1086CSX-5.0	Tape and Reel	
3-lead TO-220	−40°C to +125°C	LM1086IT-ADJ	Rails	T03B
		LM1086IT-2.85	Rails	
		LM1086IT-3.3	Rails	
		LM1086IT-5.0	Rails	
	0°C to +125°C	LM1086CT-ADJ	Rails	
		LM1086CT-2.85	Rails	
		LM1086CT-3.3	Rails	
		LM1086CT-5.0	Rails	

Simplified Schematic



DS100948-34

National Semiconductor

LM1117/LM1117I
800mA Low-Dropout Linear Regulator

General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

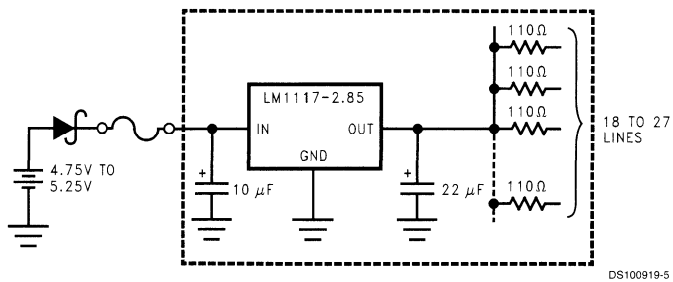
- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
  - — LM1117 0°C to 125°C
  - — LM1117I −40°C to 125°C

Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

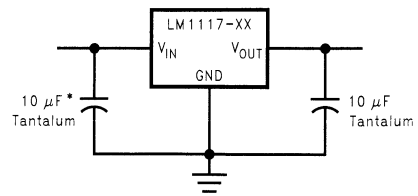
Typical Application

Active Terminator for SCSI-2 Bus



DS100919-5

Fixed Output Regulator



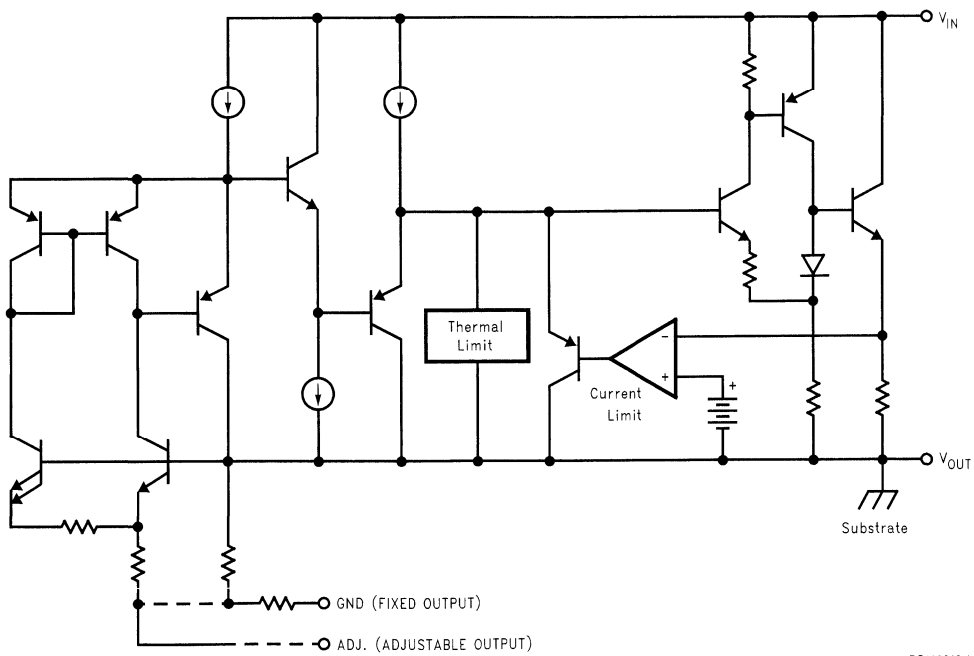
*Required if the regulator is located far from the power supply filter.

DS100919-28

Ordering Information

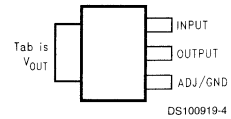
Package	Temperature Range	Part Number	Packaging Marking	Transport Media	NSC Drawing
3-lead SOT-223	0°C to +125°C	LM1117MPX-ADJ	N03A	Tape and Reel	MA04A
		LM1117MPX-1.8	N12A	Tape and Reel	
		LM1117MPX-2.5	N13A	Tape and Reel	
		LM1117MPX-2.85	N04A	Tape and Reel	
		LM1117MPX-3.3	N05A	Tape and Reel	
		LM1117MPX-5.0	N06A	Tape and Reel	
	−40°C to +125°C	LM1117IMPX-ADJ	N03B	Tape and Reel	
		LM1117IMPX-3.3	N05B	Tape and Reel	
		LM1117IMPX-5.0	N06B	Tape and Reel	
3-lead TO-220	0°C to +125°C	LM1117T-ADJ	LM1117T-ADJ	Rails	T03B
		LM1117T-2.85	LM1117T-2.85	Rails	
		LM1117T-3.3	LM1117T-3.3	Rails	
		LM1117T-5.0	LM1117T-5.0	Rails	
3-lead TO-252	0°C to +125°C	LM1117DTX-ADJ	LM1117DT-ADJ	Tape and Reel	TD03B
		LM1117DTX-1.8	LM1117DT-1.8	Tape and Reel	
		LM1117DTX-2.5	LM1117DT-2.5	Tape and Reel	
		LM1117DTX-2.85	LM1117DT-2.85	Tape and Reel	
		LM1117DTX-3.3	LM1117DT-3.3	Tape and Reel	
		LM1117DTX-5.0	LM1117DT-5.0	Tape and Reel	
	−40°C to +125°C	LM1117IDTX-ADJ	LM1117IDT-ADJ	Tape and Reel	
		LM1117IDTX-3.3	LM1117IDT-3.3	Tape and Reel	
		LM1117IDTX-5.0	LM1117IDT-5.0	Tape and Reel	

Block Diagram



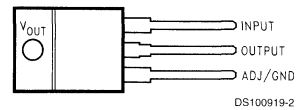
Connection Diagrams

SOT-223



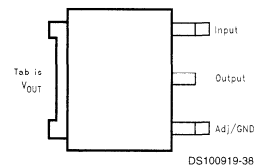
Top View

TO-220



Top View

TO-252



Top View

National Semiconductor

LM2930
3-Terminal Positive Regulator

General Description

The LM2930 3-terminal positive regulator features an ability to source 150 mA of output current with an input-output differential of 0.6V or less. Efficient use of low input voltages obtained, for example, from an automotive battery during cold crank conditions, allows 5V circuitry to be properly powered with supply voltages as low as 5.6V. Familiar regulator features such as current limit and thermal overload protection are also provided.

Designed originally for automotive applications, the LM2930 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (40V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2930 cannot be harmed by temporary mirror-image insertion.

Fixed outputs of 5V and 8V are available in the plastic TO-220 and TO-263 power packages.

Features

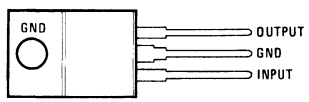
- Input-output differential less than 0.6V
- Output current in excess of 150 mA
- Reverse battery protection
- 40V load dump protection
- Internal short circuit current limit
- Internal thermal overload protection
- Mirror-image insertion protection
- P^+ Product Enhancement tested

Voltage Range

- LM2930T-5.0: 5V
- LM2930T-8.0: 8V
- LM2930S-5.0: 5V
- LM2930S-8.0: 8V

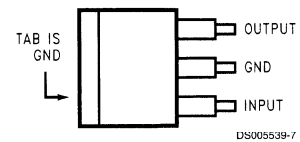
Connection Diagrams

(TO-220)
Plastic Package



Front View
Order Number LM2930T-5.0 or LM2930T-8.0
See NS Package Number T03B

(TO-263)
Plastic Surface-Mount Package



Top View

Side View

Order Number LM2930S-5.0 or LM2930S-8.0
See NS Package Number TS3B

National Semiconductor

LM2931
Series Low Dropout Regulators

General Description

The LM2931 positive voltage regulator features a very low quiescent current of 1mA or less when supplying 10mA loads. This unique characteristic and the extremely low input-output differential required for proper regulation (0.2V for output currents of 10mA) make the LM2931 the ideal regulator for standby power systems. Applications include memory standby circuits, CMOS and other low power processor power supplies as well as systems demanding as much as 100mA of output current.

Designed originally for automotive applications, the LM2931 and all regulated circuitry are protected from reverse battery installations or 2 battery jumps. During line transients, such as a load dump (60V) when the input voltage to the regulator can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both internal circuits and the load. The LM2931 cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

The LM2931 family includes a fixed 5V output (±3.8% tolerance for A grade) or an adjustable output with ON/OFF pin. Both versions are available in a TO-220 power package, TO-263 surface mount package, and an 8-lead surface mount package. The fixed output version is also available in the TO-92 plastic and 6-Bump micro SMD packages.

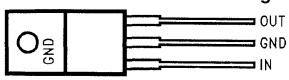
Features

- Very low quiescent current
- Output current in excess of 100 mA
- Input-output differential less than 0.6V
- Reverse battery protection
- 60V load dump protection
- −50V reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- Mirror-image insertion protection
- Available in TO-220, TO-92, TO-263, SO-8 or 6-Bump micro SMD packages
- Available as adjustable with TTL compatible switch
- See AN-1112 for micro SMD considerations

Connection Diagrams

FIXED VOLTAGE OUTPUT

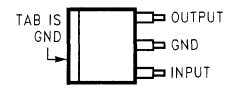
TO-220 3-Lead Power Package



00525406

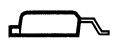
Front View

TO-263 Surface-Mount Package



00525411

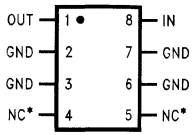
Top View



00525412

Side View

8-Pin Surface Mount

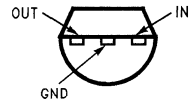


00525407

Top View

*NC = Not internally connected. Must be electrically isolated from the rest of the circuit for the micro SMD package.

TO-92 Plastic Package

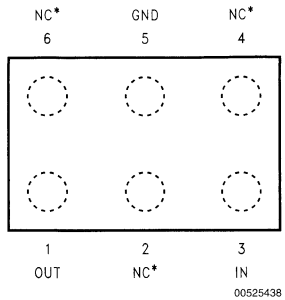


00525408

Bottom View

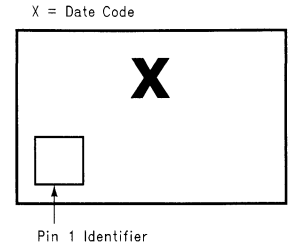
Connection Diagrams (Continued)

6-Bump micro SMD



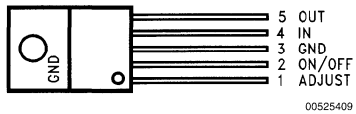
Top View
(Bump Side Down)

micro SMD Laser Mark



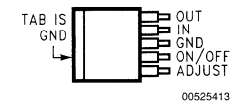
ADJUSTABLE OUTPUT VOLTAGE

TO-220 5-Lead Power Package

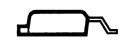


Front View

TO-263
5-Lead Surface-Mount Package

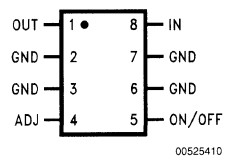


Top View



Side View

8-Pin Surface Mount



Top View

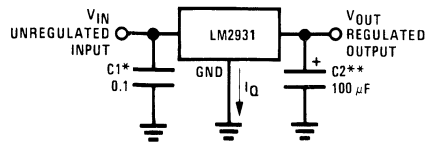
Ordering Information

Output Number	Package	Part Number	Package Marking	Transport Media	NSC Drawing
5V	3-Pin TO-220	LM2931T-5.0	LM2931T-5.0	Rails	T03B
		LM2931AT-5.0	LM2931AT-5.0	Rails	
	3-Pin TO-263	LM2931S-5.0	LM2931S-5.0	Rails	TS3B
		LM2931AS-5.0	LM2931AS-5.0	Rails	
	TO-92	LM2931Z-5.0	LM2931Z-5	1.8k Units per Box	Z03A
		LM2931AZ-5.0	LM2931AZ	1.8k Units per Box	
	8-Pin SOIC	LM2931M-5.0	2931M-5.0	Rails	M08A
		LM2931AM-5.0	2931AM-5.0	Rails	
	* 6-Bump micro SMD	LM2931IBPX-5.0	-	Tape and Reel	BPA06HTA
Adjustable, 3V to 24V	5-Pin TO-220	LM2931CT	LM2931CT	Rails	T05A
	5-Pin TO-263	LM2931CS	LM2931CS	Rails	TS5B
	8-Pin SOIC	LM2931CM	LM2931CM	Rails	M08A
3.3V	* 6-Bump micro SMD	LM2931IBPX-3.3	-	Tape and Reel	BPA06HTB

Note: The micro SMD package marking is a single digit manufacturing Date Code Only.

Typical Application

LM2931 Fixed Output

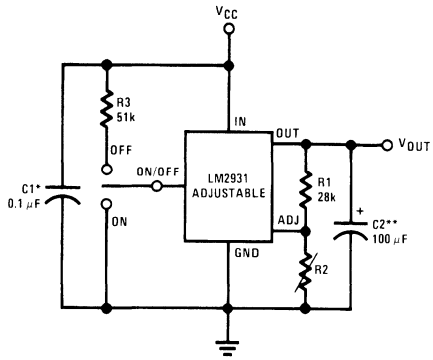


00525404

*Required if regulator is located far from power supply filter.

**C2 must be at least 100 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

LM2931 Adjustable Output



00525405

$$V_{OUT} = \text{Reference Voltage} \times \frac{R1 + R2}{R1}$$

Note: Using 27k for R1 will automatically compensate for errors in V_{OUT} due to the input bias current of the ADJ pin (approximately 1 µA).

16

National Semiconductor

LM2936-3.0
Ultra-Low Quiescent Current 3.0V Regulator

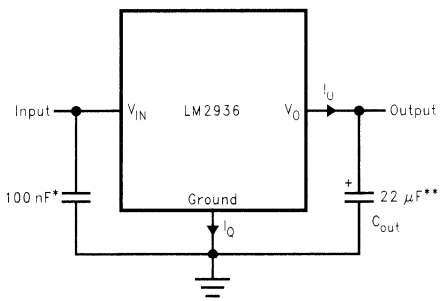
General Description

The LM2936-3.0 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 20 µA quiescent current at a 100 µA load, the LM2936-3.0 is ideally suited for automotive and other battery operated systems. The LM2936-3.0 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936-3.0 has a 40V maximum operating voltage limit, a −40°C to +125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936-3.0 is available in a TO-92 package, a SO-8 surface mount package, as well as SOT-223 and TO-252 surface mount power packages.

Features

- Ultra low quiescent current ($I_Q \leq 20$ µA for $I_O = 100$ µA)
- Fixed 3.0V, 50 mA output
- ±2% Initial output tolerance
- ±3% Output tolerance over line, load, and temperature
- Dropout voltage typically 200 mV @ $I_O = 50$ mA
- Reverse battery protection
- −50V reverse transient protection
- Internal short circuit current limit
- Internal thermal shutdown protection
- 40V operating voltage limit
- Shutdown pin available with LM2936BM package

Typical Application

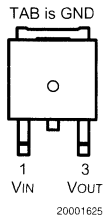


* Required if regulator is located more than 2" from power supply filter capacitor.

** Required for stability. Must be rated for 22 µF minimum over intended operating temperature range. Effective series resistance (ESR) is critical, see curve. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

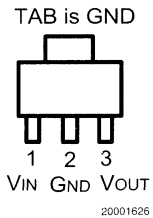
Connection Diagrams

TO-252



Top View
Order Number LM2936DT-3.0
See NS Package Number TD03B

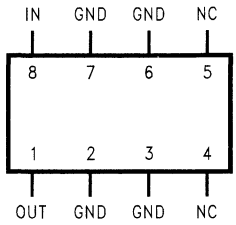
SOT-223



Top View
Order Number LM2936MP-3.0
See NS Package Number MA04A

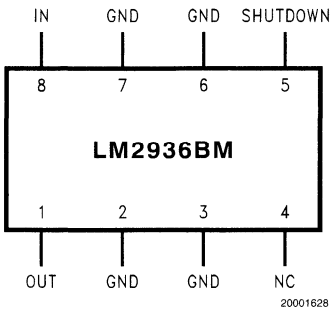
Connection Diagrams (Continued)

8-Pin SO (M)



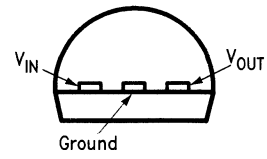
Top View
Order Number LM2936M-3.0
See NS Package Number M08A

8-Pin SO (M)



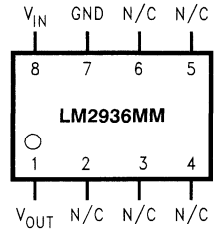
Top View
Order Number LM2936BM-3.0
See NS Package Number MO8A

TO-92



Bottom View
Order Number LM2936Z-3.0
See NS Package Number Z03A

8-Pin SOIC (MM)



Top View
Order Number LM2936MM-3.0
See NS Package Number MUA08A

National Semiconductor

LM2936-3.3
Ultra-Low Quiescent Current 3.3V Regulator

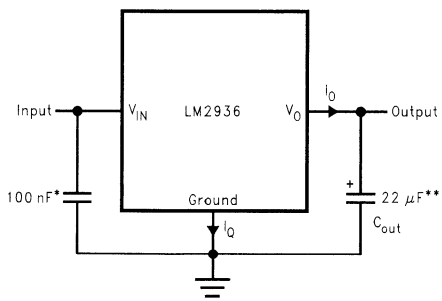
General Description

The LM2936-3.3 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 20 µA quiescent current at a 100 µA load, the LM2936-3.3 is ideally suited for automotive and other battery operated systems. The LM2936-3.3 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936-3.3 has a 40V maximum operating voltage limit, a −40°C to +125°C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936-3.3 is available in a TO-92 package, a SO-8 surface mount package, as well as SOT-223 and TO-252 surface mount power packages.

Features

- Ultra low quiescent current ($I_Q \leq 20$ µA for $I_O = 100$ µA)
- Fixed 3.3V, 50 mA output
- ±2% Initial output tolerance
- ±3% Output tolerance over line, load, and temperature
- Dropout voltage typically 200 mV @ $I_O = 50$ mA
- Reverse battery protection
- −50V reverse transient protection
- Internal short circuit current limit
- Internal thermal shutdown protection
- 40V operating voltage limit
- Shutdown pin available with LM2936BM package

Typical Application



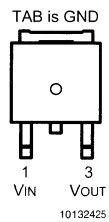
10132401

* Required if regulator is located more than 2" from power supply filter capacitor.

** Required for stability. Must be rated for 22 µF minimum over intended operating temperature range. Effective series resistance (ESR) is critical, see curve. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Connection Diagrams

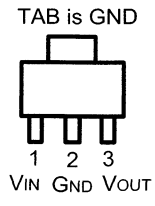
TO-252



10132425

Top View
Order Number LM2936DT-3.3
See NS Package Number TD03B

SOT-223

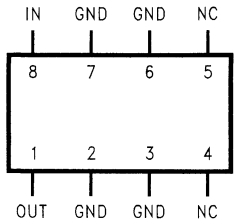


10132426

Top View
Order Number LM2936MP-3.3
See NS Package Number MA04A

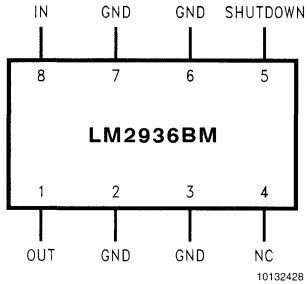
Connection Diagrams (Continued)

8-Pin SO (M)



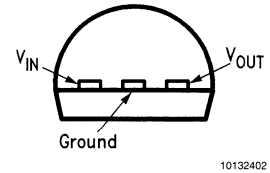
Top View
Order Number LM2936M-3.3
See NS Package Number M08A

8-Pin SO (M)



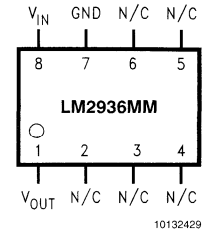
Top View
Order Number LM2936BM-3.3
See NS Package Number M08A

TO-92



Bottom View
Order Number LM2936Z-3.3
See NS Package Number Z03A

8-Pin Mini SOIC (MM)



Top View
Order Number LM2936MM-3.3
See NS Package Number MUA08A

National Semiconductor

LM2936-5.0
Ultra-Low Quiescent Current 5V Regulator

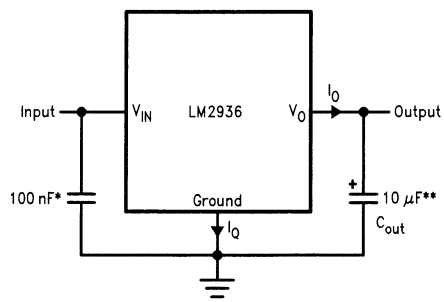
General Description

The LM2936 ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 15 µA quiescent current at a 100 µA load, the LM2936 is ideally suited for automotive and other battery operated systems. The LM2936 retains all of the features that are common to low dropout regulators including a low dropout PNP pass device, short circuit protection, reverse battery protection, and thermal shutdown. The LM2936 has a 40V maximum operating voltage limit, a −40˚C to +125˚C operating temperature range, and ±3% output voltage tolerance over the entire output current, input voltage, and temperature range. The LM2936 is available in a TO-92 package, a SO-8 surface mount package, and a TO-252 surface mount power package.

Features

- Ultra low quiescent current ($I_Q \leq 15$ µA for $I_O = 100$ µA)
- Fixed 5V, 50 mA output
- ±2% Initial output tolerance
- ±3% Output tolerance over line, load, and temperature
- Dropout voltage typically 200 mV @ $I_O = 50$ mA
- Reverse battery protection
- −50V reverse transient protection
- Internal short circuit current limit
- Internal thermal shutdown protection
- 40V operating voltage limit
- 60V operating voltage limit for LM2936HV
- Shutdown Pin available with LM2936BM package

Typical Application



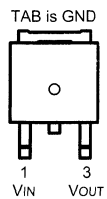
00975901

* Required if regulator is located more than 2" from power supply filter capacitor.

** Required for stability. Must be rated for 10 µF minimum over intended operating temperature range. Effective series resistance (ESR) is critical, see curve. Locate capacitor as close as possible to the regulator output and ground pins. Capacitance may be increased without bound.

Connection Diagrams

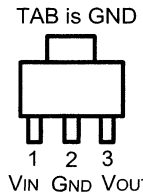
TO-252



00975925

Top View
Order Number LM2936DT-5.0
See NS Package Number TD03B

SOT-223

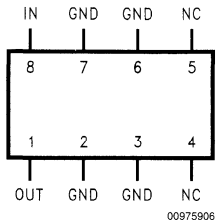


00975926

Top View
Order Number LM2936MP-5.0
See NS Package Number MA04A

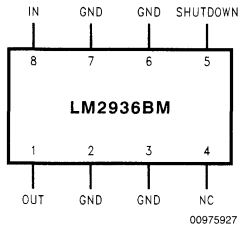
Connection Diagrams (Continued)

8-Pin SO (M)



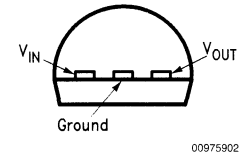
Top View
Order Number LM2936M-5.0, LM2936HVMA-5.0
See NS Package Number M08A

8-Pin SO (M)



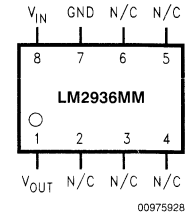
Top View
Order Number LM2936BM-5.0
See NS Package Number M08A

TO-92



Bottom View
Order Number LM2936Z-5.0
See NS Package Number Z03A

8-Pin Mini SOIC (MM)



Top View
Order Number LM2936MM-5.0
See NS Package Number MUA08A

National Semiconductor

LM2937
500 mA Low Dropout Regulator

General Description

The LM2937 is a positive voltage regulator capable of supplying up to 500 mA of load current. The use of a PNP power transistor provides a low dropout voltage characteristic. With a load current of 500 mA the minimum input to output voltage differential required for the output to remain in regulation is typically 0.5V (1V guaranteed maximum over the full operating temperature range). Special circuitry has been incorporated to minimize the quiescent current to typically only 10 mA with a full 500 mA load current when the input to output voltage differential is greater than 3V.

The LM2937 requires an output bypass capacitor for stability. As with most low dropout regulators, the ESR of this capacitor remains a critical design parameter, but the LM2937 includes special compensation circuitry that relaxes ESR requirements. The LM2937 is stable for all ESR below 3Ω. This allows the use of low ESR chip capacitors.

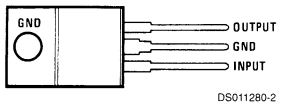
Ideally suited for automotive applications, the LM2937 will protect itself and any load circuitry from reverse battery connections, two-battery jumps and up to +60V/−50V load dump transients. Familiar regulator features such as short circuit and thermal shutdown protection are also built in.

Features

- Fully specified for operation over −40°C to +125°C
- Output current in excess of 500 mA
- Output trimmed for 5% tolerance under all operating conditions
- Typical dropout voltage of 0.5V at full rated load current
- Wide output capacitor ESR range, up to 3Ω
- Internal short circuit and thermal overload protection
- Reverse battery protection
- 60V input transient protection
- Mirror image insertion protection

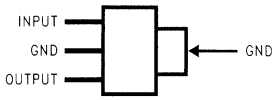
Connection Diagrams and Ordering Information

TO-220 Plastic Package



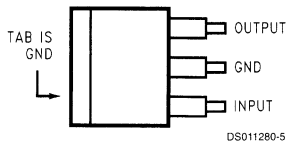
Front View
Order Number LM2937ET-5.0, LM2937ET-8.0, LM2937ET-10, LM2937ET-12 or LM2937ET-15
See NS Package Number T03B

SOT-223 Plastic Package

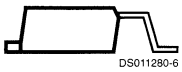


Front View
Order Number LM2937IMP-5.0, LM2937IMP-8.0, LM2937IMP-10, LM2937IMP-12 or LM2937IMP-15
See NS Package Number MP04A

TO-263 Surface-Mount Package



Top View



Side View

Order Number LM2937ES-5.0, LM2937ES-8.0, LM2937ES-10, LM2937ES-12 or LM2937ES-15
See NS Package Number TS3B

Connection Diagrams and Ordering Information (Continued)

Temperature Range	Output Voltage					NSC Package Drawing	Package
	5.0	8.0	10	12	15		
$-40^{\circ}C \leq T_J \leq 125^{\circ}C$	LM2937ES-5.0	LM2937ES-8.0	LM2937ES-10	LM2937ES-12	LM2937ES-15	TS3B	TO-263
	LM2937ET-5.0	LM2937ET-8.0	LM2937ET-10	LM2937ET-12	LM2937ET-15	T03B	TO-220
$-40^{\circ}C \leq T_J \leq 85^{\circ}C$	LM2937IMP-5.0	LM2937IMP-8.0	LM2937IMP-10	LM2937IMP-12	LM2937IMP-15	MP04A	SOT-223
	LM2937IMPX-5.0	LM2937IMPX-8.0	LM2937IMPX-10	LM2937IMPX-12	LM2937IMPX-15	MP04A	SOT-223 in Tape and Reel
SOT-223 Package Markings	L71B	L72B	L73B	L74B	L75B		

The small physical size of the SOT-223 package does not allow sufficient space to provide the complete device part number. The actual devices will be labeled with the package markings shown.

National Semiconductor

LM2937-2.5, LM2937-3.3
400mA and 500mA Voltage Regulators

General Description

The LM2937-2.5 and LM2937-3.3 are positive voltage regulators capable of supplying up to 500 mA of load current. Both regulators are ideal for converting a common 5V logic supply, or higher input supply voltage, to the lower 2.5V and 3.3V supplies to power VLSI ASIC's and microcontrollers. Special circuitry has been incorporated to minimize the quiescent current to typically only 10 mA with a full 500 mA load current when the input to output voltage differential is greater than 5V.

The LM2937 requires an output bypass capacitor for stability. As with most regulators utilizing a PNP pass transistor, the ESR of this capacitor remains a critical design parameter, but the LM2937-2.5 and LM2937-3.3 include special compensation circuitry that relaxes ESR requirements. The LM2937 is stable for all ESR ratings less than 5Ω. This allows the use of low ESR chip capacitors.

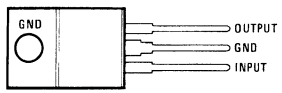
The regulators are also suited for automotive applications, with built in protection from reverse battery connections, two-battery jumps and up to +60V/−50V load dump transients. Familiar regulator features such as short circuit and thermal shutdown protection are also built in.

Features

- Fully specified for operation over −40°C to +125°C
- Output current in excess of 500 mA (400mA for SOT-223 package)
- Output trimmed for 5% tolerance under all operating conditions
- Wide output capacitor ESR range, 0.01Ω up to 5Ω
- Internal short circuit and thermal overload protection
- Reverse battery protection
- 60V input transient protection
- Mirror image insertion protection

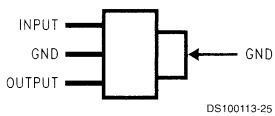
Connection Diagrams and Ordering Information

TO-220 Plastic Package



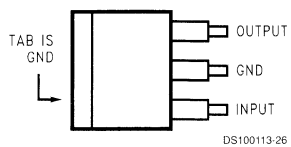
Front View
Order Number LM2937ET-2.5, LM2937ET-3.3,
See NS Package Number T03B

SOT-223 Plastic Package

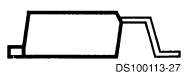


Front View
Order Number LM2937IMP-2.5, LM2937IMP-3.3,
See NS Package Number MA04A

TO-263 Surface-Mount Package



Top View



Side View

Order Number LM2937ES-2.5, LM2937ES-3.3,
See NS Package Number TS3B

Connection Diagrams and Ordering Information (Continued)

Temperature Range	Output Voltage		NSC Package Drawing	Package
	2.5	3.3		
$-40^{\circ}C \leq T_A \leq 125^{\circ}C$	LM2937ES-2.5	LM2937ES-3.3	TS3B	TO-263
	LM2937ET-2.5	LM2937ET-3.3	T03B	TO-220
$-40^{\circ}C \leq T_A \leq 85^{\circ}C$	LM2937IMP-2.5	LM2937IMP-3.3	MA04A	SOT-223
SOT-223 Package Markings	L68B	L69B		

The small physical size of the SOT-223 package does not allow sufficient space to provide the complete device part number. The actual devices will be labeled with the package markings shown.

National Semiconductor

LM2940/LM2940C
1A Low Dropout Regulator

General Description

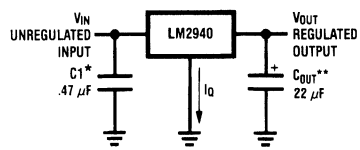
The LM2940/LM2940C positive voltage regulator features the ability to source 1A of output current with a dropout voltage of typically 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

Designed also for vehicular applications, the LM2940/LM2940C and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. The LM2940/LM2940C cannot be harmed by temporary mirror-image insertion. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- Dropout voltage typically 0.5V @I_O = 1A
- Output current in excess of 1A
- Output voltage trimmed before assembly
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- P+ Product Enhancement tested

Typical Application



*Required if regulator is located far from power supply filter.

**C_{OUT} must be at least 22 μF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

Ordering Information

Temperature Range	Output Voltage						Package
	5.0	8.0	9.0	10	12	15	
0°C ≤ T_J ≤ 125°C	LM2940CT-5.0		LM2940CT-9.0		LM2940CT-12	LM2940CT-15	TO-220
	LM2940CS-5.0		LM2940CS-9.0		LM2940CS-12	LM2940CS-15	TO-263
−40°C ≤ T_J ≤ 125°C	LM2940T-5.0	LM2940T-8.0	LM2940T-9.0	LM2940T-10	LM2940T-12		TO-220
	LM2940S-5.0	LM2940S-8.0	LM2940S-9.0	LM2940S-10	LM2940S-12		TO-263
−40°C ≤ T_J ≤ 85°C	LM2940IMP-5.0	LM2940IMP-8.0	LM2940IMP-9.0	LM2940IMP-10	LM2940IMP-12	LM2940IMP-15	SOT-223
	LM2940IMPX-5.0	LM2940IMPX-8.0	LM2940IMPX-9.0	LM2940IMPX-10	LM2940IMPX-12	LM2940IMPX-15	SOT-223 in Tape and Reel
SOT-223 Package Marking	L53B	L54B	L0EB	L55B	L56B	L70B	

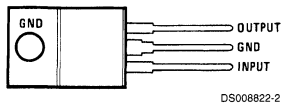
The physical size of the SOT-223 is too small to contain the full device part number. The package markings indicated are what will appear on the actual device.

Temperature Range	Output Voltage				Package
	5.0	8.0	12	15	
−55°C ≤ T_J ≤ 125°C	LM2940J-5.0/883 5962-8958701EA	LM2940J-8.0/883 5962-9088301QEA	LM2940J-12/883 5962-9088401QEA	LM2940J-15/883 5962-9088501QEA	J16A
	LM2940WG5.0/883 5962-8958701XA				WG16A

For information on military temperature range products, please go to the Mil/Aero Web Site at http://www.national.com/appinfo/milaero/index.html.

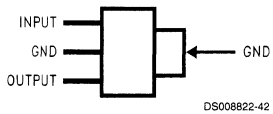
Connection Diagrams

(TO-220) Plastic Package



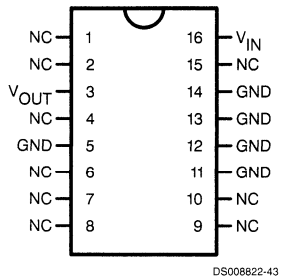
Front View
Order Number LM2940CT-5.0, LM2940CT-9.0, LM2940CT-12, LM2940CT-15, LM2940T-5.0, LM2940T-8.0, LM2940T-9.0, LM2940T-10 or LM2940T-12
See NS Package Number TO3B

3-Lead SOT-223



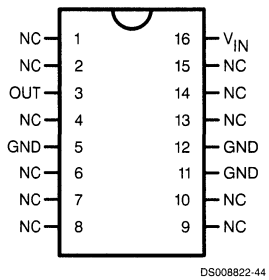
Front View
Order Part Number LM2940IMP-5.0, LM2940IMP-8.0, LM2940IMP-9.0, LM2940IMP-10, LM2940IMP-12 or LM2940IMP-15
See NS Package Number MP04A

16-Lead Dual-in-Line Package (J)



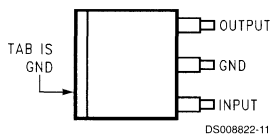
Top View
Order Number LM2940J-5.0/883 (5962-8958701EA), LM2940J-8.0/883 (5962-9088301QEA), LM2940J-12/883 (5962-9088401QEA), LM2940J-15/883 (5962-9088501QEA)
See NS Package Number J16A

16-Lead Ceramic Surface-Mount Package (WG)



Top View
Order Number LM2940WG5.0/883 (5962-8958701XA)
See NS Package Number WG16A

(TO-263) Surface-Mount Package



Top View

Side View
Order Number LM2940CS-5.0, LM2940CS-9.0, LM2940CS-12, LM2940CS-15, LM2940S-5.0, LM2940S-8.0, LM2940S-9.0, LM2940S-10 or LM2940S-12
See NS Package Number TS3B

National Semiconductor

LM2941/LM2941C
1A Low Dropout Adjustable Regulator

General Description

The LM2941 positive voltage regulator features the ability to source 1A of output current with a typical dropout voltage of 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground pin current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30 mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

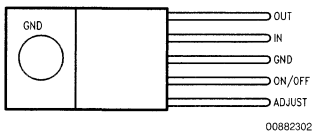
Designed also for vehicular applications, the LM2941 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- LLP space saving package
- Output voltage adjustable from 5V to 20V
- Dropout voltage typically 0.5V @ I_O = 1A
- Output current in excess of 1A
- Trimmed reference voltage
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- P^+ Product Enhancement tested
- TTL, CMOS compatible ON/OFF switch

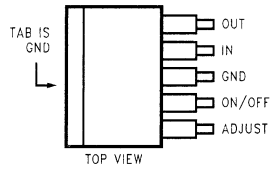
Connection Diagrams and Ordering Information

TO-220 Plastic Package

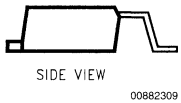


Tep View
Order Number LM2941T or LM2941CT
See NS Package Number TO5A

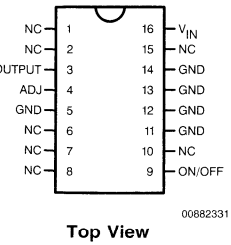
TO-263 Surface-Mount Package



Order Number LM2941S or LM2941CS
See NS Package Number TS5B

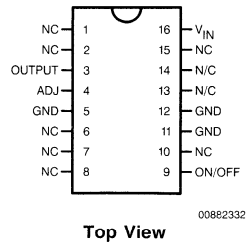


16-Lead Ceramic Dual-in-Line Package



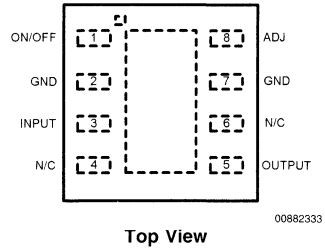
Top View
Order Number LM2941J/883
5962-9166701QEA
See NS Package Number J16A

16-Lead Ceramic Surface Mount Package



Top View
Order Number LM2941WG/883
5962-9166701QYA
See NS Package Number WG16A

8-Lead LLP Surface Mount Package



Top View
Ordering Number LM2941LD
See NS Package Number LDC08A

National Semiconductor

LM2984
Microprocessor Power Supply System

General Description

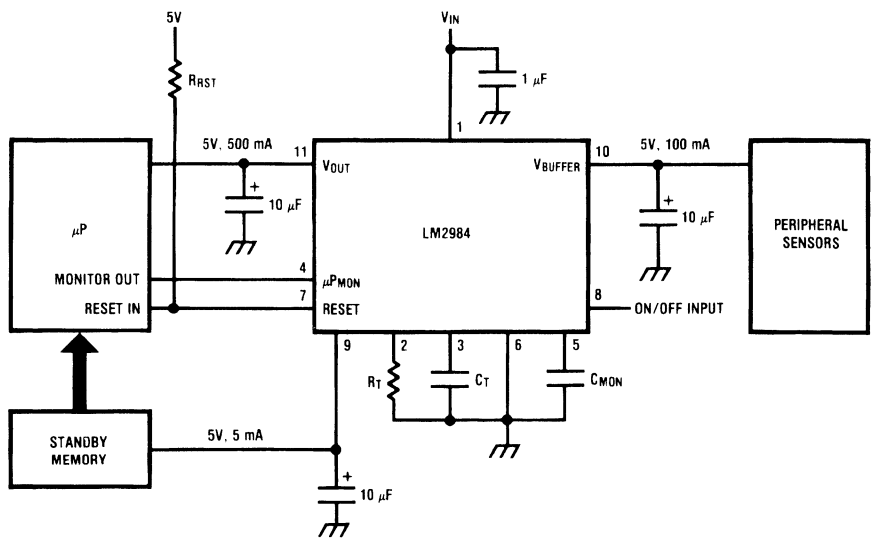
The LM2984 positive voltage regulator features three independent and tracking outputs capable of delivering the power for logic circuits, peripheral sensors and standby memory in a typical microprocessor system. The LM2984 includes circuitry which monitors both its own high-current output and also an external µP. If any error conditions are sensed in either, a reset error flag is set and maintained until the malfunction terminates. Since these functions are included in the same package with the three regulators, a great saving in board space can be realized in the typical microprocessor system. The LM2984 also features very low dropout voltages on each of its three regulator outputs (0.6V at the rated output current). Furthermore, the quiescent current can be reduced to 1 mA in the standby mode.

Designed also for vehicular applications, the LM2984 and all regulated circuitry are protected from reverse battery installations or 2-battery jumps. Familiar regulator features such as short circuit and thermal overload protection are also provided. Fixed outputs of 5V are available in the plastic TO-220 power package.

Features

- Three low dropout tracking regulators
- Output current in excess of 500 mA
- Fully specified for −40°C to +125°C operation
- Low quiescent current standby regulator
- Microprocessor malfunction RESET flag
- Delayed RESET on power-up
- Accurate pretrimmed 5V outputs
- Reverse battery protection
- Overvoltage protection
- Reverse transient protection
- Short circuit protection
- Internal thermal overload protection
- ON/OFF switch for high current outputs
- P+ Product Enhancement tested

Typical Application Circuit



DS011252-1

C_{OUT} must be at least 10 µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator. The equivalent series resistance (ESR) of this capacitor is critical; see curve.

Order Number LM2984T
See NS Package Number TA11B

National Semiconductor

LM2990
Negative Low Dropout Regulator

General Description

The LM2990 is a three-terminal, low dropout, 1 ampere negative voltage regulator available with fixed output voltages of −5, −5.2, −12, and −15V.

The LM2990 uses new circuit design techniques to provide low dropout and low quiescent current. The dropout voltage at 1A load current is typically 0.6V and a guaranteed worst-case maximum of 1V over the entire operating temperature range. The quiescent current is typically 1 mA with 1A load current and an input-output voltage differential greater than 3V. A unique circuit design of the internal bias supply limits the quiescent current to only 9 mA (typical) when the regulator is in the dropout mode ($V_{OUT} - V_{IN} \leq 3V$). Output voltage accuracy is guaranteed to ±5% over load, and temperature extremes.

The LM2990 is short-circuit proof, and thermal shutdown includes hysteresis to enhance the reliability of the device when overloaded for an extended period of time. The LM2990 is available in a 3-lead TO-220 package and is rated for operation over the automotive temperature range of −40°C to +125°C.

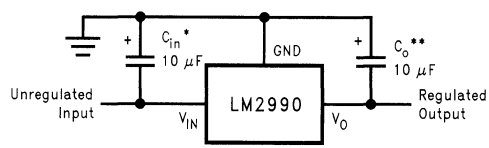
Features

- 5% output accuracy over entire operating range
- Output current in excess of 1A
- Dropout voltage typically 0.6V at 1A load
- Low quiescent current
- Internal short circuit current limit
- Internal thermal shutdown with hysteresis
- Functional complement to the LM2940 series

Applications

- Post switcher regulator
- Local, on-card, regulation
- Battery operated equipment

Typical Application



DS010801-1

*Required if the regulator is located further than 6 inches from the power supply filter capacitors. A 1 μF solid tantalum or a 10 μF aluminum electrolytic capacitor is recommended.

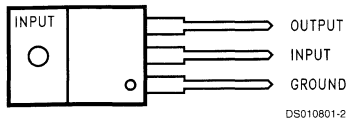
**Required for stability. Must be at least a 10 μF aluminum electrolytic or a 1 μF solid tantalum to maintain stability. May be increased without bound to maintain regulation during transients. Locate the capacitor as close as possible to the regulator. The equivalent series resistance (ESR) is critical, and should be less than 10Ω over the same operating temperature range as the regulator.

Ordering Information and Connection Diagrams

Temperature Range	Output Voltage				Package
	-5.0	-5.2	-12	-15	
−40°C to +125°C	LM2990T-5.0	LM2990T-5.2	LM2990T-12	LM2990T-15	TO-220
	LM2990S-5.0		LM2990S-12	LM2990S-15	TO-263
−55°C to +125°C	LM2990J-5.0-QML 5962-9571101QEA		LM2990J-12-QML 5962-9571001QEA	LM2990J-15-QML 5962-9570901QEA	J16A
	LM2990WG5.0-QML 5962-9571101QXA				WG16A

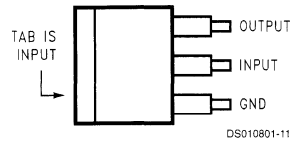
Ordering Information and Connection Diagrams (Continued)

3-Lead TO-220



Front View
Order Number LM2990T-5.0, LM2990T-5.2, LM2990T-12 or LM2990T-15
See NS Package Number T03B

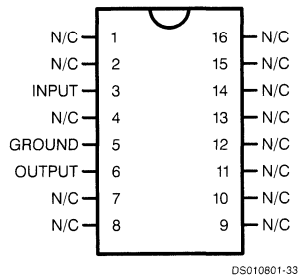
TO-263 Surface-Mount Package



Top View

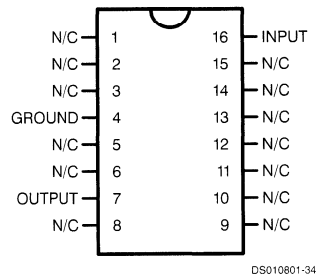
Side View
Order Number LM2990S-5.0, LM2990S-12 or LM2990S-15
See NS Package Number TS3B

16-Lead Ceramic Dual-in-Line Package



Top View
Order Number
LM2990J-5.0-QML (5962-9571101QEA), LM2990J-12-QML (5962-9571001QEA), or LM2990J-15-QML (5962-9570901QEA),
See NS Package Number J16A

16-Lead Ceramic Surface Mount Package



Top View
Order Number
LM2990WG5.0-QML (5962-9571101QXEA)
See NS Package Number WG16A

National Semiconductor

LM2991
Negative Low Dropout Adjustable Regulator

General Description

The LM2991 is a low dropout adjustable negative regulator with a output voltage range between −3V to −24V. The LM2991 provides up to 1A of load current and features a $\overline{\text{On}}$ /Off pin for remote shutdown capability.

The LM2991 uses new circuit design techniques to provide a low dropout voltage, low quiescent current and low temperature coefficient precision reference. The dropout voltage at 1A load current is typically 0.6V and a guaranteed worst-case maximum of 1V over the entire operating temperature range. The quiescent current is typically 1 mA with a 1A load current and an input-output voltage differential greater than 3V. A unique circuit design of the internal bias supply limits the quiescent current to only 9 mA (typical) when the regulator is in the dropout mode ($V_{OUT} - V_{IN} \leq 3V$).

The LM2991 is short-circuit proof, and thermal shutdown includes hysteresis to enhance the reliability of the device when inadvertently overloaded for extended periods. The LM2991 is available in 5-lead TO-220 and TO-263 packages and is rated for operation over the automotive temperature range of −40°C to +125°C. Mil-Aero versions are also available.

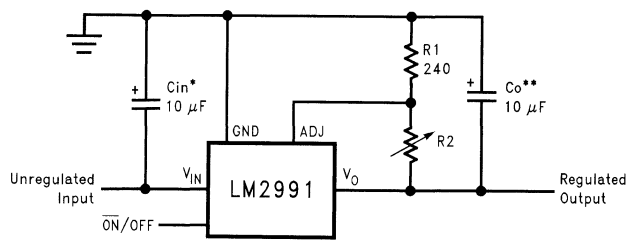
Features

- Output voltage adjustable from −3V to −24V, typically −2V to −25V
- Output current in excess of 1A
- Dropout voltage typically 0.6V at 1A load
- Low quiescent current
- Internal short circuit current limit
- Internal thermal shutdown with hysteresis
- TTL, CMOS compatible $\overline{\text{ON}}$/OFF switch
- Functional complement to the LM2941 series

Applications

- Post switcher regulator
- Local, on-card, regulation
- Battery operated equipment

Typical Application



DS011260-1

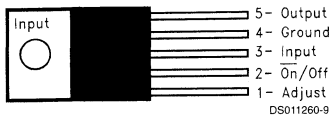
$V_{OUT} = V_{REF} (1 + R2/R1)$

*Required if the regulator is located further than 6 inches from the power supply filter capacitors. A 1 µF solid tantalum or a 10 µF aluminum electrolytic capacitor is recommended.

**Required for stability. Must be at least a 10 µF aluminum electrolytic or a 1 µF solid tantalum to maintain stability. May be increased without bound to maintain regulation during transients. Locate the capacitor as close as possible to the regulator. The equivalent series resistance (ESR) is critical, and should be less than 10Ω over the same operating temperature range as the regulator.

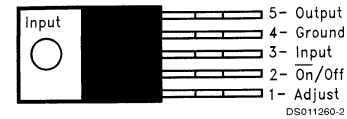
Connection Diagrams and Ordering Information

5-Lead TO-220
Straight Leads



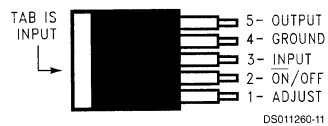
Front View
Order Number LM2991T
See NS Package Number T05A

5-Lead TO-220
Bent, Staggered Leads

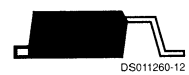


Front View
Order Number LM2991T Flow LB03
See NS Package Number T05D

TO263
5-Lead Surface-Mount Package

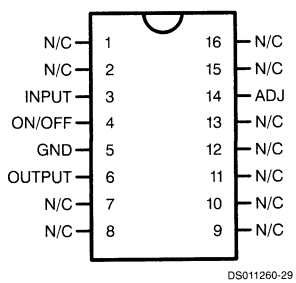


Top View



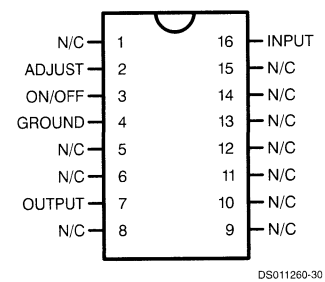
Side View
Order Number LM2991S
See NS Package Number TS5B

16-Lead Ceramic Dual-in-Line Package



Top View
Order Number LM2991J-QMLV
5962-9650501VEA
Order Number LM2991J-QML
5962-9650501QEA
See NS Package Number J16A

16-Lead Ceramic Surface-Mount Package



Top View
Order Number LM2991WG-QML
5962-9650501QXA
See NS Package Number WG16A

National Semiconductor

LM3460-1.2, -1.5
Precision Controller for GTLp and GTL Bus Termination

General Description

The LM3460 is a monolithic integrated circuit designed for precision control of GTLplus and GTL Bus termination. This controller is available in a tiny SOT23-5 package, and includes an internally compensated op amp, a bandgap reference, an NPN output transistor, and voltage setting resistors.

A trimmed precision bandgap voltage reference utilizes temperature drift curvature correction for excellent voltage stability over the operating range. The precision output control enables the termination voltage to maintain tight regulation, despite fast switching requirements on the bus.

The LM3460 controller is designed to be used with a high current (> 7A) NPN pass transistor to provide the high current needed for the bus termination. The wide bandwidth of the feedback loop provides excellent transient response, and greatly reduces the output capacitance required, thus reducing cost and board space requirements.

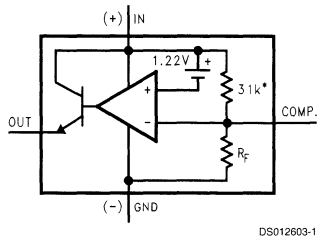
Features

- Precision output (1%)
- Output voltage can be adjusted
- Extremely fast transient response in GTLp and GTL bus termination
- Tiny SOT23-5 package
- Output voltage capability for GTL or GTLp
- Low temperature coefficient

Applications

- GTL bus termination (1.2V output @ 7A)
- GTLp bus termination (1.5V output @ 7A)
- Adjustable high-current linear regulator

Connection Diagrams and Package Information

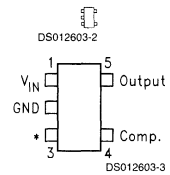


*This resistor is not used on the LM3460-1.2.

LM3460 Functional Diagram

5-Lead Outline Package (M5)

Actual Size



*No internal connection, but should be soldered to PC board for best heat transfer.

Top View

See NS package Number MF05A

Ordering Information

Voltage	Order Number	Package Marking	Supplied As
1.5	LM3460M5-1.5	D06A	1000 Unit Increments on Tape and Reel
1.5	LM3460M5X-1.5	D06A	3000 Unit Increments on Tape and Reel
1.2	LM3460M5-1.2	D09A	1000 Unit Increments on Tape and Reel
1.2	LM3460M5X-1.5	D09A	3000 Unit Increments on Tape and Reel

MARKING CODE: The first letter 'D' identifies the part as a Driver, and the next two numbers define the voltage for the part. The fourth letter indicates the grade, with 'A' designating the prime grade of product.

AVAILABILITY: The SOT23-5 package is only available in quantity of 1000 on tape and reel (designated by the letters 'M5' in the part number), or in quantity of 3000 on tape and reel (indicated by the letters 'M5X' in the part number).

Typical Applications

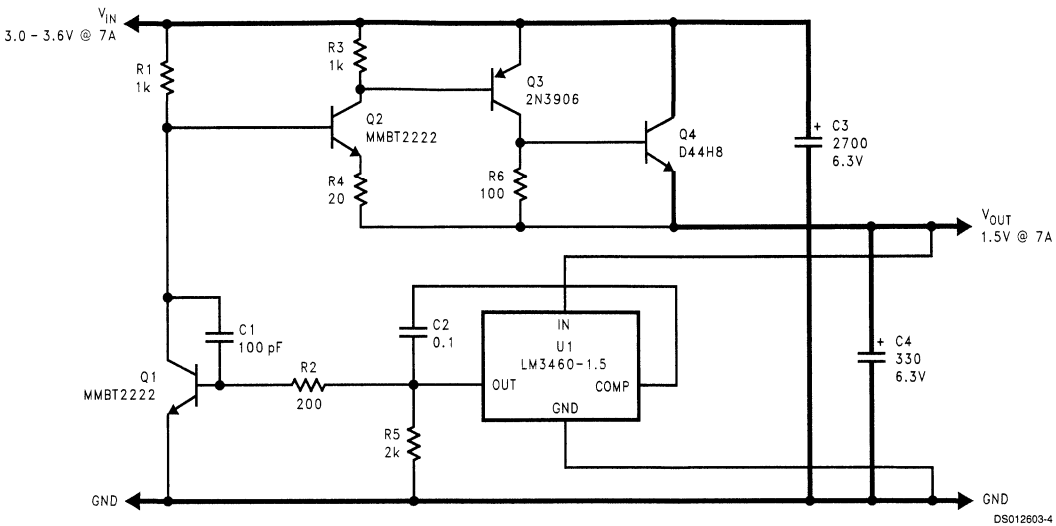


FIGURE 1. 1.5V Typical Application (See Application Information Section)

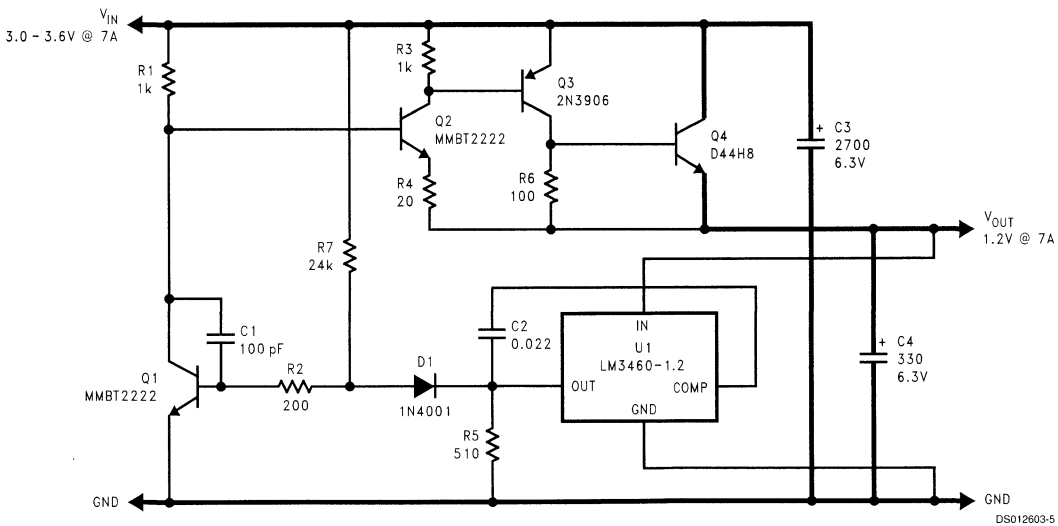


FIGURE 2. 1.2V Typical Application (See Application Information Section)

16

National Semiconductor

LM3480
100 mA, SOT-23, Quasi Low-Dropout Linear Voltage Regulator

General Description

The LM3480 is an integrated linear voltage regulator. It features operation from an input as high as 30V and a guaranteed maximum dropout of 1.2V at the full 100 mA load. Standard packaging for the LM3480 is the 3-lead SuperSOT® package.

The 5, 12, and 15V members of the LM3480 series are intended as tiny alternatives to industry standard LM78LXX series and similar devices. The 1.2V quasi low dropout of LM3480 series devices makes them a nice fit in many applications where the 2 to 2.5V dropout of LM78LXX series devices precludes their (LM78LXX series devices) use.

The LM3480 series features a 3.3V member. The SOT packaging and quasi low dropout features of the LM3480 series converge in this device to provide a very nice, very tiny 3.3V, 100 mA bias supply that regulates directly off the system 5V±5% power supply.

Key Specifications

- 30V maximum input for operation
- 1.2V guaranteed maximum dropout over full load and temperature ranges
- 100 mA guaranteed minimum load current
- ±5% guaranteed output voltage tolerance over full load and temperature ranges
- −40 to +125˚C junction temperature range for operation

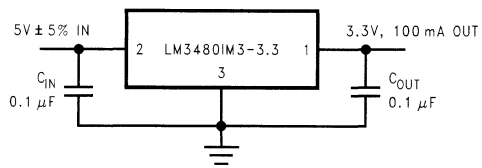
Features

- 3.3, 5, 12, and 15V versions available
- Packaged in the tiny 3-lead SuperSOT package

Applications

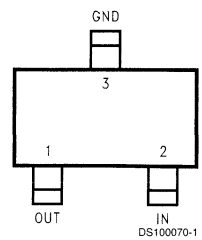
- Tiny alternative to LM78LXX series and similar devices
- Tiny 5V±5% to 3.3V, 100 mA converter
- Post regulator for switching DC/DC converter
- Bias supply for analog circuits

Typical Application Circuit



DS100070-2

Connection Diagram



DS100070-1

Top View
SOT-23 Package
3-Lead, Molded-Plastic Small-Outline Transistor (SOT) Package
Package Code MF03A (Note 1)

Ordering Information

Output Voltage (V)	Order Number (Note 2)	Package Marking (Note 3)	Comments
3.3	LM3480IM3-3.3	L0A	1000 Units on Tape and Reel
3.3	LM3480IM3X-3.3	L0A	3000 Units on Tape and Reel
5	LM3480IM3-5.0	L0B	1000 Units on Tape and Reel
5	LM3480IM3X-5.0	L0B	3000 Units on Tape and Reel
12	LM3480IM3-12	L0C	1000 Units on Tape and Reel
12	LM3480IM3X-12	L0C	3000Units on Tape and Reel
15	LM3480IM3-15	L0D	1000 Units on Tape and Reel
15	LM3480IM3X-15	L0D	3000 Units on Tape and Reel

National Semiconductor

LM3490
100 mA, SOT-23, Quasi Low-Dropout Linear Voltage Regulator with Logic-Controlled ON/$\overline{\text{OFF}}$

General Description

The LM3490 is an integrated linear voltage regulator. It features operation from an input as high as 30V and a guaranteed maximum dropout of 1.2V at the full 100 mA load. Standard packaging for the LM3490 is the 5-lead SOT-23 package. A logic-controlled ON/$\overline{\text{OFF}}$ feature makes the LM3490 ideal for powering subsystems ON and OFF as needed.

The 5, 12, and 15V members of the LM3490 series are intended as tiny alternatives to industry standard LM78LXX series and similar devices. The 1.2V quasi low dropout of LM3490 series devices makes them a nice fit in many applications where the 2 to 2.5V dropout of LM78LXX series devices precludes their (LM78LXX series devices) use.

The LM3490 series features a 3.3V member. The SOT packaging and quasi low dropout features of the LM3490 series converge in this device to provide a very nice, very tiny 3.3V, 100 mA bias supply that regulates directly off the system 5V±5% power supply.

Key Specifications

- 30V maximum input for operation
- 1.2V guaranteed maximum dropout over full load and temperature ranges
- 100 mA guaranteed load current
- ±5% guaranteed output voltage tolerance over full load and temperature ranges
- −40 to +125°C junction temperature range for operation

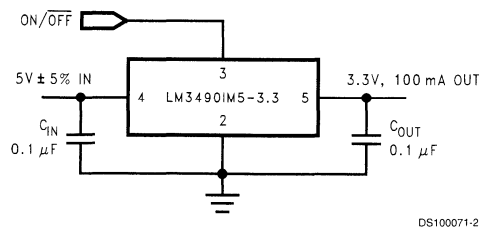
Features

- 3.3, 5, 12, and 15V versions available
- Logic-controlled ON/$\overline{\text{OFF}}$
- Packaged in the tiny 5-lead SOT-23 package

Applications

- Tiny alternative to LM78LXX series and similar devices
- Tiny 5V±5% to 3.3V, 100 mA converter
- Post regulator for switching DC/DC converter
- Bias supply for analog circuits

Typical Application Circuit



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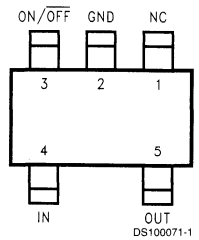
Connection Diagram



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Top View
SOT-23 Package
5-Lead, Molded-Plastic Small-Outline Transistor (SOT) Package
Package Code MF05A(Note 1)

Ordering Information

Output Voltage (V)	Order Number (Note 2)	Package Marking (Note 3)	Comments
3.3	LM3490IM5-3.3	L78B	1000 Units on Tape and Reel
3.3	LM3490IM5X-3.3	L78B	3000 Units on Tape and Reel
5	LM3490IM5-5.0	L79B	1000 Units on Tape and Reel
5	LM3490IM5X-5.0	L79B	3000 Units on Tape and Reel
12	LM3490IM5-12	L80B	1000 Units on Tape and Reel
12	LM3490IM5X-12	L80B	3000 Units on Tape and Reel
15	LM3490IM5-15	L81B	1000 Units on Tape and Reel
15	LM3490IM5X-15	L81B	3000 Units on Tape and Reel

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LM3940
1A Low Dropout Regulator for 5V to 3.3V Conversion

General Description

The LM3940 is a 1A low dropout regulator designed to provide 3.3V from a 5V supply.

The LM3940 is ideally suited for systems which contain both 5V and 3.3V logic, with prime power provided from a 5V bus.

Because the LM3940 is a true low dropout regulator, it can hold its 3.3V output in regulation with input voltages as low as 4.5V.

The T0-220 package of the LM3940 means that in most applications the full 1A of load current can be delivered without using an additional heatsink.

The surface mount TO-263 package uses minimum board space, and gives excellent power dissipation capability when soldered to a copper plane on the PC board.

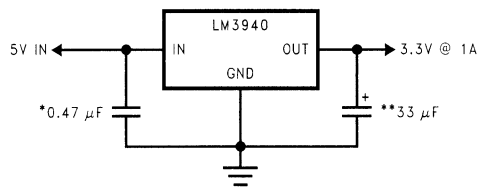
Features

- Output voltage specified over temperature
- Excellent load regulation
- Guaranteed 1A output current
- Requires only one external component
- Built-in protection against excess temperature
- Short circuit protected

Applications

- Laptop/Desktop Computers
- Logic Systems

Typical Application



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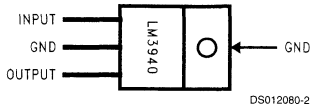
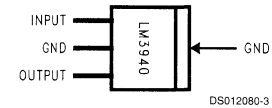
*Required if regulator is located more than 1" from the power supply filter capacitor or if battery power is used.
**See Application Hints.

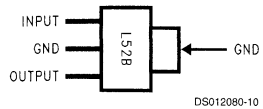
Connection Diagrams/Ordering Information



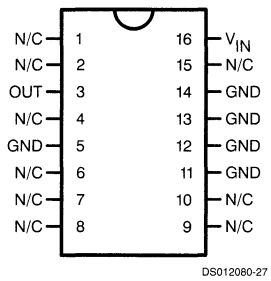
3-Lead TO-220 Package
(Front View)
Order Part Number LM3940IT-3.3
NSC Drawing Number TO3B



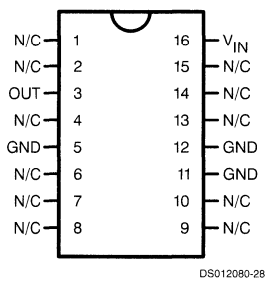
3-Lead TO-263 Package
(Front View)
Order Part Number LM3940IS-3.3
NSC Drawing Number TS3B



3-Lead SOT-223
(Front View)
Order Part Number LM3940IMP-3.3
Package Marked L52B
NSC Drawing Number MA04A



16-Lead Ceramic Dual-in-Line Package
(Top View)
Order Part Number LM3940J-3.3-QML
5962-9688401QEA
NSC Drawing Number J16A



16-Lead Ceramic Surface-Mount Package
(Top View)
Order Part Number LM3940WG-3.3-QML
5962-9688401QXA
NSC Drawing Number WG16A

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LM9070
Low-Dropout System Voltage Regulator with Keep-Alive ON/OFF Control

General Description

The LM9070 is a 5V, 3% accurate, 250 mA low-dropout voltage regulator. The regulator features an active low delayed reset output flag which can be used to reset a microprocessor system on turn-ON and in the event that the regulator output falls out of regulation for any reason. An external capacitor programs a delay time interval before the reset output can return high.

Designed for automotive application the LM9070 contains a variety of protection features such as reverse battery, over-voltage shutdown, thermal shutdown, input transient protection and a wide operating temperature range.

A unique two-input logic control scheme is used to enable or disable the regulator output. An ON/OFF input can be provided by an ignition switch derived signal while a second, Keep-Alive input, is generated by a system controller. This allows for a system to remain ON after ignition has been switched OFF. The system controller can then execute a power-down routine and after which command the regulator OFF to a low quiescent current state (60 µA max).

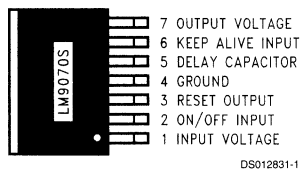
Design techniques have been employed to allow the regulator to remain operational and not generate false reset signals when subjected to high levels of RF energy (300V/m from 2 MHz to 400 MHz).

Features

- Automotive application reliability
- 3% output voltage tolerance
- Insensitive to radiated RFI
- Dropout voltage less than 800 mV with 250 mA output current
- Externally programmed reset delay interval
- Keep-alive feature with 2 logic control inputs
- 60V Load dump transient protection
- Thermal shutdown
- Short circuit protection and disable safety features
- Reverse battery protection
- Low OFF quiescent current, 50 µA maximum
- Wide operating temperature range −40°C to +125°C
- TO-263 and 20-pin power surface mount packages
- Lead form compatible with TLE4267 TO-220 regulator (package TA07D)

Connection Diagrams and Ordering Information (Top View)

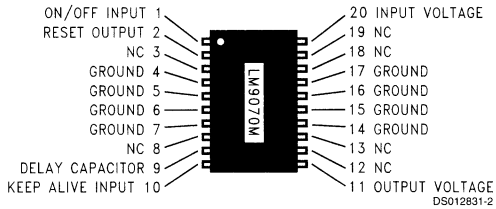
7-Lead TO-263
Surface Mount Package



Backside metal is internally connected to ground.

Order Number LM9070S
See NS Package Number TS7B

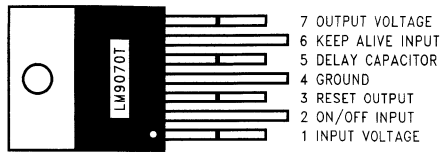
20-Pin SO Package



Order Number LM9070M
See NS Package Number M20B

Connection Diagrams and Ordering Information (Top View) (Continued)

7-Lead TO-220 Package
(Odd numbered pins bent forward away from package body)



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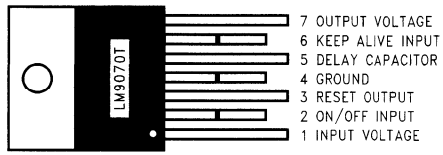
Tab is internally connected to ground.
Order Number LM9070T
See NS Package Number TA07B

7-Lead TO-220 Package
(Even numbered pins bent forward away from package body)



DS012831-4

Tab is internally connected to ground.
Order Number LM9070T/Flow LB09
See NS Package Number TA07D

National Semiconductor

LM9071
Low-Dropout System Voltage Regulator with Delayed Reset

General Description

The LM9071 is a 5V, 250 mA low-dropout voltage regulator. The regulator features an active low delayed reset output flag which can be used to reset a microprocessor system on turn-ON and in the event that the regulator output falls out of regulation for any reason. An external capacitor programs a delay time interval before the reset output can return high.

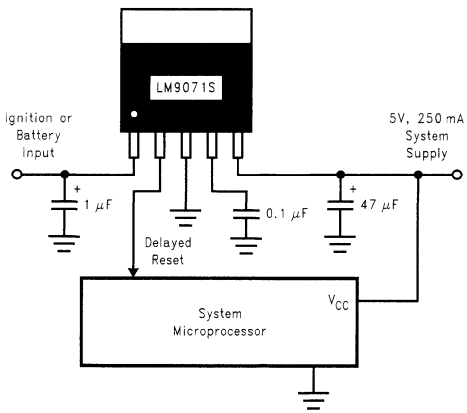
Designed for automotive application the LM9071 contains a variety of protection features such as reverse battery, over-voltage shutdown, thermal shutdown, input transient protection and a wide operating temperature range.

Design techniques have been employed to allow the regulator to remain operational and not generate false reset signals when subjected to high levels of RF energy (300V/m from 2 MHz to 400 MHz).

Features

- Automotive application reliability
- 3% output voltage tolerance
- Insensitive to radiated RFI
- Dropout voltage less than 800 mV with 250 mA output current
- Externally programmed reset delay interval
- Thermal shutdown
- Short circuit protection
- Reverse battery protection
- Wide operating temperature range −40˚C to +125˚C
- TO-220 and TO-263 power surface mount power packages
- Pin for pin compatible with the LM2927, L4947 and TLE4260

Typical Application and Connection Diagrams (Top View)



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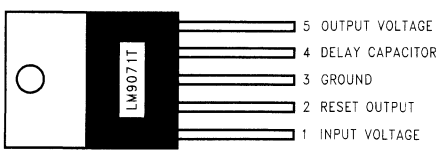
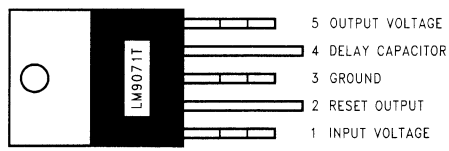
5-Lead TO-220 Package



DS012832-2

Order Number LM9071T
See NS Package Number T05A

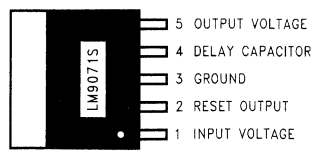
5-Lead TO-220 Package



DS012832-3

Order Number LM9071T/Flow LB03
See NS Package Number T05D

5-Lead TO-263 Surface Mount Package



DS012832-4

Tab and Backside metal on all packages internally connected to ground.

Order Number LM9071S
See NS Package Number TS5B

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LM9072
Dual Tracking Low-Dropout System Regulator

General Description

The LM9072 is a high performance voltage regulator system with operational and protection features that address many requirements of automotive applications. Two regulated outputs are provided. The main regulator provides a precision 2% maximum tolerance 5V output at 350 mA with a low dropout characteristic. The second regulator provides a 5V output that tracks the main regulator output voltage within 1.5% with load currents up to 80 mA. The tracking output is ideal for use in powering remotely located sensors with outputs that are ratiometric to the main system supply. This output is fully protected from short circuits to ground or the unregulated input supply (ignition or battery potentials in automotive applications).

The LM9072 also contains a programmable delayed system reset output. Two control inputs are provided. An ON/OFF input intended for connection to an ignition switch, and a Keep Alive input to allow a system to remain powered after ignition has been switched OFF.

For EMC concerns the LM9072 remains fully operational and does not generate false rest signals while subjected to, 1 MHz to 400 MHz bulk current injection signals greater than 100 mA on the input supply and tracking output lines.

Features

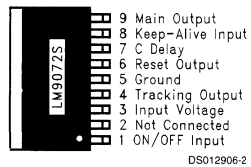
- Two 5V regulated outputs:
  — 350 mA, 2% Main output
  — 80 mA, 1.5% Tracking output
- Good EMI (1 MHz to 400 MHz, BCI) immunity
- Separate ON/OFF and Keep-Alive control inputs
- Less than 100 µA quiescent current in OFF state
- Programmable delayed reset output
- Input transient protection over 60V to −45V
- Tracking output protected from shorts to battery
- Less than 1V dropout at full load
- −40°C to +125°C operating temperature range
- Surface mount TO-263 Power Package and Standard TO-220 power package

Typical Applications

- Automotive module supply power conditioning
- Remote sensor biasing
- Ratiometric to supply sensor detection
- Continuous operation for save routines and EPROM programming after power down command
- Safety related systems—EMC operational

Connection Diagrams and Ordering Information

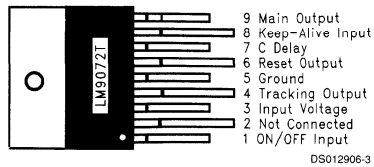
9-Lead TO-263
Surface Mount Power Package



Backside metal is internally connected to ground.

Order Number LM9072S
See NS Package Number TS9A

9-Lead TO-220 Package



Tab is internally connected to ground.

Order Number LM9072T
See NS Package Number TA9A

National Semiconductor

LM9073
Dual High Current Low-Dropout System Regulator

General Description

The LM9073 is a high performance voltage regulator system with operational and protection features that address many requirements of automotive applications. Two regulated outputs are provided. The main regulator provides a precision 2% tolerance 5V output at 700mA with a low dropout characteristic. The second output, an External Supply regulator, provides a 5V output with 2% tolerance for load currents up to 100mA. This External Supply output is fully protected from short circuit to ground or the unregulated input supply (ignition or battery potentials in automotive applications) which makes it suitable for powering remotely located load circuits or sub-systems.

The LM9073 also contains a programmable delayed system reset output. Two control inputs are provided. An ON/OFF input intended for connection to an ignition switch, and a Keep Alive input whereby a system can remain powered after ignition has been switched OFF. Additionally, a watchdog function is built in to enhance system operationally reliability.

For EMC concerns the LM9073 remains fully operational and does not generate false rest signals while subjected to greater than 100mA, 1MHz to 400MHz bulk current injection signals on the input supply and External Supply output lines.

Features

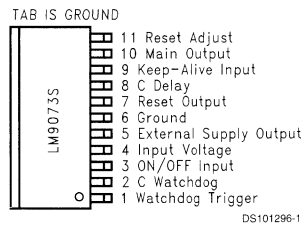
- Two 5V regulated outputs:
- 700mA, 2% Main output
- 100mA, 2% External Supply output
- External Supply output protected from shorts to battery
- Good EMI (1MHz to 400MHz, BCI) immunity
- Separate ON/OFF and Keep-Alive control inputs
- Less than 100µA quiescent current in OFF state
- Programmable delayed reset output
- Adjustable threshold voltage for generating reset
- Built-in system watchdog timer
- Input transient protection over 60V to −45V
- Less than 1V dropout at full load
- Wide −40°C to 125°C operating temperature range
- Surface mount, TO−263 and standard TO−220 power packages

Applications

- Automotive module supply power conditioning
- Remote sub−system powering
- Continuous operation for save routines and E^2PROM programing after power down command
- Safety relates systems − EMC operational with a system watchdog monitor

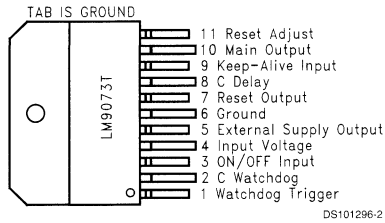
Connection Diagrams

11 Lead TO−263 Package



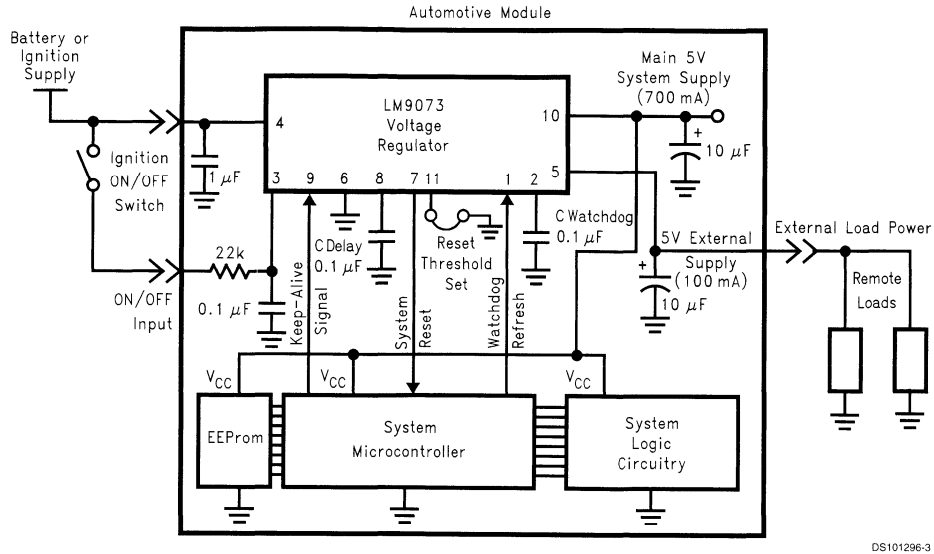
Top View
Order Number LM9073S
See NS Package Number TS11B

11 Lead TO−220 Package



Top View
Order Number LM9073T
See NS Package Number TA11B

Block Diagram



National Semiconductor

LMS1585A/LMS1587
5A and 3A Low Dropout Fast Response Regulators

General Description

The LMS1585A and LMS1587 are low dropout positive regulators with output load current of 5A and 3A respectively. Their low dropout voltage (1.2V) and fast transient response make them an excellent solution for low voltage microprocessor applications.

The LMS1585A/87 are available in adjustable versions, which can set the output voltage with only two external resistors. In addition, they are also available in 1.5V and 3.3V fixed voltage versions (Note 9).

The LMS1585A/87 circuits include a zener trimmed bandgap reference, current limiting and thermal shutdown.

The LMS1585A/87 series are available in TO-220 and TO-263 packages.

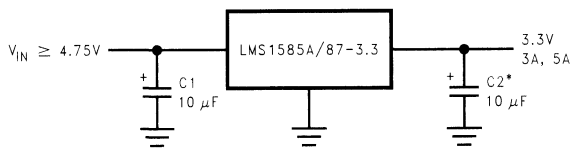
Features

- Fast transient response
- Available in Adjustable, 1.5V, and 3.3V versions
- Current limiting and thermal protection
- Commercial temp. range 0°C to 125°C
- Industrial temp. range −40°C to 125°C
- Line regulation 0.005% (typical)
- Load regulation 0.05% (typical)
- Direct replacement for LT™1585A/87

Applications

- Pentium™ processor supplies
- PowerPC™ supplies
- Other microprocessor supplies
- Low voltage logic supplies

Typical Application



* REQUIRED FOR STABILITY

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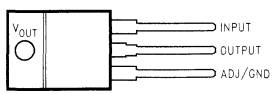
Connection Diagrams

TO-220



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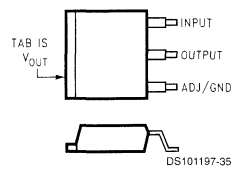
Top View

TO-263



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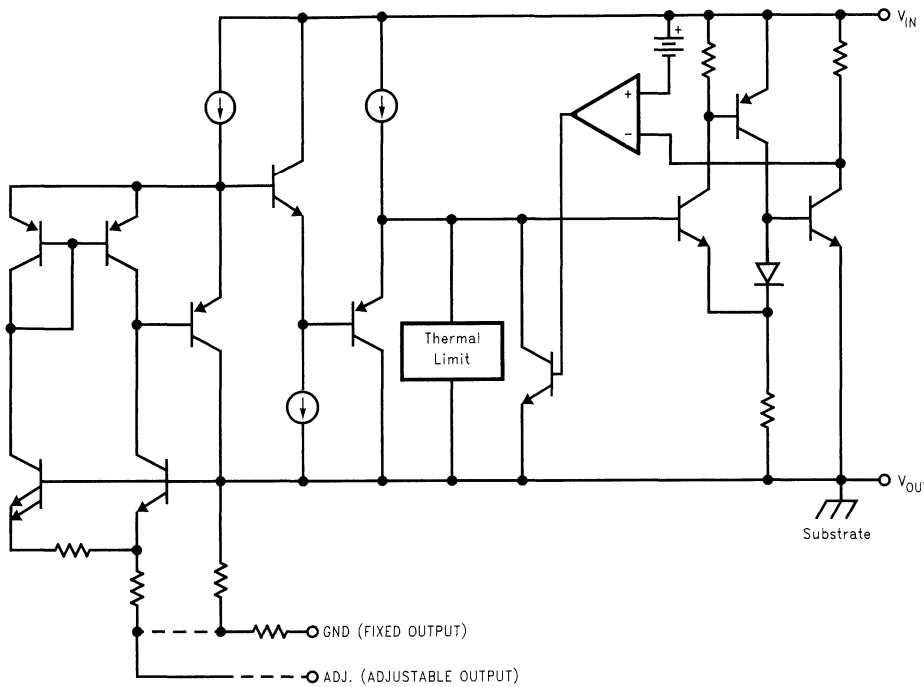
Top View

Ordering Information

Output Current	Package	Temperature Range	Part Number	Transport Media	NSC Drawing
3A	TO-263	0°C to 125°C	LMS1587CS-ADJ	Rails	TS3B
			LMS1587CSX-ADJ	Tape and Reel	
			LMS1587CS-1.5	Rails	
			LMS1587CSX-1.5	Tape and Reel	
			LMS1587CS-3.3	Rails	
			LMS1587CSX-3.3	Tape and Reel	
		−40°C to 125°C	LMS1587IS-ADJ	Rails	
			LMS1587ISX-ADJ	Tape and Reel	
			LMS1587IS-1.5	Rails	
			LMS1587ISX-1.5	Tape and Reel	
			LMS1587IS-3.3	Rails	
			LMS1587ISX-3.3	Tape and Reel	
	TO-220	0°C to 125°C	LMS1587CT-ADJ	Rails	T03B
			LMS1587CT-1.5	Rails	
			LMS1587CT-3.3	Rails	
		−40°C to 125°C	LMS1587IT-ADJ	Rails	
			LMS1587IT-1.5	Rails	
			LMS1587IT-3.3	Rails	
5A	TO-263	0°C to 125°C	LMS1585ACS-ADJ	Rails	TS3B
			LMS1585ACSX-ADJ	Tape and Reel	
			LMS1585ACS-1.5	Rails	
			LMS1585ACSX-1.5	Tape and Reel	
			LMS1585ACS-3.3	Rails	
			LMS1585ACSX-3.3	Tape and Reel	
		−40°C to 125°C	LMS1585AIS-ADJ	Rails	
			LMS1585AISX-ADJ	Tape and Reel	
			LMS1585AIS-1.5	Rails	
			LMS1585AISX-1.5	Tape and Reel	
			LMS1585AIS-3.3	Rails	
			LMS1585AISX-3.3	Tape and Reel	
	TO-220	0°C to 125°C	LMS1585ACT-ADJ	Rails	T03B
			LMS1585ACT-1.5	Rails	
			LMS1585ACT-3.3	Rails	
		−40°C to 125°C	LMS1585AIT-ADJ	Rails	
			LMS1585AIT-1.5	Rails	
			LMS1585AIT-3.3	Rails	

Simplified Schematic



DS101197-14

National Semiconductor

LMS5213
80mA, µCap, Low Dropout Voltage Regulator in SC70

General Description

The LMS5213 is a µCap, low dropout voltage regulator with very low quiescent current, 220µA typical, at 80mA load. It also has very low dropout voltage, typically 20mV at light load and 330mV at 80mA.

The LMS5213 provides up to 80mA and consumes a typical of 1µA in disable mode.

The LMS5213 is optimized to work with low value, low cost ceramic capacitors. The output typically require only 0.47µF of output capacitance for stability. The enable pin can be tied to V_{IN} for easy device layout.

The LMS5213 is designed for portable, battery powered equipment applications with small space requirements.

The LMS5213 is available in a space saving 5-pin SC70 package. Performance is specified for the −40°C to +125°C temperature range and is available in 2.8V, 3.0V and 3.3V fixed voltages. For other output voltage options, please contact National Semiconductor.

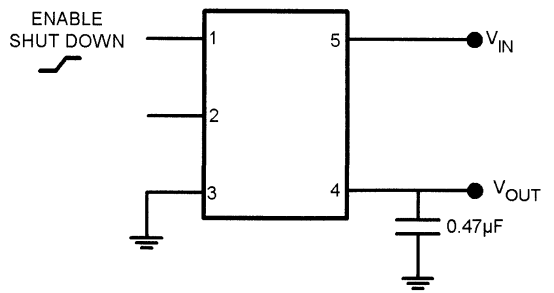
Features

- Space saving SC70 package
- Available in 2.8V, 3.0V, and 3.3V fixed voltages
- Guaranteed 80mA output
- Low quiescent current
- Low dropout voltage
- Low temperature coefficient
- Current and thermal limiting
- Logic-controlled shutdown
- Stability with low-ESR ceramic capacitors
- Pin-to-pin replacement for Mic™ 5213

Applications

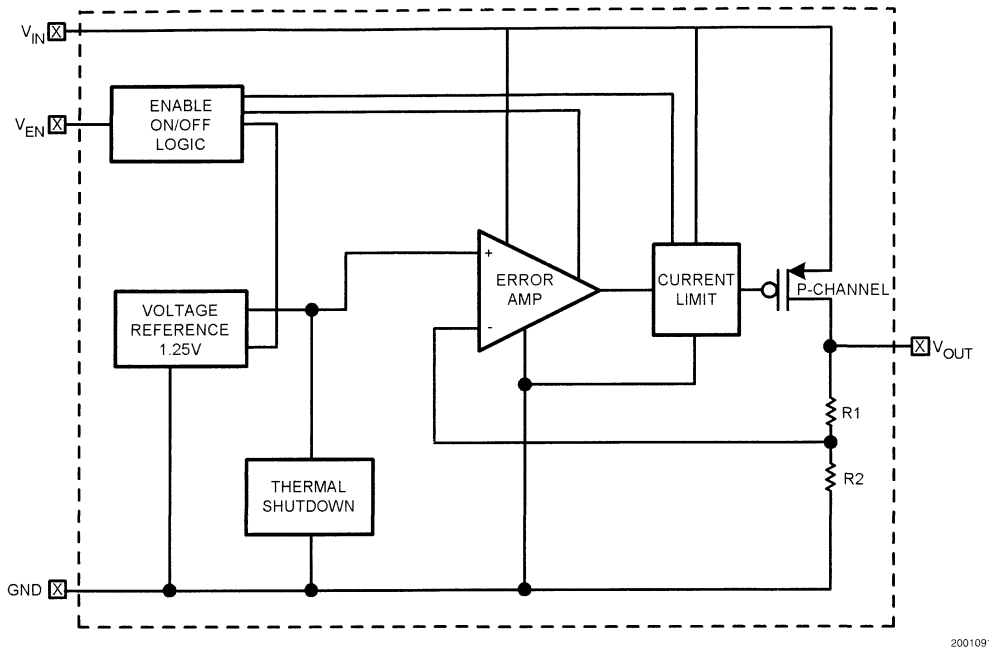
- Cellular Phones
- Battery-powered equipment
- Bar code scanner
- Laptop/palmtop computer
- High-efficiency linear power supplies

Typical Application



20010919

Simplified Schematic

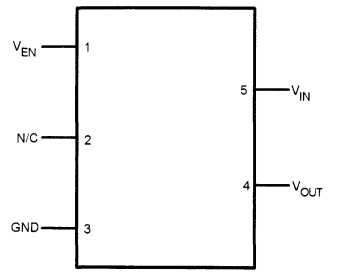


Pin Description

Pin Number	Pin Name	Pin Function
1	V_{EN}	Enable Input Logic, Logic High = Enabled Logic Low = Shutdown
2	NC	Not internally connected
3	GND	Ground
4	V_{OUT}	Output Voltage
5	V_{IN}	Input Voltage

Connection Diagram

SC70-5



20010921

Top View

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
5-Pin SC70	LMS5213IM7-2.8	L0E	1k Units Tape and Reel	MAA05A
	LMS5213IM7X-2.8		3k Units Tape and Reel	
	LMS5213IM7-3.0	L1E	1k Units Tape and Reel	
	LMS5213IM7X-3.0		3k Units Tape and Reel	
	LMS5213IM7-3.3	L2E	1k Units Tape and Reel	
	LMS5213IM7X-3.3		3k Units Tape and Reel	

National Semiconductor

LMS8117A
1A Low-Dropout Linear Regulator

General Description

The LMS8117A is a series of low dropout voltage regulators with a dropout of 1.2V at 1A of load current. It has the same pin-out as National Semiconductor's industry standard LM317.

The LMS8117A is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in two fixed voltages, 1.8V and 3.3V.

The LMS8117A offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LMS8117A series is available in SOT-223 and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

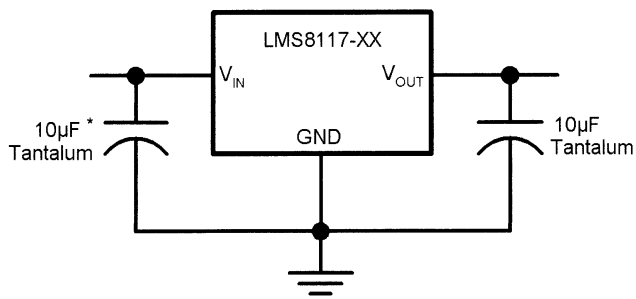
- Available in 1.8V, 3.3V, and Adjustable Versions
- Space Saving SOT-223 and TO-252 Packages
- Current Limiting and Thermal Protection
- Output Current 1A
- Temperature Range 0°C to 125°C
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)

Applications

- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators
- Battery Charger
- Battery Powered Instrumentation

Typical Application

Fixed Output Regulator



*Required if the regulator is located far from the power supply filter

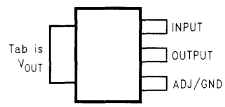
DS101196-28

Ordering Information

Package	Temperature Range (T_J) 0°C to +125°C	Packaging Marking	Transport Media	NSC Drawing
3-lead SOT-223	LMS8117AMP-ADJ	LS0A	1k Tape and Reel	MP04A
	LMS8117AMPX-ADJ	LS0A	2k Tape and Reel	
	LMS8117AMP-1.8	LS00	1k Tape and Reel	
	LMS8117AMPX-1.8	LS00	2k Tape and Reel	
	LMS8117AMP-3.3	LS01	1k Tape and Reel	
	LMS8117AMPX-3.3	LS01	2k Tape and Reel	
3-lead TO-252	LMS8117ADT-ADJ	LMS8117ADT-ADJ	Rails	TD03B
	LMS8117ADTX-ADJ	LMS8117ADT-ADJ	2.5k Tape and Reel	
	LMS8117ADT-1.8	LMS8117ADT-1.8	Rails	
	LMS8117ADTX-1.8	LMS8117ADT-1.8	2.5k Tape and Reel	
	LMS8117ADT-3.3	LMS8117ADT-3.3	Rails	
	LMS8117ADTX-3.3	LMS8117ADT-3.3	2.5k Tape and Reel	

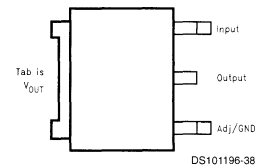
Connection Diagrams

SOT-223



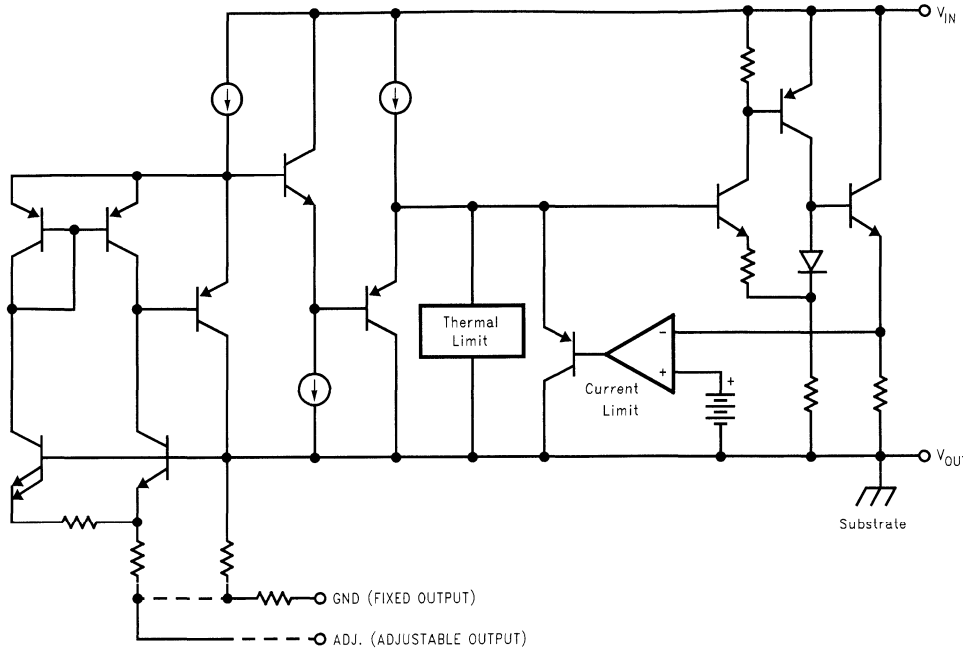
Top View

TO-252



Top View

Block Diagram



DS101196-1

National Semiconductor

LP2950/LP2951
Series of Adjustable Micropower Voltage Regulators

General Description

The LP2950 and LP2951 are micropower voltage regulators with very low quiescent current (75 µA typ.) and very low dropout voltage (typ. 40 mV at light loads and 380 mV at 100 mA). They are ideally suited for use in battery-powered systems. Furthermore, the quiescent current of the LP2950/LP2951 increases only slightly in dropout, prolonging battery life.

The LP2950-5.0 is available in the surface-mount D-Pak package, and in the popular 3-pin TO-92 package for pin-compatibility with older 5V regulators. The 8-lead LP2951 is available in plastic, ceramic dual-in-line, or metal can packages and offers additional system functions.

One such feature is an error flag output which warns of a low output voltage, often due to falling batteries on the input. It may be used for a power-on reset. A second feature is the logic-compatible shutdown input which enables the regulator to be switched on and off. Also, the part may be pin-strapped for a 5V, 3V, or 3.3V output (depending on the version), or programmed from 1.24V to 29V with an external pair of resistors.

Careful design of the LP2950/LP2951 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typ.), extremely good load and line regulation (.05% typ.) and a very low output voltage temperature coefficient, making the part useful as a low-power voltage reference.

Features

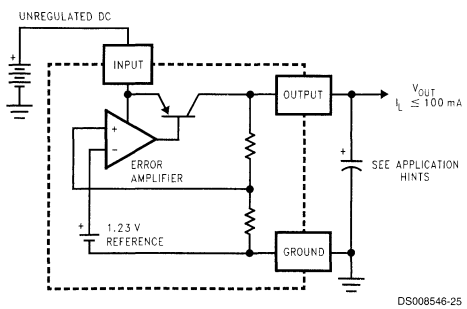
- 5V, 3V, and 3.3V versions available
- High accuracy output voltage
- Guaranteed 100 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight load and line regulation
- Very low temperature coefficient
- Use as Regulator or Reference
- Needs minimum capacitance for stability
- Current and Thermal Limiting
- Stable with low-ESR output capacitors

LP2951 versions only

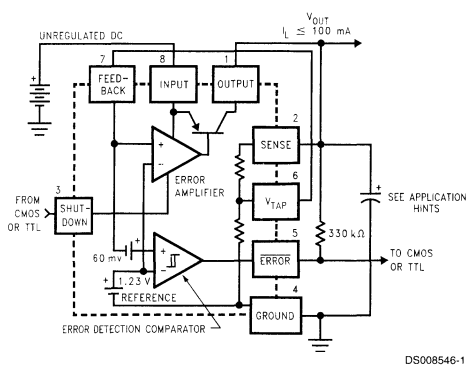
- Error flag warns of output dropout
- Logic-controlled electronic shutdown
- Output programmable from 1.24 to 29V

Block Diagram and Typical Applications

LP2950



LP2951



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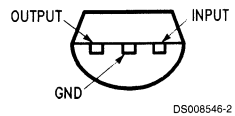
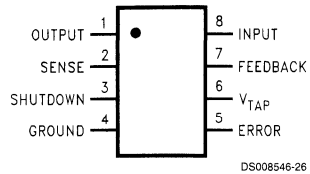
Connection Diagrams

TO-92 Plastic Package (Z)



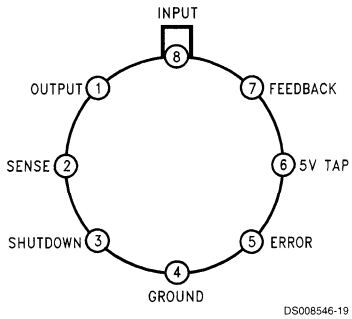
Bottom View

Dual-In-Line Packages (N, J)
Surface-Mount Package (M, MM)



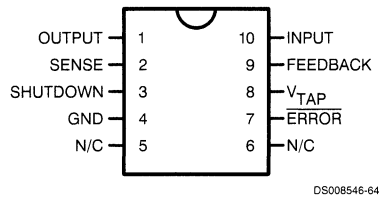
Top View

Metal Can Package (H)



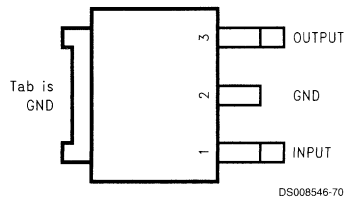
Top View

10-Lead Ceramic Surface-Mount Package (WG)



Top View

TO-252 (D-Pak)



Front View

Ordering Information

Package	Output Voltage			Temperature
	3.0V	3.3V	5.0V	(°C)
TO-92 (Z)	LP2950ACZ-3.0 LP2950CZ-3.0	LP2950ACZ-3.3 LP2950CZ-3.3	LP2950ACZ-5.0 LP2950CZ-5.0	$-40 < T_J < 125$
TO-252 (D-Pak)	LP2950CDT-3.0	LP2950CDT-3.3	LP2950CDT-5.0	$-40 < T_J < 125$
N (N-08E)	LP2951ACN-3.0 LP2951CN-3.0	LP2951ACN-3.3 LP2951CN-3.3	LP2951ACN LP2951CN	$-40 < T_J < 125$
M (M08A)	LP2951ACM-3.0 LP2951CM-3.0	LP2951ACM-3.3 LP2951CM-3.3	LP2951ACM LP2951CM	$-40 < T_J < 125$
MM (MUA08A) in Tape and Reel	LP2951ACMM-3.0 LP2951CMM-3.0	LP2951ACMM-3.3 LP2951CMM-3.3	LP2951ACMM LP2951CMM	$-40 < T_J < 125$
J (J08A)			LP2951ACJ LP2951CJ LP2951J LP2951J/883 5926-3870501MPA	$-40 < T_J < 125$ $-55 < T_J < 150$
H (H08C)			LP2951H/883 5962-3870501MGA	$-55 < T_J < 150$
WG (WG10A)			LP2951WG/883 5962-3870501MXA	$-55 < T_J < 150$

Package Marking for MM Package:

Order Number	Package Marking
LP2951ACMM	L0DA
LP2951CMM	L0DB
LP2951ACMM-3.3	L0CA
LP2951CMM-3.3	L0CB
LP2951ACMM-3.0	L0BA
LP2951CMM-3.0	L0BB

National Semiconductor

LP2952/LP2952A/LP2953/LP2953A
Adjustable Micropower Low-Dropout Voltage Regulators

General Description

The LP2952 and LP2953 are micropower voltage regulators with very low quiescent current (130 µA typical at 1 mA load) and very low dropout voltage (typ. 60 mV at light load and 470 mV at 250 mA load current). They are ideally suited for battery-powered systems. Furthermore, the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2952 and LP2953 retain all the desirable characteristics of the LP2951, but offer increased output current, additional features, and an improved shutdown function.

The internal crowbar pulls the output down quickly when the shutdown is activated.

The error flag goes low if the output voltage drops out of regulation.

Reverse battery protection is provided.

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good line and load regulation.

The parts are available in DIP and surface mount packages.

Features

- Output voltage adjusts from 1.23V to 29V
- Guaranteed 250 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse battery protection
- 50 mA (typical) output pulldown crowbar
- 5V and 3.3V versions available

LP2953 Versions Only

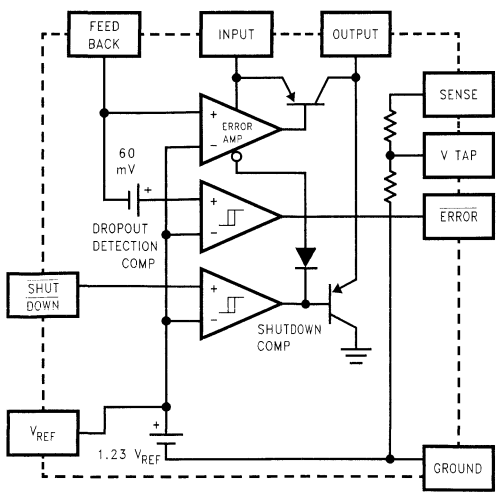
- Auxiliary comparator included with CMOS/TTL compatible output levels. Can be used for fault detection, low input line detection, etc.

Applications

- High-efficiency linear regulator
- Regulator with under-voltage shutdown
- Low dropout battery-powered regulator
- Snap-ON/Snap-OFF regulator

Block Diagrams

LP2952



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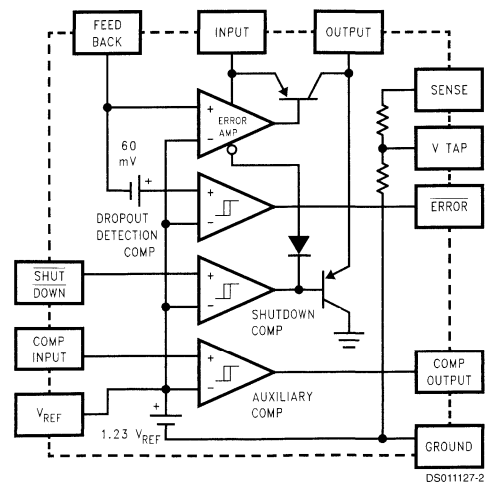
LP2953



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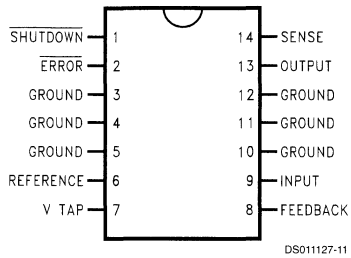
Pinout Drawings

LP2952
14-Pin DIP



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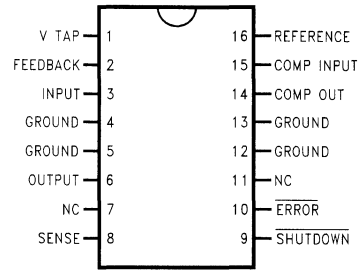
LP2953
16-Pin DIP



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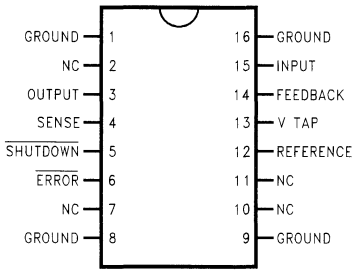
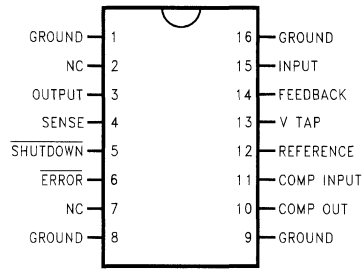
LP2952
16-Pin SO



DS011127-12

LP2953
16-Pin SO



DS011127-14

Ordering Information

LP2952

Order Number	Temp. Range (T_J) °C	Package	NSC Drawing Number
LP2952IN, LP2952AIN, LP2952IN-3.3, LP2952AIN-3.3	−40 to +125	14-Pin Molded DIP	N14A
LP2952IM, LP2952AIM, LP2952IM-3.3, LP2952AIM-3.3	−40 to +125	16-Pin Surface Mount	M16A

LP2953

Order Number	Temp. Range (T_J) °C	Package	NSC Drawing Number
LP2953IN, LP2953AIN, LP2953IN-3.3, LP2953AIN-3.3	−40 to +125	16-Pin Molded DIP	N16A
LP2953IM, LP2953AIM, LP2953IM-3.3, LP2953AIM-3.3	−40 to +125	16-Pin Surface Mount	M16A
LP2953AMJ/883 5962-9233601MEA LP2953AMJ-QMLV 5962-9233601VEA	−55 to +150	16-Pin Ceramic DIP	J16A
LP2953AMWG/883 5962-9233601QXA LP2953AMWG-QMLV 5962-9233601VXA	−55 to +150	16-Pin Ceramic Surface Mount	WG16A

National Semiconductor

LP2954/LP2954A
5V and Adjustable Micropower Low-Dropout Voltage Regulators

General Description

The LP2954 is a 5V micropower voltage regulator with very low quiescent current (90 µA typical at 1 mA load) and very low dropout voltage (typically 60 mV at light loads and 470 mV at 250 mA load current).

The quiescent current increases only slightly at dropout (120 µA typical), which prolongs battery life.

The LP2954 with a fixed 5V output is available in the three-lead TO-220 and TO-263 packages. The adjustable LP2954 is provided in an 8-lead surface mount, small outline package. The adjustable version also provides a resistor network which can be pin strapped to set the output to 5V.

Reverse battery protection is provided.

The tight line and load regulation (0.04% typical), as well as very low output temperature coefficient make the LP2954 well suited for use as a low-power voltage reference.

Output accuracy is guaranteed at both room temperature and over the entire operating temperature range.

Features

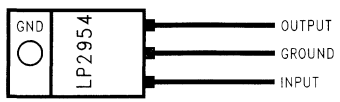
- 5V output within 1.2% over temperature (A grade)
- Adjustable 1.23 to 29V output voltage available (LP2954IM and LP2954AIM)
- Guaranteed 250 mA output current
- Extremely low quiescent current
- Low dropout voltage
- Reverse battery protection
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Pin compatible with LM2940 and LM340 (5V version only)
- Adjustable version adds error flag to warn of output drop and a logic-controlled shutdown

Applications

- High-efficiency linear regulator
- Low dropout battery-powered regulator

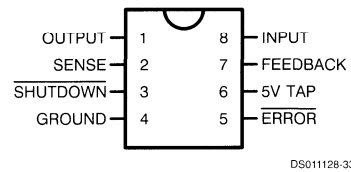
Package Outlines and Ordering Information

TO-220 3–Lead Plastic Package



Front View
Order Number LP2954AIT or LP2954IT
See NS Package T03B

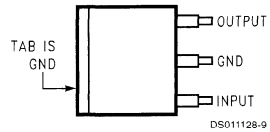
SO-8 Small Outline Surface Mount



Top View
Order Number LP2954AIM or LP2954IM
See NS Package M08A

Package Outlines and Ordering Information (Continued)

TO-263 3-Lead Plastic Surface-Mount Package



Top View

Side View
Order Number LP2954AIS or LP2954IS
See NS Package TS3B

Ordering Information

Order Number	Temp. Range (T_J) °C	Package (JEDEC)	NS Package Number
LP2954AIT	−40 to +125	TO-220	TO3B
LP2954IT			
LP2954AIS	−40 to +125	TO-263	TS3B
LP2954IS			
LP2954AIM	−40 to +125	SO-8	M08A
LP2954IM			

16

National Semiconductor

LP2956/LP2956A
Dual Micropower Low-Dropout Voltage Regulators

General Description

The LP2956 is a micropower voltage regulator with very low quiescent current (170 µA typical at light loads) and very low dropout voltage (typically 60 mV at 1 mA load current and 470 mV at 250 mA load current on the main output).

The LP2956 retains all the desirable characteristics of the LP2951, but offers increased output current (main output), an auxiliary LDO adjustable regulated output (75 mA), and additional features.

The auxiliary output is always on (regardless of main output status), so it can be used to power memory circuits.

Quiescent current increases only slightly at dropout, which prolongs battery life.

The error flag goes low if the main output voltage drops out of regulation.

An open-collector auxiliary comparator is included, whose inverting input is tied to the 1.23V reference.

Reverse battery protection is provided.

The parts are available in DIP and surface mount packages.

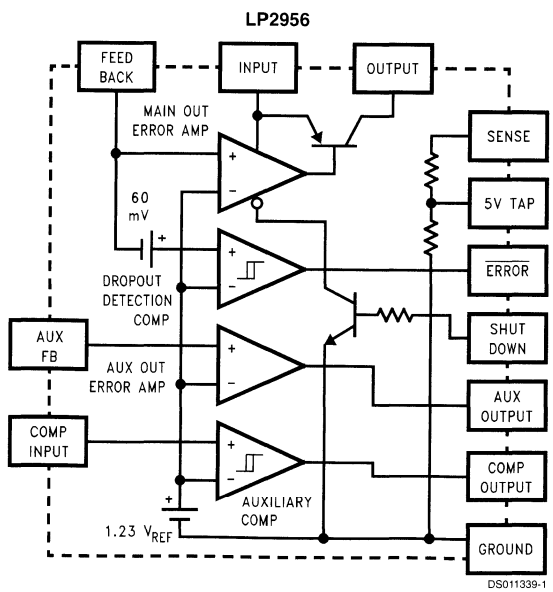
Features

- Output voltage adjusts from 1.23V to 29V
- Guaranteed 250 mA current (main output)
- Auxiliary LDO (75 mA) adjustable output
- Auxiliary comparator with open-collector output
- Shutdown pin for main output
- Extremely low quiescent current
- Low dropout voltage
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Reverse battery protection

Applications

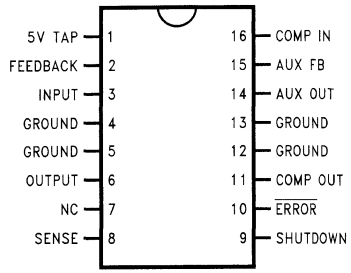
- High-efficiency linear regulator
- Low dropout battery-powered regulator
- µP system regulator with switchable high-current V_{CC}

Block Diagram



Connection Diagrams

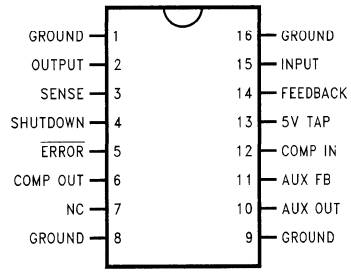
16–Pin DIP



DS011339-2

Order Number LP2956IN or LP2956AIN
See NS Package Number N16A
Order Number LP2956AMJ-QML or 5962-9554701QEA
See NS Package Number J16A

16-Pin Surface Mount



DS011339-3

Order Number LP2956IM or LP2956AIM
See NS Package Number M16A

National Semiconductor

LP2957/LP2957A
5V Low-Dropout Regulator for µP Applications

General Description

The LP2957 is a 5V micropower voltage regulator with electronic shutdown, error flag, very low quiescent current (150 µA typical at 1 mA load), and very low dropout voltage (470 mV typical at 250 mA load current).

Output can be wired for snap-on/snap-off operation to eliminate transition voltage states where µP operation may be unpredictable.

Output crowbar (50 mA typical pull-down current) will bring down the output quickly when the regulator snaps off or when the shutdown function is activated.

The part has tight line and load regulation (0.04% typical) and low output temperature coefficient (20 ppm/°C typical).

The accuracy of the 5V output is guaranteed at room temperature and over the full operating temperature range.

The LP2957 is available in the five-lead TO-220 and TO-263 packages.

Features

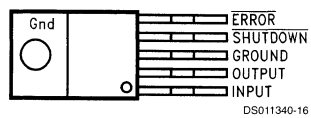
- 5V output within 1.4% over temperature (A grade)
- Easily programmed for snap-on/snap-off output
- Guaranteed 250 mA output current
- Extremely low quiescent current
- Low Input-Output voltage required for regulation
- Reverse battery protection
- Extremely tight line and load regulation
- Very low temperature coefficient
- Current and thermal limiting
- Error flag signals when output is out of regulation

Applications

- High-efficiency linear regulator
- Battery-powered regulator

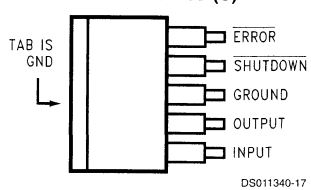
Package Outlines

Bent, Staggered Leads
5-Lead TO-220 (T)

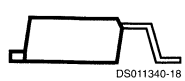


Top View
Order Number LP2957AIT or LP2957IT
See NS Package Number T05D

Plastic Surface Mount Package
5-Lead TO-263 (S)



Top View



Side View
Order Number LP2957AIS or LP2957IS
See NS Package Number TS5B

National Semiconductor

LP2960
Adjustable Micropower 0.5A Low-Dropout Regulators

General Description

The LP2960 is a micropower voltage regulator with very low dropout voltage (12 mV typical at 1 mA load and 470 mV typical at 500 mA load) and very low quiescent current (450 µA typical at 1 mA load).

The LP2960 is ideally suited for battery-powered systems: the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2960 retains all the desirable characteristics of the LP2953, and offers increased output current.

The error flag goes low any time the output drops more than 5% out of regulation.

Reverse battery protection is provided.

The LP2960 requires only 10 µF of output capacitance for stability (5V version).

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good regulation characteristics.

The parts are available in 16-pin plastic DIP and 16-pin surface mount packages.

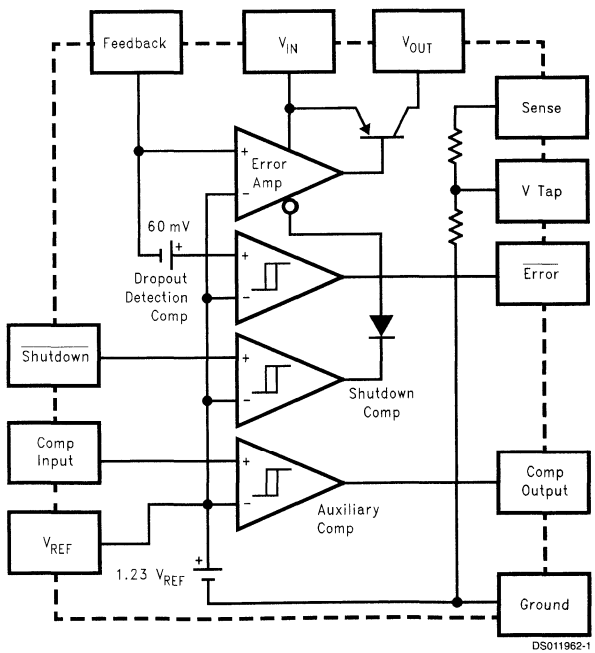
Features

- Output voltage adjusts from 1.23V–29V
- Guaranteed 500 mA output current
- 5V and 3.3V versions available
- 16-pin DIP and 16-pin SO packages
- Low dropout voltage
- Low quiescent current
- Tight line and load regulation
- Low temperature coefficient
- Current limiting and thermal protection
- Logic-level shutdown
- Can be wired for snap-ON and snap-OFF
- Reverse battery protection

Applications

- High-efficiency linear regulator
- Regulator with under-voltage shutdown
- Low dropout battery-powered regulator
- Cellular telephones

Block Diagram



National Semiconductor

LP2966
Dual 150mA Ultra Low-Dropout Regulator

General Description

The LP2966 dual ultra low-dropout (LDO) regulator operates from a +2.70V to +7.0V input supply. Each output delivers 150mA over full temperature range. The IC operates with extremely low drop-out voltage and quiescent current, which makes it very suitable for battery powered and portable applications. Each LDO in the LP2966 has independent shutdown capability. The LP2966 provides low noise performance with low ground pin current in an extremely small MSOP-8 package (refer to package dimensions and connection diagram for more information on MSOP-8 package). A wide range of preset voltage options are available for each output. In addition to the voltage combinations listed in the ordering information table, many more are available upon request with minimum orders. In all, 256 voltage combinations are possible.

Key Specifications

Dropout Voltage: Varies linearly with load current. Typically 0.9 mV at 1mA load current and 135mV at 150mA load current.

Ground Pin Current: Typically 300µA at 1mA load current and 340µA at 100mA load current (with one shutdown pin pulled low).

Shutdown Mode: Less than 1µA quiescent current when both shutdown pins are pulled low.

Error Flag: Open drain output, goes low when the corresponding output drops 10% below nominal.

Precision Output Voltage: Multiple output voltage options available ranging from 1.8V to 5.0V with a guaranteed accuracy of ±1% at room temperature.

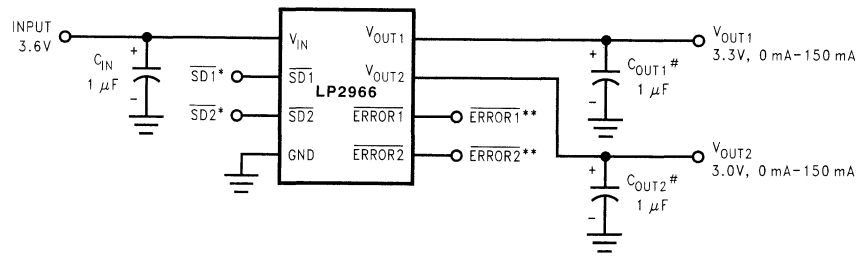
Features

- Ultra low drop-out voltage
- Low ground pin current
- <1µA quiescent current in shutdown mode
- Independent shutdown of each LDO regulator
- Output voltage accuracy ±1%
- Guaranteed 150mA output current at each output
- Low output noise
- Error Flags indicate status of each output
- Available in MSOP-8 surface mount packages
- Low output capacitor requirements (1µF)
- Operates with Low ESR ceramic capacitors in most applications
- Over temperature/over current protection
- -40°C to +125°C junction temperature range

Applications

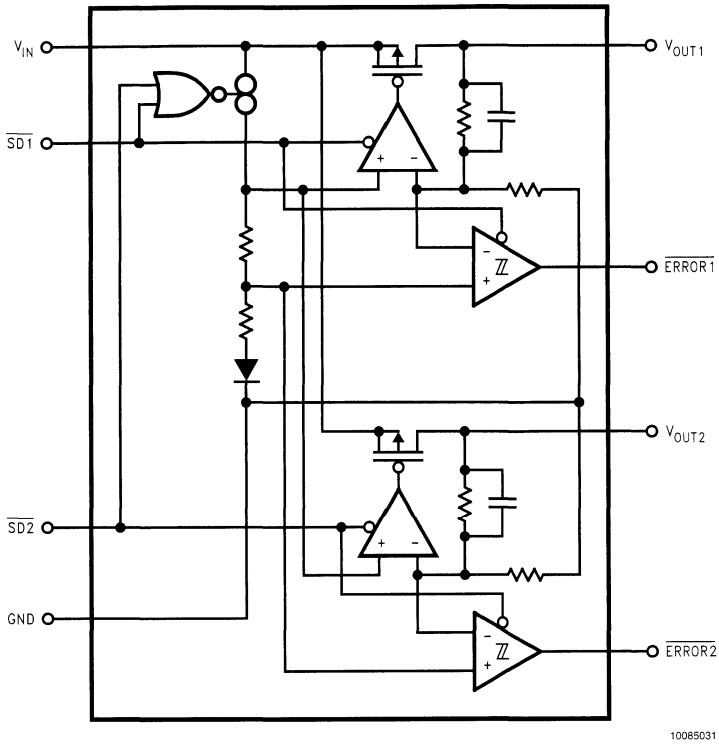
- Cellular and Wireless Applications
- Palmtop/Laptop Computer
- GPS systems
- Flat panel displays
- Post regulators
- USB applications
- Hand held equipment and multimeters
- Wireless data terminals
- Other battery powered applications

Typical Application Circuit

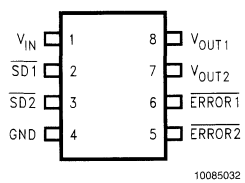


*SD1 and SD2 must be actively terminated through a pull up resistor. Tie to V_{IN} if not used.
**ERROR1 and ERROR2 are open drain outputs. These pins must be connected to ground if not used.
Minimum output capacitance is 1µF to insure stability over full load current range. More capacitance improves superior dynamic performance and provides additional stability margin.

Block Diagram



Connection Diagram



Top View
Mini SO-8 Package
8-Lead Small Outline Integrated Circuit (SOIC)
Package Code: MSOP-8

Pin Description

Pin	Name	Function
1	VIN	Input Supply pin
2	$\overline{SD1}$	Active low shutdown pin for output 1
3	$\overline{SD2}$	Active low shutdown pin for output 2
4	GND	Ground
5	$\overline{ERROR2}$	Error flag for output 2 - Normally high impedance, should be connected to ground if not used.
6	$\overline{ERROR1}$	Error flag for output 1 - Normally high impedance, should be connected to ground if not used.
7	VOUT2	Output 2
8	VOUT1	Output 1

TABLE 1. Ordering Information

The following voltage options and their combinations are possible.
5.0V, 4.0V, 3.8V, 3.6V, 3.3V, 3.2V, 3.1V, 3.0V, 2.9V, 2.8V, 2.7V, 2.6V, 2.5V, 2.4V, 2.0V and 1.8V

Output Voltage 1	Output Voltage 2	Order Number	Package Marking	Supplied As:
5.0	5.0	LP2966IMM-5050	LAFB	1000 units on tape and reel
5.0	5.0	LP2966IMMX-5050	LAFB	3500 units on tape and reel
3.6	3.6	LP2966IMM-3636	LAEB	1000 units on tape and reel
3.6	3.6	LP2966IMMX-3636	LAEB	3500 units on tape and reel
3.3	3.6	LP2966IMM-3336	LAHB	1000 units on tape and reel
3.3	3.6	LP2966IMMX-3336	LAHB	3500 units on tape and reel
3.3	3.3	LP2966IMM-3333	LADB	1000 units on tape and reel
3.3	3.3	LP2966IMMX-3333	LADB	3500 units on tape and reel
3.3	2.5	LP2966IMM-3325	LARB	1000 units on tape and reel
3.3	2.5	LP2966IMMX-3325	LARB	3500 units on tape and reel
3.0	3.0	LP2966IMM-3030	LACB	1000 units on tape and reel
3.0	3.0	LP2966IMMX-3030	LACB	3500 units on tape and reel
2.8	3.0	LP2966IMM-2830	LASB	1000 units on tape and reel
2.8	3.0	LP2966IMMX-2830	LASB	3500 units on tape and reel
2.8	2.8	LP2966IMM-2828	LABB	1000 units on tape and reel
2.8	2.8	LP2966IMMX-2828	LABB	3500 units on tape and reel
2.5	2.5	LP2966IMM-2525	LAAB	1000 units on tape and reel
2.5	2.5	LP2966IMMX-2525	LAAB	3500 units on tape and reel
1.8	3.3	LP2966IMM-1833	LCFB	1000 units on tape and reel
1.8	3.3	LP2966IMMX-1833	LCFB	3500 units on Tape and reel
1.8	3.0	LP2966IMM-1830	LEYB	1000 units on tape and reel
1.8	3.0	LP2966IMMX-1830	LEYB	3500 units on Tape and reel
1.8	1.8	LP2966IMM-1818	LA9B	1000 units on tape and reel
1.8	1.8	LP2966IMMX-1818	LA9B	3500 units on tape and reel

The voltage options and combinations shown in *Table 1* are available. For other custom voltage options or combinations of voltage options, please contact your nearest National Semiconductor Sales Office.

National Semiconductor

LP2967
Dual Micropower 150 mA Low-Dropout Regulator in micro SMD Package

General Description

The LP2967 is a 150 mA, dual fixed-output voltage regulator designed to provide ultra low-dropout and low noise in battery powered applications.

Using an optimized VIP (Vertically Integrated PNP) process, the LP2967 delivers unequalled performance in all specifications critical to battery powered designs:

Dropout Voltage: Typically 240 mV at 150 mA load, and 6 mV at 1 mA load for each output.

Ground Pin Current: Typically 1 mA at 150 mA load, and 200 µA at 1 mA load for each output.

Enhanced Stability: The LP2967 is stable with output capacitor ESR as low as 5 mΩ, which allows the use of ceramic capacitors on the output.

Sleep Mode: Less than 2 µA quiescent current when SD pins are pulled low.

Smallest Possible Size: micro SMD package uses absolute minimum board space.

Precision Output: 1.25% tolerance.

Low Noise: By adding a 100 nF bypass capacitor, output noise can be reduced to 30 µV (typical).

Multiple voltage options, from 1.8V to 5.0V, are available. Consult factory for custom voltages.

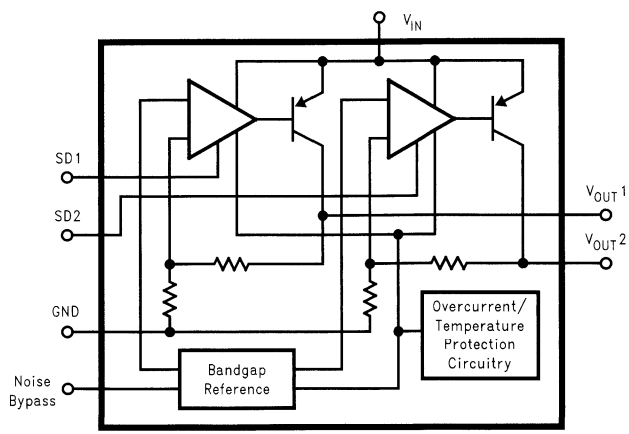
Features

- Ultra low drop-out voltage
- Guaranteed 150mA output current, 300 mA peak
- Smallest possible size (micro SMD package)
- Requires minimum external components
- Stable with 2.2 µF tantalum or ceramic capacitor
- Output voltage accuracy ±1%
- < 2 µA quiescent current when shut down
- Wide supply voltage range (16V max.)
- Low Z_{OUT}: 0.3Ω typical (10 Hz to 1 MHz)
- Over temperature/over current protection
- −40°C to +125°C junction temperature range
- Custom voltages available

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistance (PDA)
- Camcorder, Personal Stereo and Camera

Block Diagram



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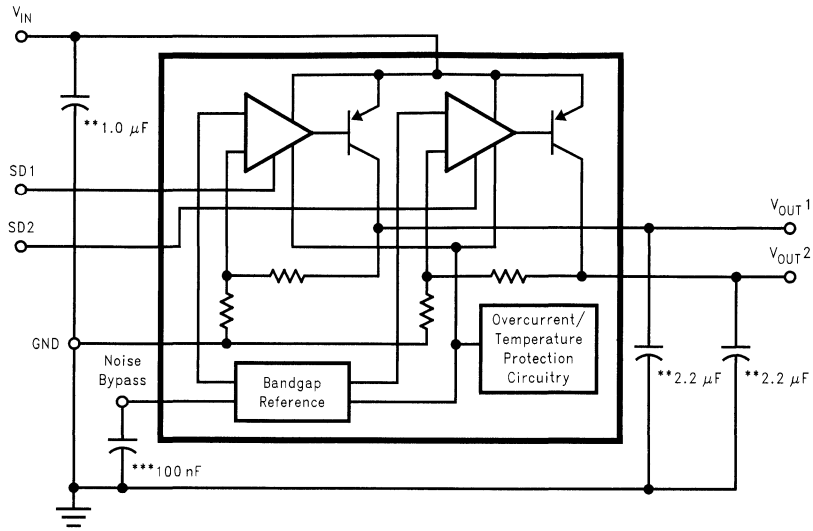
Basic Application Circuit



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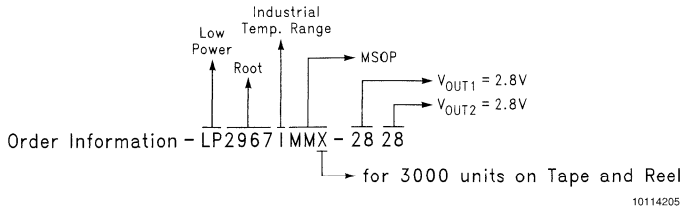
*SD1 and SD2 must be actively terminated. Tie them to V_{IN} if their functions are not needed.
**Minimum capacitance are shown to ensure stability (may be increased without limit).
*** Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current.

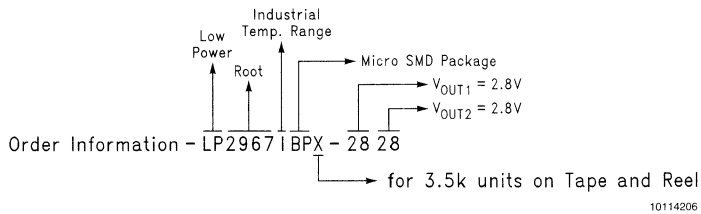
Ordering Information

Output Voltage (V)		Grade	Order Information	Package Marking	Supplied As
V_{OUT1}	V_{OUT2}				
For MSOP Package					
2.5	2.8	STD	LP2967IMM-2528	LCAB	1000 Units Tape and Reel
2.5	2.8	STD	LP2967IMMX-2528	LCAB	3000 Units Tape and Reel
2.5	3.3	STD	LP2967IMM-2533	LCBB	1000 Units Tape and Reel
2.5	3.3	STD	LP2967IMMX-2533	LCBB	3000 Units Tape and Reel
2.6	2.6	STD	LP2967IMM-2626	LCLB	1000 Units Tape and Reel
2.6	2.6	STD	LP2967IMMX-2626	LCLB	3000 Units Tape and Reel
2.8	2.8	STD	LP2967IMM-2828	LAQB	1000 Units Tape and Reel
2.8	2.8	STD	LP2967IMMX-2828	LAQB	3000 Units Tape and Reel
2.8	3.3	STD	LP2967IMM-2833	LCCB	1000 Units Tape and Reel
2.8	3.3	STD	LP2967IMMX-2833	LCCB	3000 Units Tape and Reel
For 8-Bump micro SMD Package (BPA08)					
1.8	2.5	STD	LP2967IBP-1825	L0P	1000 Units Tape and Reel
1.8	2.5	STD	LP2967IBPX-1825	L0P	3500 Units Tape and Reel
2.5	2.8	STD	LP2967IBP-2528	CA	1000 Units Tape and Reel
2.5	2.8	STD	LP2967IBPX-2528	CA	3500 Units Tape and Reel
2.5	3.3	STD	LP2967IBP-2533	CB	1000 Units Tape and Reel
2.5	3.3	STD	LP2967IBPX-2533	CB	3500 Units Tape and Reel
2.6	2.6	STD	LP2967IBP-2626	CL	1000 Units Tape and Reel
2.6	2.6	STD	LP2967IBPX-2626	CL	3500 Units Tape and Reel
2.8	2.8	STD	LP2967IBP-2828	AQ	1000 Units Tape and Reel
2.8	2.8	STD	LP2967IBPX-2828	AQ	3500 Units Tape and Reel
2.8	3.3	STD	LP2967IBP-2833	CC	1000 Units Tape and Reel
2.8	3.3	STD	LP2967IBPX-2833	CC	3500 Units Tape and Reel

Ordering Information (Continued)



10114205



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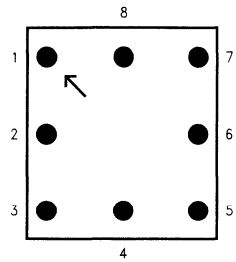
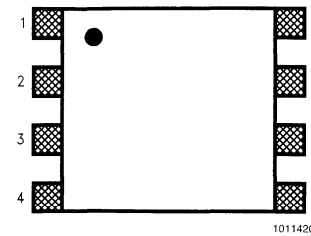
Package Outline and Connection Diagram



Top View
micro SMD
8-Bump micro SMD Package
Code: BP



Top View
Mini SO-8 Package
8-Lead Small Outline Integrated Circuit (SOIC) Package
Code: MM

Pin Description

Name	Pin Number		Function
	micro SMD	MSOP	
$V_{OUT}2$	1	7	Output voltage of the second LDO
SD2	2	6	Shutdown input for the second LDO
BYPASS	3	5	Bypass capacitor for the bandgap
GND	4	-	Ground Substrate
GND	5	4	Common Ground
SD1	6	3	Shutdown input for the first LDO
V_{OUT} 1	7	2	Output voltage of the first LDO
V_{IN}	8	1, 8	Common input voltage for both LDOs

National Semiconductor

LP2975
MOSFET LDO Driver/Controller

General Description

A high-current LDO regulator is simple to design with the LP2975 LDO Controller. Using an external P-FET, the LP2975 will deliver an ultra low dropout regulator with extremely low quiescent current.

High open loop gain assures excellent regulation and ripple rejection performance.

The trimmed internal bandgap reference provides precise output voltage over the entire operating temperature range.

Dropout voltage is "user selectable" by sizing the external FET: the minimum input-output voltage required for operation is the maximum load current multiplied by the $R_{DS}(ON)$ of the FET.

Overcurrent protection of the external FET is easily implemented by placing a sense resistor in series with V_{IN}. The 57 mV detection threshold of the current sense circuitry minimizes dropout voltage and power dissipation in the resistor.

The standard product versions available provide output voltages of 12V, 5V, or 3.3V with guaranteed 25°C accuracy of 1.5% ("A" grade) and 2.5% (standard grade).

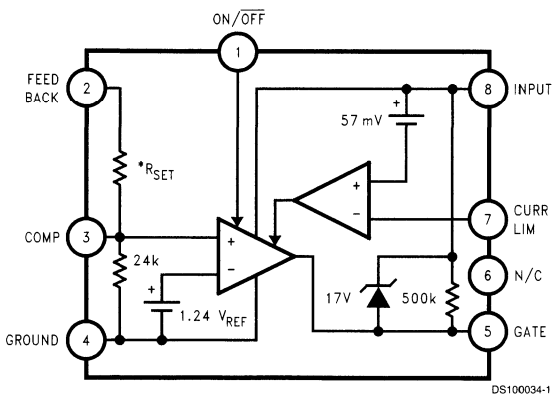
Features

- Simple to use, few external components
- Ultra-small mini SO-8 package
- 1.5% (A grade) precision output voltage
- Low-power shutdown input
- < 1 µA in shutdown
- Low operating current (180 µA typical @ V_{IN} = 5V)
- Wide supply voltage range (1.8V to 24V)
- Built-in current limit amplifier
- Overtemperature protection
- 12V, 5V, and 3.3V standard output voltages
- Can be programmed using external divider
- −40°C to +125°C junction temperature range

Applications

- High-current 5V to 3.3V regulator
- Post regulator for switching converter
- Current-limited switch

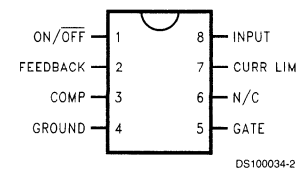
Block Diagram



*R_{SET} values are: 208k for 12V part, 72.8k for 5V part, and 39.9k for 3.3V part.

Connection Diagram

Surface Mount Mini SO-8 Package



Top View
For Order Numbers
See *Table 1* of this Document
See NS Package Number MUA08A

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Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage	Grade	Order Information	Package Marking	Supplied As:
12	A	LP2975AIMMX-12	L47A	3500 Units on Tape and Reel
12	A	LP2975AIMM-12	L47A	1000 Units on Tape and Reel
12	STD	LP2975IMMX-12	L47B	3500 Units on Tape and Reel
12	STD	LP2975IMM-12	L47B	1000 Units on Tape and Reel
5.0	A	LP2975AIMMX-5.0	L46A	3500 Units on Tape and Reel
5.0	A	LP2975AIMM-5.0	L46A	1000 Units on Tape and Reel
5.0	STD	LP2975IMMX-5.0	L46B	3500 Units on Tape and Reel
5.0	STD	LP2975IMM-5.0	L46B	1000 Units on Tape and Reel
3.3	A	LP2975AIMMX-3.3	L45A	3500 Units on Tape and Reel
3.3	A	LP2975AIMM-3.3	L45A	1000 Units on Tape and Reel
3.3	STD	LP2975IMMX-3.3	L45B	3500 Units on Tape and Reel
3.3	STD	LP2975IMM-3.3	L45B	1000 Units on Tape and Reel

National Semiconductor

LP2978
Micropower SOT, 50 mA Low-Noise Ultra Low-Dropout Regulator
Designed for Use with Very Low ESR Output Capacitors

General Description

The LP2978 is a 50 mA, fixed-output voltage regulator designed to provide ultra low-dropout and low noise in battery powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2978 delivers unequalled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

Ground Pin Current: Typically 350 µA @ 50 mA load, and 75 µA @ 1 mA load.

Enhanced Stability: The LP2978 is stable with output capacitor ESR as low as 5 mΩ, which allows the use of ceramic capacitors on the output.

Sleep Mode: Less than 1 µA quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size: SOT-23 package uses absolute minimum board space.

Precision Output: 1% tolerance output voltages available (A grade).

Low Noise: By adding a 10 nF bypass capacitor, output noise can be reduced to 30 µV (typical).

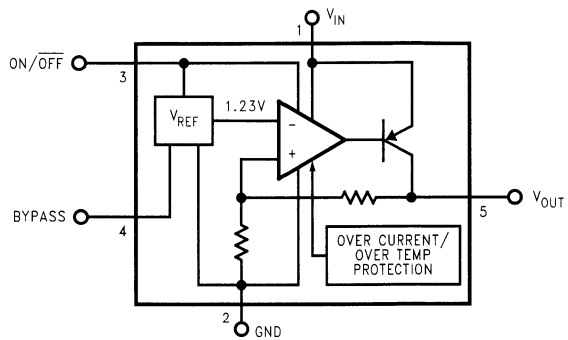
Features

- Ultra low dropout voltage
- Smallest possible size (SOT-23 Package)
- Requires minimum external components
- Stable with low-ESR output capacitor
- <1 µA quiescent current when shut down
- Low ground pin current at all loads
- Output voltage accuracy 1% (A Grade)
- High peak current capability
- Wide supply voltage range (16V max)
- Low Z_{OUT}: 0.3Ω typical (10 Hz to 1 MHz)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range
- Custom voltages available

Applications

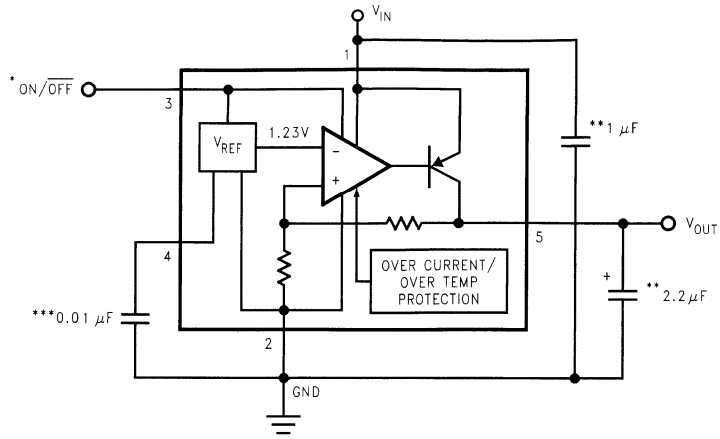
- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



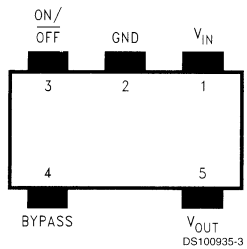
DS100935-1

Basic Application Circuit



*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.
**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see Application Hints).
***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see Application Hints).

Connection Diagram



See NS Package Number MF05A

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied As:
3.8	A	LP2978AIM5X-3.8	LØLA	3000 Units on Tape and Reel
3.8	A	LP2978AIM5-3.8	LØLA	1000 Units on Tape and Reel
3.8	STD	LP2978IM5X-3.8	LØLB	3000 Units on Tape and Reel
3.8	STD	LP2978IM5-3.8	LØLB	1000 Units on Tape and Reel

National Semiconductor

LP2980
Micropower 50 mA Ultra Low-Dropout Regulator In SOT-23 and micro SMD Packages

General Description

The LP2980 is a 50 mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2980 delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage. Typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

Ground Pin Current. Typically 375 µA @ 50 mA load, and 80 µA @ 1 mA load.

Sleep Mode. Less than 1 µA quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size. SOT-23 and micro SMD packages use an absolute minimum board space.

Minimum Part Count. Requires only 1 µF of external capacitance on the regulator output.

Precision Output. 0.5% tolerance output voltages available (A grade).

5.0V, 3.3V, and 3.0V versions available as standard products.

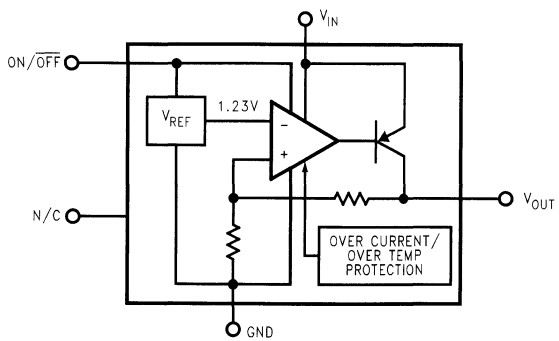
Features

- Ultra low dropout voltage
- Output voltage accuracy 0.5% (A Grade)
- Guaranteed 50 mA output current
- Smallest possible size (SOT-23, micro SMD package)
- Requires only 1 µF external capacitance
- < 1 µA quiescent current when shutdown
- Low ground pin current at all load currents
- High peak current capability (150 mA typical)
- Wide supply voltage range (16V max)
- Fast dynamic response to line and load
- Low Z_{OUT} over wide frequency range
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



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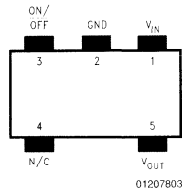
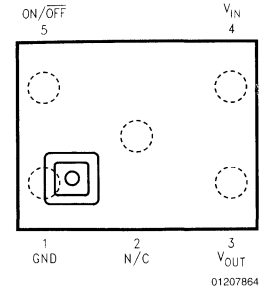
Connection Diagrams

5-Lead Small Outline Package (M5)



Top View
See NS Package Number MF05A
For ordering information see *Table 1*

micro SMD, 5 Bump Package (BPA05)



Top View
See NS Package Number BPA05

Note: The actual physical placement of the package marking will vary from part to part. Package marking contains date code and lot traceability information, and will vary considerably. Package marking does not correlate to device type.

Ordering Information

TABLE 1. Package Marking and Order Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5-Lead Small Outline Package (M5)				
For output voltages ≤ 2.3V, refer to LP2980LV datasheet. If a non-standard voltage is required, see LP2980-ADJ.				
2.5	A	LP2980AIM5X-2.5	L0NA	3000 Units on Tape and Reel
2.5	A	LP2980AIM5-2.5	L0NA	1000 Units on Tape and Reel
2.5	STD	LP2980IM5X-2.5	L0NB	3000 Units on Tape and Reel
2.5	STD	LP2980IM5-2.5	L0NB	1000 Units on Tape and Reel
2.6	A	LP2980AIM5X-2.6	L48A	3000 Units on Tape and Reel
2.6	A	LP2980AIM5-2.6	L48A	1000 Units on Tape and Reel
2.6	STD	LP2980IM5X-2.6	L48B	3000 Units on Tape and Reel
2.6	STD	LP2980IM5-2.6	L48B	1000 Units on Tape and Reel
2.7	A	LP2980AIM5X-2.7	L26A	3000 Units on Tape and Reel
2.7	A	LP2980AIM5-2.7	L26A	1000 Units on Tape and Reel
2.7	STD	LP2980IM5X-2.7	L26B	3000 Units on Tape and Reel
2.7	STD	LP2980IM5-2.7	L26B	1000 Units on Tape and Reel
2.8	A	LP2980AIM5X-2.8	L13A	3000 Units on Tape and Reel
2.8	A	LP2980AIM5-2.8	L13A	1000 Units on Tape and Reel
2.8	STD	LP2980IM5X-2.8	L13B	3000 Units on Tape and Reel
2.8	STD	LP2980IM5-2.8	L13B	1000 Units on Tape and Reel
2.9	A	LP2980AIM5X-2.9	L12A	3000 Units on Tape and Reel
2.9	A	LP2980AIM5-2.9	L12A	1000 Units on Tape and Reel
2.9	STD	LP2980IM5X-2.9	L12B	3000 Units on Tape and Reel
2.9	STD	LP2980IM5-2.9	L12B	1000 Units on Tape and Reel
3.0	A	LP2980AIM5X-3.0	L02A	3000 Units on Tape and Reel
3.0	A	LP2980AIM5-3.0	L02A	1000 Units on Tape and Reel
3.0	STD	LP2980IM5X-3.0	L02B	3000 Units on Tape and Reel
3.0	STD	LP2980IM5-3.0	L02B	1000 Units on Tape and Reel
3.1	A	LP2980AIM5X-3.1	L30A	3000 Units on Tape and Reel
3.1	A	LP2980AIM5-3.1	L30A	1000 Units on Tape and Reel
3.1	STD	LP2980IM5X-3.1	L30B	3000 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Order Information (Continued)

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
3.1	STD	LP2980IM5-3.1	L30B	1000 Units on Tape and Reel
3.2	A	LP2980AIM5X-3.2	L31A	3000 Units on Tape and Reel
3.2	A	LP2980AIM5-3.2	L31A	1000 Units on Tape and Reel
3.2	STD	LP2980IM5X-3.2	L31B	3000 Units on Tape and Reel
3.2	STD	LP2980IM5-3.2	L31B	1000 Units on Tape and Reel
3.3	A	LP2980AIM5X-3.3	L00A	3000 Units on Tape and Reel
3.3	A	LP2980AIM5-3.3	L00A	1000 Units on Tape and Reel
3.3	STD	LP2980IM5X-3.3	L00B	3000 Units on Tape and Reel
3.3	STD	LP2980IM5-3.3	L00B	1000 Units on Tape and Reel
3.5	A	LP2980AIM5X-3.5	L27A	3000 Units on Tape and Reel
3.5	A	LP2980AIM5-3.5	L27A	1000 Units on Tape and Reel
3.5	STD	LP2980IM5X-3.5	L27B	3000 Units on Tape and Reel
3.5	STD	LP2980IM5-3.5	L27B	1000 Units on Tape and Reel
3.6	A	LP2980AIM5X-3.6	L28A	3000 Units on Tape and Reel
3.6	A	LP2980AIM5-3.6	L28A	1000 Units on Tape and Reel
3.6	STD	LP2980IM5X-3.6	L28B	3000 Units on Tape and Reel
3.6	STD	LP2980IM5-3.6	L28B	1000 Units on Tape and Reel
3.8	A	LP2980AIM5X-3.8	L21A	3000 Units on Tape and Reel
3.8	A	LP2980AIM5-3.8	L21A	1000 Units on Tape and Reel
3.8	STD	LP2980IM5X-3.8	L21B	3000 Units on Tape and Reel
3.8	STD	LP2980IM5-3.8	L21B	1000 Units on Tape and Reel
4.0	A	LP2980AIM5X-4.0	L25A	3000 Units on Tape and Reel
4.0	A	LP2980AIM5-4.0	L25A	1000 Units on Tape and Reel
4.0	STD	LP2980IM5X-4.0	L25B	3000 Units on Tape and Reel
4.0	STD	LP2980IM5-4.0	L25B	1000 Units on Tape and Reel
4.5	A	LP2980AIM5X-4.5	L0XA	3000 Units on Tape and Reel
4.5	A	LP2980AIM5-4.5	L0XA	1000 Units on Tape and Reel
4.5	STD	LP2980IM5X-4.5	L0XB	3000 Units on Tape and Reel
4.5	STD	LP2980IM5-4.5	L0XB	1000 Units on Tape and Reel
4.7	A	LP2980AIM5X-4.7	L37A	3000 Units on Tape and Reel
4.7	A	LP2980AIM5-4.7	L37A	1000 Units on Tape and Reel
4.7	STD	LP2980IM5X-4.7	L37B	3000 Units on Tape and Reel
4.7	STD	LP2980IM5-4.7	L37B	1000 Units on Tape and Reel
5.0	A	LP2980AIM5X-5.0	L01A	3000 Units on Tape and Reel
5.0	A	LP2980AIM5-5.0	L01A	1000 Units on Tape and Reel
5.0	STD	LP2980IM5X-5.0	L01B	3000 Units on Tape and Reel
5.0	STD	LP2980IM5-5.0	L01B	1000 Units on Tape and Reel
micro SMD, 5 Bump Package (BPA05)				
3.3	A	LP2980AIBP-3.3		250 Units on Tape and Reel
3.3	A	LP2980AIBPX-3.3		3000 Units on Tape and Reel
3.3	STD	LP2980IBP-3.3		250 Units on Tape and Reel
3.3	STD	LP2980IBPX-3.3		3000 Units on Tape and Reel
5.0	A	LP2980AIBP-5.0		250 Units on Tape and Reel
5.0	A	LP2980AIBPX-5.0		3000 Units on Tape and Reel
5.0	STD	LP2980IBP-5.0		250 Units on Tape and Reel
5.0	STD	LP2980IBPX-5.0		3000 Units on Tape and Reel

National Semiconductor

LP2981
Micropower 100 mA Ultra Low-Dropout Regulator in SOT-23 and micro SMD Packages

General Description

The LP2981 is a 100 mA, fixed-output voltage regulator designed specifically to meet the requirements of battery-powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2981 delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage. Typically 200 mV @ 100 mA load, and 7 mV @ 1 mA load.

Ground Pin Current. Typically 600 µA @ 100 mA load, and 80 µA @ 1 mA load.

Sleep Mode. Less than 1 µA quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size. SOT-23 and micro SMD packages use an absolute minimum board space.

Precision Output. 0.75% tolerance output voltages available (A grade).

Eleven voltage options, from 2.5V to 5.0V, are available as standard products.

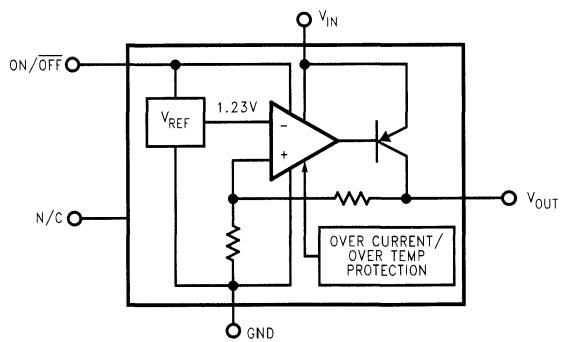
Features

- Ultra low dropout voltage
- Output voltage accuracy 0.75% (A Grade)
- Guaranteed 100 mA output current
- Smallest possible size (SOT-23, micro SMD package)
- < 1 µA quiescent current when shutdown
- Low ground pin current at all load currents
- High peak current capability (300 mA typical)
- Wide supply voltage range (16V max)
- Fast dynamic response to line and load
- Low Z_{OUT} over wide frequency range
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



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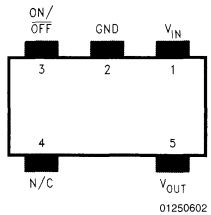
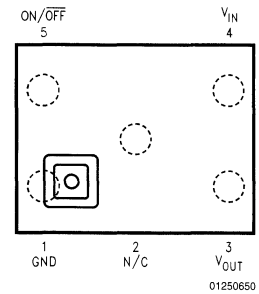
Connection Diagrams

5-Lead Small Outline Package (M5)



Top View
See NS Package Number MF05A
For ordering information see *Table 1*

micro SMD, 5 Bump Package (BPA05)



Top View
See NS Package Number BPA05

Note: The actual physical placement of the package marking will vary from part to part. Package marking contains date code and lot traceability information, and will vary considerably. Package marking does not correlate to device type.

Ordering Information

TABLE 1. Package Marking and Order Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5-Lead Small Outline Package (M5)				
2.5	A	LP2981AIM5X-2.5	L0CA	3000 Units on Tape and Reel
2.5	A	LP2981AIM5-2.5	L0CA	1000 Units on Tape and Reel
2.5	STD	LP2981IM5X-2.5	L0CB	3000 Units on Tape and Reel
2.5	STD	LP2981IM5-2.5	L0CB	1000 Units on Tape and Reel
2.7	A	LP2981AIM5X-2.7	L0DA	3000 Units on Tape and Reel
2.7	A	LP2981AIM5-2.7	L0DA	1000 Units on Tape and Reel
2.7	STD	LP2981IM5X-2.7	L0DB	3000 Units on Tape and Reel
2.7	STD	LP2981IM5-2.7	L0DB	1000 Units on Tape and Reel
2.8	A	LP2981AIM5X-2.8	L77A	3000 Units on Tape and Reel
2.8	A	LP2981AIM5-2.8	L77A	1000 Units on Tape and Reel
2.8	STD	LP2981IM5X-2.8	L77B	3000 Units on Tape and Reel
2.8	STD	LP2981IM5-2.8	L77B	1000 Units on Tape and Reel
2.9	A	LP2981AIM5X-2.9	L0VA	3000 Units on Tape and Reel
2.9	A	LP2981AIM5-2.9	L0VA	1000 Units on Tape and Reel
2.9	STD	LP2981IM5X-2.9	L0VB	3000 Units on Tape and Reel
2.9	STD	LP2981IM5-2.9	L0VB	1000 Units on Tape and Reel
3.0	A	LP2981AIM5X-3.0	L05A	3000 Units on Tape and Reel
3.0	A	LP2981AIM5-3.0	L05A	1000 Units on Tape and Reel
3.0	STD	LP2981IM5X-3.0	L05B	3000 Units on Tape and Reel
3.0	STD	LP2981IM5-3.0	L05B	1000 Units on Tape and Reel
3.1	A	LP2981AIM5X-3.1	L38A	3000 Units on Tape and Reel
3.1	A	LP2981AIM5-3.1	L38A	1000 Units on Tape and Reel
3.1	STD	LP2981IM5X-3.1	L38B	3000 Units on Tape and Reel
3.1	STD	LP2981IM5-3.1	L38B	1000 Units on Tape and Reel
3.2	A	LP2981AIM5X-3.2	L35A	3000 Units on Tape and Reel
3.2	A	LP2981AIM5-3.2	L35A	1000 Units on Tape and Reel
3.2	STD	LP2981IM5X-3.2	L35B	3000 Units on Tape and Reel
3.2	STD	LP2981IM5-3.2	L35B	1000 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Order Information (Continued)

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
3.3	A	LP2981AIM5X-3.3	L04A	3000 Units on Tape and Reel
3.3	A	LP2981AIM5-3.3	L04A	1000 Units on Tape and Reel
3.3	STD	LP2981IM5X-3.3	L04B	3000 Units on Tape and Reel
3.3	STD	LP2981IM5-3.3	L04B	1000 Units on Tape and Reel
3.6	A	LP2981AIM5X-3.6	L0JA	3000 Units on Tape and Reel
3.6	A	LP2981AIM5-3.6	L0JA	1000 Units on Tape and Reel
3.6	STD	LP2981IM5X-3.6	L0JB	3000 Units on Tape and Reel
3.6	STD	LP2981IM5-3.6	L0JB	1000 Units on Tape and Reel
3.8	A	LP2981AIM5X-3.8	L36A	3000 Units on Tape and Reel
3.8	A	LP2981AIM5-3.8	L36A	1000 Units on Tape and Reel
3.8	STD	LP2981IM5X-3.8	L36B	3000 Units on Tape and Reel
3.8	STD	LP2981IM5-3.8	L36B	1000 Units on Tape and Reel
4.0	A	LP2981AIM5X-4.0	L0ZA	3000 Units on Tape and Reel
4.0	A	LP2981AIM5-4.0	L0ZA	1000 Units on Tape and Reel
4.0	STD	LP2981IM5X-4.0	L0ZB	3000 Units on Tape and Reel
4.0	STD	LP2981IM5-4.0	L0ZB	1000 Units on Tape and Reel
4.7	A	LP2981AIM5X-4.7	L0GA	3000 Units on Tape and Reel
4.7	A	LP2981AIM5-4.7	L0GA	1000 Units on Tape and Reel
4.7	STD	LP2981IM5X-4.7	L0GB	3000 Units on Tape and Reel
4.7	STD	LP2981IM5-4.7	L0GB	1000 Units on Tape and Reel
5.0	A	LP2981AIM5X-5.0	L03A	3000 Units on Tape and Reel
5.0	A	LP2981AIM5-5.0	L03A	1000 Units on Tape and Reel
5.0	STD	LP2981IM5X-5.0	L03B	3000 Units on Tape and Reel
5.0	STD	LP2981IM5-5.0	L03B	1000 Units on Tape and Reel
micro SMD, 5 Bump Package (BPA05)				
2.5	A	LP2981AIBP-2.5		250 Units on Tape and Reel
2.5	A	LP2981AIBPX-2.5		3000 Units on Tape and Reel
2.5	STD	LP2981IBP-2.5		250 Units on Tape and Reel
2.5	STD	LP2981IBPX-2.5		3000 Units on Tape and Reel
3.2	A	LP2981AIBP-3.2		250 Units on Tape and Reel
3.2	A	LP2981AIBPX-3.2		3000 Units on Tape and Reel
3.2	STD	LP2981IBP-3.2		250 Units on Tape and Reel
3.2	STD	LP2981IBPX-3.2		3000 Units on Tape and Reel
3.3	A	LP2981AIBP-3.3		250 Units on Tape and Reel
3.3	A	LP2981AIBPX-3.3		3000 Units on Tape and Reel
3.3	STD	LP2981IBP-3.3		250 Units on Tape and Reel
3.3	STD	LP2981IBPX-3.3		3000 Units on Tape and Reel

National Semiconductor

LP2982
Micropower 50 mA Ultra Low-Dropout Regulator in SOT-23 and micro SMD Packages

General Description

The LP2982 is a 50 mA, fixed-output voltage regulator designed to provide ultra low dropout and lower noise in battery powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2982 delivers unequaled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 120 mV @ 50 mA load, and 7 mV @ 1 mA load.

Ground Pin Current: Typically 375 µA @ 50 mA load, and 80 µA @ 1 mA load.

Sleep Mode: Less than 1 µA quiescent current when on/off pin is pulled low.

Smallest Possible Size: SOT-23 and micro SMD packages use absolute minimum board space.

Precision Output: 1.0% tolerance output voltages available (A grade).

Low Noise: By adding an external bypass capacitor, output noise can be reduced to 30 µV (typical).

Ten output voltage versions, from 2.5V to 5.0V, are available as standard products.

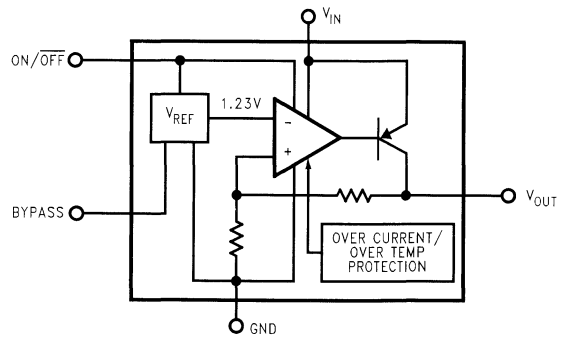
Features

- Ultra low dropout voltage
- Guaranteed 50 mA output current
- Typical dropout voltage 180 mV @ 80 mA
- Smallest possible size (SOT-23, micro SMD package)
- Requires minimum external components
- < 1 µA quiescent current when shutdown
- Low ground pin current at all loads
- Output voltage accuracy 1.0% (A Grade)
- High peak current capability (150 mA typical)
- Wide supply voltage range (16V max)
- Low Z_{OUT} 0.3Ω typical (10 Hz to 1 MHz)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range
- Custom voltages available

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



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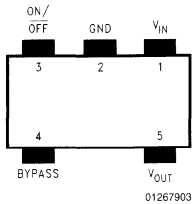
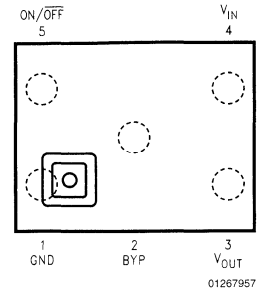
Connection Diagrams

5-Lead Small Outline Package (M5)



Top View
See NS Package Number MF05A
For ordering information see *Table 1*

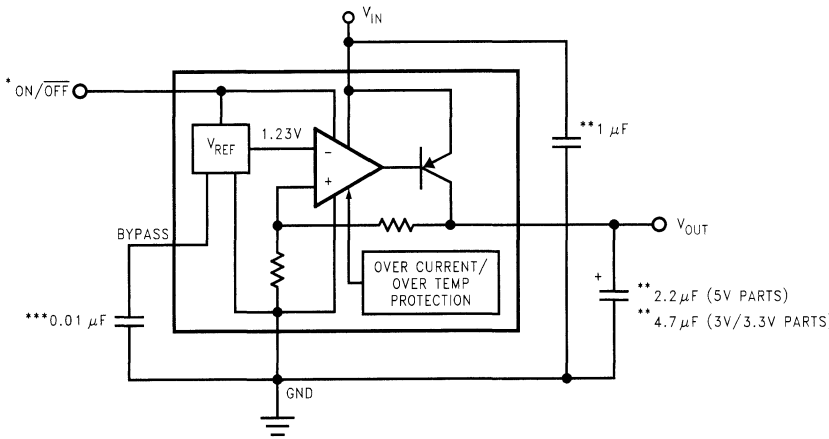
micro SMD, 5 Bump Package (BPA05)



Top View
See NS Package Number BPA05

Note: The actual physical placement of the package marking will vary from part to part. Package marking contains date code and lot traceability information, and will vary considerably. Package marking does not correlate to device type.

Basic Application Circuit



*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.

**Minimum capacitance is shown to insure stability over full load current range. More capacitance provides superior dynamic performance (see Application Hints).

***See Application Hints.

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5-Lead Small Outline Package (M5)				
2.5	A	LP2982AIM5X-2.5	L58A	3000 Units on Tape and Reel
2.5	A	LP2982AIM5-2.5	L58A	1000 Units on Tape and Reel
2.5	STD	LP2982IM5X-2.5	L58B	3000 Units on Tape and Reel
2.5	STD	LP2982IM5-2.5	L58B	1000Units on Tape and Reel
2.6	A	LP2982AIM5X-2.6	LBYA	3000 Units on Tape and Reel
2.6	A	LP2982AIM5-2.6	LBYA	1000 Units on Tape and Reel
2.6	STD	LP2982IM5X-2.6	LBYB	3000 Units on Tape and Reel
2.6	STD	LP2982IM5-2.6	LBYB	1000Units on Tape and Reel
2.8	A	LP2982AIM5X-2.8	L60A	3000 Units on Tape and Reel
2.8	A	LP2982AIM5-2.8	L60A	1000 Units on Tape and Reel
2.8	STD	LP2982IM5X-2.8	L60B	3000 Units on Tape and Reel
2.8	STD	LP2982IM5-2.8	L60B	1000 Units on Tape and Reel
3.0	A	LP2982AIM5X-3.0	L20A	3000 Units on Tape and Reel
3.0	A	LP2982AIM5-3.0	L20A	1000 Units on Tape and Reel
3.0	STD	LP2982IM5X-3.0	L20B	3000 Units on Tape and Reel
3.0	STD	LP2982IM5-3.0	L20B	1000 Units on Tape and Reel
3.3	A	LP2982AIM5X-3.3	L19A	3000 Units on Tape and Reel
3.3	A	LP2982AIM5-3.3	L19A	1000 Units on Tape and Reel
3.3	STD	LP2982IM5X-3.3	L19B	3000 Units on Tape and Reel
3.3	STD	LP2982IM5-3.3	L19B	1000 Units on Tape and Reel
3.6	A	LP2982AIM5X-3.6	L0BA	3000 Units on Tape and Reel
3.6	A	LP2982AIM5-3.6	L0BA	1000 Units on Tape and Reel
3.6	STD	LP2982IM5X-3.6	L0BB	3000 Units on Tape and Reel
3.6	STD	LP2982IM5-3.6	L0BB	1000 Units on Tape and Reel
3.8	A	LP2982AIM5X-3.8	L76A	3000 Units on Tape and Reel
3.8	A	LP2982AIM5-3.8	L76A	1000 Units on Tape and Reel
3.8	STD	LP2982IM5X-3.8	L76B	3000 Units on Tape and Reel
3.8	STD	LP2982IM5-3.8	L76B	1000 Units on Tape and Reel
4.0	A	LP2982AIM5X-4.0	L29A	3000 Units on Tape and Reel
4.0	A	LP2982AIM5-4.0	L29A	1000 Units on Tape and Reel
4.0	STD	LP2982IM5X-4.0	L29B	3000 Units on Tape and Reel
4.0	STD	LP2982IM5-4.0	L29B	1000 Units on Tape and Reel
4.5	A	LP2982AIM5X-4.5	LA8A	3000 Units on Tape and Reel
4.5	A	LP2982AIM5-4.5	LA8A	1000 Units on Tape and Reel
4.5	STD	LP2982IM5X-4.5	LA8B	3000 Units on Tape and Reel
4.5	STD	LP2982IM5-4.5	LA8B	1000 Units on Tape and Reel
4.7	A	LP2982AIM5X-4.7	L0HA	3000 Units on Tape and Reel
4.7	A	LP2982AIM5-4.7	L0HA	1000 Units on Tape and Reel
4.7	STD	LP2982IM5X-4.7	L0HB	3000 Units on Tape and Reel
4.7	STD	LP2982IM5-4.7	L0HB	1000 Units on Tape and Reel
5.0	A	LP2982AIM5X-5.0	L18A	3000 Units on Tape and Reel
5.0	A	LP2982AIM5-5.0	L18A	1000 Units on Tape and Reel
5.0	STD	LP2982IM5X-5.0	L18B	3000 Units on Tape and Reel
5.0	STD	LP2982IM5-5.0	L18B	1000 Units on Tape and Reel
5.3	A	LP2982AIM5X-5.3	LBZA	3000 Units on Tape and Reel
5.3	A	LP2982AIM5-5.3	LBZA	1000 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5.3	STD	LP2982IM5X-5.3	LBZB	3000 Units on Tape and Reel
5.3	STD	LP2982IM5-5.3	LBZB	1000 Units on Tape and Reel
micro SMD, 5 Bump Package (BPA05)				
2.8	A	LP2982AIBP-2.8		250 Units on Tape and Reel
2.8	A	LP2982AIBPX-2.8		3000 Units on Tape and Reel
2.8	STD	LP2982IBP-2.8		250 Units on Tape and Reel
2.8	STD	LP2982IBPX-2.8		3000 Units on Tape and Reel
3.0	A	LP2982AIBP-3.0		250 Units on Tape and Reel
3.0	A	LP2982AIBPX-3.0		3000 Units on Tape and Reel
3.0	STD	LP2982IBP-3.0		250 Units on Tape and Reel
3.0	STD	LP2982IBPX-3.0		3000 Units on Tape and Reel

National Semiconductor

LP2983
Micropower 150 mA Voltage Regulator in SOT-23 Package For Output Voltages ≤ 1.2V
Designed for Use with Very Low ESR Output Capacitors

General Description

The LP2983 is a 150 mA, fixed-output voltage regulator designed to provide tight voltage regulation in applications with output voltages ≤ 1.2V.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2983 delivers unequalled performance in all critical specifications:

Ground Pin Current: Typically 825 µA @ 150 mA load, and 75 µA @ 1 mA load.

Enhanced Stability: The LP2983 is stable with output capacitor ESR down to zero, which allows the use of ceramic capacitors on the output.

Smallest Possible Size: SOT-23 package uses absolute minimum board space.

Precision Output: 1% tolerance output voltages available (A grade).

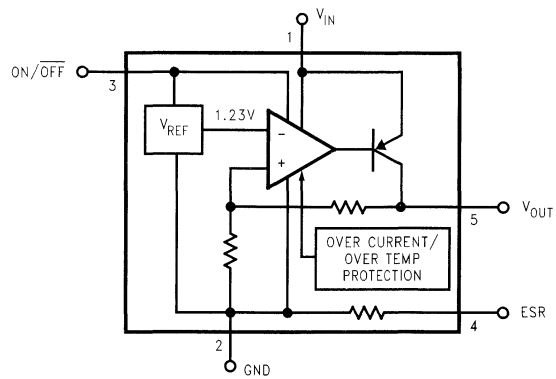
Features

- Guaranteed 150 mA output current
- Smallest possible size (SOT-23 package)
- Requires minimum external components
- Stable with low-ESR output capacitor
- Low ground pin current at all loads
- Output voltage accuracy 1% (A Grade)
- High peak current capability
- Wide supply voltage range (16V max)
- Low Z_{OUT}: 0.3Ω typical (10 Hz to 1 MHz)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



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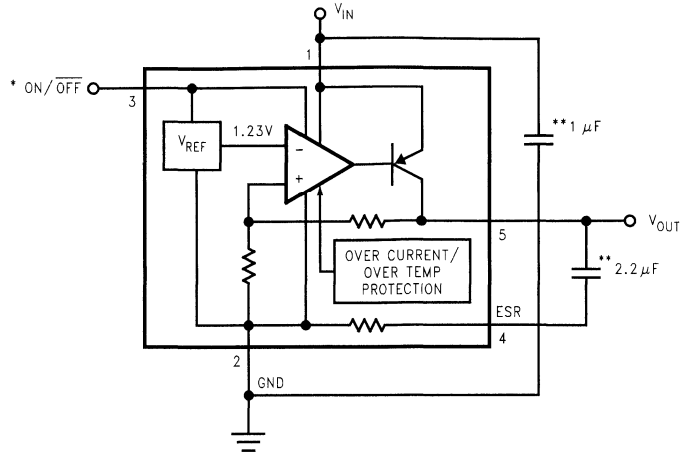
Basic Application Circuit

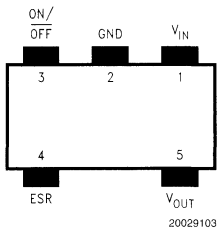


*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.

**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see Application Hints).

Connection Diagram

5-Lead Small Outline Package (M5)



Top View
See NS Package Number MF05A
For ordering information see *Table 1*

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
0.9	A	LP2983AIM5X-0.9	LEJA	3000 Units on Tape and Reel
0.9	A	LP2983AIM5-0.9	LEJA	1000 Units on Tape and Reel
0.9	STD	LP2983IM5X-0.9	LEJB	3000 Units on Tape and Reel
0.9	STD	LP2983IM5-0.9	LEJB	1000 Units on Tape and Reel
1.0	A	LP2983AIM5X-1.0	LENA	3000 Units on Tape and Reel
1.0	A	LP2983AIM5-1.0	LENA	1000 Units on Tape and Reel
1.0	STD	LP2983IM5X-1.0	LENB	3000 Units on Tape and Reel
1.0	STD	LP2983IM5-1.0	LENB	1000 Units on Tape and Reel
1.2	A	LP2983AIM5X-1.2	LELA	3000 Units on Tape and Reel
1.2	A	LP2983AIM5-1.2	LELA	1000 Units on Tape and Reel
1.2	STD	LP2983IM5X-1.2	LELB	3000 Units on Tape and Reel
1.2	STD	LP2983IM5-1.2	LELB	1000 Units on Tape and Reel

National Semiconductor

LP2985
Micropower 150 mA Low-Noise Ultra Low-Dropout Regulator in SOT-23 and micro SMD Packages
Designed for Use with Very Low ESR Output Capacitors

General Description

The LP2985 is a 150 mA, fixed-output voltage regulator designed to provide ultra low-dropout and low noise in battery powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2985 delivers unequalled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 300 mV @ 150 mA load, and 7 mV @ 1 mA load.

Ground Pin Current: Typically 850 µA @ 150 mA load, and 75 µA @ 1 mA load.

Enhanced Stability: The LP2985 is stable with output capacitor ESR as low as 5 mΩ, which allows the use of ceramic capacitors on the output.

Sleep Mode: Less than 1 µA quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size: SOT-23 and micro SMD packages use absolute minimum board space.

Precision Output: 1% tolerance output voltages available (A grade).

Low Noise: By adding a 10 nF bypass capacitor, output noise can be reduced to 30 µV (typical).

Multiple voltage options, from 2.5V to 5.0V, are available as standard products. Consult factory for custom voltages.

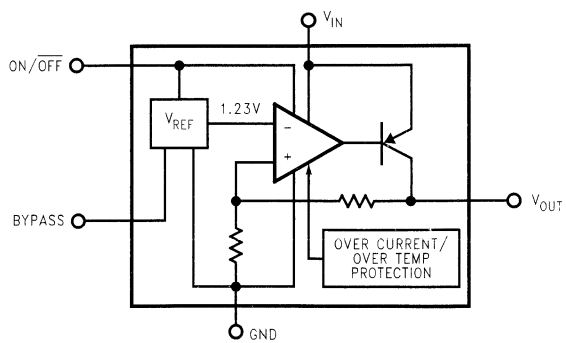
Features

- Ultra low dropout voltage
- Guaranteed 150 mA output current
- Smallest possible size (SOT-23, micro SMD package)
- Requires minimum external components
- Stable with low-ESR output capacitor
- <1 µA quiescent current when shut down
- Low ground pin current at all loads
- Output voltage accuracy 1% (A Grade)
- High peak current capability
- Wide supply voltage range (16V max)
- Low Z_{OUT}: 0.3Ω typical (10 Hz to 1 MHz)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range
- Custom voltages available

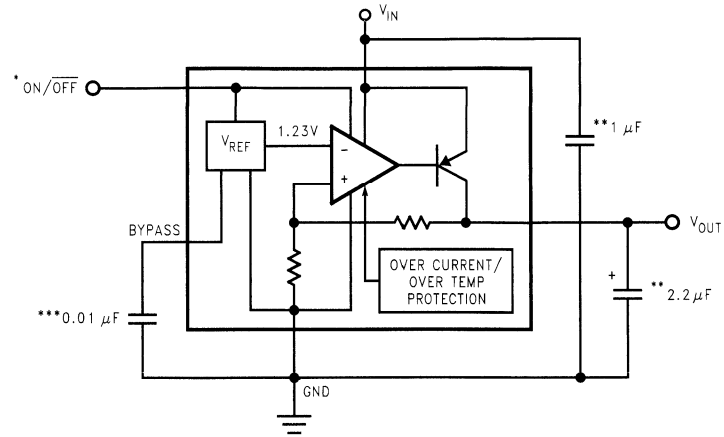
Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



Basic Application Circuit



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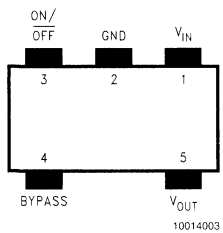
*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.

**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see Application Hints).

***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see Application Hints).

Connection Diagrams

5-Lead Small Outline Package (M5)



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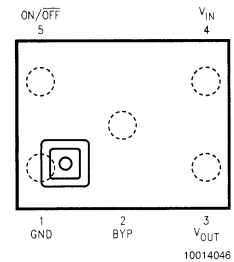
Top View
See NS Package Number MF05A
For ordering information see *Table 1*

micro SMD, 5 Bump Package (BPA05)



10014046

Top View
See NS Package Number BPA05

Note: The actual physical placement of the package marking will vary from part to part. Package marking contains date code and lot traceability information, and will vary considerably. Package marking does not correlate to device type.

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5-Lead Small Outline Package (M5)				
For output voltages ≤ 2.3V, refer to LP2985LV datasheet.				
2.5	A	LP2985AIM5X-2.5	LAUA	3000 Units on Tape and Reel
2.5	A	LP2985AIM5-2.5	LAUA	1000 Units on Tape and Reel
2.5	STD	LP2985IM5X-2.5	LAUB	3000 Units on Tape and Reel
2.5	STD	LP2985IM5-2.5	LAUB	1000 Units on Tape and Reel
2.6	A	LP2985AIM5X-2.6	LCEA	3000 Units on Tape and Reel
2.6	A	LP2985AIM5-2.6	LCEA	1000 Units on Tape and Reel
2.6	STD	LP2985IM5X-2.6	LCEB	3000 Units on Tape and Reel
2.6	STD	LP2985IM5-2.6	LCEB	1000 Units on Tape and Reel
2.7	A	LP2985AIM5X-2.7	LALA	3000 Units on Tape and Reel
2.7	A	LP2985AIM5-2.7	LALA	1000 Units on Tape and Reel
2.7	STD	LP2985IM5X-2.7	LALB	3000 Units on Tape and Reel
2.7	STD	LP2985IM5-2.7	LALB	1000 Units on Tape and Reel
2.8	A	LP2985AIM5X-2.8	L0KA	3000 Units on Tape and Reel
2.8	A	LP2985AIM5-2.8	L0KA	1000 Units on Tape and Reel
2.8	STD	LP2985IM5X-2.8	L0KB	3000 Units on Tape and Reel
2.8	STD	LP2985IM5-2.8	L0KB	1000 Units on Tape and Reel
2.9	A	LP2985AIM5X-2.9	LAXA	3000 Units on Tape and Reel
2.9	A	LP2985AIM5-2.9	LAXA	1000 Units on Tape and Reel
2.9	STD	LP2985IM5X-2.9	LAXB	3000 Units on Tape and Reel
2.9	STD	LP2985IM5-2.9	LAXB	1000 Units on Tape and Reel
3.0	A	LP2985AIM5X-3.0	L0OA	3000 Units on Tape and Reel
3.0	A	LP2985AIM5-3.0	L0OA	1000 Units on Tape and Reel
3.0	STD	LP2985IM5X-3.0	L0OB	3000 Units on Tape and Reel
3.0	STD	LP2985IM5-3.0	L0OB	1000 Units on Tape and Reel
3.1	A	LP2985AIM5X-3.1	L0PA	3000 Units on Tape and Reel
3.1	A	LP2985AIM5-3.1	L0PA	1000 Units on Tape and Reel
3.1	STD	LP2985IM5X-3.1	L0PB	3000 Units on Tape and Reel
3.1	STD	LP2985IM5-3.1	L0PB	1000 Units on Tape and Reel
3.2	A	LP2985AIM5X-3.2	L0QA	3000 Units on Tape and Reel
3.2	A	LP2985AIM5-3.2	L0QA	1000 Units on Tape and Reel
3.2	STD	LP2985IM5X-3.2	L0QB	3000 Units on Tape and Reel
3.2	STD	LP2985IM5-3.2	L0QB	1000 Units on Tape and Reel
3.3	A	LP2985AIM5X-3.3	L0RA	3000 Units on Tape and Reel
3.3	A	LP2985AIM5-3.3	L0RA	1000 Units on Tape and Reel
3.3	STD	LP2985IM5X-3.3	L0RB	3000 Units on Tape and Reel
3.3	STD	LP2985IM5-3.3	L0RB	1000 Units on Tape and Reel
3.5	A	LP2985AIM5X-3.5	LAIA	3000 Units on Tape and Reel
3.5	A	LP2985AIM5-3.5	LAIA	1000 Units on Tape and Reel
3.5	STD	LP2985IM5X-3.5	LAIB	3000 Units on Tape and Reel
3.5	STD	LP2985IM5-3.5	LAIB	1000 Units on Tape and Reel
3.6	A	LP2985AIM5X-3.6	L0SA	3000 Units on Tape and Reel
3.6	A	LP2985AIM5-3.6	L0SA	1000 Units on Tape and Reel
3.6	STD	LP2985IM5X-3.6	L0SB	3000 Units on Tape and Reel
3.6	STD	LP2985IM5-3.6	L0SB	1000 Units on Tape and Reel
3.8	A	LP2985AIM5X-3.8	L0YA	3000 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
3.8	A	LP2985AIM5-3.8	L0YA	1000 Units on Tape and Reel
3.8	STD	LP2985IM5X-3.8	L0YB	3000 Units on Tape and Reel
3.8	STD	LP2985IM5-3.8	L0YB	1000 Units on Tape and Reel
4.0	A	LP2985AIM5X-4.0	L0TA	3000 Units on Tape and Reel
4.0	A	LP2985AIM5-4.0	L0TA	1000 Units on Tape and Reel
4.0	STD	LP2985IM5X-4.0	L0TB	3000 Units on Tape and Reel
4.0	STD	LP2985IM5-4.0	L0TB	1000 Units on Tape and Reel
4.5	A	LP2985AIM5X-4.5	LA7A	3000 Units on Tape and Reel
4.5	A	LP2985AIM5-4.5	LA7A	1000 Units on Tape and Reel
4.5	STD	LP2985IM5X-4.5	LA7B	3000 Units on Tape and Reel
4.5	STD	LP2985IM5-4.5	LA7B	1000 Units on Tape and Reel
4.7	A	LP2985AIM5X-4.7	LAJA	3000 Units on Tape and Reel
4.7	A	LP2985AIM5-4.7	LAJA	1000 Units on Tape and Reel
4.7	STD	LP2985IM5X-4.7	LAJB	3000 Units on Tape and Reel
4.7	STD	LP2985IM5-4.7	LAJB	1000 Units on Tape and Reel
4.8	A	LP2985AIM5X-4.8	LAKA	3000 Units on Tape and Reel
4.8	A	LP2985AIM5-4.8	LAKA	1000 Units on Tape and Reel
4.8	STD	LP2985IM5X-4.8	LAKB	3000 Units on Tape and Reel
4.8	STD	LP2985IM5-4.8	LAKB	1000 Units on Tape and Reel
5.0	A	LP2985AIM5X-5.0	L0UA	3000 Units on Tape and Reel
5.0	A	LP2985AIM5-5.0	L0UA	1000 Units on Tape and Reel
5.0	STD	LP2985IM5X-5.0	L0UB	3000 Units on Tape and Reel
5.0	STD	LP2985IM5-5.0	L0UB	1000 Units on Tape and Reel
5.3	A	LP2985AIM5X-5.3	LFYA	3000 Units on Tape and Reel
5.3	A	LP2985AIM5-5.3	LFYA	1000 Units on Tape and Reel
5.3	STD	LP2985IM5X-5.3	LFYB	3000 Units on Tape and Reel
5.3	STD	LP2985IM5-5.3	LFYB	1000 Units on Tape and Reel
micro SMD, 5 Bump Package (BPA05)				
2.4	A	LP2985AIBP-2.4		250 Units on Tape and Reel
2.4	A	LP2985AIBPX-2.4		3000 Units on Tape and Reel
2.4	STD	LP2985IBP-2.4		250 Units on Tape and Reel
2.4	STD	LP2985IBPX-2.4		3000 Units on Tape and Reel
2.5	A	LP2985AIBP-2.5		250 Units on Tape and Reel
2.5	A	LP2985AIBPX-2.5		3000 Units on Tape and Reel
2.5	STD	LP2985IBP-2.5		250 Units on Tape and Reel
2.5	STD	LP2985IBPX-2.5		3000 Units on Tape and Reel
2.6	A	LP2985AIBP-2.6		250 Units on Tape and Reel
2.6	A	LP2985AIBPX-2.6		3000 Units on Tape and Reel
2.6	STD	LP2985IBP-2.6		250 Units on Tape and Reel
2.6	STD	LP2985IBPX-2.6		3000 Units on Tape and Reel
2.8	A	LP2985AIBP-2.8		250 Units on Tape and Reel
2.8	A	LP2985AIBPX-2.8		3000 Units on Tape and Reel
2.8	STD	LP2985IBP-2.8		250 Units on Tape and Reel
2.8	STD	LP2985IBPX-2.8		3000 Units on Tape and Reel
2.9	A	LP2985AIBP-2.9		250 Units on Tape and Reel
2.9	A	LP2985AIBPX-2.9		3000 Units on Tape and Reel
2.9	STD	LP2985IBP-2.9		250 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
2.9	STD	LP2985IBPX-2.9		3000 Units on Tape and Reel
3.0	A	LP2985AIBP-3.0		250 Units on Tape and Reel
3.0	A	LP2985AIBPX-3.0		3000 Units on Tape and Reel
3.0	STD	LP2985IBP-3.0		250 Units on Tape and Reel
3.0	STD	LP2985IBPX-3.0		3000 Units on Tape and Reel
3.3	A	LP2985AIBP-3.3		250 Units on Tape and Reel
3.3	A	LP2985AIBPX-3.3		3000 Units on Tape and Reel
3.3	STD	LP2985IBPX-3.3		250 Units on Tape and Reel
3.3	STD	LP2985IBPX-3.3		3000 Units on Tape and Reel
3.6	A	LP2985AIBP-3.6		250 Units on Tape and Reel
3.6	A	LP2985AIBPX-3.6		3000 Units on Tape and Reel
3.6	STD	LP2985IBP-3.6		250 Units on Tape and Reel
3.6	STD	LP2985IBPX-3.6		3000 Units on Tape and Reel
4.0	A	LP2985AIBP-4.0		250 Units on Tape and Reel
4.0	A	LP2985AIBPX-4.0		3000 Units on Tape and Reel
4.0	STD	LP2985IBP-4.0		250 Units on Tape and Reel
4.0	STD	LP2985IBPX-4.0		3000 Units on Tape and Reel
5.0	A	LP2985AIBP-5.0		250 Units on Tape and Reel
5.0	A	LP2985AIBPX-5.0		3000 Units on Tape and Reel
5.0	STD	LP2985IBP-5.0		250 Units on Tape and Reel
5.0	STD	LP2985IBPX-5.0		3000 Units on Tape and Reel

National Semiconductor

LP2986
Micropower, 200 mA Ultra Low-Dropout Fixed or Adjustable Voltage Regulator

General Description

The LP2986 is a 200 mA precision LDO voltage regulator which offers the designer a higher performance version of the industry standard LP2951.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2986 delivers superior performance:

Dropout Voltage: Typically 180 mV @ 200 mA load, and 1 mV @ 1 mA load.

Ground Pin Current: Typically 1 mA @ 200 mA load, and 200 µA @ 10 mA load.

Sleep Mode: The LP2986 draws less than 1 µA quiescent current when shutdown pin is pulled low.

Error Flag: The built-in error flag goes low when the output drops approximately 5% below nominal.

Precision Output: The standard product versions available can be pin-strapped (using the internal resistive divider) to provide output voltages of 5.0V, 3.3V, or 3.0V with guaranteed accuracy of 0.5% ("A" grade) and 1% (standard grade) at room temperature.

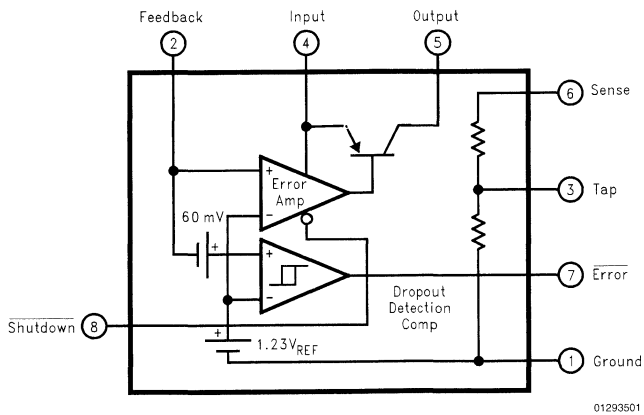
Features

- Ultra low dropout voltage
- Guaranteed 200 mA output current
- SO-8 and mini-SO8 surface mount packages
- <1 µA quiescent current when shutdown
- Low ground pin current at all loads
- 0.5% output voltage accuracy ("A" grade)
- High peak current capability (400 mA typical)
- Wide supply voltage range (16V max)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Camcorder, Personal Stereo, Camera

Block Diagram



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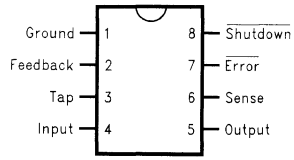
Connection Diagrams

Surface Mount Packages:



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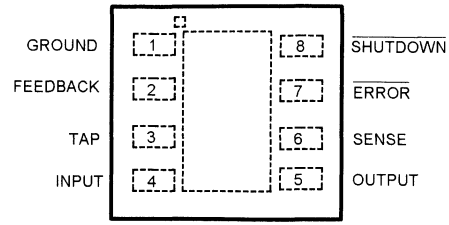
SO-8/Mini SO-8 Package
See NS Package Drawing Number M08A/MUA08A

8-Lead LLP Surface Mount Package



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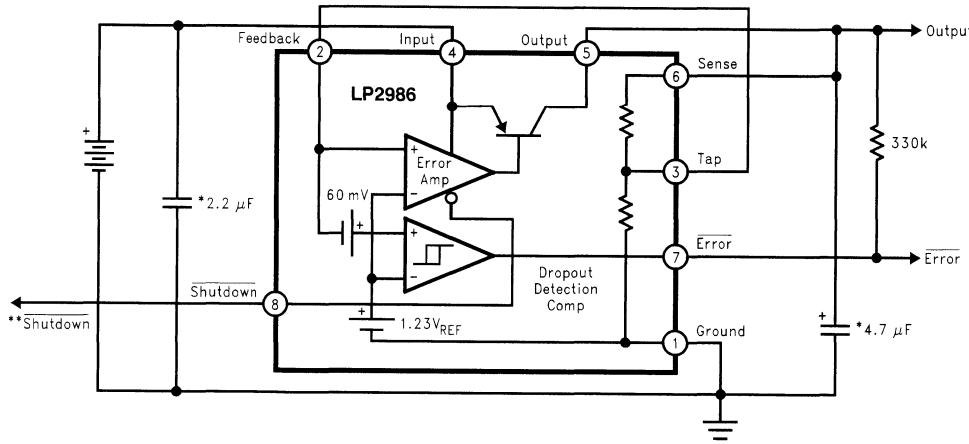
Top View
See NS Package Drawing Number LDC08A

Basic Application Circuits

Application Using Internal Resistive Divider



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

** Shutdown input must be actively terminated. Tie to V_{IN} if not used.

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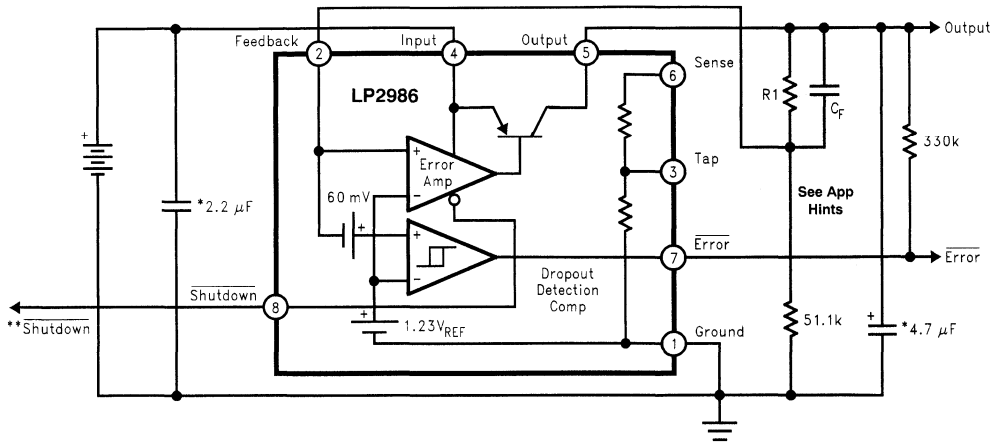
Basic Application Circuits (Continued)

Application Using External Divider



* Minimum capacitance shown to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

** Shutdown input must be actively terminated. Tie to V_{IN} if not used.

01293504

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
Mini SO-8				
5	A	LP2986AIMMX-5.0	L41A	3500 Units on Tape and Reel
5	A	LP2986AIMM-5.0	L41A	1000 Units on Tape and Reel
5	STD	LP2986IMMX-5.0	L41B	3500 Units on Tape and Reel
5	STD	LP2986IMM-5.0	L41B	1000 Units on Tape and Reel
3.3	A	LP2986AIMMX-3.3	L40A	3500 Units on Tape and Reel
3.3	A	LP2986AIMM-3.3	L40A	1000 Units on Tape and Reel
3.3	STD	LP2986IMMX-3.3	L40B	3500 Units on Tape and Reel
3.3	STD	LP2986IMM-3.3	L40B	1000 Units on Tape and Reel
3.0	A	LP2986AIMMX-3.0	L39A	3500 Units on Tape and Reel
3.0	A	LP2986AIMM-3.0	L39A	1000 Units on Tape and Reel
3.0	STD	LP2986IMMX-3.0	L39B	3500 Units on Tape and Reel
3.0	STD	LP2986IMM-3.0	L39B	1000 Units on Tape and Reel

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Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
SO-8				
5	A	LP2986AIMX-5.0	2986AIM5.0	2500 Units on Tape and Reel
5	A	LP2986AIM-5.0	2986AIM5.0	Shipped in Anti-Static Rails
5	STD	LP2986IMX-5.0	2986IM5.0	2500 Units on Tape and Reel
5	STD	LP2986IM-5.0	2986IM5.0	Shipped in Anti-Static Rails
3.3	A	LP2986AIMX-3.3	2986AIM3.3	2500 Units on Tape and Reel
3.3	A	LP2986AIM-3.3	2986AIM3.3	Shipped in Anti-Static Rails
3.3	STD	LP2986IMX-3.3	2986IM3.3	2500 Units on Tape and Reel
3.3	STD	LP2986IM-3.3	2986IM3.3	Shipped in Anti-Static Rails
3.0	A	LP2986AIMX-3.0	2986AIM3.0	2500 Units on Tape and Reel
3.0	A	LP2986AIM-3.0	2986AIM3.0	Shipped in Anti-Static Rails
3.0	STD	LP2986IMX-3.0	2986IM3.0	2500 Units on Tape and Reel
3.0	STD	LP2986IM-3.0	2986IM3.0	Shipped in Anti-Static Rails
8-Lead LLP				
5	A	LP2986AILD-5	L006A	1000 Units on Tape and Reel
5	A	LP2986AILDX-5	L006A	4500 Units on Tape and Reel
5	STD	LP2986ILD-5	L006AB	1000 Units on Tape and Reel
5	STD	LP2986ILDX-5	L006AB	4500 Units on Tape and Reel
3.3	A	LP2986AILD-3.3	L005A	1000 Units on Tape and Reel
3.3	A	LP2986AILDX-3.3	L005A	4500 Units on Tape and Reel
3.3	STD	LP2986ILD-3.3	L005AB	1000 Units on Tape and Reel
3.3	STD	LP2986ILDX-3.3	L005AB	4500 Units on Tape and Reel
3.0	A	LP2986AILD-3.0	L004A	1000 Units on Tape and Reel
3.0	A	LP2986AILDX-3.0	L004A	4500 Units on Tape and Reel
3.0	STD	LP2986ILD-3.0	L004AB	1000 Units on Tape and Reel
3.0	STD	LP2986ILDX-3.0	L004AB	4500 Units on Tape and Reel

National Semiconductor

LP2987/LP2988
Micropower, 200 mA Ultra Low-Dropout Voltage Regulator with Programmable Power-On Reset Delay; Low Noise Version Available (LP2988)

General Description

The LP2987/8 are fixed-output 200 mA precision LDO voltage regulators with power-ON reset delay which can be implemented using a single external capacitor.

The LP2988 is specifically designed for noise-critical applications. A single external capacitor connected to the Bypass pin reduces regulator output noise.

Using an optimized VIP™ (Vertically Integrated PNP) process, these regulators deliver superior performance:

Dropout Voltage: 180 mV @ 200 mA load, and 1 mV @ 1 mA load (typical).

Ground Pin Current: 1 mA @ 200 mA load, and 200 µA @ 10 mA load (typical).

Sleep Mode: The LP2987/8 draws less than 2 µA quiescent current when shutdown pin is held low.

Error Flag/Reset: The error flag goes low when the output drops approximately 5% below nominal. This pin also provides a power-ON reset signal if a capacitor is connected to the DELAY pin.

Precision Output: Standard product versions of the LP2987 and LP2988 are available with output voltages of 5.0V, 3.8V, 3.3V, 3.2V, 3.0V, or 2.8V, with guaranteed accuracy of 0.5% ("A" grade) and 1% (standard grade) at room temperature.

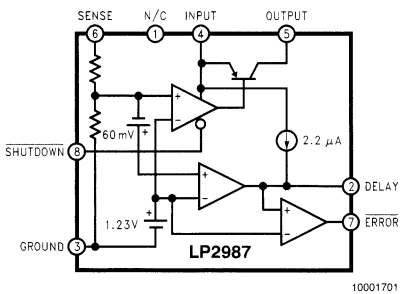
Features

- Ultra low dropout voltage
- Power-ON reset delay requires only one component
- Bypass pin for reduced output noise (LP2988)
- Guaranteed continuous output current 200 mA
- Guaranteed peak output current > 250 mA
- SO-8 and mini SO-8 surface mount packages
- <2 µA quiescent current when shutdown
- Low ground pin current at all loads
- 0.5% output voltage accuracy ("A" grade)
- Wide supply voltage range (16V max)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Camcorder, Personal Stereo, Camera

Block Diagrams



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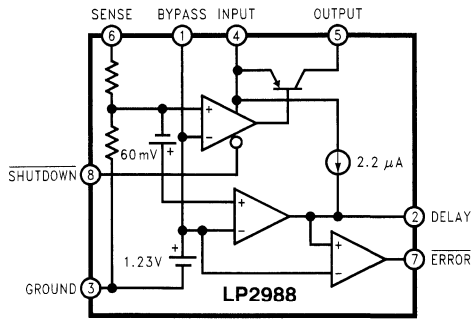

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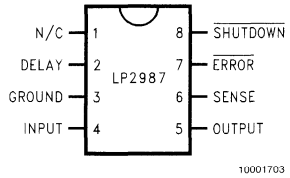
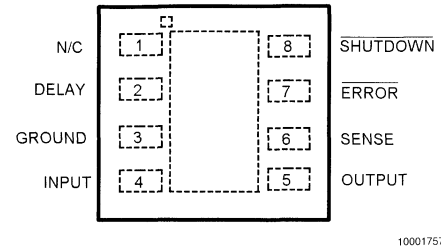
Connection Diagrams (LP2987)

Surface Mount Packages:



Top View
SO-8/Mini SO-8 Package
See NS Package Drawing Number M08A/MUA08A
For ordering information, refer to *Table 1* in this document.

8-Lead LLP Surface Mount Package



Top View
See NS Package Drawing Number LDC08A

Ordering Information (LP2987)

TABLE 1. Package Marking and Ordering Information

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
5	A	LP2987AIMMX-5.0	L44A	3500 Units on Tape and Reel
5	A	LP2987AIMM-5.0	L44A	1000 Units on Tape and Reel
5	STD	LP2987IMMX-5.0	L44B	3500 Units on Tape and Reel
5	STD	LP2987IMM-5.0	L44B	1000 Units on Tape and Reel
3.8	A	LP2987AIMMX-3.8	L96A	3500 Units on Tape and Reel
3.8	A	LP2987AIMM-3.8	L96A	1000 Units on Tape and Reel
3.8	STD	LP2987IMMX-3.8	L96B	3500 Units on Tape and Reel
3.8	STD	LP2987IMM-3.8	L96B	1000 Units on Tape and Reel
3.3	A	LP2987AIMMX-3.3	L43A	3500 Units on Tape and Reel
3.3	A	LP2987AIMM-3.3	L43A	1000 Units on Tape and Reel
3.3	STD	LP2987IMMX-3.3	L43B	3500 Units on Tape and Reel
3.3	STD	LP2987IMM-3.3	L43B	1000 Units on Tape and Reel
3.2	A	LP2987AIMMX-3.2	L66A	3500 Units on Tape and Reel
3.2	A	LP2987AIMM-3.2	L66A	1000 Units on Tape and Reel
3.2	STD	LP2987IMMX-3.2	L66B	3500 Units on Tape and Reel
3.2	STD	LP2987IMM-3.2	L66B	1000 Units on Tape and Reel
3.0	A	LP2987AIMMX-3.0	L42A	3500 Units on Tape and Reel
3.0	A	LP2987AIMM-3.0	L42A	1000 Units on Tape and Reel

Ordering Information (LP2987) (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
3.0	STD	LP2987IMMX-3.0	L42B	3500 Units on Tape and Reel
3.0	STD	LP2987IMM-3.0	L42B	1000 Units on Tape and Reel
2.8	A	LP2987AIMMX-2.8	L89A	3500 Units on Tape and Reel
2.8	A	LP2987AIMM-2.8	L89A	1000 Units on Tape and Reel
2.8	STD	LP2987IMMX-2.8	L89B	3500 Units on Tape and Reel
2.8	STD	LP2987IMM-2.8	L89B	1000 Units on Tape and Reel
5	A	LP2987AIMX-5.0	2987AIM5.0	2500 Units on Tape and Reel
5	A	LP2987AIM-5.0	2987AIM5.0	Shipped in Anti-Static Rails
5	STD	LP2987IMX-5.0	2987IM5.0	2500 Units on Tape and Reel
5	STD	LP2987IM-5.0	2987IM5.0	Shipped in Anti-Static Rails
3.8	A	LP2987AIMX-3.8	2987AIM3.8	2500 Units on Tape and Reel
3.8	A	LP2987AIM-3.8	2987AIM3.8	Shipped in Anti-Static Rails
3.8	STD	LP2987IMX-3.8	2987IM3.8	2500 Units on Tape and Reel
3.8	STD	LP2987IM-3.8	2987IM3.8	Shipped in Anti-Static Rails
3.3	A	LP2987AIMX-3.3	2987AIM3.3	2500 Units on Tape and Reel
3.3	A	LP2987AIM-3.3	2987AIM3.3	Shipped in Anti-Static Rails
3.3	STD	LP2987IMX-3.3	2987IM3.3	2500 Units on Tape and Reel
3.3	STD	LP2987IM-3.3	2987IM3.3	Shipped in Anti-Static Rails
3.2	A	LP2987AIMX-3.2	2987AIM3.2	2500 Units on Tape and Reel
3.2	A	LP2987AIM-3.2	2987AIM3.2	Shipped in Anti-Static Rails
3.2	STD	LP2987IMX-3.2	2987IM3.2	2500 Units on Tape and Reel
3.2	STD	LP2987AIM-3.2	2987IM3.2	Shipped in Anti-Static Rails
3.0	A	LP2987IMX-3.0	2987AIM3.0	2500 Units on Tape and Reel
3.0	A	LP2987AIM-3.0	2987AIM3.0	Shipped in Anti-Static Rails
3.0	STD	LP2987IMX-3.0	2987IM3.0	2500 Units on Tape and Reel

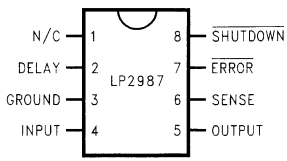
Ordering Information (LP2987) (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
3.0	STD	LP2987IM-3.0	2987IM3.0	Shipped in Anti-Static Rails
2.8	A	LP2987AIMX-2.8	2987AIM2.8	2500 Units on Tape and Reel
2.8	A	LP2987AIM-2.8	2987AIM2.8	Shipped in Anti-Static Rails
2.8	STD	LP2987IMX-2.8	2987IM2.8	2500 Units on Tape and Reel
2.8	STD	LP2987AIM-2.8	2987AIM2.8	Shipped in Anti-Static Rails
8-Lead LLP				
5	A	LP2987AILD-5	L009A	1000 Units on Tape and Reel
5	A	LP2987AILDX-5	L009A	4500 Units on Tape and Reel
5	STD	LP2987ILD-5	L009AB	1000 Units on Tape and Reel
5	STD	LP2987ILDX-5	L009AB	4500 Units on Tape and Reel
3.3	A	LP2987AILD-3.3	L008A	1000 Units on Tape and Reel
3.3	A	LP2987AILDX-3.3	L008A	4500 Units on Tape and Reel
3.3	STD	LP2987ILD-3.3	L008AB	1000 Units on Tape and Reel
3.3	STD	LP2987ILDX-3.3	L008AB	4500 Units on Tape and Reel
3.0	A	LP2987AILD-3.0	L007A	1000 Units on Tape and Reel
3.0	A	LP2987AILDX-3.0	L007A	4500 Units on Tape and Reel
3.0	STD	LP2987ILD-3.0	L007AB	1000 Units on Tape and Reel
3.0	STD	LP2987ILDX-3.0	L007AB	4500 Units on Tape and Reel

Connection Diagrams (LP2988)

Surface Mount Packages:



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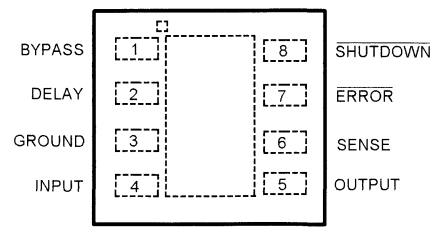
Top View
SO-8/Mini SO-8 Package
See NS Package Drawing Number M08A/MUA08A
For ordering information, refer to *Table 1* in this document.

8-Lead LLP Surface Mount Package



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Top View
See NS Package Drawing Number LDC08A

Ordering Information (LP2988)

TABLE 2. Package Marking and Ordering Information

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
5.0	A	LP2988AIMMX-5.0	L51A	3500 Units on Tape and Reel
5.0	A	LP2988AIMM-5.0	L51A	1000 Units on Tape and Reel
5.0	STD	LP2988IMMX-5.0	L51B	3500 Units on Tape and Reel
5.0	STD	LP2988IMM-5.0	L51B	1000 Units on Tape and Reel
3.8	A	LP2988AIMMX-3.8	L0AA	3500 Units on Tape and Reel
3.8	A	LP2988AIMM-3.8	L0AA	1000 Units on Tape and Reel
3.8	STD	LP2988IMMX-3.8	L0AB	3500 Units on Tape and Reel
3.8	STD	LP2988IMM-3.8	L0AB	1000 Units on Tape and Reel
3.3	A	LP2988AIMMX-3.3	L50A	3500 Units on Tape and Reel
3.3	A	LP2988AIMM-3.3	L50A	1000 Units on Tape and Reel
3.3	STD	LP2988IMMX-3.3	L50B	3500 Units on Tape and Reel
3.3	STD	LP2988IMM-3.3	L50B	1000 Units on Tape and Reel
3.2	A	LP2988AIMMX-3.2	L67A	3500 Units on Tape and Reel
3.2	A	LP2988AIMM-3.2	L67A	1000 Units on Tape and Reel
3.2	STD	LP2988IMMX-3.2	L67B	3500 Units on Tape and Reel
3.2	STD	LP2988IMM-3.2	L67B	1000 Units on Tape and Reel
3.0	A	LP2988AIMMX-3.0	L49A	3500 Units on Tape and Reel
3.0	A	LP2988AIMM-3.0	L49A	1000 Units on Tape and Reel
3.0	STD	LP2988IMMX-3.0	L49B	3500 Units on Tape and Reel
3.0	STD	LP2988IMM-3.0	L49B	1000 Units on Tape and Reel
2.8	A	LP2988AIMMX-2.8	L0IA	3500 Units on Tape and Reel
2.8	A	LP2988AIMM-2.8	L0IA	1000 Units on Tape and Reel
2.8	STD	LP2988IMMX-2.8	L0IB	3500 Units on Tape and Reel
2.8	STD	LP2988IMM-2.8	L0IB	1000 Units on Tape and Reel
2.7	A	LP2988AIMMX-2.7	LCVA	3500 Units on Tape and Reel

Ordering Information (LP2988) (Continued)

TABLE 2. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
2.7	A	LP2988AIMM-2.7	LCVA	1000 Units on Tape and Reel
2.7	STD	LP2988IMMX-2.7	LCVB	3500 Units on Tape and Reel
2.7	STD	LP2988IMM-2.7	LCVB	1000 Units on Tape and Reel
2.5	A	LP2988AIMMX-2.5	L99A	3500 Units on Tape and Reel
2.5	A	LP2988AIMM-2.5	L99A	1000 Units on Tape and Reel
2.5	STD	LP2988IMMX-2.5	L99B	3500 Units on Tape and Reel
2.5	STD	LP2988IMM-2.5	L99B	1000 Units on Tape and Reel
5.0	A	LP2988AIMX-5.0	2988AIM5.0	2500 Units on Tape and Reel
5.0	A	LP2988AIM-5.0	2988AIM5.0	Shipped in Anti-Static Rails
5.0	STD	LP2988IMX-5.0	2988IM5.0	2500 Units on Tape and Reel
5.0	STD	LP2988IM-5.0	2988IM5.0	Shipped in Anti-Static Rails
3.8	A	LP2988AIMX-3.8	2988AIM3.8	2500 Units on Tape and Reel
3.8	A	LP2988AIM-3.8	2988AIM3.8	Shipped in Anti-Static Rails
3.8	STD	LP2988IMX-3.8	2988IM3.8	2500 Units on Tape and Reel
3.8	STD	LP2988IM-3.8	2988IM3.8	Shipped in Anti-Static Rails
3.3	A	LP2988AIMX-3.3	2988AIM3.3	2500 Units on Tape and Reel
3.3	A	LP2988AIM-3.3	2988AIM3.3	Shipped in Anti-Static Rails
3.3	STD	LP2988IMX-3.3	2988IM3.3	2.5k Units on Tape and Reel
3.3	STD	LP2988IM-3.3	2988IM3.3	Shipped in Anti-Static Rails
3.2	A	LP2988AIMX-3.2	2988AIM3.2	2500 Units on Tape and Reel
3.2	A	LP2988AIM-3.2	2988AIM3.2	Shipped in Anti-Static Rails
3.2	STD	LP2988IMX-3.2	2988IM3.2	2500 Units on Tape and Reel
3.2	STD	LP2988IM-3.2	2988IM3.2	Shipped in Anti-Static Rails
3.0	A	LP2988AIMX-3.0	2988AIM3.0	2500 Units on Tape and Reel
3.0	A	LP2988AIM-3.0	2988AIM3.0	Shipped in Anti-Static Rails

Ordering Information (LP2988) (Continued)

TABLE 2. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
3.0	STD	LP2988IMX-3.0	2988IM3.0	2500 Units on Tape and Reel
3.0	STD	LP2988IM-3.0	2988IM3.0	Shipped in Anti-Static Rails
2.8	A	LP2988AIMX-2.8	2988AIM2.8	2500 Units on Tape and Reel
2.8	A	LP2988AIM-2.8	2988AIM2.8	Shipped in Anti-Static Rails
2.8	STD	LP2988IMX-2.8	2988IM2.8	2500 Units on Tape and Reel
2.8	STD	LP2988IM-2.8	2988IM2.8	Shipped in Anti-Static Rails
2.7	A	LP2988AIMX-2.7	2988AIM2.7	2500 Units on Tape and Reel
2.7	A	LP2988AIM-2.7	2988AIM2.7	Shipped in Anti-Static Rails
2.7	STD	LP2988IMX-2.7	2988IM2.7	2500 Units on Tape and Reel
2.7	STD	LP2988IM-2.7	2988IM2.7	Shipped in Anti-Static Rails
2.5	A	LP2988AIMX-2.5	2988AIM2.5	2500 Units on Tape and Reel
2.5	A	LP2988AIM-2.5	2988AIM2.5	Shipped in Anti-Static Rails
2.5	STD	LP2988IMX-2.5	2988IM2.5	2500 Units on Tape and Reel
2.5	STD	LP2988IM-2.5	2988IM2.5	Shipped in Anti-Static Rails
8-Lead LLP				
5	A	LP2988AILD-5	L01DA	1000 Units on Tape and Reel
5	A	LP2988AILDX-5	L01DA	4500 Units on Tape and Reel
5	STD	LP2988ILD-5	L01DAB	1000 Units on Tape and Reel
5	STD	LP2988ILDX-5	L01DAB	4500 Units on Tape and Reel
3.3	A	LP2988AILD-3.3	L01CA	1000 Units on Tape and Reel
3.3	A	LP2988AILDX-3.3	L01CA	4500 Units on Tape and Reel
3.3	STD	LP2988ILD-3.3	L01CAB	1000 Units on Tape and Reel
3.3	STD	LP2988ILDX-3.3	L01CAB	4500 Units on Tape and Reel
3.0	A	LP2988AILD-3.0	L01BA	1000 Units on Tape and Reel
3.0	A	LP2988AILDX-3.0	L01BA	4500 Units on Tape and Reel

Ordering Information (LP2988) (Continued)

TABLE 2. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
3.0	STD	LP2988ILD-3.0	L01BAB	1000 Units on Tape and Reel
3.0	STD	LP2988ILDX-3.0	L01BAB	4500 Units on Tape and Reel
2.5	A	LP2988AILD-2.5	L01AA	1000 Units on Tape and Reel
2.5	A	LP2988AILDX-2.5	L01AA	4500 Units on Tape and Reel
2.5	STD	LP2988ILD-2.5	L01AAB	1000 Units on Tape and Reel
2.5	STD	LP2988ILDX-2.5	L01AAB	4500 Units on Tape and Reel

National Semiconductor

LP2989
Micropower/Low Noise, 500 mA Ultra Low-Dropout Regulator
For Use with Ceramic Output Capacitors

General Description

The LP2989 is a fixed-output 500 mA precision LDO regulator designed for use with ceramic output capacitors.

Output noise can be reduced to 18μV (typical) by connecting an external 10 nF capacitor to the bypass pin.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2989 delivers superior performance:

Dropout Voltage: Typically 310 mV @ 500 mA load, and 1 mV @ 100 μA load.

Ground Pin Current: Typically 3 mA @ 500 mA load, and 110 μA @ 100 μA load.

Sleep Mode: The LP2989 draws less than 0.8 μA quiescent current when shutdown pin is pulled low.

Error Flag: The built-in error flag goes low when the output drops approximately 5% below nominal.

Precision Output: Guaranteed output voltage accuracy is 0.75% ("A" grade) and 1.25% (standard grade) at room temperature.

For output voltages < 2V, see LP2989LV datasheet.

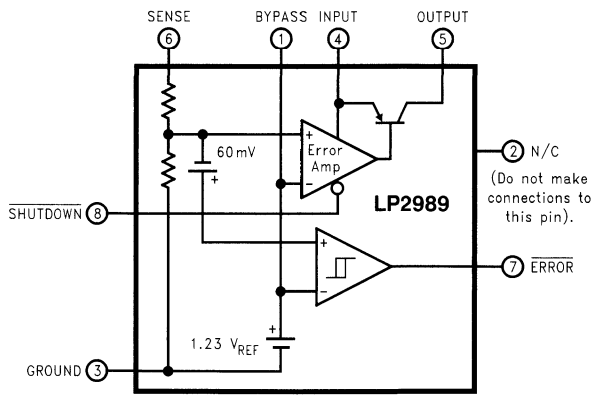
Features

- Ultra low dropout voltage
- Guaranteed 500 mA continuous output current
- Very low output noise with external capacitor
- SO-8, Mini SO-8, 8 Lead LLP surface mount packages
- <0.8 μA quiescent current when shutdown
- Low ground pin current at all loads
- 0.75% output voltage accuracy ("A" grade)
- High peak current capability (800 mA typical)
- Wide supply voltage range (16V max)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

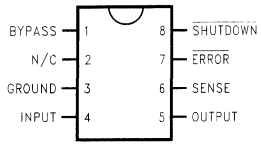
- Notebook/Desktop PC
- PDA/Palmtop Computer
- Wireless Communication Terminals
- SMPS Post-Regulator

Block Diagram



Connection Diagrams

Surface Mount Packages:



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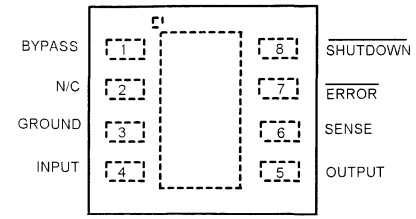
SO-8/Mini SO-8 Package
See NS Package Drawing Numbers M08A/MUA08A

8 Lead LLP Surface Mount Package



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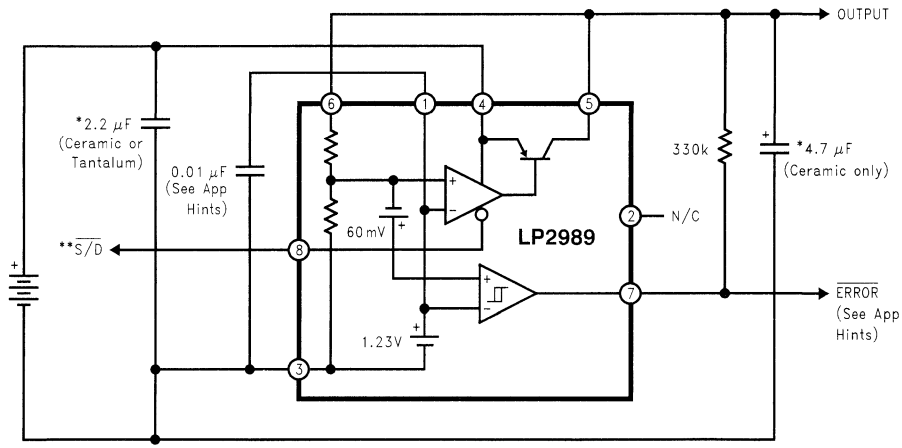
Top View
See NS Package Number LDC08A

Basic Application Circuit



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*Capacitance values shown are minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response. See Application Hints.

**Shutdown must be actively terminated (see App. Hints). Tie to INPUT (Pin4) if not used

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
8 Lead LLP				
2.5	A	LP2989AILD-2.5	L01FA	1000 Units on Tape and Reel
2.5	A	LP2989AILDX-2.5	L01FA	4500 Units on Tape and Reel
2.5	STD	LP2989ILD-2.5	L01FAB	1000 Units on Tape and Reel
2.5	STD	LP2989ILDX-2.5	L01FAB	4500 Units on Tape and Reel
2.8	A	LP2989AILD-2.8	L000A	1000 Units on Tape and Reel
2.8	A	LP2989AILDX-2.8	L000A	4500 Units on Tape and Reel
2.8	STD	LP2989ILD-2.8	L000AB	1000 Units on Tape and Reel
2.8	STD	LP2989ILDX-2.8	L000AB	4500 Units on Tape and Reel
2.85	A	LP2989AILD-285	L01TA	1000 Units on Tape and Reel
2.85	A	LP2989AILDX-285	L01TA	4500 Units on Tape and Reel
2.85	STD	LP2989ILD-285	L01TAB	1000 Units on Tape and Reel
2.85	STD	LP2989ILDX-285	L01TAB	4500 Units on Tape and Reel
3.0	A	LP2989AILD-3.0	L01HA	1000 Units on Tape and Reel
3.0	A	LP2989AILDX-3.0	L01HA	4500 Units on Tape and Reel
3.0	STD	LP2989ILD-3.0	L01HAB	1000 Units on Tape and Reel
3.0	STD	LP2989ILDX-3.0	L01HAB	4500 Units on Tape and Reel
3.3	A	LP2989AILD-3.3	L01JA	1000 Units on Tape and Reel
3.3	A	LP2989AILDX-3.3	L01JA	4500 Units on Tape and Reel
3.3	STD	LP2989ILD-3.3	L01JAB	1000 Units on Tape and Reel
3.3	STD	LP2989ILDX-3.3	L01JAB	4500 Units on Tape and Reel
4.0	A	LP2989AILD-4.0	L01LA	1000 Units on Tape and Reel
4.0	A	LP2989AILDX-4.0	L01LA	4500 Units on Tape and Reel
4.0	STD	LP2989ILD-4.0	L01LAB	1000 Units on Tape and Reel
4.0	STD	LP2989ILDX-4.0	L01LAB	4500 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
5.0	A	LP2989AILD-5.0	L01KA	1000 Units on Tape and Reel
5.0	A	LP2989AILDX-5.0	L01KA	4500 Units on Tape and Reel
5.0	STD	LP2989ILD-5.0	L01KAB	1000 Units on Tape and Reel
5.0	STD	LP2989ILDX-5.0	L01KAB	4500 Units on Tape and Reel
8 Lead MSOP (MM)				
2.5	A	LP2989AIMM-2.5	LA0A	1000 Units on Tape and Reel
2.5	A	LP2989AIMMX-2.5	LA0A	3500 Units on Tape and Reel
2.5	STD	LP2989IMM-2.5	LA0B	1000 Units on Tape and Reel
2.5	STD	LP2989IMMX-2.5	LA0B	3500 Units on Tape and Reel
2.8	A	LP2989AIMM-2.8	LA6A	1000 Units on Tape and Reel
2.8	A	LP2989AIMMX-2.8	LA6A	3500 Units on Tape and Reel
2.8	STD	LP2989IMM-2.8	LA6B	1000 Units on Tape and Reel
2.8	STD	LP2989IMMX-2.8	LA6B	3500 Units on Tape and Reel
3.0	A	LP2989AIMM-3.0	LA1A	1000 Units on Tape and Reel
3.0	A	LP2989AIMMX-3.0	LA1A	3500 Units on Tape and Reel
3.0	STD	LP2989IMM-3.0	LA1B	1000 Units on Tape and Reel
3.0	STD	LP2989IMMX-3.0	LA1B	3500 Units on Tape and Reel
3.3	A	LP2989AIMM-3.3	LA2A	1000 Units on Tape and Reel
3.3	A	LP2989AIMMX-3.3	LA2A	3500 Units on Tape and Reel
3.3	STD	LP2989IMM-3.3	LA2B	1000 Units on Tape and Reel
3.3	STD	LP2989IMMX-3.3	LA2B	3500 Units on Tape and Reel
5.0	A	LP2989AIMM-5.0	LA4A	1000 Units on Tape and Reel
5.0	A	LP2989AIMMX-5.0	LA4A	3500 Units on Tape and Reel
5.0	STD	LP2989IMM-5.0	LA4B	1000 Units on Tape and Reel
5.0	STD	LP2989IMMX-5.0	LA4B	3500 Units on Tape and Reel

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Grade	Order Information	Package Marking	Supplied as:
SO-8 (M)				
2.5	A	LP2989AIMX-2.5	LP2989AIM2.5	2500 Units on Tape and Reel
2.5	A	LP2989AIM-2.5	LP2989AIM2.5	Shipped in Anti-Static Rails
2.5	STD	LP2989IMX-2.5	LP2989IM2.5	2500 Units on Tape and Reel
2.5	STD	LP2989IM-2.5	LP2989IM2.5	Shipped in Anti-Static Rails
3.3	A	LP2989AIMX-3.3	LP2989AIM3.3	2500 Units on Tape and Reel
3.3	A	LP2989AIM-3.3	LP2989AIM3.3	Shipped in Anti-Static Rails
3.3	STD	LP2989IMX-3.3	LP2989IM3.3	2500 Units on Tape and Reel
3.3	STD	LP2989IM-3.3	LP2989IM3.3	Shipped in Anti-Static Rails
5.0	A	LP2989AIMX-5.0	LP2989AIM5.0	2500 Units on Tape and Reel
5.0	A	LP2989AIM-5.0	LP2989AIM5.0	Shipped in Anti-Static Rails
5.0	STD	LP2989IMX-5.0	LP2989IM5.0	2500 Units on Tape and Reel
5.0	STD	LP2989IM-5.0	LP2989IM5.0	Shipped in Anti-Static Rails

For output voltages < 2V, see LP2989LV datasheet.

National Semiconductor

LP2992
Micropower 250 mA Low-Noise Ultra Low-Dropout Regulator in SOT-23 and LLP Packages
Designed for Use with Very Low ESR Output Capacitors

General Description

The LP2992 is a 250 mA, fixed-output voltage regulator designed to provide ultra low-dropout and low noise in battery powered applications.

Using an optimized VIP™ (Vertically Integrated PNP) process, the LP2992 delivers unequalled performance in all specifications critical to battery-powered designs:

Dropout Voltage: Typically 450 mV @ 250 mA load, and 5 mV @ 1 mA load.

Ground Pin Current: Typically 1500 µA @ 250 mA load, and 75 µA @ 1 mA load.

Enhanced Stability: The LP2992 is stable with output capacitor ESR as low as 5 mΩ, which allows the use of ceramic capacitors on the output.

Sleep Mode: Less than 1 µA quiescent current when ON/OFF pin is pulled low.

Smallest Possible Size: SOT-23 and LLP packages use absolute minimum board space.

Precision Output: 1% tolerance output voltages available (A grade).

Low Noise: By adding a 10 nF bypass capacitor, output noise can be reduced to 30 µV (typical).

Multiple voltage options, from 1.5V to 5.0V, are available as standard products. Consult factory for custom voltages.

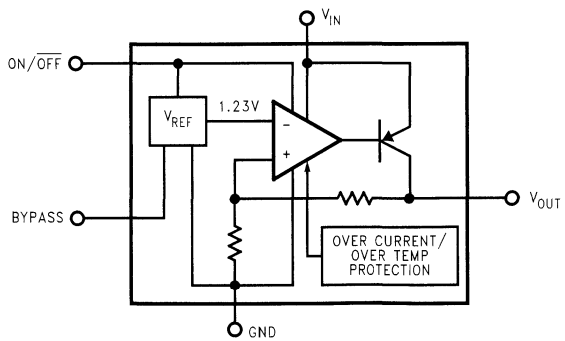
Features

- Ultra low dropout voltage
- Guaranteed 250 mA output current
- Smallest possible size (SOT-23, LLP package)
- Requires minimum external components
- Stable with low-ESR output capacitor
- <1 µA quiescent current when shut down
- Low ground pin current at all loads
- Output voltage accuracy 1% (A Grade)
- High peak current capability
- Wide supply voltage range (16V max)
- Low Z_{OUT}: 0.3Ω typical (10 Hz to 1 MHz)
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range
- Custom voltages available

Applications

- Cellular Phone
- Palmtop/Laptop Computer
- Personal Digital Assistant (PDA)
- Camcorder, Personal Stereo, Camera

Block Diagram



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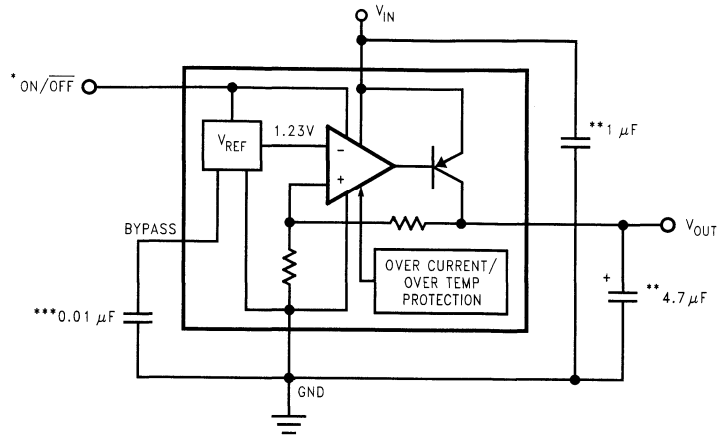
Basic Application Circuit



20029402

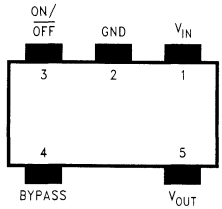
*ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not to be used.

**Minimum capacitance is shown to ensure stability (may be increased without limit). Ceramic capacitor required for output (see Application Hints).

***Reduces output noise (may be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see Application Hints).

Connection Diagrams

5-Lead Small Outline Package (M5)



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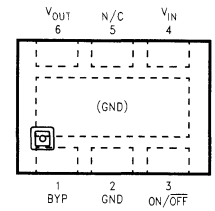
Top View
See NS Package Number MF05A
For ordering information see *Table 1*

6-Lead LLP Package (LD)



20029446

Top View
See NS Package Number NLDBA006
Outline Drawing LDE06A

Ordering Information

TABLE 1. Package Marking and Ordering Information

Output Voltage (V)	Grade	Order Information	Package Marking	Supplied as:
5-Lead Small Outline Package (M5)				
1.5	A	LP2992AIM5X-1.5	LFBA	3000 Units on Tape and Reel
1.5	A	LP2992AIM5-1.5	LFBA	1000 Units on Tape and Reel
1.5	STD	LP2992IM5X-1.5	LFBB	3000 Units on Tape and Reel
1.5	STD	LP2992IM5-1.5	LFBB	1000 Units on Tape and Reel
1.8	A	LP2992AIM5X-1.8	LFCA	3000 Units on Tape and Reel
1.8	A	LP2992AIM5-1.8	LFCA	1000 Units on Tape and Reel
1.8	STD	LP2992IM5X-1.8	LFCB	3000 Units on Tape and Reel
1.8	STD	LP2992IM5-1.8	LFCB	1000 Units on Tape and Reel
2.5	A	LP2992AIM5X-2.5	LFDA	3000 Units on Tape and Reel
2.5	A	LP2992AIM5-2.5	LFDA	1000 Units on Tape and Reel
2.5	STD	LP2992IM5X-2.5	LFDB	3000 Units on Tape and Reel
2.5	STD	LP2992IM5-2.5	LFDB	1000 Units on Tape and Reel
3.3	A	LP2992AIM5X-3.3	LFEA	3000 Units on Tape and Reel
3.3	A	LP2992AIM5-3.3	LFEA	1000 Units on Tape and Reel
3.3	STD	LP2992IM5X-3.3	LFEB	3000 Units on Tape and Reel
3.3	STD	LP2992IM5-3.3	LFEB	1000 Units on Tape and Reel
5.0	A	LP2992AIM5X-5.0	LFFA	3000 Units on Tape and Reel
5.0	A	LP2992AIM5-5.0	LFFA	1000 Units on Tape and Reel
5.0	STD	LP2992IM5X-5.0	LFFB	3000 Units on Tape and Reel
5.0	STD	LP2992IM5-5.0	LFFB	1000 Units on Tape and Reel
6-Lead LLP Package (LDE06A)				
1.5	A	LP2992AILDX-1.5	L011A	4500 Units on Tape and Reel
1.5	A	LP2992AILD-1.5	L011A	1000 Units on Tape and Reel
1.5	STD	LP2992ILDX-1.5	L011AB	4500 Units on Tape and Reel
1.5	STD	LP2992ILD-1.5	L011AB	1000 Units on Tape and Reel
1.8	A	LP2992AILDX-1.8	L012A	4500 Units on Tape and Reel
1.8	A	LP2992AILD-1.8	L012A	1000 Units on Tape and Reel
1.8	STD	LP2992ILDX-1.8	L012AB	4500 Units on Tape and Reel
1.8	STD	LP2992ILD-1.8	L012AB	1000 Units on Tape and Reel
2.5	A	LP2992AILDX-2.5	L013A	4500 Units on Tape and Reel
2.5	A	LP2992AILD-2.5	L013A	1000 Units on Tape and Reel
2.5	STD	LP2992ILDX-2.5	L013AB	4500 Units on Tape and Reel
2.5	STD	LP2992ILD-2.5	L013AB	1000 Units on Tape and Reel
3.3	A	LP2992AILDX-3.3	L014A	4500 Units on Tape and Reel
3.3	A	LP2992AILD-3.3	L014A	1000 Units on Tape and Reel
3.3	STD	LP2992ILDX-3.3	L014AB	4500 Units on Tape and Reel
3.3	STD	LP2992ILD-3.3	L014AB	1000 Units on Tape and Reel
5.0	A	LP2992AILDX-5.0	L015A	4500 Units on Tape and Reel
5.0	A	LP2992AILD-5.0	L015A	1000 Units on Tape and Reel
5.0	STD	LP2992ILDX-5.0	L015AB	4500 Units on Tape and Reel
5.0	STD	LP2992ILD-5.0	L015AB	1000 Units on Tape and Reel

National Semiconductor

LP3961/LP3964
800mA Fast Ultra Low Dropout Linear Regulators

General Description

The LP3961/LP3964 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very fast to step changes in load which makes them suitable for low voltage microprocessor applications. The LP3961/LP3964 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3961/LP3964 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 24mV at 80mA load current and 240mV at 800mA load current.

Ground Pin Current: Typically 4mA at 800mA load current.

Shutdown Mode: Typically 15µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3961).

SENSE: Sense pin improves regulation at remote loads. (For LP3964)

Precision Output Voltage: Multiple output voltage options are available ranging from 1.2V to 5.0V and adjustable (LP3964), with a guaranteed accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

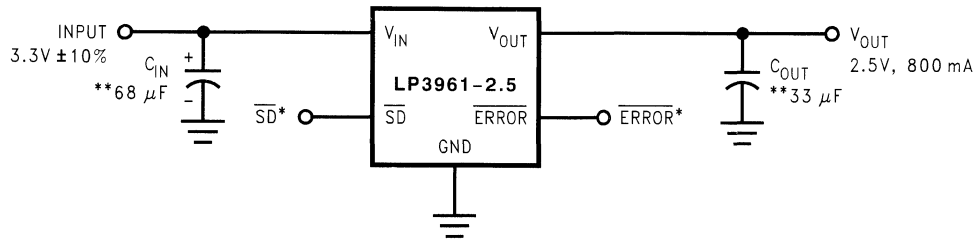
Features

- Ultra low dropout voltage
- Low ground pin current
- Load regulation of 0.02%
- 15µA quiescent current in shutdown mode
- Guaranteed output current of 0.8A DC
- Available in SOT-223,TO-263 and TO-220 packages
- Output voltage accuracy ± 1.5%
- $\overline{\text{Error}}$ flag indicates output status (LP3961)
- Sense option improves better load regulation (LP3964)
- Extremely low output capacitor requirements
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Microprocessor power supplies
- GTL, GTL+, BTL, and SSTL bus terminators
- Power supplies for DSPs
- SCSI terminator
- Post regulators
- High efficiency linear regulators
- Battery chargers
- Other battery powered applications

Typical Application Circuits

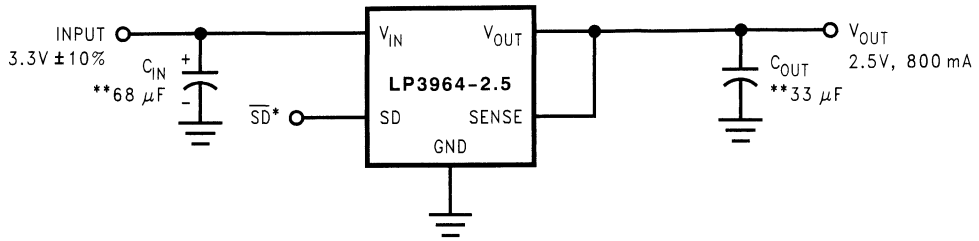


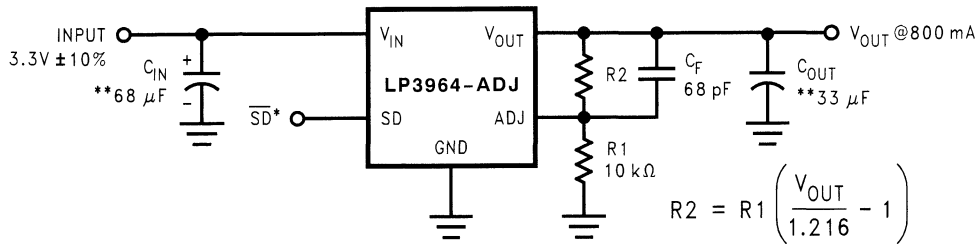
10112901

*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints.

Typical Application Circuits (Continued)



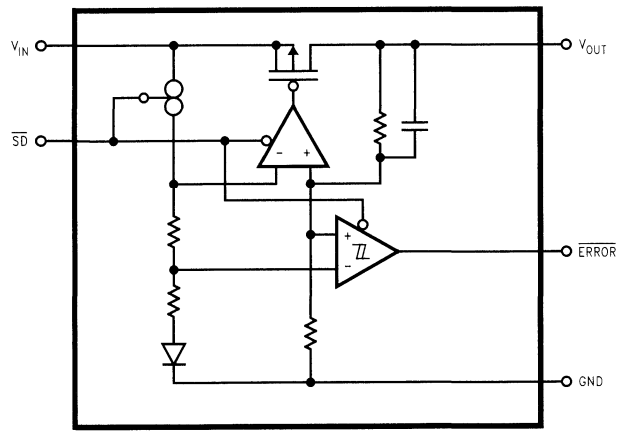


10112902

*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.

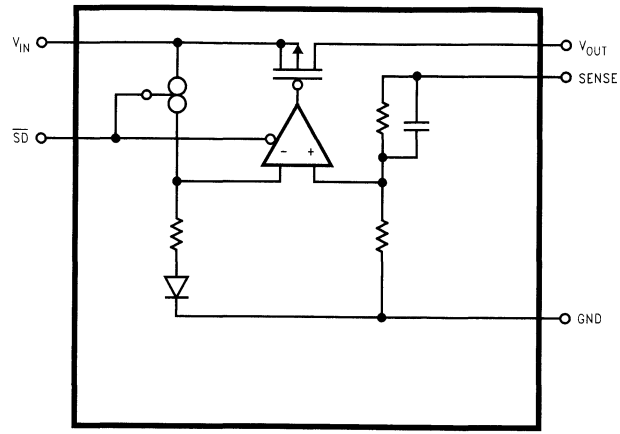
** See Application Hints

Block Diagram LP3961



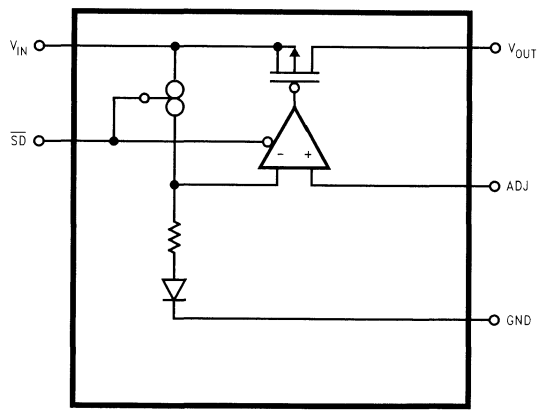
10112903

Block Diagram LP3964



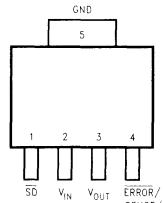
10112929

Block Diagram LP3964-ADJ

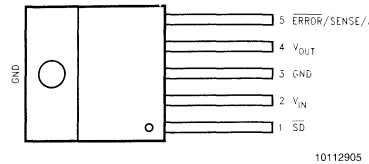


10112930

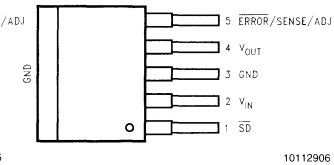
Connection Diagrams



Top View
SOT 223-5 Package



Top View
TO220-5 Package
Bent, Staggered Leads



Top View
TO263-5 Package

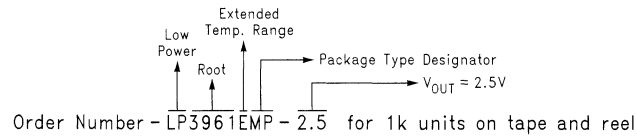
Pin Description for SOT223-5 Package

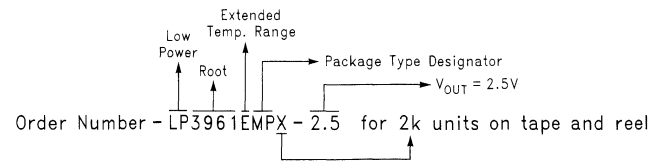
Pin #	LP3961		LP3964	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
4	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin or output Adjust Pin
5	GND	Ground	GND	Ground

Pin Description for TO220-5 and TO263-5 Packages

Pin #	LP3961		LP3964	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin or output Adjust Pin

Ordering Information





Package Type Designator is 'MP' for SOT223 package, 'T' for TO220 package, and 'S' for TO263 package.

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
5.0	LP3961EMP-5.0	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBSB	1000 units on Tape and Reel
5.0	LP3961EMPX-5.0	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBSB	2000 units on Tape and Reel
3.3	LP3961EMP-3.3	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LAZB	1000 units on Tape and Reel
3.3	LP3961EMPX-3.3	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LAZB	2000 units on Tape and Reel
2.5	LP3961EMP-2.5	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBBB	1000 units on Tape and Reel
2.5	LP3961EMPX-2.5	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBBB	2000 units on Tape and Reel
1.8	LP3961EMP-1.8	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBAB	1000 units on Tape and Reel
1.8	LP3961EMPX-1.8	800mA, $\overline{\text{Error}}$ Flag	SOT223-5	LBAB	2000 units on Tape and Reel
5.0	LP3964EMP-5.0	800mA, SENSE	SOT223-5	LBUB	1000 units on Tape and Reel
5.0	LP3964EMPX-5.0	800mA, SENSE	SOT223-5	LBUB	2000 units on Tape and Reel
3.3	LP3964EMP-3.3	800mA, SENSE	SOT223-5	LBJB	1000 units on Tape and Reel
3.3	LP3964EMPX-3.3	800mA, SENSE	SOT223-5	LBJB	2000 units on Tape and Reel
2.5	LP3964EMP-2.5	800mA, SENSE	SOT223-5	LBHB	1000 units on Tape and Reel
2.5	LP3964EMPX-2.5	800mA, SENSE	SOT223-5	LBHB	2000 units on Tape and Reel
1.8	LP3964EMP-1.8	800mA, SENSE	SOT223-5	LBFB	1000 units on Tape and Reel
1.8	LP3964EMPX-1.8	800mA, SENSE	SOT223-5	LBFB	2000 units on Tape and Reel
ADJ	LP3964EMP-ADJ	800mA, ADJ	SOT223-5	LBPB	1000 units on Tape and Reel
ADJ	LP3964EMPX-ADJ	800mA, ADJ	SOT223-5	LBPB	2000 units on Tape and Reel
5.0	LP3961ES-5.0	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-5.0	Rail
5.0	LP3961ESX-5.0	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ESX-5.0	Tape and Reel
3.3	LP3961ES-3.3	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-3.3	Rail
3.3	LP3961ESX-3.3	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-3.3	Tape and Reel
2.5	LP3961ES-2.5	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-2.5	Rail
2.5	LP3961ESX-2.5	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-2.5	Tape and Reel
1.8	LP3961ES-1.8	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-1.8	Rail
1.8	LP3961ESX-1.8	800mA, $\overline{\text{Error}}$ Flag	TO263-5	LP3961ES-1.8	Tape and Reel
5.0	LP3964ES-5.0	800mA, SENSE	TO263-5	LP3964ES-5.0	Rail
5.0	LP3964ESX-5.0	800mA, SENSE	TO263-5	LP3964ES-5.0	Tape and Reel
3.3	LP3964ES-3.3	800mA, SENSE	TO263-5	LP3964ES-3.3	Rail
3.3	LP3964ESX-3.3	800mA, SENSE	TO263-5	LP3964ES-3.3	Tape and Reel
2.5	LP3964ES-2.5	800mA, SENSE	TO263-5	LP3964ES-2.5	Rail

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
2.5	LP3964ESX-2.5	800mA, SENSE	TO263-5	LP3964ES-2.5	Tape and Reel
1.8	LP3964ES-1.8	800mA, SENSE	TO263-5	LP3964ES-1.8	Rail
1.8	LP3964ESX-1.8	800mA, SENSE	TO263-5	LP3964ES-1.8	Tape and Reel
ADJ	LP3964ES-ADJ	800mA, ADJ	TO263-5	LP3964ES-ADJ	Rail
ADJ	LP3964ESX-ADJ	800mA, ADJ	TO263-5	LP3964ES-ADJ	Tape and Reel
5.0	LP3961ET-5.0	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-5.0	Rail
3.3	LP3961ET-3.3	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-3.3	Rail
2.5	LP3961ET-2.5	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-2.5	Rail
1.8	LP3961ET-1.8	800mA, $\overline{\text{Error}}$ Flag	TO220-5	LP3961ET-1.8	Rail
5.0	LP3964ET-5.0	800mA, SENSE	TO220-5	LP3964ET-5.0	Rail
3.3	LP3964ET-3.3	800mA, SENSE	TO220-5	LP3964ET-3.3	Rail
2.5	LP3964ET-2.5	800mA, SENSE	TO220-5	LP3964ET-2.5	Rail
1.8	LP3964ET-1.8	800mA, SENSE	TO220-5	LP3964ET-1.8	Rail
ADJ	LP3964ET-ADJ	800mA, ADJ	TO220-5	LP3964ET-ADJ	Rail

National Semiconductor

LP3962/LP3965
1.5A Fast Ultra Low Dropout Linear Regulators

General Description

The LP3962/LP3965 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very fast to step changes in load which makes them suitable for low voltage microprocessor applications. The LP3962/LP3965 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3962/LP3965 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 38mV at 150mA load current and 380mV at 1.5A load current.

Ground Pin Current: Typically 5mA at 1.5A load current.

Shutdown Mode: Typically 15µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3962).

SENSE: Sense pin improves regulation at remote loads. (For LP3965)

Precision Output Voltage: Multiple output voltage options are available ranging from 1.2V to 5.0V and adjustable (LP3965), with a guaranteed accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

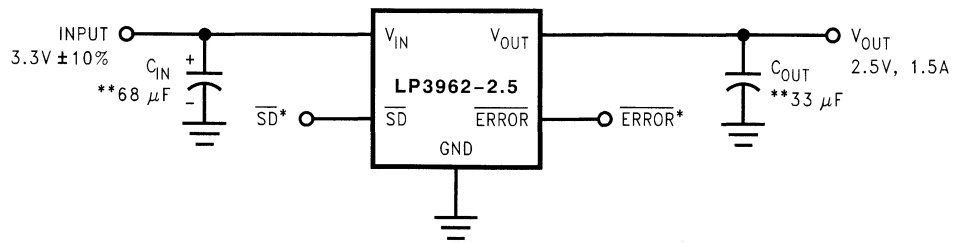
Features

- Ultra low dropout voltage
- Low ground pin current
- Load regulation of 0.04%
- 15µA quiescent current in shutdown mode
- Guaranteed output current of 1.5A DC
- Available in SOT-223,TO-263 and TO-220 packages
- Output voltage accuracy ± 1.5%
- $\overline{\text{Error}}$ flag indicates output status (LP3962)
- Sense option improves better load regulation (LP3965)
- Extremely low output capacitor requirements
- Overtemperature/overcurrent protection
- −40˚C to +125˚C junction temperature range

Applications

- Microprocessor power supplies
- GTL, GTL+, BTL, and SSTL bus terminators
- Power supplies for DSPs
- SCSI terminator
- Post regulators
- High efficiency linear regulators
- Battery chargers
- Other battery powered applications

Typical Application Circuits



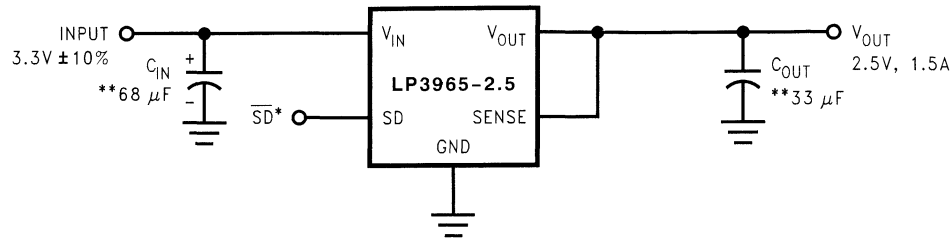
10126601

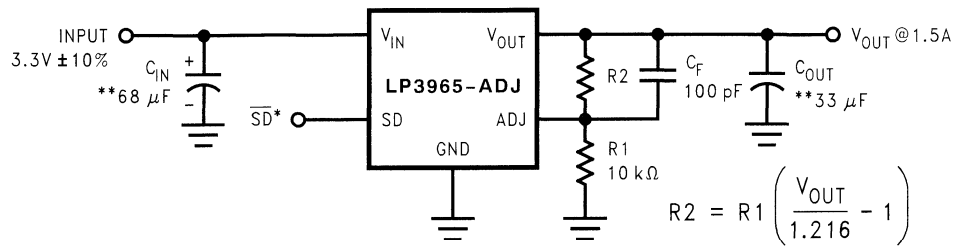
*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints.

16

Typical Application Circuits (Continued)

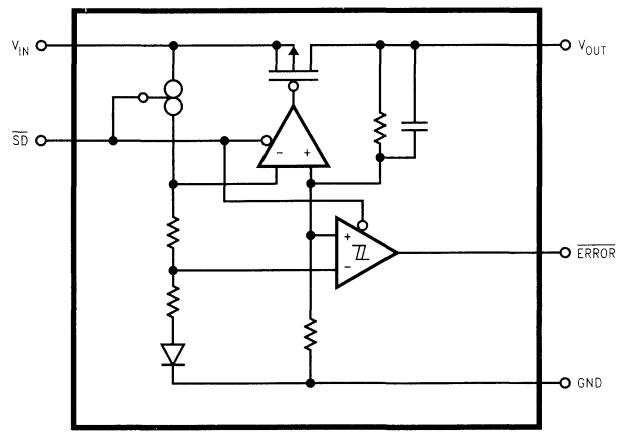




10126634

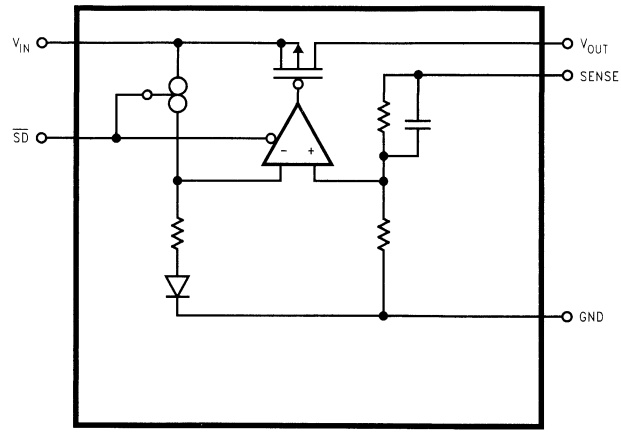
*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.
** See Application Hints.

Block Diagram LP3962



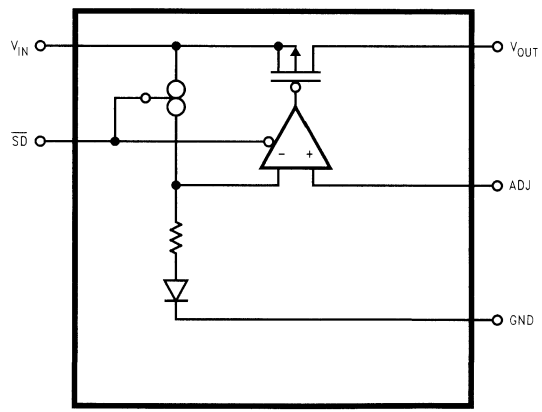
10126603

Block Diagram LP3965



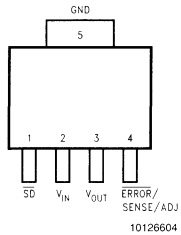
10126629

Block Diagram LP3965-ADJ

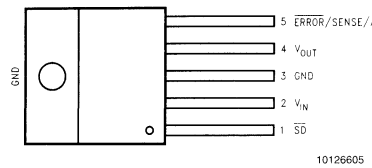


10126635

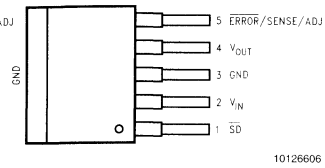
Connection Diagrams



Top View
SOT 223-5 Package



Top View
TO220-5 Package
Bent, Staggered Leads



Top View
TO263-5 Package

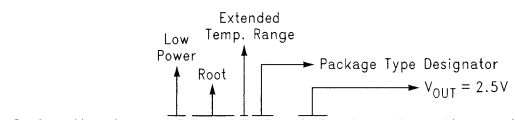
Pin Description for SOT223-5 Package

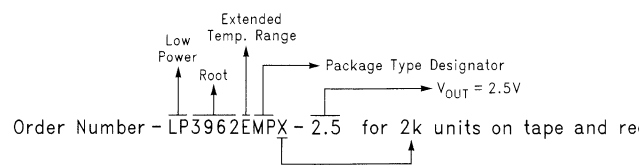
Pin #	LP3962		LP3965	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
4	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin or Output Adjust Pin
5	GND	Ground	GND	Ground

Pin Description for TO220-5 and TO263-5 Packages

Pin #	LP3962		LP3965	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin or Output Adjust Pin

Ordering Information





Package Type Designator is 'MP' for SOT223 package, 'T' for TO220 package, and 'S' for TO263 package.

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
5.0	LP3962EMP-5.0	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBTB	1000 units on Tape and Reel
5.0	LP3962EMPX-5.0	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBTB	2000 units on Tape and Reel
3.3	LP3962EMP-3.3	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBEB	1000 units on Tape and Reel
3.3	LP3962EMPX-3.3	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBEB	2000 units on Tape and Reel
2.5	LP3962EMP-2.5	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBDB	1000 units on Tape and Reel
2.5	LP3962EMPX-2.5	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBDB	2000 units on Tape and Reel
1.8	LP3962EMP-1.8	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBCB	1000 units on Tape and Reel
1.8	LP3962EMPX-1.8	1.5A, $\overline{\text{Error}}$ Flag	SOT223-5	LBCB	2000 units on Tape and Reel
5.0	LP3965EMP-5.0	1.5A, SENSE	SOT223-5	LBVB	1000 units on Tape and Reel
5.0	LP3965EMPX-5.0	1.5A, SENSE	SOT223-5	LBVB	2000 units on Tape and Reel
3.3	LP3965EMP-3.3	1.5A, SENSE	SOT223-5	LBNB	1000 units on Tape and Reel
3.3	LP3965EMPX-3.3	1.5A, SENSE	SOT223-5	LBNB	2000 units on Tape and Reel
2.5	LP3965EMP-2.5	1.5A, SENSE	SOT223-5	LBLB	1000 units on Tape and Reel
2.5	LP3965EMPX-2.5	1.5A, SENSE	SOT223-5	LBLB	2000 units on Tape and Reel
1.8	LP3965EMP-1.8	1.5A, SENSE	SOT223-5	LBKB	1000 units on Tape and Reel
1.8	LP3965EMPX-1.8	1.5A, SENSE	SOT223-5	LBKB	2000 units on Tape and Reel
ADJ	LP3965EMP-ADJ	1.5A, ADJ	SOT223-5	LBRB	1000 units on Tape and Reel
ADJ	LP3965EMPX-ADJ	1.5A, ADJ	SOT223-5	LBRB	2000 units on Tape and Reel
5.0	LP3962ES-5.0	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-5.0	Rail
5.0	LP3962ESX-5.0	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ESX-5.0	Tape and Reel
3.3	LP3962ES-3.3	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-3.3	Rail
3.3	LP3962ESX-3.3	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-3.3	Tape and Reel
2.5	LP3962ES-2.5	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-2.5	Rail
2.5	LP3962ESX-2.5	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-2.5	Tape and Reel
1.8	LP3962ES-1.8	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-1.8	Rail
1.8	LP3962ESX-1.8	1.5A, $\overline{\text{Error}}$ Flag	TO263-5	LP3962ES-1.8	Tape and Reel
5.0	LP3965ES-5.0	1.5A, SENSE	TO263-5	LP3965ES-5.0	Rail
5.0	LP3965ESX-5.0	1.5A, SENSE	TO263-5	LP3965ES-5.0	Tape and Reel
3.3	LP3965ES-3.3	1.5A, SENSE	TO263-5	LP3965ES-3.3	Rail
3.3	LP3965ESX-3.3	1.5A, SENSE	TO263-5	LP3965ES-3.3	Tape and Reel
2.5	LP3965ES-2.5	1.5A, SENSE	TO263-5	LP3965ES-2.5	Rail

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
2.5	LP3965ESX-2.5	1.5A, SENSE	TO263-5	LP3965ES-2.5	Tape and Reel
1.8	LP3965ES-1.8	1.5A, SENSE	TO263-5	LP3965ES-1.8	Rail
1.8	LP3965ESX-1.8	1.5A, SENSE	TO263-5	LP3965ES-1.8	Tape and Reel
ADJ	LP3965ES-ADJ	1.5A, ADJ	TO263-5	LP3965ES-ADJ	Rail
ADJ	LP3965ESX-ADJ	1.5A, ADJ	TO263-5	LP3965ES-ADJ	Tape and Reel
5.0	LP3962ET-5.0	1.5A, $\overline{\text{Error}}$ Flag	TO220-5	LP3962ET-5.0	Rail
3.3	LP3962ET-3.3	1.5A, $\overline{\text{Error}}$ Flag	TO220-5	LP3962ET-3.3	Rail
2.5	LP3962ET-2.5	1.5A, $\overline{\text{Error}}$ Flag	TO220-5	LP3962ET-2.5	Rail
1.8	LP3962ET-1.8	1.5A, $\overline{\text{Error}}$ Flag	TO220-5	LP3962ET-1.8	Rail
5.0	LP3965ET-5.0	1.5A, SENSE	TO220-5	LP3965ET-5.0	Rail
3.3	LP3965ET-3.3	1.5A, SENSE	TO220-5	LP3965ET-3.3	Rail
2.5	LP3965ET-2.5	1.5A, SENSE	TO220-5	LP3965ET-2.5	Rail
1.8	LP3965ET-1.8	1.5A, SENSE	TO220-5	LP3965ET-1.8	Rail
ADJ	LP3965ET-ADJ	1.5A, ADJ	TO220-5	LP3965ET-ADJ	Rail

National Semiconductor

LP3963/LP3966
3A Fast Ultra Low Dropout Linear Regulators

General Description

The LP3963/LP3966 series of fast ultra low-dropout linear regulators operate from a +2.5V to +7.0V input supply. Wide range of preset output voltage options are available. These ultra low dropout linear regulators respond very quickly to step changes in load which makes them suitable for low voltage microprocessor applications. The LP3963/LP3966 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3963/LP3966 to operate under extremely low dropout conditions.

Dropout Voltage: Ultra low dropout voltage; typically 80mV at 300mA load current and 800mV at 3A load current.

Ground Pin Current: Typically 6mA at 3A load current.

Shutdown Mode: Typically 15µA quiescent current when the shutdown pin is pulled low.

$\overline{\text{Error}}$ Flag: $\overline{\text{Error}}$ flag goes low when the output voltage drops 10% below nominal value (for LP3963).

SENSE: Sense pin improves regulation at remote loads. (For LP3966)

Precision Output Voltage: Multiple output voltage options are available ranging from 1.2V to 5.0V and adjustable (LP3966), with a guaranteed accuracy of ±1.5% at room temperature, and ±3.0% over all conditions (varying line, load, and temperature).

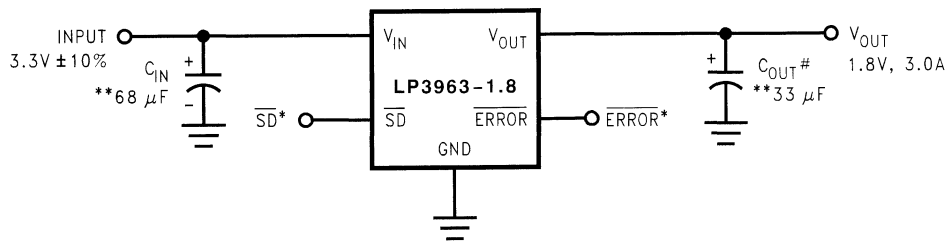
Features

- Ultra low dropout voltage
- Low ground pin current
- Load regulation of 0.06%
- 15µA quiescent current in shutdown mode
- Guaranteed output current of 3A DC
- Available in TO-263 and TO-220 packages
- Output voltage accuracy ± 1.5%
- $\overline{\text{Error}}$ flag indicates output status (LP3963)
- Sense option improves load regulation (LP3966)
- Minimum output capacitor requirements
- Overtemperature/overcurrent protection
- −40°C to +125°C junction temperature range

Applications

- Microprocessor power supplies
- GTL, GTL+, BTL, and SSTL bus terminators
- Power supplies for DSPs
- SCSI terminator
- Post regulators
- High efficiency linear regulators
- Battery chargers
- Other battery powered applications

Typical Application Circuits



10126701

*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints

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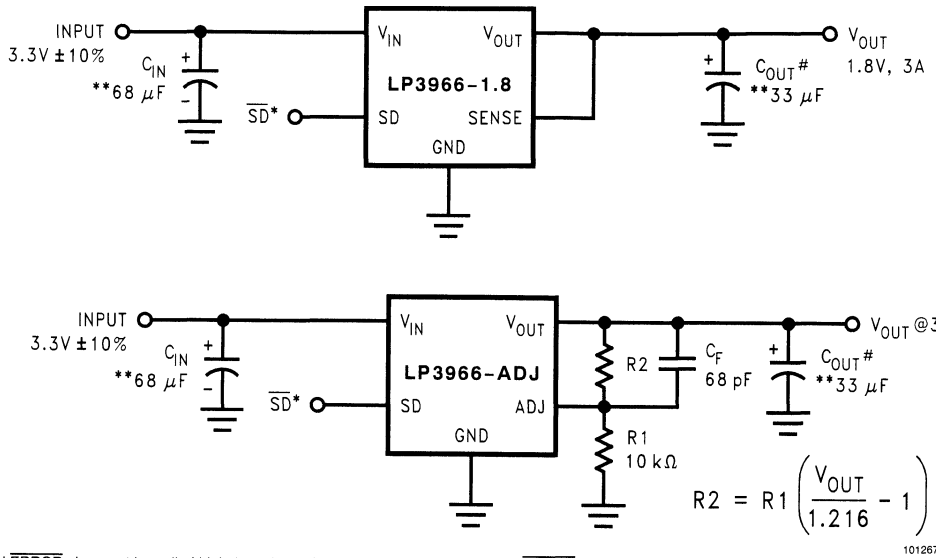
Typical Application Circuits (Continued)

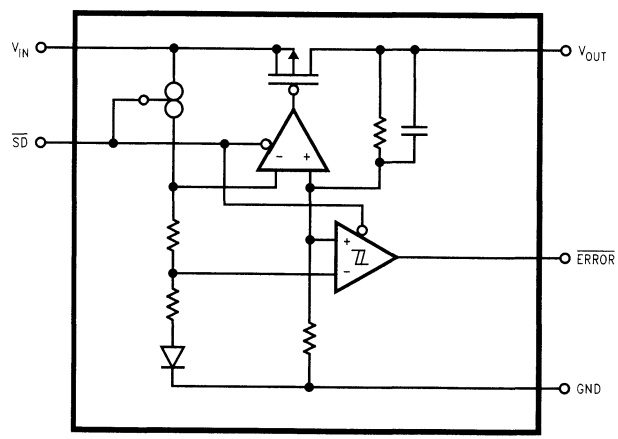


10126734

*$\overline{SD}$ and $\overline{ERROR}$ pins must be pulled high through a 10kΩ pull-up resistor. Connect the $\overline{ERROR}$ pin to ground if this function is not used. See applications section for more information.

** See Application Hints

Block Diagram LP3963



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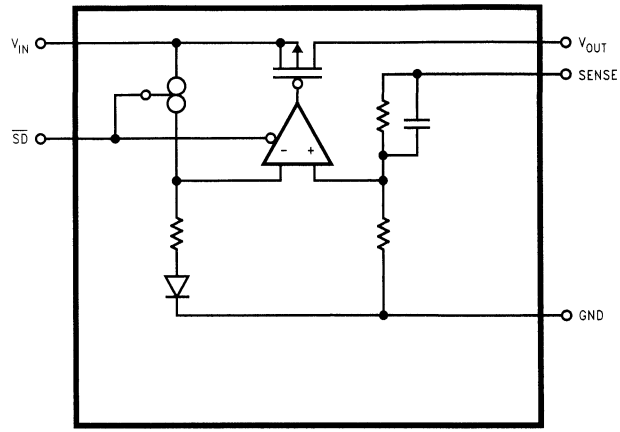
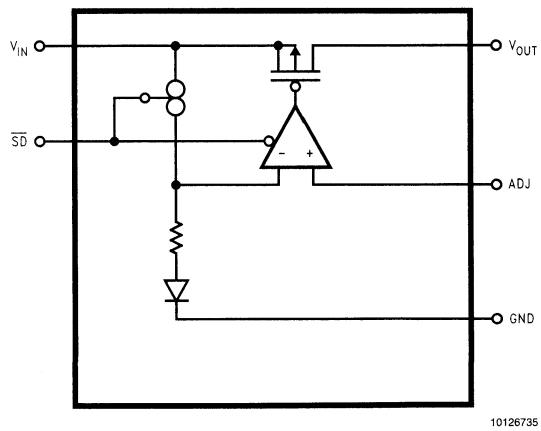
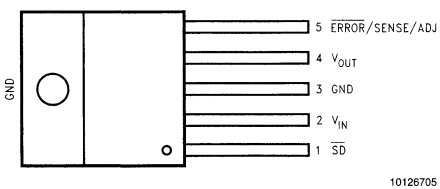
Block Diagram LP3966



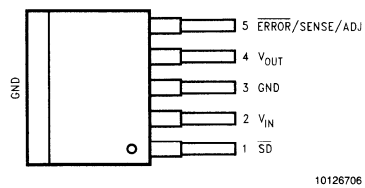
Block Diagram LP3966-ADJ



Connection Diagrams



Top View
TO220-5 Package
Bent, Staggered Leads



Top View
TO263-5 Package

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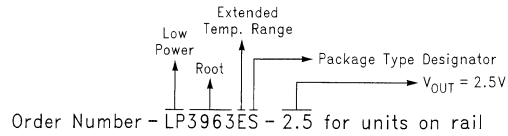
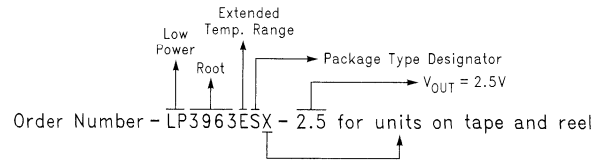
Pin Description for TO220-5 and TO263-5 Packages

Pin #	LP3963		LP3966	
	Name	Function	Name	Function
1	$\overline{SD}$	Shutdown	$\overline{SD}$	Shutdown
2	V_{IN}	Input Supply	V_{IN}	Input Supply
3	GND	Ground	GND	Ground
4	V_{OUT}	Output Voltage	V_{OUT}	Output Voltage
5	$\overline{ERROR}$	$\overline{ERROR}$ Flag	SENSE/ADJ	Remote Sense Pin/Output Adjust Pin

Ordering Information





Package Type Designator is 'T' for TO220 package, and 'S' for TO263 package.

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
5.0	LP3963ES-5.0	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-5.0	Rail
5.0	LP3963ESX-5.0	3A, $\overline{Error}$ Flag	TO263-5	LP3963ESX-5.0	Tape and Reel
3.3	LP3963ES-3.3	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-3.3	Rail
3.3	LP3963ESX-3.3	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-3.3	Tape and Reel
2.5	LP3963ES-2.5	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-2.5	Rail
2.5	LP3963ESX-2.5	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-2.5	Tape and Reel
1.8	LP3963ES-1.8	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-1.8	Rail
1.8	LP3963ESX-1.8	3A, $\overline{Error}$ Flag	TO263-5	LP3963ES-1.8	Tape and Reel
5.0	LP3966ES-5.0	3A, SENSE	TO263-5	LP3966ES-5.0	Rail
5.0	LP3966ESX-5.0	3A, SENSE	TO263-5	LP3966ESX-5.0	Tape and Reel
3.3	LP3966ES-3.3	3A, SENSE	TO263-5	LP3966ES-3.3	Rail
3.3	LP3966ESX-3.3	3A, SENSE	TO263-5	LP3966ES-3.3	Tape and Reel
2.5	LP3966ES-2.5	3A, SENSE	TO263-5	LP3966ES-2.5	Rail
2.5	LP3966ESX-2.5	3A, SENSE	TO263-5	LP3966ES-2.5	Tape and Reel
1.8	LP3966ES-1.8	3A, SENSE	TO263-5	LP3966ES-1.8	Rail
1.8	LP3966ESX-1.8	3A, SENSE	TO263-5	LP3966ES-1.8	Tape and Reel
ADJ	LP3966ES-ADJ	3A, ADJ	TO263-5	LP3966ES-ADJ	Rail
ADJ	LP3966ESX-ADJ	3A, ADJ	TO263-5	LP3966ES-ADJ	Tape and Reel
5.0	LP3963ET-5.0	3A, $\overline{Error}$ Flag	TO220-5	LP3963ET-5.0	Rail
3.3	LP3963ET-3.3	3A, $\overline{Error}$ Flag	TO220-5	LP3963ET-3.3	Rail
2.5	LP3963ET-2.5	3A, $\overline{Error}$ Flag	TO220-5	LP3963ET-2.5	Rail
1.8	LP3963ET-1.8	3A, $\overline{Error}$ Flag	TO220-5	LP3963ET-1.8	Rail

Ordering Information (Continued)

TABLE 1. Package Marking and Ordering Information (Continued)

Output Voltage	Order Number	Description (Current, Option)	Package Type	Package Marking	Supplied As:
5.0	LP3966ET-5.0	3A, SENSE	TO220-5	LP3966ET-5.0	Rail
3.3	LP3966ET-3.3	3A, SENSE	TO220-5	LP3966ET-3.3	Rail
2.5	LP3966ET-2.5	3A, SENSE	TO220-5	LP3966ET-2.5	Rail
1.8	LP3966ET-1.8	3A, SENSE	TO220-5	LP3966ET-1.8	Rail
ADJ	LP3966ET-ADJ	3A, ADJ	TO220-5	LP3966ET-ADJ	Rail

National Semiconductor

LP3981
Micropower, 300mA Ultra Low-Dropout CMOS Voltage Regulator

General Description

The LP3981's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies. This high power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 300 mA, from a 2.5V to 6V input, consuming less than 1µA in disable mode and has fast turn-on time less than 200µs.

The LP3981 is available in MSOP-8 package. For LP3981 in LLP-6 package, contact NSC sales offices. Performance is specified for −40°C to +125°C temperature range. The device available in the following output voltages; 2.5V, 2.7V, 2.8V, 2.83V, 3.03V and 3.3V as standard. Other output options can be made available, please contact your local NSC sales office.

Key Specifications

- 2.5 to 6.0V input range
- 300mA guaranteed output
- 60dB PSRR at 1kHz
- ≤1µA quiescent current when shut down
- Fast Turn-On time: 120 µs (typ.)
- 132mV typ dropout with 300mA load
- 35µVrms output noise over 10Hz to 100kHz
- −40 to +125°C junction temperature range for operation
- 2.5V, 2.7V, 2.8V, 2.83V, 3.03V and 3.3V outputs standard

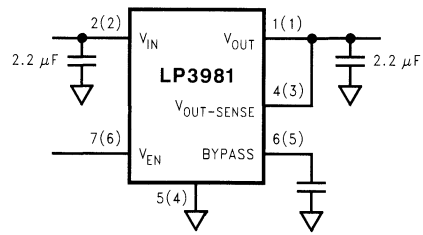
Features

- Small, space saving MSOP-8
- Low Thermal Resistance in LLP-6 package gives excellent power capability
- Logic controlled enable
- Stable with ceramic and high quality tantalum capacitors
- Fast turn-on
- Thermal shutdown and short-circuit current limit

Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- Tiny 3.3V ± 5% to 2.5V, 300mA converter

Typical Application Circuit



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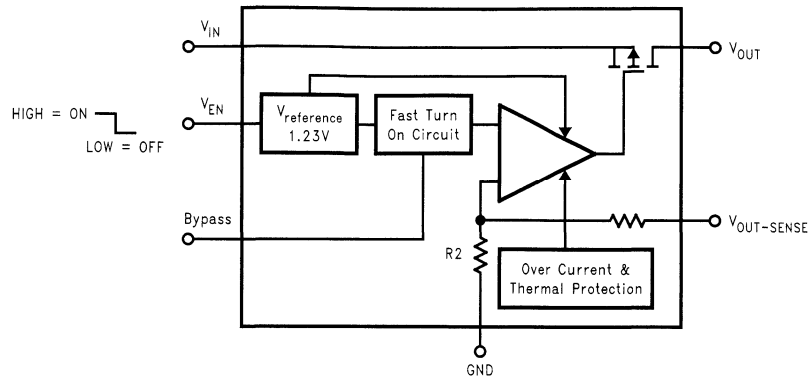
Note: Pin Numbers in parenthesis indicate LLP-6 package.

Block Diagram

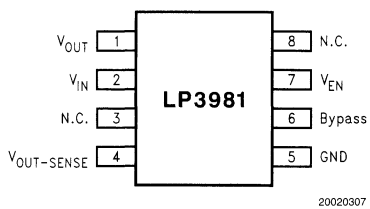


Pin Descriptions

Name	MSOP-8	LLP-6	Function
V_{EN}	7	6	Enable Input Logic, Enable High
GND	5	4	Common Ground
V_{OUT}	1	1	Output Voltage of the LDO
V_{IN}	2	2	Input Voltage of the LDO
Bypass	6	5	Optional bypass capacitor for noise reduction
$V_{OUT-SENSE}$	4	3	Output. Voltage Sense Pin. Should be connected to V_{OUT} for proper operation.
N.C	3, 8		

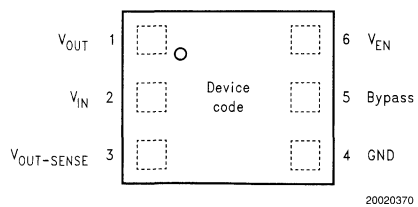
Connection Diagrams

MSOP-8 Package



Top View
See NS Package Number MUA008AE

LLP-6 Package



Top View
See NS Package Number LDC06D

Ordering Information

For LLP-6 Package*

Output Voltage (V)	Grade	LP3981 Supplied as 250 Units, Tape and Reel	LP3981 Supplied as 3000 Units, Tape and Reel	Package Marking
2.5	STD	LP3981ILD-2.5	LP3981ILDX-2.5	LO1UB
2.7	STD	LP3981ILD-2.7	LP3981ILDX-2.7	LO1VB
2.8	STD	LP3981ILD-2.8	LP3981ILDX-2.8	LO1ZB
2.83	STD	LP3981ILD-2.83	LP3981ILDX-2.85	L01SB
3.03	STD	LP3981ILD-3.03	LP3981ILDX-3.03	LO1YB
3.3	STD	LP3981ILD-3.3	LP3981ILDX-3.3	LO1XB

For MSOP-8 Package

Output Voltage (V)	Grade	LP3981 Supplied as 1000 Units, Tape and Reel	LP3981 Supplied as 3000 Units, Tape and Reel	Package Marking
2.5*	STD	LP3981IMM-2.5	LP3981IMMX-2.5	LFKB
2.7*	STD	LP3981IMM-2.7	LP3981IMMX-2.7	LFLB
2.8*	STD	LP3981IMM-2.8	LP3981IMMX-2.8	LFTB
2.83	STD	LP3981IMM-2.83	LP3981IMMX-2.83	LDUB
3.03	STD	LP3981IMM-3.03	LP3981IMMX-3.03	LFPB
3.3*	STD	LP3981IMM-3.3	LP3981IMMX-3.3	LFNB

*Please contact factory for availability.

National Semiconductor

LP3984
Micropower, 150mA Ultra Low-Dropout CMOS Voltage Regulator in Subminiature 4-I/O micro SMD Package

General Description

The LP3984 is designed for portable and wireless applications with demanding performance and space requirements.

The LP3984's performance is optimized for battery powered systems to deliver extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA, from a 2.5V to 6V input, consuming less than 1.2µA in disable mode and has fast turn-on time less than 20µs.

The LP3984 is available in micro SMD and 5 pin SOT-23 package. Performance is specified for −40°C to +125°C temperature range and is available in 1.5V, 1.8V, 2.0V, and 3.1V output voltages. For other output voltage options from 1.5V to 3.5V, please contact National Semiconductor sales office.

Key Specifications

- 2.5 to 6.0V input range
- 150mA guaranteed output
- 60dB PSRR at 1kHz, 40dB at 10kHz @ $3.1V_{IN}$
- ≤1.2µA quiescent current when shut down
- Fast Turn-On time: 20 µs (typ.)
- 75mV typ dropout with 150mA load
- −40 to +125°C junction temperature range for operation
- 1.5V, 1.8V, 2.0V, and 3.1V

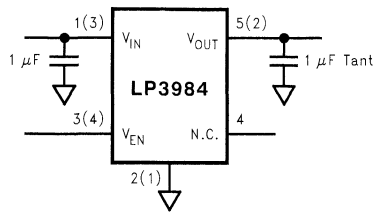
Features

- Miniature 4-I/O micro SMD and SOT-23-5 package
- Logic controlled enable
- Stable with tantalum capacitors
- 1 µF Tantalum output capacitor
- Fast turn-on
- Thermal shutdown and short-circuit current limit

Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances

Typical Application Circuit



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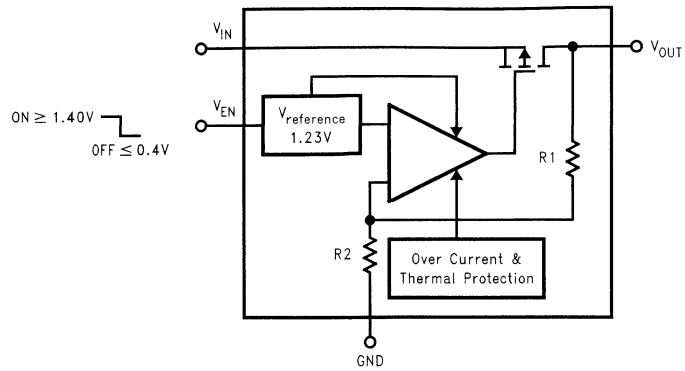
Note: Pin Numbers in parenthesis indicate micro SMD package.

Block Diagram

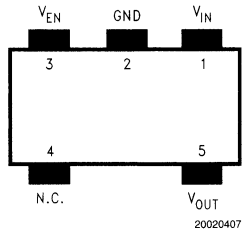


Pin Descriptions

Name	µSMD	SOT	Function
V_{EN}	4	3	Enable Input Logic, Enable High
GND	1	2	Common Ground
V_{OUT}	2	5	Output Voltage of the LDO
V_{IN}	3	1	Input Voltage of the LDO
N.C.		4	No Connection

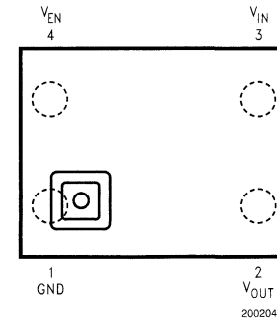
Connection Diagrams

SOT-23-5 Package



Top View
See NS Package Number MF05A

micro SMD, 4 Bump Package



Top View
See NS Package Number BPA04

Note: The actual physical placement of the package marking will vary from part to part. The package marking will designate the date code. Package marking does not correlate to device type in any way.

Ordering Information

For micro SMD Package

Output Voltage (V)	Grade	LP3984 Supplied as 250 Units, Tape and Reel	LP3984 Supplied as 3000 Units, Tape and Reel
1.5	STD	LP3984IBP-1.5	LP3984IBPX-1.5
1.8	STD	LP3984IBP-1.8	LP3984IBPX-1.8
2.0	STD	LP3984IBP-2.0	LP3984IBPX-2.0
3.1	STD	LP3984IBP-3.1	LP3984IBPX-3.1

For SOT Package

Output Voltage (V)	Grade	LP3984 Supplied as 1000 Units, Tape and Reel	LP3984 Supplied as 3000 Units, Tape and Reel	Package Marking
1.5	STD	LP3984IMF-1.5	LP3984IMFX-1.5	LEAB
1.8	STD	LP3984IMF-1.8	LP3984IMFX-1.8	LEBB
2.0	STD	LP3984IMF-2.0	LP3984IMFX-2.0	LECB
3.1	STD	LP3984IMF-3.1	LP3984IMFX-3.1	LEDB

National Semiconductor

LP3985
Micropower, 150mA Low-Noise Ultra Low-Dropout CMOS Voltage Regulator

General Description

The LP3985 is designed for portable and wireless applications with demanding performance and space requirements.

LP3985 is stable with a small 1µF ±30% ceramic or high-quality tantalum output capacitor requiring smallest possible PC board area. The total application circuit area is less than 2.0mm x 2.5mm, a fraction of a 1202 case size.

The LP3985's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Optional external bypass capacitor reduces the output noise further without slowing down the load transient response. Fast start-up time is achieved by utilizing an internal power-on circuit that actively pre-charges the bypass capacitor.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA, from a 2.5V to 6V input, consuming less than 1.5µA in disable mode and has fast turn-on time less than 200µs.

The LP3985 is available in micro SMD and 5 pin SOT-23 package. Performance is specified for −40°C to +125°C temperature range and is available in 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V. 3.1V, 3.2V, 3.3V, 4.7V and 5.0V output voltages. For other output voltage options from 2.5V to 5.0V or for a dual LP3985, please contact National Semiconductor sales office.

Key Specifications

- 2.5 to 6.0V input range
- 150mA guaranteed output
- 60dB PSRR at 1kHz, 50dB at 10kHz @ $3.1V_{IN}$
- ≤1.5µA quiescent current when shut down
- Fast Turn-On time: 200 µs (typ.)
- 100mV maximum dropout with 150mA load
- 30µVrms output noise over 10Hz to 100kHz
- −40 to +125°C junction temperature range for operation
- 2.5V, 2.6V, 2.7V, 2.8V, 2.85V, 2.9V, 3.0V, 3.1V, 3.2V, 3.3V, 4.7V and 5.0V outputs standard

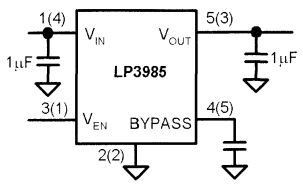
Features

- Miniature 5-I/O micro SMD and SOT-23-5 package
- Logic controlled enable
- Stable with ceramic and high quality tantalum capacitors
- Fast turn-on
- Thermal shutdown and short-circuit current limit

Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances

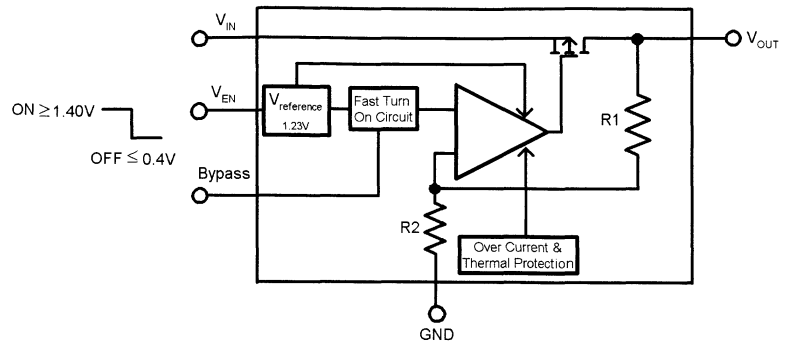
Typical Application Circuit



10136402

Note: Pin Numbers in parenthesis indicate micro SMD package.
* Optional Noise Reduction Capacitor.

Block Diagram



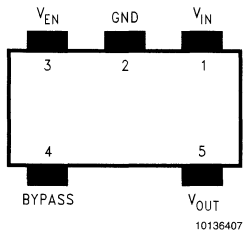
10136401

Pin Description

Name	µSMD	SOT	Function
V_{EN}	1	3	Enable Input Logic, Enable High
GND	2	2	Common Ground
V_{OUT}	3	5	Output Voltage of the LDO
V_{IN}	4	1	Input Voltage of the LDO
BYPASS	5	4	Optional Bypass Capacitor for Noise Reduction

Connection Diagrams

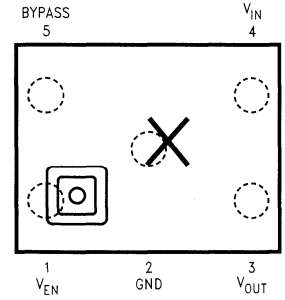
SOT-23-5 Package (MF)



10136407

Top View
See NS Package Number MF05A

micro SMD, 5 Bump Package (BPA05)



10136470

Top View
See NS Package Number BPA05

Note: The actual physical placement of the package marking will vary from part to part. The package marking 'X' will designate the date code and will vary considerably. Package marking does not correlate to device type in any way.

Ordering Information

For micro SMD Package

Output Voltage (V)	Grade	LP3985 Supplied as 250 Units, Tape and Reel	LP3985 Supplied as 3000 Units, Tape and Reel
2.5	STD	LP3985IBP-2.5	LP3985IBPX-2.5
2.6	STD	LP3985IBP-2.6	LP3985IBPX-2.6
2.7	STD	LP3985IBP-2.7	LP3985IBPX-2.7
2.8	STD	LP3985IBP-2.8	LP3985IBPX-2.8
2.85	STD	LP3985IBP-2.85	LP3985IBPX-2.85
2.9	STD	LP3985IBP-2.9	LP3985IBPX-2.9
3.0	STD	LP3985IBP-3.0	LP3985IBPX-3.0
3.1	STD	LP3985IBP-3.1	LP3985IBPX-3.1
3.2	STD	LP3985IBP-3.2	LP3985IBPX-3.2
3.3	STD	LP3985IBP-3.3	LP3985IBPX-3.3
4.7	STD	LP3985IBP-4.7	LP3985IBPX-4.7
5.0	STD	LP3985IBP-5.0	LP3985IBPX-5.0

For SOT Package

Output Voltage (V)	Grade	LP3985 Supplied as 1000 Units, Tape and Reel	LP3985 Supplied as 3000 Units, Tape and Reel	Package Marking
2.5	STD	LP3985IM5-2.5	LP3985IM5X-2.5	LCSB
2.6	STD	LP3985IM5-2.6	LP3985IM5X-2.6	LCTB
2.7	STD	LP3985IM5-2.7	LP3985IM5X-2.7	LCUB
2.8	STD	LP3985IM5-2.8	LP3985IM5X-2.8	LCJB
2.85	STD	LP3985IM5-2.85	LP3985IM5X-2.85	LCXB
2.9	STD	LP3985IM5-2.9	LP3985IM5X-2.9	LCYB
3.0	STD	LP3985IM5-3.0	LP3985IM5X-3.0	LCRB
3.1	STD	LP3985IM5-3.1	LP3985IM5X-3.1	LCZB
3.2	STD	LP3985IM5-3.2	LP3985IM5X-3.2	LDPB
3.3	STD	LP3985IM5-3.3	LP3985IM5X-3.3	LDQB
4.7	STD	LP3985IM5-4.7	LP3985IM5X-4.7	LDRB
5.0	STD	LP3985IM5-5.0	LP3985IM5X-5.0	LDSB

National Semiconductor

LP3986
Dual Micropower 150 mA Ultra Low-Dropout CMOS Voltage Regulators in micro SMD Package

General Description

The LP3986 is a 150 mA dual low dropout regulator designed for portable and wireless applications with demanding performance and board space requirements.

The LP3986 is stable with a small 1 µF ±30% ceramic output capacitor requiring smallest possible board space.

The LP3986's performance is optimized for battery powered systems to deliver ultra low noise, extremely low dropout voltage and low quiescent current independent of load current. Regulator ground current increases very slightly in dropout, further prolonging the battery life. Optional external bypass capacitor reduces the output noise further without slowing down the load transient response. Fast start-up time is achieved by utilizing a speed-up circuit that actively pre-charges the bypass capacitor. Power supply rejection is better than 60 dB at low frequencies and 55 dB at 10 kHz. High power supply rejection is maintained at lower input voltage levels common to battery operated circuits.

The LP3986 is available in micro SMD package. Performance is specified for −40°C to +125°C temperature range. For single LDO applications, please refer to the LP3985 datasheet.

Features

- Miniature 8-I/O micro SMD package
- Stable with 1µF ceramic and high quality tantalum output capacitors
- Fast turn-on
- Two independent regulators
- Logic controlled enable
- Over current and thermal protection
- Optional noise reduction capacitor

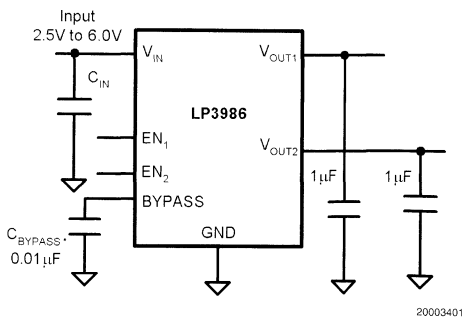
Key Specifications

- Guaranteed 150 mA output current per regulator
- 1nA typical quiescent current when both regulators in shutdown mode
- 60 mV typical dropout voltage at 150 mA output current
- 115 µA typical ground current
- 40 µV typical output noise
- 200 µs fast turn-on circuit
- −40°C to +125°C junction temperature

Applications

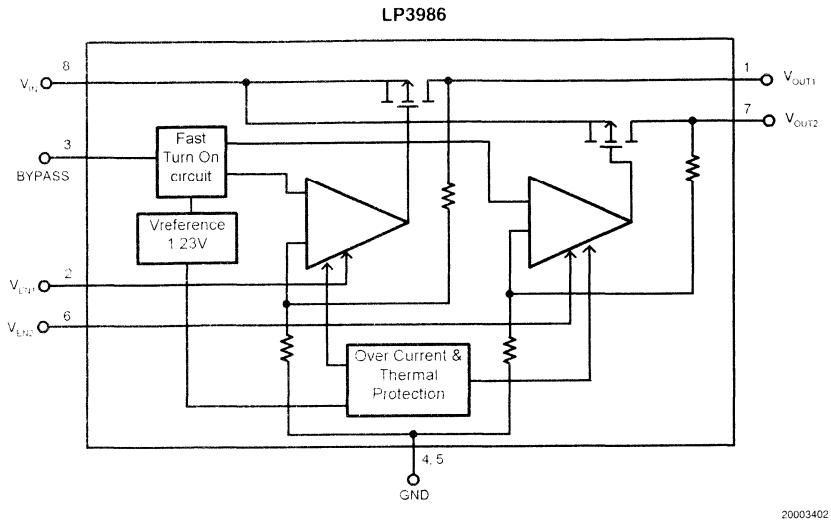
- CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- Portable battery applications

Typical Application Circuit

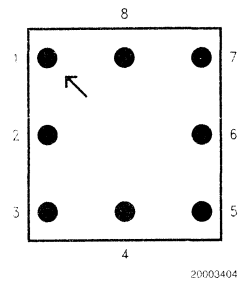


*Optional Noise Bypass Capacitor.

Block Diagram



Package Outline and Connection Diagram



Top View
8 Bump micro SMD Package
See NS Package Number BLA08

Pin Description

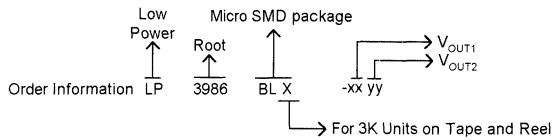
Name	µSMD	Function
V_{OUT2}	1	Output Voltage of the second LDO
EN_2	2	Enable input for the second LDO
BYPASS	3	Bypass capacitor for the bandgap
GND	4	Common ground
GND	5	Common ground
EN_1	6	Enable input for the first LDO
V_{OUT1}	7	Output Voltage of the first LDO
V_{IN}	8	Common input for both LDOs

Ordering Information

For micro SMD Package

Output Voltage (V)	Grade	LP3986 Supplied as 250 Units, Tape and Reel	LP3986 Supplied as 3000 Units, Tape and Reel
2.82.8*	STD	LP3986BL-2828	LP3986BLX2828
2.852.85	STD	LP3986BL-285285	LP3986BLX285285
2.52.8*	STD	LP3986BL-2528	LP3986BLX2528
3.03.0*	STD	LP3986BL-3030	LP3986BLX3030
3.13.1*	STD	LP3986BL-3131	LP3986BLX3131

* Please contact factory for availability.



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National Semiconductor

PRELIMINARY

LP3987
Micropower micro SMD 150 mA Ultra Low-Dropout CMOS Voltage Regulators with sleep MODE

General Description

The LP3987 is a 150mA fixed output voltage regulator with very low dropout voltage designed specially to meet requirements of battery-powered applications. The additional sleep MODE feature will reduce current consumption during standby operation to prolong the usage of battery.

Dropout Voltage: 100mV maximum dropout with 150mA load.

Shutdown: Less than 1µA quiescent current.

Sleep Mode: Typically 14µA quiescent current during sleep MODE to reduce battery consumption.

Enhanced Stability: The LP3987 is stable with minimum 1µF±20% low ESR ceramic output capacitor as low as 5mΩ and high quality tantalum capacitors.

The LP3987 is available in 5 Bump micro SMD package. Performance is specified for −40°C to 125°C.

For other voltage options, please contact National Semiconductor Corporation.

Features

- Miniature 5-I/O micro SMD package
- Stable with ceramic and high quality tantalum output capacitors
- Logic controlled enable
- Thermal Shutdown and short-circuit current limit

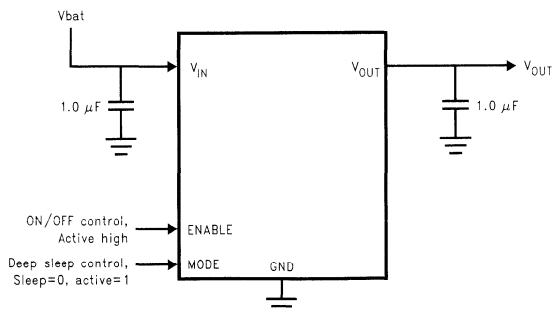
Key Specifications

- 3.05 to 6.0V input range
- Guaranteed 150 mA output current
- 1µA quiscent current on shutdown
- 100 mV maximum dropout with 150 mA load
- 50dB PSRR at 10KHz
- Sleep MODE features
- Over temperature & over current protection
- −40°C to +125°C junction temperature range for operation

Applications

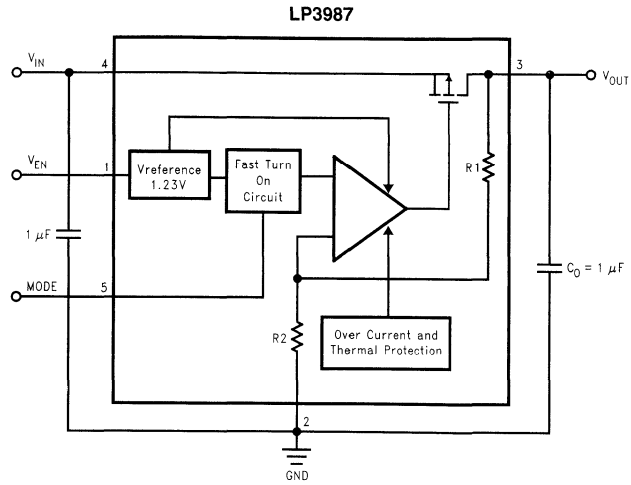
- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- µP/DSP Power Supplies
- Digital Cameras
- SRAM Backup

Typical Application Circuit

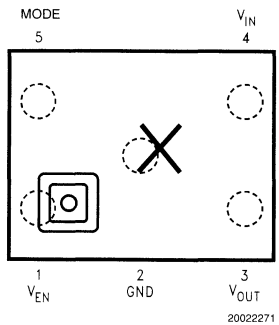


20022201

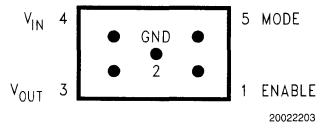
Block Diagram



Package Outline and Connection Diagram



Top View
5 I/O micro SMD Package
See NS Package Number BPA05



Bottom View
5 I/O micro SMD Package
See NS Package Number BPA05

Pin Descriptions

Pin	Name	Function
1	Enable	Active High Enable, Low = Shutdown
2	GND	Ground
3	V_{OUT}	Regulated Supply Output
4	V_{IN}	Unregulated Supply Input
5	MODE	Power Mode Control, Active = 1, Sleep Mode = 0

Ordering Information

BP refers as 0.170mm bump size

Output Voltage (V)	Grade	LP3987 Supplied as 250 Units, Tape and Reel	LP3987 Supplied as 3000 Units, Tape and Reel
2.85	STD	LP3987IBP-2.85	LP3987IBPX-2.85

National Semiconductor

LP3988
Micropower, 150mA Ultra Low-Dropout CMOS Voltage Regulator With Power Good

General Description

The LP3988 is a 150mA low dropout regulator designed specially to meet requirements of Portable battery-applications. The LP3988 is designed to work with a space saving, small 1µF ceramic capacitor. The LP3988 features an Error Flag output that indicates a faulty output condition.

The LP3988's performance is optimized for battery powered systems to deliver low noise, extremely low dropout voltage and low quiescent current. Regulator ground current increases only slightly in dropout, further prolonging the battery life.

Power supply rejection is better than 60 dB at low frequencies and starts to roll off at 10 kHz. High power supply rejection is maintained down to lower input voltage levels common to battery operated circuits.

The device is ideal for mobile phone and similar battery powered wireless applications. It provides up to 150 mA, from a 3.1V to 6V input, consuming less than 1 µA in disable mode and has fast turn-on time less than 200µs.

The LP3988 is available 5 pin SOT-23 package. Performance is specified for −40˚C to +125˚C temperature range and is available in 2.5, 2.6, 2.85 and 3.0V output voltage.

Key Specifications

- 3.1 to 6.0V input range
- 150mA guaranteed output
- 40dB PSRR at 10kHz
- ≤1 µA quiescent current when shut down
- Fast Turn-On time: 100 µs (typ.)
- 80 mV typ dropout with 150mA load
- −40 to +125˚C junction temperature range for operation
- 2.5, 2.6V, 2.85V and 3.0V*

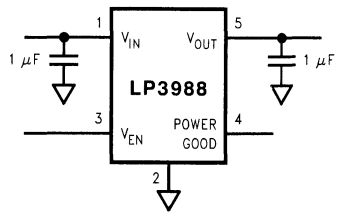
Features

- SOT-23-5 package
- Power-good flag output
- Logic controlled enable
- Stable with ceramic and high quality tantalum capacitors
- Fast turn-on
- Thermal shutdown and short-circuit current limit

Applications

- CDMA cellular handsets
- Wideband CDMA cellular handsets
- GSM cellular handsets
- Portable information appliances
- Tiny 3.3V ± 5% to 2.85V, 150mA converter

Typical Application Circuit



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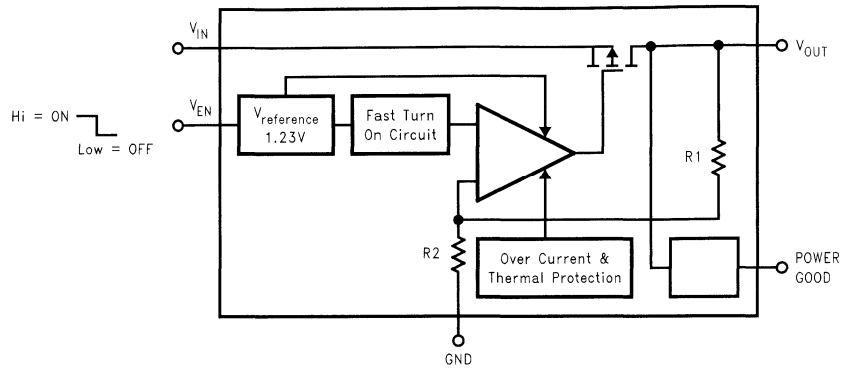
Block Diagram

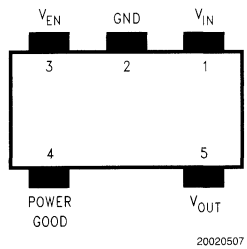


Pin Descriptions

Name	SOT	Function
V_{EN}	3	Enable Input Logic, Enable High
GND	2	Common Ground
V_{OUT}	5	Output Voltage of the LDO
V_{IN}	1	Input Voltage of the LDO
Power Good	4	Power Good Flag (output): open-drain output, connected to an external pull-up resistor. Active low indicates an output voltage out of tolerance condition.

Connection Diagram

SOT-23-5 Package (MF)



Top View
See NS Package Number MF05A

Ordering Information

Output Voltage (V)	Grade	LP3988 Supplied as 1000 Units, Tape and Reel	LP3988 Supplied as 3000 Units, Tape and Reel	Package Marking
2.5	STD	LP3988IMF-2.5	LP3988IMFX-2.5	LFSB
2.6	STD	LP3988IMF-2.6	LP3988IMFX-2.6	LDJB
2.85	STD	LP3988IMF-2.85	LP3988IMFX-2.85	LDLB
3.0	STD	LP3988IMF-3.0	LP3988IMFX-3.0	LFAB

Section 17

Voltage Regulators - Switching and SIMPLE SWITCHER

Section 17 Contents

National Semiconductor

Switching Regulators Selection Guide

SWITCHING REGULATORS FOR COMPUTING VOLTAGE CONVERSION

Part Number	Number Of Regulated Voltages	Linear Regulator Output (Note 1)	Switching Regulator			Input Voltage		Switching Frequency	Applications
			Output Adj. Range (V), Output Current	Initial Accuracy (Note 2)	5-Bit DAC	Min	Max		
Notebook and Battery Voltage Conversion									
LM2612	1		1.05, 1.3, 1.5, 1.8	2%		2.8	5.5	500-1000	Handheld Portable Electronics
LM2621	1		1.2 to 14V, 1A (Note 3)	3%		0.65	22	400-2000	PC Card Supply, TFT/LCD Bias Supply
LM2622	1		1.26 to 17V	2.5%		2	12	600-1250	General Purpose Boost
LM2640	3	5V	2.2 to 6V, controller	2%		5.5	30	200	Main V3.3, V5; $V_{STANDBY}$ 5V
LM2641	3	5V	2.2 to 6V, controller	2%		5.5	30	300	Main V3.3, V5; $V_{STANDBY}$ 5V
LM2650	1		1.5 to 16V, 3A	5%		4.5	18	90-300	Main V3.3, V5; V_{GTL}; V_{AGP}
LM2651	1		1.5 to 3.3V, 1.5A	3.8%		4	14	90-300	Main V3.3, V5; V_{GTL}; V_{AGP}
LM2653	1		1.5 to 3.3V, 1.5A			4	12	300	CPU $V_{I/O}$;V_{L2}; Video Chip Supply
LM2655	1		1.5 to 3.3V, 1.5A	3.5%		4	14	300	CPU $V_{I/O}$;V_{L2}; Video Chip Supply
LM2700	1		1.26 to 17V	2.5%		2	12	600-1250	General Purpose Boost
Desktop Voltage Conversion									
LM2633	3	Adj	0.925 to 2.0	1.5%	✓	4.5	30	250	CPU V_{CORE}, $V_{I/O}$
LM2636	1		1.3 to 3.5V, controller	1.5%	✓	4.5	5.5	50-1000	CPU V_{CORE}, $V_{I/O}$; V_{GTL}; V_{AGP}
LM2637	3	1.5V, 2.5V	1.3 to 3.5V, controller	1.5%	✓	4.75	5.25	50-1000	CPU V_{CORE}, $V_{I/O}$; V_{GTL}; V_{CLK}; V_{AGP}
LM2638	3	1.5V, 2.5V	1.3 to 3.5V, controller	1.5%	✓	4.75	5.25	50-1000	CPU V_{CORE}, $V_{I/O}$; V_{GTL}; V_{CLK}; V_{AGP}; $V_{STANDBY}$ 2.5V, 3.3V
LM2639	1		1.3 to 3.5V, Controller	1.5%	✓	4.75	5.25	40-10,000 (3 or 4 phase)	CPU V_{CORE}, $V_{I/O}$; V_{GTL}; V_{AGP}
LM2645	4	3.3 adj	1.3 to 5.5	1.5%		4.5	3.0	200-300	Main V3.3, V5; V_{GTL}; V_{AGP}
LM2720	1		1.3 to 3.5V, Controller	1.5%	✓	4.75	5.25	40-10,000 (3 or 4 phase)	CPU V_{CORE}, $V_{I/O}$; V_{GTL}; V_{AGP}

Note 1: For LM2637 and LM2638, output voltages of linear controllers default to the fixed values shown but are also adjustable.

Note 2: Accuracy of switching controller over temperature.

Note 3: LM2621 is a boost converter with a 2.85A (typ) switch. Maximum load current is up to 1A in most applications, but it is limited at lower input voltages. Consult datasheet for further information.

HIGH-PERFORMANCE & GENERAL-PURPOSE SWITCHING REGULATORS (includes SIMPLE SWITCHER® power converters)

Part Number	Output Voltage (Note 4)	Input Voltage		Operating Temperature (Note 5)	Switching Frequency	Conversion Efficiency	Package (Note 6)
		Min	Max				
BUCK CONVERTERS							
500 mA Output Current							
LM2671	3.3V, 5V, 12V, Adj	8V	40V	Ind	260-400	94%	M,N
LM2674	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	94%	M,N
LM2594/ HV	3.3V, 5V, 12V, Adj	4.75V	40V/60V	Ind	150	88%	M,N
LM2597/HV	3.3V, 5V, 12V, Adj	4.75V	40V/60V	Ind	150	88%	M,N
LM2574/ HV	3.3V, 5V, 12V, 15V, Adj	4.75V	40V/60V	Ind	52	80%	M,N
1.0 A Output Current							
LM2672	3.3V, 5V, 12V, Adj	8V	40V	Ind	260-400	94%	M,N
LM2675	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	94%	M,N
LM2595	3.3V, 5V, 12V, Adj	4.75V	40V	Ind	150	90%	S, T
LM2595Mil	3.3V, 5V, 12V, Adj	4.75V	40V	Mil	150	90%	J
LM2598	3.3V, 5V, 12V, Adj	4.75V	40V	Ind	150	90%	S, T
LM1575/HV	5V, 12V, 15V, Adj	4.75V	40V/60V	Mil	52	85%	K
LM2575/ HV	3.3V, 5V, 12V,15V, Adj	4.75V	40V/60V	Ind	52	85%	M, N, S, T
LM2590/ HV	3.3V, 5V, 12V, Adj	4.5V	60V	Ind	150	90%	S, T
LM2591/ HV	3.3V, 5V, 12V, Adj	4.5V	60V	Ind	150	90%	S, T
LM2592/ HV	3.3V, 5V, 12V, Adj	4.5V	60V	Ind	150	90%	S, T
LM2593/ HV	3.3V, 5V, 12V, Adj	4.5V	60V	Ind	150	90%	S, T
1.5 A Output Current							
LM2651	1.8, 2.5, 3.3, Adj	4	14	Ind	300	93%	MTC
LM2653	Adj (1.5 to 3.3V)	4	14	Ind	300	93%	MTC
2.5 A Output Current							
LM2655	3.3, Adj	4	14	Ind	300	93%	MTC
3.0 A Output Current							
LM2670	3.3V, 5V, 12V, Adj	8V	40V	Ind	260-400	94%	S, T
LM2673	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	94%	S, T
LM2676	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	94%	S, T
LM2596	3.3V, 5V, 12V, Adj	4.75V	40V	Ind	150	90%	S, T
LM2599	3.3V, 5V, 12V, Adj	4.75V	40V	Ind	150	90%	S, T
LM2576/ HV	3.3V, 5V, 12V,15V, Adj	6V	40V/60V	Ind	52	85%	S, T
5.0 A Output Current							
LM2677	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	92%	S, T
LM2678	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	92%	S, T
LM2679	3.3V, 5V, 12V, Adj	8V	40V	Ind	260	92%	S, T
BOOST/FLYBACK CONVERTERS							
				1.0 A Switch Current			
LM2698	Adj (2.2 to 17V)	2.2	12	Ind	600	90%	MM
2.0 A Switch Current							
LM2611		2.7	14	Ind	1400		MF
2.85 A Switch Current							
LM2621	Adj (1.2 to 14V)	0.65	22	Ind	400-2000	87%	MM
3.0 A Switch Current							
LM2585	3.3V, 5V, 12V, Adj	4V	40V	Ind	100	90%	S, T
LM2586	3.3V, 5V, 12V, Adj	4V	40V	Ind	100-200	90%	S, T

HIGH-PERFORMANCE & GENERAL-PURPOSE SWITCHING REGULATORS (includes SIMPLE SWITCHER® power converters) (Continued)

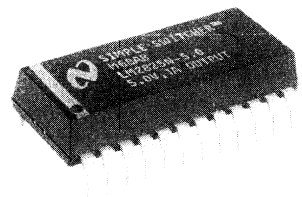
Part Number	Output Voltage (Note 4)	Input Voltage		Operating Temperature (Note 5)	Switching Frequency	Conversion Efficiency	Package (Note 6)
		Min	Max				
BUCK CONVERTERS							
500 mA Output Current							
3.0 A Switch Current							
LM1577	12V, 15V, Adj	3.5V	40V	Ind	52	80%	K
LM2577	12V, 15V, Adj	3.5V	40V	Ind	52	80%	M, N, S, T
5.0 A Switch Current							
LM2587	3.3V, 5V, 12V, Adj	4V	40V	Ind	100	90%	S, T
LM2588	3.3V, 5V, 12V, Adj	4V	40V	Ind	100-200	90%	S, T

PWM CONTROLLERS & MULTI-PURPOSE SWITCHING REGULATORS

Part Number	Input Voltage Range	Output Adj. Range	Switching Frequency (kHz)	Output	Package (Note 6)
LM1578A	2V to 40V	1.0V min.	0.001 to100	Open Transistor (0.75A)	H08
LM2578A	2V to 40V	1.0V min.	0.001 to100	Open Transistor (0.75A)	N08
LM3578A	2V to 40V	1.0V min.	0.001 to100	Open Transistor (0.75A)	M08, N08
LM2630	4.5V to 30V	1.8 to 6V	200 to 400	FET drive	MTC20
LM2631	4.5V to 30V	1.5 to 6V	200 to 400	FET drive	MTC20
LM2622 ~	2V to 12V		600 to 1000		MUA08A
LM2524D	5V to 40V	1.5V min.	1 to 550	Dual Alternating Open Transistor (0.2A)	N16
LM3524D	5V to 40V	1.5V min.	1 to 550	Dual Alternating Open Transistor (0.2A)	M16, N16
LM2640	5.5V to 30V	2.2 to 6V	200	FET drive	MTC28
LM2641	5V to 30V	7V to 15V	300	FET drive	MTC28
LM3477	3V to 35V		500	High-Side N-Channel FET drive	MSOP-8
LM3478	2.95V to 40V	1.25V	100 to 1000	Low-Side N-Channel FET drive	MSOP-8
LM3488	2.95V to 40V	1.25V	100 to 1000	Low-Side N-Channel FET drive	MSOP-8

INTEGRATED POWER SUPPLY SELECTION GUIDE

Integrated power supplies provide a complete DC-DC Converter, including capacitors and inductor, in a single molded dual-in-line package.



MS101096-1

Part Number	V_{IN}	V_{OUT}	I_{OUT}	Application	Package (Note 6)
LM2825-3.3	4.75V to 40V	3.3V	1A	Buck	N24
LM2825-5.0	7V to 40V	5.0V	1A	Buck	N24
LM2825-12	15V to 40V	12V	0.75A	Buck	N24
LM2825-ADJ	4.5V to 40V	1.23V to 8V	1A	Buck	N24
LM2825H-ADJ	9V to 40V	7V to 15V	0.55A	Buck	N24

Note 4: All switching converters have Current Limiting and Thermal Shutdown features Adj output voltage can be set typically from 1.23V to (V_{IN} max - 3V).

Note 5: Under Temp. Range the letters indicate temperature range. Ind = Industrial Temperature of -40 C to +125 C. Mil = Military Temperature of -55 C to +150 C.

Note 6: Under Package, the letter identifies the type of package. Numbers following the package letter indicate number of pins.

BP = micro SMD Package

MM = Miniature Small Outline Molded Package (MSOP)

K = Metal Can (TO-3)

M = Small Outline Molded Package (Surface Mount)

MTC = Molded Thin Shrink Small Outline Package (TSSOP)

LLP = Leadless Leadframe Package

N = Molded Dual-In-Line Package

S = TO-263 (Power Surface Mount)

K = TO-220 (Power Through Hole)

J = Aluminum Nitride Ceramic Dual-In-Line Package

National Semiconductor

Switching Regulators Definition Of Terms

Boost Regulator: A switching regulator topology in which a lower DC voltage is converted to a higher DC voltage. Also known as a *Step-Up Regulator.*

Buck Regulator: A switching regulator topology in which a higher DC voltage is converted to a lower DC voltage. Also known as a *Step-Down Regulator*

Buck-Boost Regulator: A switching regulator topology in which a positive DC voltage is converted to a negative DC voltage without the use of a transformer. A variation of this topology produces a positive DC output voltage which is between the positive DC output voltage maximum and minimum limits, i.e., providing both buck and boost functions.

Burst Mode: The mode of operation in a switching regulator that results when the load current is reduced to the point where the minimum duty cycle of each pulse provides more energy than the load demands, thus causing the controller to 'skip' pulses (or sets of pulses) to maintain the output voltage at its correct value.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Duty Cycle (D): The ratio of the period time the output switch os ON to the total oscillator period.

$$D = t_{ON}/T$$

Capacitor Ripple Current: The RMS value of the maximum allowable alternating current at which a capacitor can be operated continuously at a specified temperature. This parameter is specified by the capacitor manufacturer, and must be considered when a capacitor is used as a part of a switching regulator input or output filter.

Catch Diode: The diode which provides a return path for the load current when the regulator switch is OFF. For switching regulators, the types of diodes normally used include Schottky-barrier, fast-recovery, and ultra-fast recovery. Also known as a *steering diode* or *free-wheeling diode.*

Collector Saturation Voltage: With the emitter grounded and the switch ON, the collector-to-emitter voltage of an NPN transistor switch at a specified collector current.

Compensation: The circuitry required to provide adequate stability for the regulator control loop.

Continuous Mode Operation: Relates to the inductor current. In the continuous mode, the inductor current is always greater than zero. In discontinuous mode, the inductor current falls to zero before the end of each switching cycle.

Current Limit Sense Voltage: For regulator ICs that have externally-controlled limit, the current limit sense voltage is the voltage that must be applied (between two specified pins) to turn the output transistor OFF and start other current limit functions within the IC.

Current-Mode Control: A method of feedback control used in switching regulators where both the output voltage and the switch current are used to control the switching element.

Diode Recovery Time: The period of time it takes the current through a diode to return to zero after the forward voltage is removed (i.e., the diode is turned OFF).

Discontinuous Mode Operation: See *Continuous Mode Operation*

Efficiency (η): The proportion of input power actually delivered to the load.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}}$$

Electromagnetic Interference (EMI): A generic term which is used to refer to any type of unwanted electromagnetic radiation coming from a system such as a switching regulator.

Emitter Saturation Voltage: With the collector pulled up to the DC input voltage and the switch ON, the collector-to-emitter voltage of a NPN transistor switch at a specified emitter current.

Error Amplifier (or Comparator): An amplifier (or comparator) which is used to detect the difference between a feedback voltage (usually proportional to the output voltage) and a DC reference voltage. The resulting error voltage is used in the regulator control circuitry to adjust the switch on-time. This error amplifier may be either a transconductance-type or an operational amplifier.

ESR: A parasitic element of every capacitor, the ESR (equivalent series resistance) is the purely resistive component of a real capacitor's impedance. It is modeled as a resistor in series with the capacitive element, and its value is usually determined by the device construction.

ESL: A parasitic element of every capacitor, which limits its effectiveness at high frequencies. The ESL (equivalent series inductance) is the pure inductance component of a device. Its value is usually determined by the device construction, especially its leads. It is modeled as an inductor in series with the capacitive element.

E·T$_{OP}$: See *Operating Volt-Microsecond Constant.*

Flyback Regulator: A switching regulator topology in which a DC voltage is converted to another DC voltage by means of a transformer which stores energy delivered by a switch during the switch ON time, and transfers the energy to an output storage capacitor during the switch OFF time.

Inductor Ripple Current (ΔI_{IND}): The peak-to-peak value of the inductor current waveform, typically a sawtooth waveform when the regulator is operating in the continuous mode.

Inductor Saturation: The condition which exists when an inductor cannot hold any more magnetic flux. When an inductor saturates, its inductance appears to decrease and the resistive component dominates. Inductor current is then limited only by the DC resistance of the wire and the available source current.

Inverting Regulator: A switching regulator which converts a positive DC voltage to a negative DC voltage. The buck-boost topology is often used for this function.

Magnetic Flux Interference: Unwanted interference emitted by magnetic components (transformers and inductors) in the form of magnetic flux. Magnetic flux interference can be minimized by the use of magnetic cores (such as toroid or pot core) which contain the flux, or by shielding with materials such as steel or mu-metal. Aluminium and copper are not effective in shielding flux.

Operating Volt-Microsecond Constant: The product (in Volts X microseconds) of the voltage applied to the switching regulator inductor and the period of time the voltage is applied. Abbreviated as $E \cdot T_{OP}$, this constant is a measure of the energy-handling capability of an inductor, and is dependent upon the type of core used, its core area, the number of turns of wire used, and the applied duty cycle.

Oscillator Frequency: The frequency of the internal oscillator used in the control of the switching regulator. Generally the same as the *switching frequency*, for most regulators the oscillator frequency is fixed, either internally or by an external resistor and/or capacitor.

Output Ripple Voltage: The AC component of the switching regulator output voltage. It is usually dominated by the output capacitor ESR multiplied by the applied ripple current, but may have high-frequency spikes caused by effects of output capacitor ESL.

Pulse-Width Modulation (PWM): A method of control used in a switching regulator where the duty cycle of the switching element is used to control the output voltage.

Radio Frequency Interference (RFI): High-frequency electromagnetic radiation resulting from the high switching speeds of switching transistors and rectifiers, often causing problems in nearby circuitry that is sensitive to the large noise 'spikes' that are often associated with it. RFI can be easily shielded by a good electrical conductor such as copper or aluminium.

Snubber: A network used to limit the voltage developed across a component. The network usually consists of a zero diode, or a diode in series with a parallel resistor and capacitor. In a switching regulator, the snubber is most often used to limit the switch voltage of a flyback regulator.

Soft Start: In a switching regulator, a soft start limits the duty cycle of the regulator during start up. This in turn limits the energy the regulator demands from its source while building up the output voltage from its initial condition of 0V.

Standby Quiescent Current: For a regulator with an ON/OFF pin, this is the supply current (or ground pin current) required by the regulator IC when in the standby (OFF) mode.

Switch: In a switching regulator, a transistor or MOSFET used to deliver energy, in pulses, into energy storage devices (such as inductors, transformers, or capacitors) for use by a load.

Switching Frequency: See *Oscillator Frequency.*

Step Response: The transient response of a regulator output after the load current is 'stepped' from one value to another. This test is often used for evaluating the loop stability of a regulator.

Transient Response Time: The period of time it takes the output of a regulator to return to a steady-state value after a change in line voltage or load current. See also *Step Response.*

Voltage Mode Control: A method of control used in a switching regulator where the feedback from the output voltage is used to provide control of the switching element.

National Semiconductor

LM1575/LM2575/LM2575HV
SIMPLE SWITCHER® 1A Step-Down Voltage Regulator

General Description

The LM2575 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, 15V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM2575 series offers a high-efficiency replacement for popular three-terminal linear regulators. It substantially reduces the size of the heat sink, and in many cases no heat sink is required.

A standard series of inductors optimized for use with the LM2575 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring 50 μA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

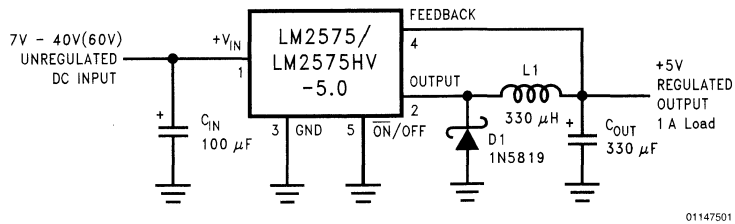
Features

- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Adjustable version output voltage range, 1.23V to 37V (57V for HV version) ±4% max over line and load conditions
- Guaranteed 1A output current
- Wide input voltage range, 40V up to 60V for HV version
- Requires only 4 external components
- 52 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- P+ Product Enhancement tested

Applications

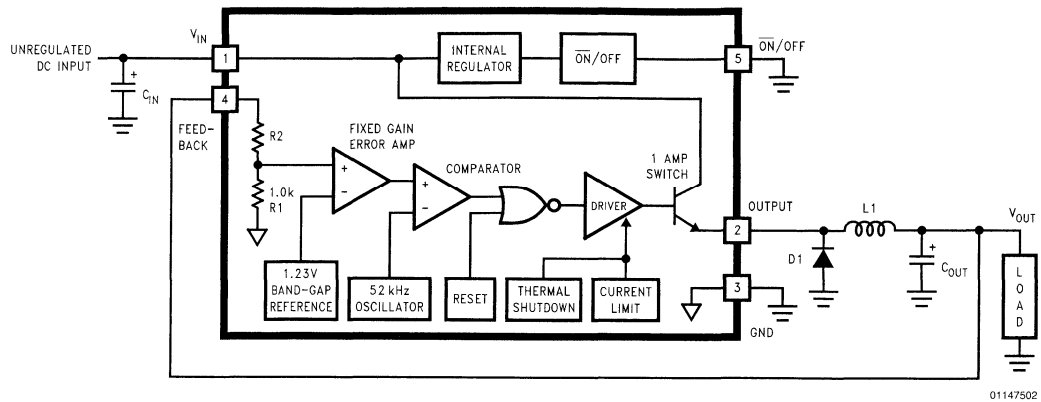
- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regualtor for linear regulators
- On-card switching regulators
- Positive to negative converter (Buck-Boost)

Typical Application (Fixed Output Voltage Versions)



Note: Pin numbers are for the TO-220 package.

Block Diagram and Typical Application



3.3V, R2 = 1.7k

5V, R2 = 3.1k

12V, R2 = 8.84k

15V, R2 = 11.3k

For ADJ. Version

R1 = Open, R2 = 0Ω

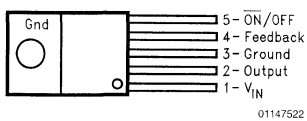
Note: Pin numbers are for the TO-220 package.

FIGURE 1.

Connection Diagrams

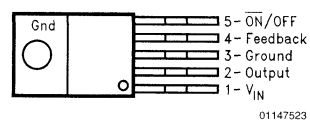
(XX indicates output voltage option. See Ordering Information table for complete part number.)

Straight Leads
5–Lead TO-22 (T)

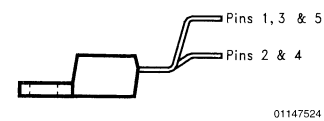


Top View
LM2575T-XX or LM2575HVT-XX
See NS Package Number T05A

Bent, Staggered Leads
5-Lead TO-220 (T)

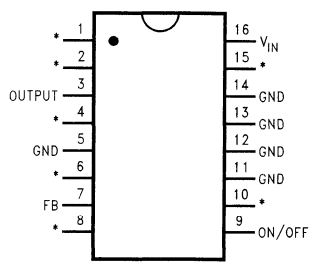


Top View



Side View
LM2575T-XX Flow LB03 or
LM2575HVT-XX Flow LB03
See NS Package Number T05D

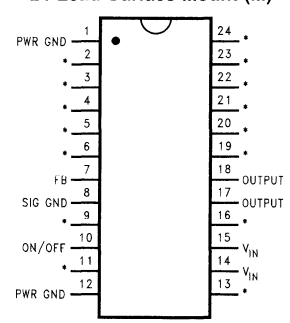
16–Lead DIP (N or J)



Top View
LM2575N-XX or LM2575HVN-XX
See NS Package Number N16A
LM1575J-XX-QML
See NS Package Number J16A

*No Internal Connection

24-Lead Surface Mount (M)

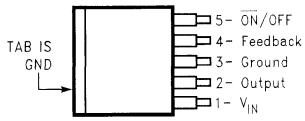


Top View
LM2575M-XX or LM2575HVM-XX
See NS Package Number M24B

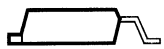
*No Internal Connection

Connection Diagrams (XX indicates output voltage option. See Ordering Information table for complete part number.) (Continued)

TO-263(S)
5-Lead Surface-Mount Package



Top View



Side View
LM2575S-XX or LM2575HVS-XX
See NS Package Number TS5B

Ordering Information

Package Type	NSC Package Number	Standard Voltage Rating (40V)	High Voltage Rating (60V)	Temperature Range
5-Lead TO-220 Straight Leads	T05A	LM2575T-3.3	LM2575HVT-3.3	$-40\ C \le T_J \le +125\ C$
		LM2575T-5.0	LM2575HVT-5.0	
		LM2575T-12	LM2575HVT-12	
		LM2575T-15	LM2575HVT-15	
		LM2575T-ADJ	LM2575HVT-ADJ	
5-Lead TO-220 Bent and Staggered Leads	T05D	LM2575T-3.3 Flow LB03	LM2575HVT-3.3 Flow LB03	
		LM2575T-5.0 Flow LB03	LM2575HVT-5.0 Flow LB03	
		LM2575T-12 Flow LB03	LM2575HVT-12 Flow LB03	
		LM2575T-15 Flow LB03	LM2575HVT-15 Flow LB03	
		LM2575T-ADJ Flow LB03	LM2575HVT-ADJ Flow LB03	
16-Pin Molded DIP	N16A	LM2575N-5.0	LM2575HVN-5.0	
		LM2575N-12	LM2575HVN-12	
		LM2575N-15	LM2575HVN-15	
		LM2575N-ADJ	LM2575HVN-ADJ	
24-Pin Surface Mount	M24B	LM2575M-5.0	LM2575HVM-5.0	
		LM2575M-12	LM2575HVM-12	
		LM2575M-15	LM2575HVM-15	
		LM2575M-ADJ	LM2575HVM-ADJ	
5-Lead TO-236 Surface Mount	TS5B	LM2575S-3.3	LM2575HVS-3.3	
		LM2575S-5.0	LM2575HVS-5.0	
		LM2575S-12	LM2575HVS-12	
		LM2575S-15	LM2575HVS-15	
		LM2575S-ADJ	LM2575HVS-ADJ	
16-Pin Ceramic DIP	J16A	LM1575J-3.3-QML		$-55\ C \le T_J \le +150\ C$
		LM1575J-5.0-QML		
		LM1575J-12-QML		
		LM1575J-15-QML		
		LM1575J-ADJ-QML		

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National Semiconductor

LM1577/LM2577
SIMPLE SWITCHER® Step-Up Voltage Regulator

General Description

The LM1577/LM2577 are monolithic integrated circuits that provide all of the power and control functions for step-up (boost), flyback, and forward converter switching regulators. The device is available in three different output voltage versions: 12V, 15V, and adjustable.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Listed in this data sheet are a family of standard inductors and flyback transformers designed to work with these switching regulators.

Included on the chip is a 3.0A NPN switch and its associated protection circuitry, consisting of current and thermal limiting, and undervoltage lockout. Other features include a 52 kHz fixed-frequency oscillator that requires no external components, a soft start mode to reduce in-rush current during start-up, and current mode control for improved rejection of input voltage and output load transients.

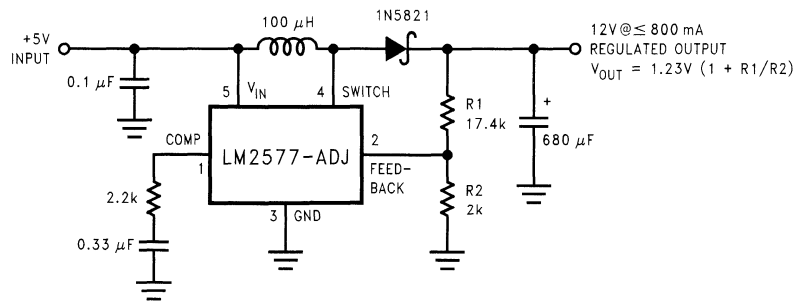
Features

- Requires few external components
- NPN output switches 3.0A, can stand off 65V
- Wide input voltage range: 3.5V to 40V
- Current-mode operation for improved transient response, line regulation, and current limit
- 52 kHz internal oscillator
- Soft-start function reduces in-rush current during start-up
- Output switch protected by current limit, under-voltage lockout, and thermal shutdown

Typical Applications

- Simple boost regulator
- Flyback and forward regulators
- Multiple-output regulator

Typical Application



Note: Pin numbers shown are for TO-220 (T) package.

Ordering Information

Temperature Range	Package Type	Output Voltage			NSC Package Drawing	Package
		12V	15V	ADJ		
$-40^{\circ}C \le T_A \le +125^{\circ}C$	24-Pin Surface Mount	LM2577M-12	LM2577M-15	LM2577M-ADJ	M24B	SO
	16-Pin Molded DIP	LM2577N-12	LM2577N-15	LM2577N-ADJ	N16A	N
	5-Lead Surface Mount	LM2577S-12	LM2577S-15	LM2577S-ADJ	TS5B	TO-263
	5-Straight Leads	LM2577T-12	LM2577T-15	LM2577T-ADJ	T05A	TO-220
	5-Bent Staggered Leads	LM2577T-12 Flow LB03	LM2577T-15 Flow LB03	LM2577T-ADJ Flow LB03	T05D	TO-220
$-55^{\circ}C \le T_A \le +150^{\circ}C$	4-Pin TO-3	LM1577K-12/883	LM1577K-15/883	LM1577K-ADJ/883	K04A	TO-3

National Semiconductor

LM2524D/LM3524D
Regulating Pulse Width Modulator

General Description

The LM3524D family is an improved version of the industry standard LM3524. It has improved specifications and additional features yet is pin for pin compatible with existing 3524 families. New features reduce the need for additional external circuitry often required in the original version.

The LM3524D has a ±1% precision 5V reference. The current carrying capability of the output drive transistors has been raised to 200 mA while reducing V_{CEsat} and increasing V_{CE} breakdown to 60V. The common mode voltage range of the error-amp has been raised to 5.5V to eliminate the need for a resistive divider from the 5V reference.

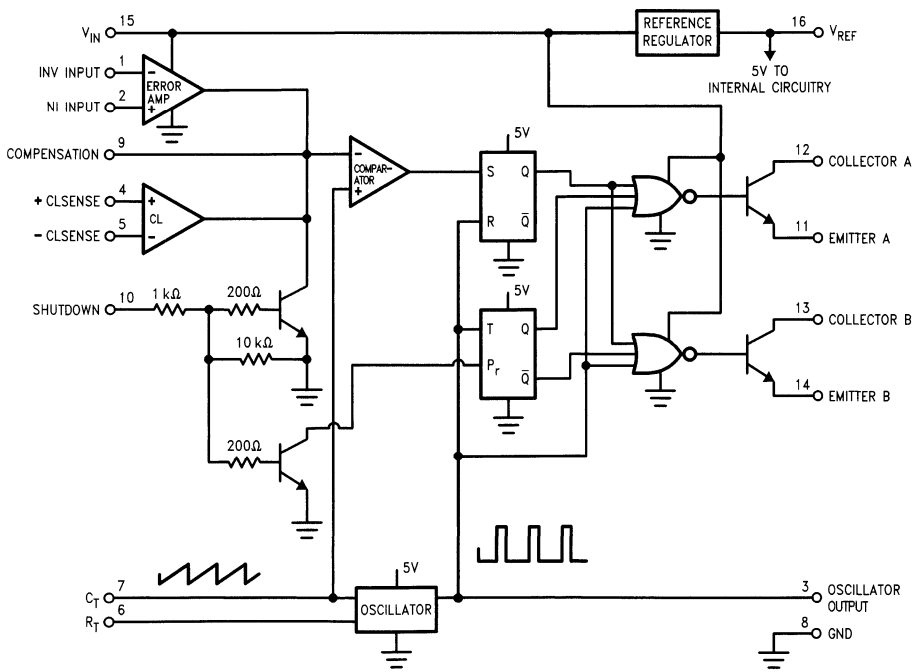
In the LM3524D the circuit bias line has been isolated from the shut-down pin. This prevents the oscillator pulse amplitude and frequency from being disturbed by shut-down. Also at high frequencies (≅300 kHz) the max. duty cycle per output has been improved to 44% compared to 35% max. duty cycle in other 3524s.

In addition, the LM3524D can now be synchronized externally, through pin 3. Also a latch has been added to insure one pulse per period even in noisy environments. The LM3524D includes double pulse suppression logic that insures when a shut-down condition is removed the state of the T-flip-flop will change only after the first clock pulse has arrived. This feature prevents the same output from being pulsed twice in a row, thus reducing the possibility of core saturation in push-pull designs.

Features

- Fully interchangeable with standard LM3524 family
- ±1% precision 5V reference with thermal shut-down
- Output current to 200 mA DC
- 60V output capability
- Wide common mode input range for error-amp
- One pulse per period (noise suppression)
- Improved max. duty cycle at high frequencies
- Double pulse suppression
- Synchronize through pin 3

Block Diagram



National Semiconductor

LM2574/LM2574HV
SIMPLE SWITCHER™ 0.5A Step-Down Voltage Regulator

General Description

The LM2574 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, 15V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM2574 series offers a high-efficiency replacement for popular three-terminal linear regulators. Because of its high efficiency, the copper traces on the printed circuit board are normally the only heat sinking needed.

A standard series of inductors optimized for use with the LM2574 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring 50 μA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

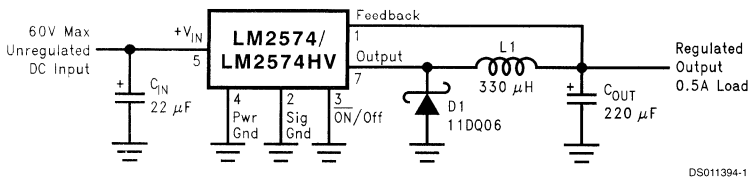
Features

- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Adjustable version output voltage range, 1.23V to 37V (57V for HV version) ±4% max over line and load conditions
- Guaranteed 0.5A output current
- Wide input voltage range, 40V, up to 60V for HV version
- Requires only 4 external components
- 52 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (Buck-Boost)

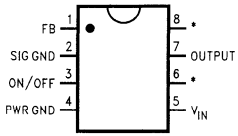
Typical Application (Fixed Output Voltage Versions)



Note: Pin numbers are for 8-pin DIP package.

Connection Diagrams

8-Lead DIP



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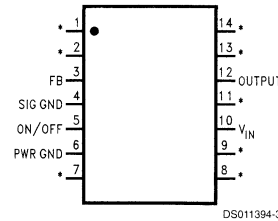
* No internal connection, but should be soldered to PC board for best heat transfer.

Top View
Order Number LM2574-3.3HVN, LM2574HVN-5.0, LM2574HVN-12, LM2574HVN-15, LM2574HVN-ADJ, LM2574N-3.3, LM2574N-5.0, LM2574N-12, LM2574N-15 or LM2574N-ADJ
See NS Package Number N08A

14-Lead Wide Surface Mount (WM)



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Top View
Order Number LM2574HVM-3.3, LM2574HVM-5.0, LM2574HVM-12, LM2574HVM-15, LM2574HVM-ADJ, LM2574M-3.3 LM2574M-5.0, LM2574M-12, LM2574M-15 or LM2574M-ADJ
See NS Package Number M14B

National Semiconductor

LM2576/LM2576HV Series
SIMPLE SWITCHER® 3A Step-Down Voltage Regulator

General Description

The LM2576 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving 3A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, 15V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation and a fixed-frequency oscillator.

The LM2576 series offers a high-efficiency replacement for popular three-terminal linear regulators. It substantially reduces the size of the heat sink, and in some cases no heat sink is required.

A standard series of inductors optimized for use with the LM2576 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring 50 µA (typical) standby current. The output switch includes cycle-by-cycle current limiting, as well as thermal shutdown for full protection under fault conditions.

Features

- 3.3V, 5V, 12V, 15V, and adjustable output versions
- Adjustable version output voltage range, 1.23V to 37V (57V for HV version) ±4% max over line and load conditions
- Guaranteed 3A output current
- Wide input voltage range, 40V up to 60V for HV version
- Requires only 4 external components
- 52 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection
- P+ Product Enhancement tested

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter (Buck-Boost)

Typical Application (Fixed Output Voltage Versions)

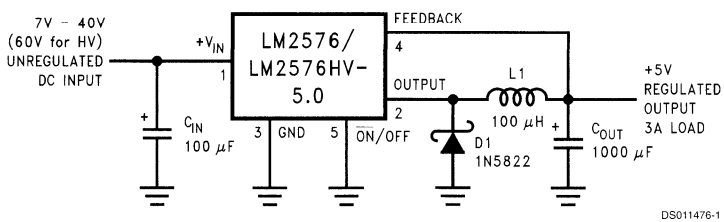
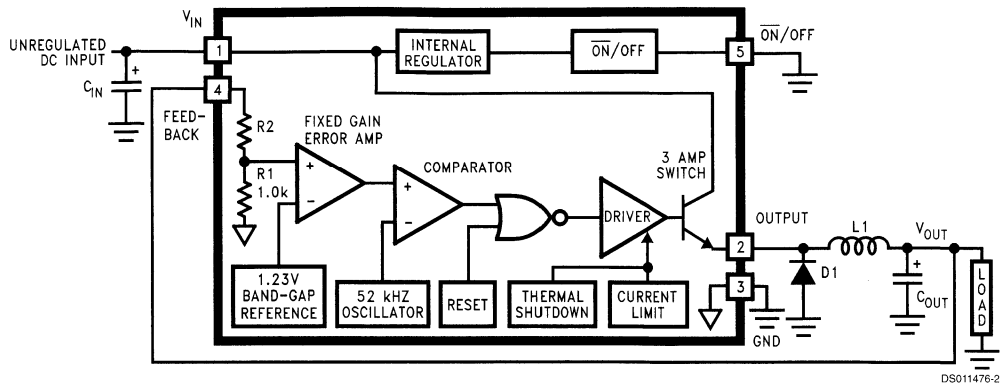


FIGURE 1.

Block Diagram



3.3V R2 = 1.7k
5V, R2 = 3.1k
12V, R2 = 8.84k
15V, R2 = 11.3k
For ADJ. Version
R1 = Open, R2 = 0Ω
Patent Pending

Ordering Information

Temperature Range	Output Voltage					NS Package Number	Package Type
	3.3	5.0	12	15	ADJ		
−40°C ≤ T_A ≤ 125°C	LM2576HVS-3.3	LM2576HVS-5.0	LM2576HVS-12	LM2576HVS-15	LM2576HVS-ADJ	TS5B	TO-263
	LM2576S-3.3	LM2576S-5.0	LM2576S-12	LM2576S-15	LM2576S-ADJ		
	LM2576HVSX-3.3	LM2576HVSX-5.0	LM2576HVSX-12	LM2576HVSX-15	LM2576HVSX-ADJ	TS5B Tape & Reel	
	LM2576SX-3.3	LM2576SX-5.0	LM2576SX-12	LM2576SX-15	LM2576SX-ADJ		
	LM2576HVT-3.3	LM2576HVT-5.0	LM2576HVT-12	LM2576HVT-15	LM2576HVT-ADJ	T05A	TO-220
	LM2576T-3.3	LM2576T-5.0	LM2576T-12	LM2576T-15	LM2576T-ADJ		
	LM2576HVT-3.3 Flow LB03	LM2576HVT-5.0 Flow LB03	LM2576HVT-12 Flow LB03	LM2576HVT-15 Flow LB03	LM2576HVT-ADJ Flow LB03	T05D	
	LM2576T-3.3 Flow LB03	LM2576T-5.0 Flow LB03	LM2576T-12 Flow LB03	LM2576T-15 Flow LB03	LM2576T-ADJ Flow LB03		

National Semiconductor

LM2578A/LM3578A Switching Regulator

General Description

The LM2578A is a switching regulator which can easily be set up for such DC-to-DC voltage conversion circuits as the buck, boost, and inverting configurations. The LM2578A features a unique comparator input stage which not only has separate pins for both the inverting and non-inverting inputs, but also provides an internal 1.0V reference to each input, thereby simplifying circuit design and p.c. board layout. The output can switch up to 750 mA and has output pins for its collector and emitter to promote design flexibility. An external current limit terminal may be referenced to either the ground or the V_{in} terminal, depending upon the application. In addition, the LM2578A has an on board oscillator, which sets the switching frequency with a single external capacitor from <1 Hz to 100 kHz (typical).

The LM2578A is an improved version of the LM2578, offering higher maximum ratings for the total supply voltage and output transistor emitter and collector voltages.

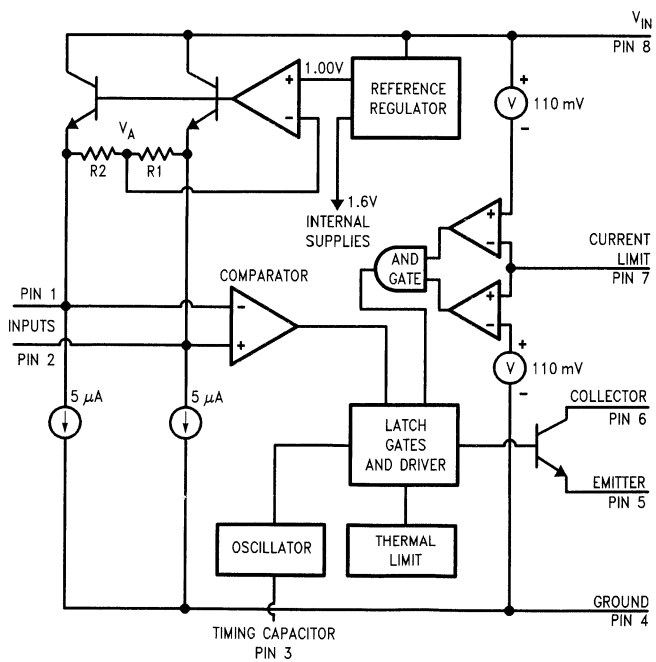
Features

- Inverting and non-inverting feedback inputs
- 1.0V reference at inputs
- Operates from supply voltages of 2V to 40V
- Output current up to 750 mA, saturation less than 0.9V
- Current limit and thermal shut down
- Duty cycle up to 90%

Applications

- Switching regulators in buck, boost, inverting, and single-ended transformer configurations
- Motor speed control
- Lamp flasher

Functional Diagram



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National Semiconductor

LM2585
SIMPLE SWITCHER® 3A Flyback Regulator

General Description

The LM2585 series of regulators are monolithic integrated circuits specifically designed for flyback, step-up (boost), and forward converter applications. The device is available in 4 different output voltage versions: 3.3V, 5.0V, 12V, and adjustable.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Included in the datasheet are typical circuits of boost and flyback regulators. Also listed are selector guides for diodes and capacitors and a family of standard inductors and flyback transformers designed to work with these switching regulators.

The power switch is a 3.0A NPN device that can stand-off 65V. Protecting the power switch are current and thermal limiting circuits, and an undervoltage lockout circuit. This IC contains a 100 kHz fixed-frequency internal oscillator that permits the use of small magnetics. Other features include soft start mode to reduce in-rush current during start up, current mode control for improved rejection of input voltage and output load transients and cycle-by-cycle current limiting. An output voltage tolerance of ±4%, within specified input voltages and output load conditions, is guaranteed for the power supply system.

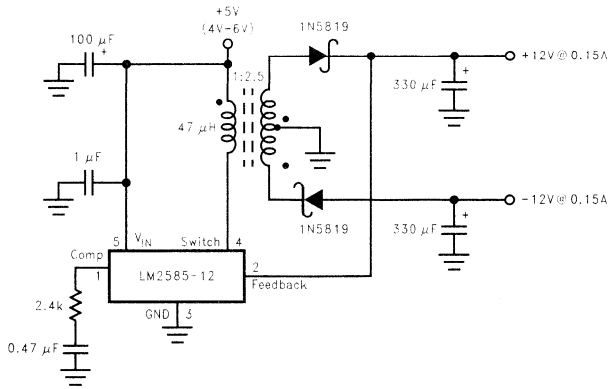
Features

- Requires few external components
- Family of standard inductors and transformers
- NPN output switches 3.0A, can stand off 65V
- Wide input voltage range: 4V to 40V
- Current-mode operation for improved transient response, line regulation, and current limit
- 100 kHz switching frequency
- Internal soft-start function reduces in-rush current during start-up
- Output transistor protected by current limit, under voltage lockout, and thermal shutdown
- System Output Voltage Tolerance of ±4% max over line and load conditions

Typical Applications

- Flyback regulator
- Multiple-output regulator
- Simple boost regulator
- Forward converter

Flyback Regulator



Ordering Information

Package Type	NSC Package Drawing	Order Number
5-Lead TO-220 Bent, Staggered Leads	T05D	LM2585T-3.3, LM2585T-5.0, LM2585T-12, LM2585T-ADJ
5-Lead TO-263	TS5B	LM2585S-3.3, LM2585S-5.0, LM2585S-12, LM2585S-ADJ
5-Lead TO-263 Tape and Reel	TS5B	LM2585SX-3.3, LM2585SX-5.0, LM2585SX-12, LM2585SX-ADJ

National Semiconductor

LM2586
SIMPLE SWITCHER® 3A Flyback Regulator with Shutdown

General Description

The LM2586 series of regulators are monolithic integrated circuits specifically designed for flyback, step-up (boost), and forward converter applications. The device is available in 4 different output voltage versions: 3.3V, 5.0V, 12V, and adjustable.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Included in the datasheet are typical circuits of boost and flyback regulators. Also listed are selector guides for diodes and capacitors and a family of standard inductors and flyback transformers designed to work with these switching regulators.

The power switch is a 3.0A NPN device that can stand-off 65V. Protecting the power switch are current and thermal limiting circuits, and an undervoltage lockout circuit. This IC contains an adjustable frequency oscillator that can be programmed up to 200 kHz. The oscillator can also be synchronized with other devices, so that multiple devices can operate at the same switching frequency.

Other features include soft start mode to reduce in-rush current during start up, and current mode control for improved rejection of input voltage and output load transients and cycle-by-cycle current limiting. The device also has a shutdown pin, so that it can be turned off externally. An output voltage tolerance of ±4%, within specified input voltages and output load conditions, is guaranteed for the power supply system.

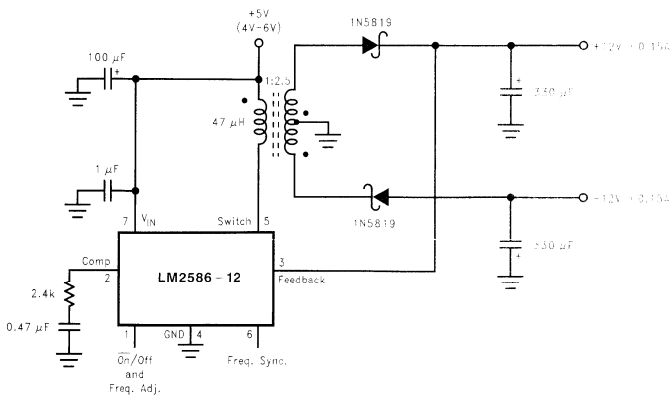
Features

- Requires few external components
- Family of standard inductors and transformers
- NPN output switches 3.0A, can stand off 65V
- Wide input voltage range: 4V to 40V
- Adjustable switching frequency: 100 kHz to 200 kHz
- External shutdown capability
- Draws less than 60 µA when shut down
- Frequency synchronization
- Current-mode operation for improved transient response, line regulation, and current limit
- Internal soft-start function reduces in-rush current during start-up
- Output transistor protected by current limit, under voltage lockout, and thermal shutdown
- System output voltage tolerance of ±4% max over line and load conditions

Typical Applications

- Flyback regulator
- Forward converter
- Multiple-output regulator
- Simple boost regulator

Flyback Regulator



Ordering Information

Package Type	NSC Package Drawing	Order Number
7-Lead TO-220 Bent, Staggered Leads	TA07B	LM2586T-3.3, LM2586T-5.0, LM2586T-12, LM2586T-ADJ
7-Lead TO-263	TS7B	LM2586S-3.3, LM2586S-5.0, LM2586S-12, LM2586S-ADJ
7-Lead TO-263 Tape and Reel	TS7B	LM2586SX-3.3, LM2586SX-5.0, LM2586SX-12, LM2586SX-ADJ

National Semiconductor

LM2587
SIMPLE SWITCHER® 5A Flyback Regulator

General Description

The LM2587 series of regulators are monolithic integrated circuits specifically designed for flyback, step-up (boost), and forward converter applications. The device is available in 4 different output voltage versions: 3.3V, 5.0V, 12V, and adjustable.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Included in the datasheet are typical circuits of boost and flyback regulators. Also listed are selector guides for diodes and capacitors and a family of standard inductors and flyback transformers designed to work with these switching regulators.

The power switch is a 5.0A NPN device that can stand-off 65V. Protecting the power switch are current and thermal limiting circuits, and an undervoltage lockout circuit. This IC contains a 100 kHz fixed-frequency internal oscillator that permits the use of small magnetics. Other features include soft start mode to reduce in-rush current during start up, current mode control for improved rejection of input voltage and output load transients and cycle-by-cycle current limiting. An output voltage tolerance of ±4%, within specified input voltages and output load conditions, is guaranteed for the power supply system.

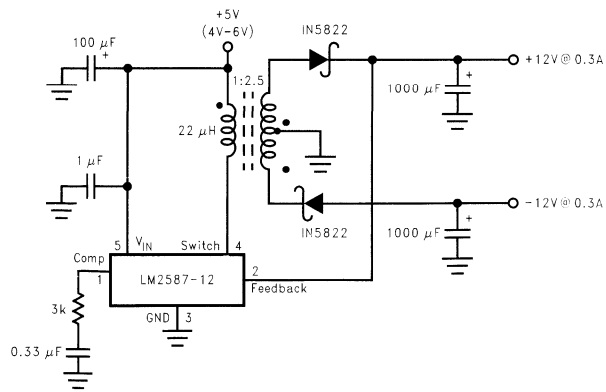
Features

- Requires few external components
- Family of standard inductors and transformers
- NPN output switches 5.0A, can stand off 65V
- Wide input voltage range: 4V to 40V
- Current-mode operation for improved transient response, line regulation, and current limit
- 100 kHz switching frequency
- Internal soft-start function reduces in-rush current during start-up
- Output transistor protected by current limit, under voltage lockout, and thermal shutdown
- System Output Voltage Tolerance of ±4% max over line and load conditions

Typical Applications

- Flyback regulator
- Multiple-output regulator
- Simple boost regulator
- Forward converter

Flyback Regulator



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Ordering Information

Package Type	NSC Package Drawing	Order Number
5-Lead TO-220 Bent, Staggered Leads	T05D	LM2587T-3.3, LM2587T-5.0, LM2587T-12, LM2587T-ADJ
5-Lead TO-263	TS5B	LM2587S-3.3, LM2587S-5.0, LM2587S-12, LM2587S-ADJ
5-Lead TO-263 Tape and Reel	TS5B	LM2587SX-3.3, LM2587SX-5.0, LM2587SX-12, LM2587SX-ADJ

National Semiconductor

LM2588
SIMPLE SWITCHER® 5A Flyback Regulator with Shutdown

General Description

The LM2588 series of regulators are monolithic integrated circuits specifically designed for flyback, step-up (boost), and forward converter applications. The device is available in 4 different output voltage versions: 3.3V, 5.0V, 12V, and adjustable.

Requiring a minimum number of external components, these regulators are cost effective, and simple to use. Included in the datasheet are typical circuits of boost and flyback regulators. Also listed are selector guides for diodes and capacitors and a family of standard inductors and flyback transformers designed to work with these switching regulators.

The power switch is a 5.0A NPN device that can stand-off 65V. Protecting the power switch are current and thermal limiting circuits, and an undervoltage lockout circuit. This IC contains an adjustable frequency oscillator that can be programmed up to 200 kHz. The oscillator can also be synchronized with other devices, so that multiple devices can operate at the same switching frequency.

Other features include soft start mode to reduce in-rush current during start up, and current mode control for improved rejection of input voltage and output load transients and cycle-by-cycle current limiting. The device also has a shutdown pin, so that it can be turned off externally. An output voltage tolerance of ±4%, within specified input voltages and output load conditions, is guaranteed for the power supply system.

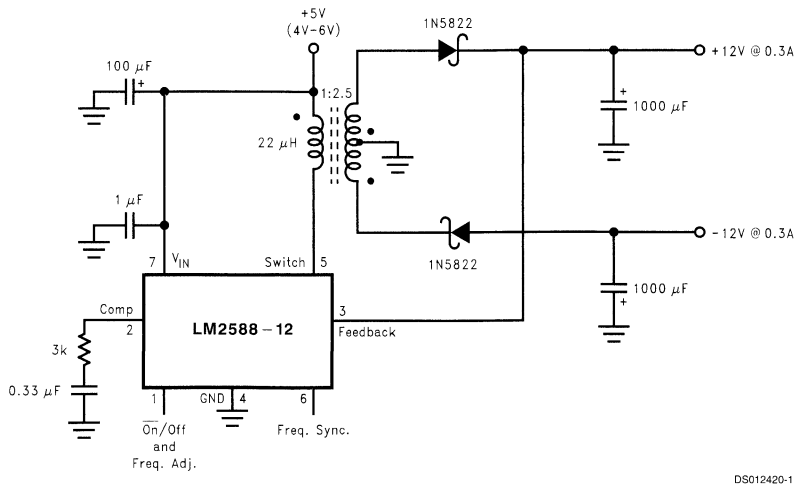
Features

- Requires few external components
- Family of standard inductors and transformers
- NPN output switches 5.0A, can stand off 65V
- Wide input voltage range: 4V to 40V
- Adjustable switching frequency: 100 kHz to 200 kHz
- External shutdown capability
- Draws less than 60 µA when shut down
- Frequency synchronization
- Current-mode operation for improved transient response, line regulation, and current limit
- Internal soft-start function reduces in-rush current during start-up
- Output transistor protected by current limit, under voltage lockout, and thermal shutdown
- System output voltage tolerance of ±4% max over line and load conditions

Typical Applications

- Flyback regulator
- Forward converter
- Multiple-output regulator
- Simple boost regulator

Flyback Regulator



Ordering Information

Package Type	NSC Package Drawing	Order Number
7-Lead TO-220 Bent, Staggered Leads	TA07B	LM2588T-3.3, LM2588T-5.0, LM2588T-12, LM2588T-ADJ
7-Lead TO-263	TS7B	LM2588S-3.3, LM2588S-5.0, LM2588S-12, LM2588S-ADJ
7-Lead TO-263 Tape and Reel	TS7B	LM2588SX-3.3, LM2588SX-5.0, LM2588SX-12, LM2588SX-ADJ

National Semiconductor

LM2590HV
SIMPLE SWITCHER®Power Converter 150 kHz 1A Step-Down Voltage Regulator, with Features

General Description

The LM2590HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, and an adjustable output version.

This series of switching regulators is similar to the LM2591HV with additional supervisory and performance features.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications, fixed-frequency oscillator, Shutdown/Soft-start, output error flag and flag delay.

The LM2590HV operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 7-lead TO-220 package with several different lead bend options, and a 7-lead TO-263 Surface mount package.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 90 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

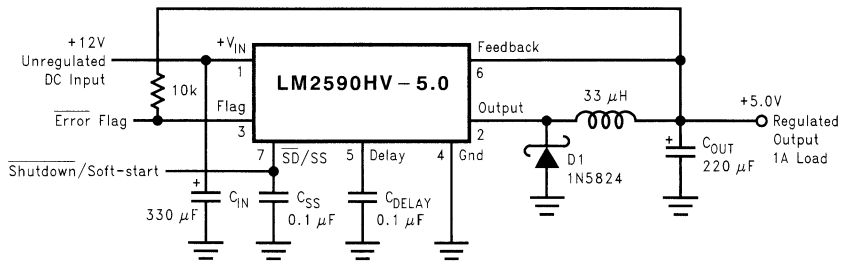
- 3.3V, 5V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 57V ±4% max over line and load conditions
- Guaranteed 1A output load current
- Available in 7-pin TO-220 and TO-263 (surface mount) Package
- Input voltage range up to 60V
- 150 kHz fixed frequency internal oscillator
- Shutdown/Soft-start
- Out of regulation error flag
- Error flag delay
- Low power standby mode, I_Q typically 90 µA
- High Efficiency
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Note: † Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



National Semiconductor

LM2591HV
SIMPLE SWITCHER®Power Converter 150 kHz 1A Step-Down Voltage Regulator

General Description

The LM2591HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, and an adjustable output version.

This series of switching regulators is similar to the LM2590HV, but without some of the supervisory and performance features of the latter.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications and a fixed-frequency oscillator.

The LM2591HV operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 5-lead TO-220 package with several different lead bend options, and a 5-lead TO-263 Surface mount package.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 90 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

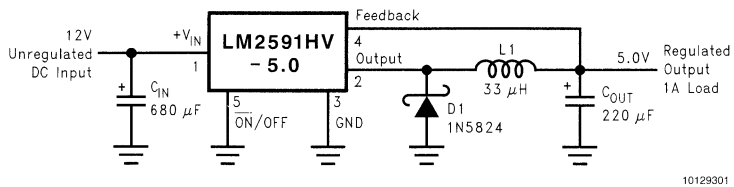
- 3.3V, 5V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 57V ±4% max over line and load conditions
- Guaranteed 1A output load current
- Available in 5-pin TO-220 and TO-263 (surface mount) Package
- Input voltage range up to 60V
- 150 kHz fixed frequency internal oscillator
- On/Off control
- Low power standby mode, I_Q typically 90 µA
- High Efficiency
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Note: † Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



10129301

National Semiconductor

LM2592HV
SIMPLE SWITCHER®Power Converter 150 kHz 2A Step-Down Voltage Regulator

General Description

The LM2592HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 2A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, and an adjustable output version.

This series of switching regulators is similar to the LM2593HV, but without some of the supervisory and performance features of the latter.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications and a fixed-frequency oscillator.

The LM2592HV operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 5-lead TO-220 package with several different lead bend options, and a 5-lead TO-263 Surface mount package.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 90 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

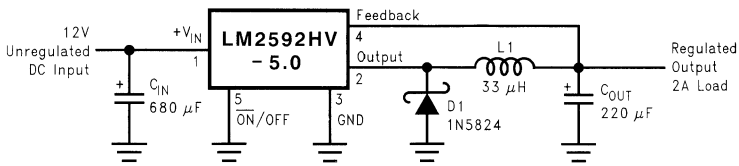
- 3.3V, 5V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 57V ±4% max over line and load conditions
- Guaranteed 2A output load current
- Available in 5-pin TO-220 and TO-263 (surface mount) Package
- Input voltage range up to 60V
- 150 kHz fixed frequency internal oscillator
- On/Off control
- Low power standby mode, I_Q typically 90 µA
- High Efficiency
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Note: † Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



10129401

National Semiconductor

LM2593HV
SIMPLE SWITCHER®Power Converter 150 kHz 2A Step-Down Voltage Regulator, with Features

General Description

The LM2593HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 2A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, and an adjustable output version.

This series of switching regulators is similar to the LM2592HV with additional supervisory and performance features.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications, fixed-frequency oscillator, Shutdown/Soft-start, output error flag and flag delay.

The LM2593HV operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 7-lead TO-220 package with several different lead bend options, and a 7-lead TO-263 Surface mount package.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 90 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

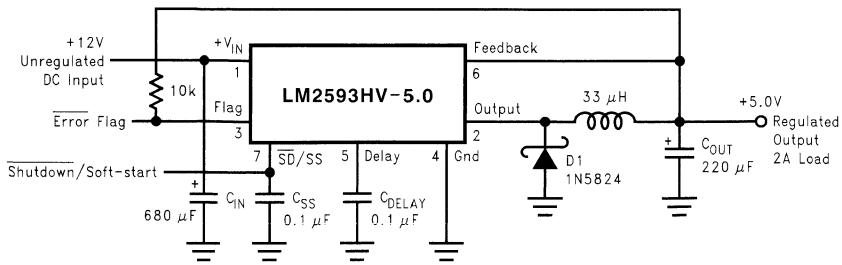
- 3.3V, 5V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 57V ±4% max over line and load conditions
- Guaranteed 2A output load current
- Available in 7-pin TO-220 and TO-263 (surface mount) Package
- Input voltage range up to 60V
- 150 kHz fixed frequency internal oscillator
- Shutdown/Soft-start
- Out of regulation error flag
- Error flag delay
- Low power standby mode, I_Q typically 90 µA
- High Efficiency
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Note: † Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



National Semiconductor

LM2594/LM2594HV
SIMPLE SWITCHER® Power Converter 150 kHz 0.5A Step-Down Voltage Regulator

General Description

The LM2594/LM2594HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version, and are packaged in a 8-lead DIP and a 8-lead surface mount package.

Requiring a minimum number of external components, these regulators are simple to use and feature internal frequency compensation†, a fixed-frequency oscillator, and improved line and load regulation specifications.

The LM2594/LM2594HV series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its high efficiency, the copper traces on the printed circuit board are normally the only heat sinking needed.

A standard series of inductors (both through hole and surface mount types) are available from several different manufacturers optimized for use with the LM2594/LM2594HV series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 85 µA standby current. Self protection features include a two stage frequency reducing current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

The LM2594HV is for applications requiring an input voltage up to 60V.

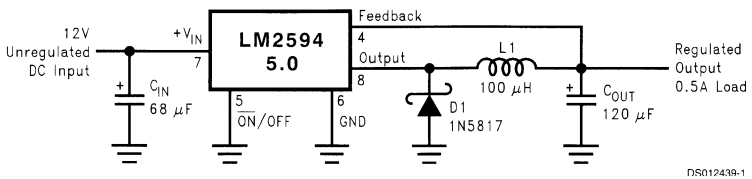
Features

- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V (57V for the HV version)±4% max over line and load conditions
- Available in 8-pin surface mount and DIP-8 package
- Guaranteed 0.5A output current
- Input voltage range up to 60V
- Requires only 4 external components
- 150 kHz fixed frequency internal oscillator
- TTL Shutdown capability
- Low power standby mode, I_Q typically 85 µA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

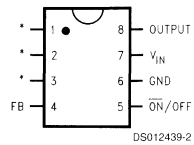
- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative convertor

Typical Application (Fixed Output Voltage Versions)



Connection Diagrams and Order Information

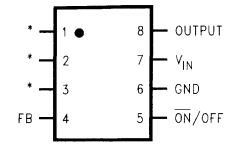
8-Lead DIP (N)



DS012439-2

Top View
Order Number
LM2594N-3.3, LM2594N-5.0,
LM2594N-12 or LM2594N-ADJ
LM2594HVN-3.3, LM2594HVN-5.0,
LM2594HVN-12 or LM2594HVN-ADJ
See NS Package Number N08E

8-Lead Surface Mount (M)



DS012439-3

Top View
Order Number LM2594M-3.3,
LM2594M-5.0, LM2594M-12 or
LM2594M-ADJ
LM2594HVM-3.3, LM2594HVM-5.0,
LM2594HVM-12 or LM2594HVM-ADJ
See NS Package Number M08A

*No internal connection, but should be soldered to pc board for best heat transfer.

‡Patent Number 5,382,918.

National Semiconductor

LM2595
SIMPLE SWITCHER® Power Converter 150 kHz 1A Step-Down Voltage Regulator

General Description

The LM2595 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, and a fixed-frequency oscillator.

The LM2595 series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 5-lead TO-220 package with several different lead bend options, and a 5-lead TO-263 surface mount package. Typically, for output voltages less than 12V, and ambient temperatures less than 50°C, no heat sink is required.

A standard series of inductors are available from several different manufacturers optimized for use with the LM2595 series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under specified input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 85 µA stand-by current. Self protection features include a two stage frequency reducing current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

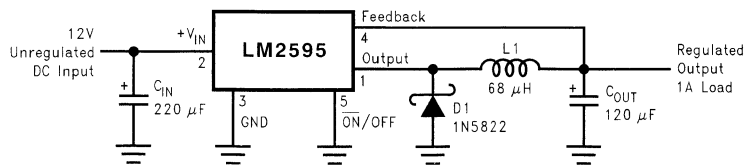
- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V ±4% max over line and load conditions
- Available in TO-220 and TO-263 (surface mount) packages
- Guaranteed 1A output load current
- Input voltage range up to 40V
- Requires only 4 external components
- Excellent line and load regulation specifications
- 150 kHz fixed frequency internal oscillator
- TTL shutdown capability
- Low power standby mode, I_Q typically 85 µA
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to negative converter

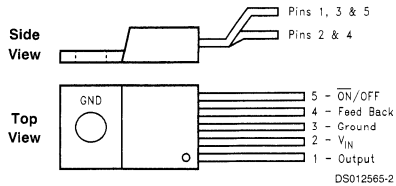
Note: † Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



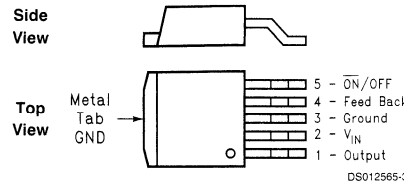
Connection Diagrams and Ordering Information

Bent and Staggered Leads, Through Hole Package
5–Lead TO-220 (T)



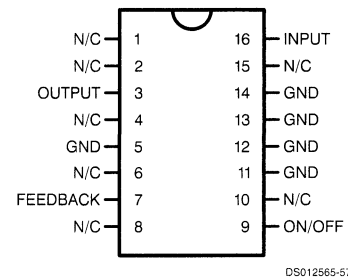
Order Number LM2595T-3.3, LM2595T-5.0, LM2595T-12 or LM2595T-ADJ
See NS Package Number T05D

Surface Mount Package
5-Lead TO-263 (S)



Order Number LM2595S-3.3, LM2595S-5.0, LM2595S-12 or LM2595S-ADJ
See NS Package Number TS5B

16-Lead Ceramic Dual-in-Line Package (J)



Order Number LM2595J-3.3-QML (5962-9687901QEA),
LM2595J-5.0-QML (5962-9650301QEA),
LM2595J-12-QML (5962-9650201QEA),
or LM2595J-ADJ-QML (5962-9650401QEA)
See NS Package Number J16A

For specifications and information about Military-Aerospace products, please see the Mil-Aero web page at http://www.national.com/appinfo/milaero/index.html.

National Semiconductor

LM2596
SIMPLE SWITCHER® Power Converter 150 kHz 3A Step-Down Voltage Regulator

General Description

The LM2596 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 3A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, and a fixed-frequency oscillator.

The LM2596 series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 5-lead TO-220 package with several different lead bend options, and a 5-lead TO-263 surface mount package.

A standard series of inductors are available from several different manufacturers optimized for use with the LM2596 series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under specified input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 80 µA standby current. Self protection features include a two stage frequency reducing current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

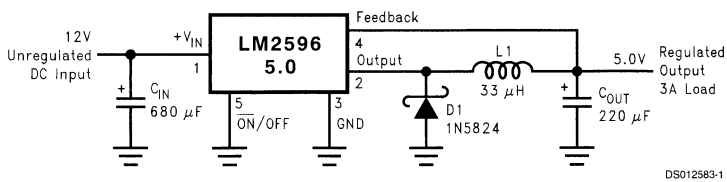
- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V ±4% max over line and load conditions
- Available in TO-220 and TO-263 packages
- Guaranteed 3A output load current
- Input voltage range up to 40V
- Requires only 4 external components
- Excellent line and load regulation specifications
- 150 kHz fixed frequency internal oscillator
- TTL shutdown capability
- Low power standby mode, I_Q typically 80 µA
- High efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- On-card switching regulators
- Positive to negative converter

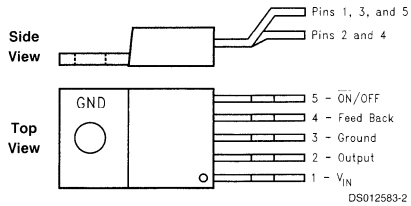
Note: †Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



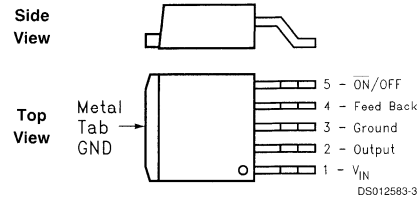
Connection Diagrams and Ordering Information

Bent and Staggered Leads, Through Hole Package
5-Lead TO-220 (T)



Order Number LM2596T-3.3, LM2596T-5.0, LM2596T-12 or LM2596T-ADJ
See NS Package Number T05D

Surface Mount Package
5-Lead TO-263 (S)



Order Number LM2596S-3.3, LM2596S-5.0, LM2596S-12 or LM2596S-ADJ
See NS Package Number TS5B

National Semiconductor

LM2597/LM2597HV
SIMPLE SWITCHER® Power Converter 150 kHz 0.5A Step-Down Voltage Regulator, with Features

General Description

The LM2597/LM2597HV series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 0.5A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version, and are packaged in an 8-lead DIP and an 8-lead surface mount package.

This series of switching regulators is similar to the LM2594 series, with additional supervisory and performance features added.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications, fixed-frequency oscillator, Shutdown /Soft-start, error flag delay and error flag output.

The LM2597/LM2597HV series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its high efficiency, the copper traces on the printed circuit board are normally the only heat sinking needed.

A standard series of inductors (both through hole and surface mount types) are available from several different manufacturers optimized for use with the LM2597/LM2597HV series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 85 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

The LM2597HV is for use in applications requiring and input voltage up to 60V.

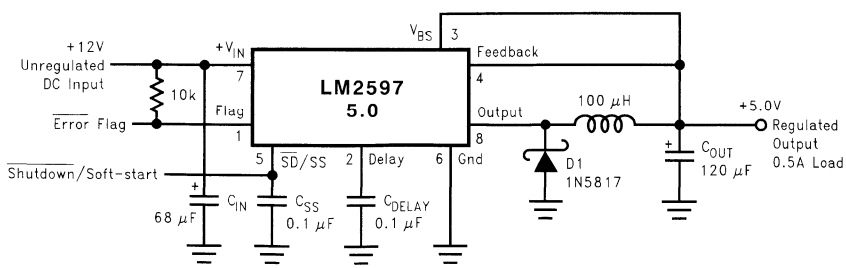
Features

- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V (57V for HV version)±4% max over line and load conditions
- Guaranteed 0.5A output current
- Available in 8-pin surface mount and DIP-8 package
- Input voltage range up to 60V
- 150 kHz fixed frequency internal oscillator
- Shutdown /Soft-start
- Out of regulation error flag
- Error output delay
- Bias Supply Pin (V_{BS}) for internal circuitry improves efficiency at high input voltages
- Low power standby mode, I_Q typically 85 µA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Typical Application (Fixed Output Voltage Versions)



†Patent Number 5,382,918.

National Semiconductor

LM2598
SIMPLE SWITCHER® Power Converter 150 kHz 1A Step-Down Voltage Regulator, with Features

General Description

The LM2598 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version.

This series of switching regulators is similar to the LM2595 series, with additional supervisory and performance features added.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications, fixed-frequency oscillator, $\overline{\text{Shutdown}}$ /Soft-start, error flag delay and error flag output.

The LM2598 series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 7-lead TO-220 package with several different lead bend options, and a 7-lead TO-263 surface mount package. Typically, for output voltages less than 12V, and ambient temperatures less than 50°C, no heat sink is required.

A standard series of inductors (both through hole and surface mount types) are available from several different manufacturers optimized for use with the LM2598 series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 85 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

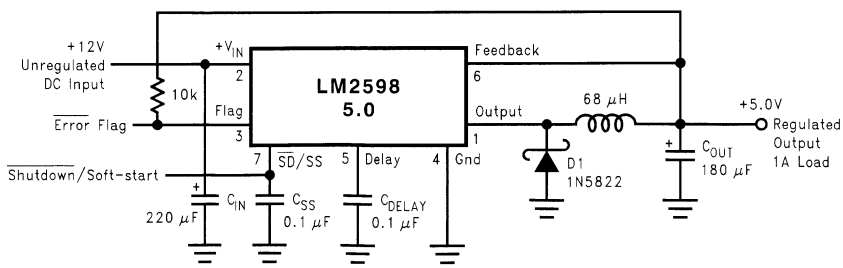
Features

- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V ±4% max over line and load conditions
- Guaranteed 1A output current
- Available in 7-pin TO-220 and TO-263 (surface mount) package
- Input voltage range up to 40V
- Excellent line and load regulation specifications
- 150 kHz fixed frequency internal oscillator
- $\overline{\text{Shutdown}}$ /Soft-start
- Out of regulation error flag
- Error output delay
- Low power standby mode, I_Q typically 85 µA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

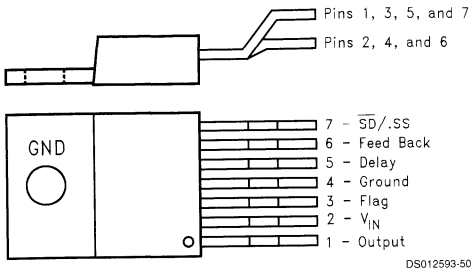
- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Typical Application (Fixed Output Voltage Versions)



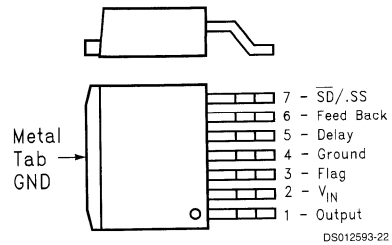
Connection Diagrams and Order Information

Bent and Staggered Leads, Through Hole Package
7-Lead TO-220 (T)



Order Number LM2598T-3.3, LM2598T-5.0, LM2598T-12 or LM2598T-ADJ
See NS Package Number TA07B

Surface Mount Package
7-Lead TO-263 (S)



Order Number LM2598S-3.3, LM2598S-5.0, LM2598S-12 or LM2598S-ADJ
See NS Package Number TS7B

National Semiconductor

LM2599
SIMPLE SWITCHER® Power Converter 150 kHz 3A Step-Down Voltage Regulator, with Features

General Description

The LM2599 series of regulators are monolithic integrated circuits that provide all the active functions for a step-down (buck) switching regulator, capable of driving a 3A load with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5V, 12V, and an adjustable output version.

This series of switching regulators is similar to the LM2596 series, with additional supervisory and performance features added.

Requiring a minimum number of external components, these regulators are simple to use and include internal frequency compensation†, improved line and load specifications, fixed-frequency oscillator, $\overline{\text{Shutdown}}$/Soft-start, error flag delay and error flag output.

The LM2599 series operates at a switching frequency of 150 kHz thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Available in a standard 7-lead TO-220 package with several different lead bend options, and a 7-lead TO-263 Surface mount package.

A standard series of inductors (both through hole and surface mount types) are available from several different manufacturers optimized for use with the LM2599 series. This feature greatly simplifies the design of switch-mode power supplies.

Other features include a guaranteed ±4% tolerance on output voltage under all conditions of input voltage and output load conditions, and ±15% on the oscillator frequency. External shutdown is included, featuring typically 80 µA standby current. Self protection features include a two stage current limit for the output switch and an over temperature shutdown for complete protection under fault conditions.

Features

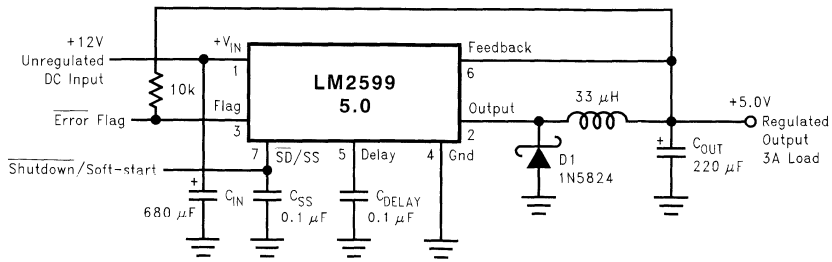
- 3.3V, 5V, 12V, and adjustable output versions
- Adjustable version output voltage range, 1.2V to 37V ±4% max over line and load conditions
- Guaranteed 3A output current
- Available in 7-pin TO-220 and TO-263 (surface mount) Package
- Input voltage range up to 40V
- 150 kHz fixed frequency internal oscillator
- $\overline{\text{Shutdown}}$/Soft-start
- Out of regulation error flag
- Error output delay
- Low power standby mode, I_Q typically 80 µA
- High Efficiency
- Uses readily available standard inductors
- Thermal shutdown and current limit protection

Applications

- Simple high-efficiency step-down (buck) regulator
- Efficient pre-regulator for linear regulators
- On-card switching regulators
- Positive to Negative converter

Note: † Patent Number 5,382,918.

Typical Application (Fixed Output Voltage Versions)



National Semiconductor

LM2611
1.4MHz Cuk Converter

General Description

The LM2611 is a current mode, PWM inverting switching regulator. Operating from a 2.7 - 14V supply, it is capable of producing a regulated negative output voltage of up to $-(36\text{-}V_{IN(MAX)})$. The LM2611 utilizes an input and output inductor, which enables low voltage ripple and RMS current on both the input and the output. With a switching frequency of 1.4MHz, the inductors and output capacitor can be physically small and low cost. High efficiency is achieved through the use of a low $R_{DS(ON)}$ FET.

The LM2611 features a shutdown pin, which can be activated when the part is not needed to lower the Iq and save battery life. A negative feedback (NFB) pin provides a simple method of setting the output voltage, using just two resistors. Cycle-by-cycle current limiting and internal compensation further simplify the use of the LM2611.

The LM2611 is available is a small SOT23-5 package. It comes in two grades:

	Grade A	Grade B
Current Limit	1.2A	0.9A
$R_{DS(ON)}$	0.5Ω	0.7Ω

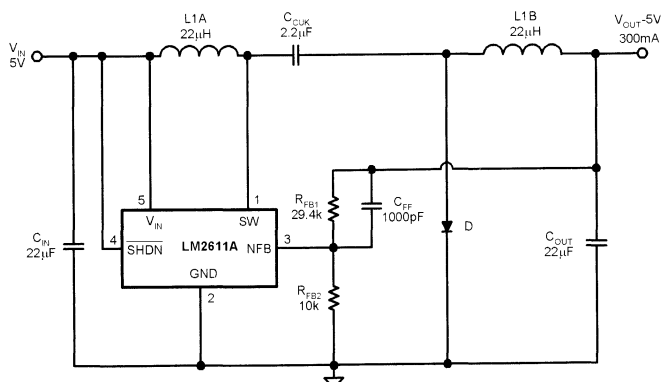
Features

- 1.4MHz switching frequency
- Low $R_{DS(ON)}$ DMOS FET
- 1mVp-p output ripple
- −5V at 300mA from 5V input
- Better regulation than a charge pump
- Uses tiny capacitors and inductors
- Wide input range: 2.7V to 14V
- Low shutdown current: <1uA
- 5-lead SOT-23 package

Applications

- MR Head Bias
- Digital camera CCD bias
- LCD bias
- GaAs FET bias
- Positive to negative conversion

Typical Application Circuit



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
C_{CUK}: TAIYO YUDEN X5R EMK316BJ225ML
C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CLS62-220 or CR32-220 (UNCOUPLED)

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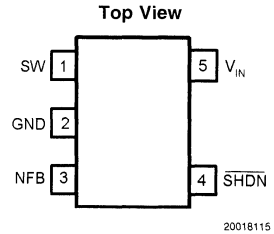
Connection Diagram



5-lead SOT-23 Package
NS Package Number MF05A

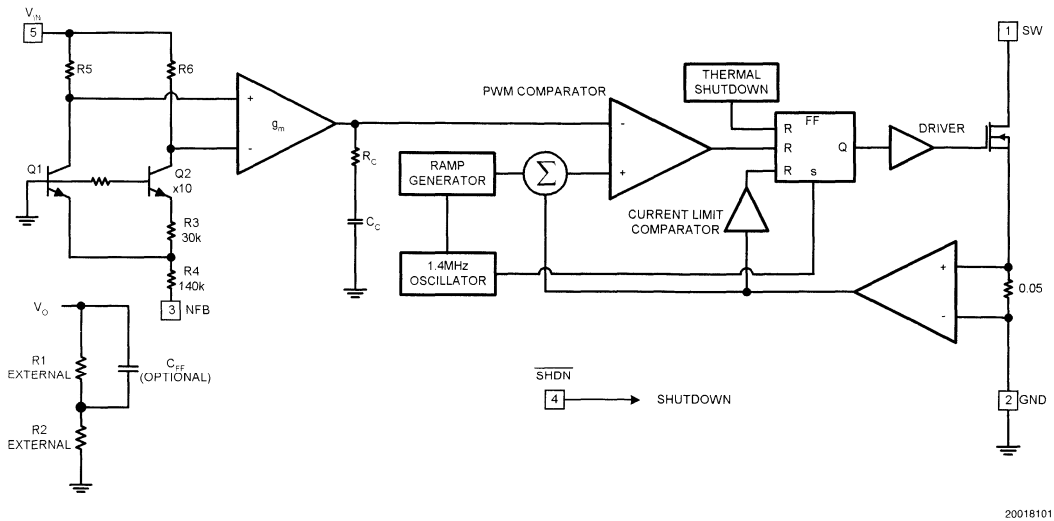
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As	Package ID
LM2611AMF	SOT23-5	MF05A	1K Tape and Reel	S40A
LM2611AMFX			3K Tape and Reel	S40A
LM2611BMF			1K Tape and Reel	S40B
LM2611BMFX			3K Tape and Reel	S40B

Pin Description

Pin	Name	Function
1	SW	Drain of internal switch. Connect at the node of the input inductor and Cuk capacitor.
2	GND	Analog and power ground.
3	NFB	Negative feedback. Connect to output via external resistor divider to set output voltage.
4	$\overline{SHDN}$	Shutdown control input. V_{IN} = Device on. Ground = Device in shutdown.
5	V_{IN}	Analog and power input. Filter out high frequency noise with a 0.1 µF ceramic capacitor placed close to the pin.

Block Diagram



National Semiconductor

LM2612
400mA Sub-miniature, Programmable, Step-Down DC-DC Converter for Ultra Low-Voltage Circuits

General Description

The LM2612 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Lithium-Ion cell. It provides up to 400mA (300mA for B grade), over an input voltage range of 2.8V to 5.5V. Pin programmable output voltages of 1.05V, 1.3V, 1.5V or 1.8V allow adjustment for MPU voltage options without board redesign or external feedback resistors.

The device has three pin-selectable modes for maximizing battery life in mobile phones and similar portable applications. Low-noise PWM mode offers 600kHz fixed-frequency operation to reduce interference in RF and data acquisition applications during full-power operation. In PWM mode, internal synchronous rectification provides high efficiency (91% typ. at $1.8V_{OUT}$). A SYNC input allows synchronizing the switching frequency in a range of 500kHz to 1MHz to avoid noise from intermodulation with system frequencies. Low-current hysteretic PFM mode reduces quiescent current to 150 µA (typ.) during system standby. Shutdown mode turns the device off and reduces battery consumption to 0.1µA (typ.). Additional features include soft start and current overload protection.

The LM2612 is available in a 10 pin micro SMD packge. This package uses National's wafer level chip-scale micro SMD technology and offers the smallest possible size. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

Key Specifications

- Operates from a single LiION cell (2.8V to 5.5V)
- Pin programmable output voltage (1.05V, 1.3V, 1.5V and 1.8V)
- 400mA maximum load capability (300mA for B grade)
- ±2% PWM mode DC output voltage precision
- 2mV typ PWM mode output voltage ripple
- 150 µA typ PFM mode quiescent current
- 0.1µA typ shutdown mode current
- Internal synchronous rectification for high PWM mode efficiency (91% at $2.8V_{IN}$, $1.8V_{OUT}$)
- 600kHz PWM mode switching frequency
- SYNC input for PWM mode frequency synchronization from 500kHz to 1MHz

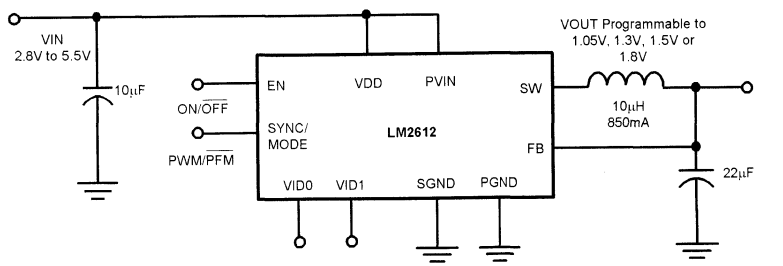
Features

- Sub-miniature 10-pin micro SMD package
- Only three tiny surface-mount external components required
- Uses small ceramic capacitors.
- Internal soft start
- Current overload protection
- No external compensation required

Applications

- Mobile Phones
- Hand-Held Radios
- Battery Powered Devices

Typical Application Circuit



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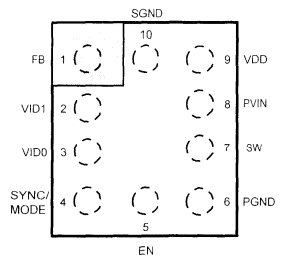
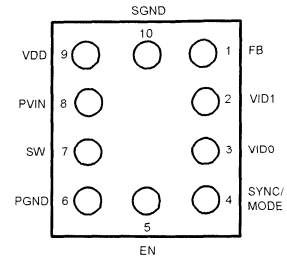
Connection Diagrams
micro SMD package



TOP VIEW



BOTTOM VIEW

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
10-Pin micro SMD			
LM2612ABP	10-bump Wafer Level Chip Scale (micro SMD)	BPA10VWB	250 Units, Tape and Reel
LM2612BBP			250 Units, Tape and Reel
LM2612ABPX			3000 Units, Tape and Reel
LM2612BBPX			3000 Units, Tape and Reel

Pin Description

Pin Number	Pin Name	Function
1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor (Figure 1)
2	VID1	Output Voltage Control Inputs. Set the output voltage using these digital inputs (see Table 1). The output defaults to 1.5V if these pins are unconnected.
3	VID0	
4	SYNC/MODE	Synchronization Input. Use this digital input for frequency selection or modulation control. Set: SYNC/MODE = high for low-noise 600kHz PWM mode SYNC/MODE = low for low-current PFM mode SYNC/MODE = a 500kHz - 1MHz external clock for synchronization to an external clock in PWM mode. See *Synchronization and Operating Modes* in the *Device Information* section.
5	EN	Enable Input. Set this CMOS Schmitt trigger digital input high to VDD for normal operation. For shutdown, set low to SGND. Set EN low during power-up and other low supply voltage conditions. (See *Shutdown Mode* in the *Device Information* section.)
6	PGND	Power Ground
7	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the 850mA max Switch Peak Current Limit specification of the LM2612 (*Figure 1*)
8	PVIN	Power Supply Input to the internal PFET switch. Connect to the input filter capacitor (*Figure 1*).
9	VDD	Analog Supply Input. If board layout is not optimum, an optional 0.1µF ceramic capacitor is suggested (*Figure 1*)
10	SGND	Analog and Control Ground

National Semiconductor

LM2621
Low Input Voltage, Step-Up DC-DC Converter

General Description

The LM2621 is a high efficiency, step-up DC-DC switching regulator for battery-powered and low input voltage systems. It accepts an input voltage between 1.2V and 14V and converts it into a regulated output voltage. The output voltage can be adjusted between 1.24V and 14V. It has an internal 0.17Ω N-Channel MOSFET power switch. Efficiencies up to 90% are achievable using the LM2621.

The high switching frequency (adjustable up to 2MHz) of the LM2621 allows for tiny surface mount inductors and capacitors. Because of the unique constant-duty-cycle gated oscillator topology very high efficiencies are realized over a wide load range. The supply current is reduced to 80µA because of the BiCMOS process technology. In the shutdown mode, the supply current is less than 2.5µA.

The LM2621 is available in a Mini-SO-8 package. This package uses half the board area of a standard 8-pin SO and has a height of just 1.09 mm.

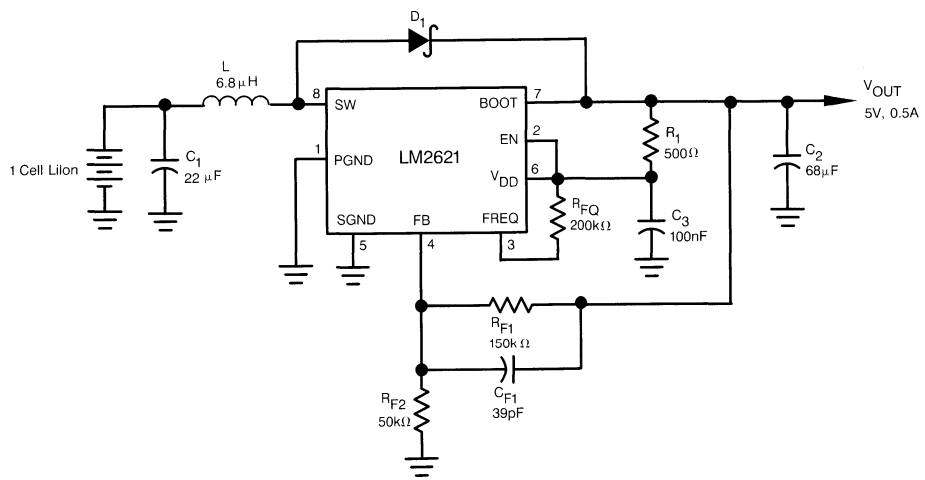
Features

- Small Mini-SO8 Package (Half the Footprint of Standard 8-Pin SO Package)
- 1.09 mm Package Height
- Up to 2 MHz Switching Frequency
- 1.2V to 14V Input Voltage
- 1.24V - 14V Adjustable Output Voltage
- Up to 1A Load Current
- 0.17 Ω Internal MOSFET
- Up to 90% Regulator Efficiency
- 80 µA Typical Operating Current
- <2.5µA Guaranteed Supply Current In Shutdown

Applications

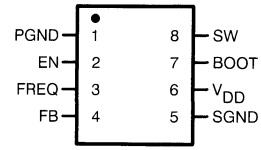
- PDAs, Cellular Phones
- 2-Cell and 3-Cell Battery-Operated Equipment
- PCMCIA Cards, Memory Cards
- Flash Memory Programming
- TFT/LCD Applications
- 3.3V to 5.0V Conversion
- GPS Devices
- Two-Way Pagers
- Palmtop Computers
- Hand-Held Instruments

Typical Application Circuit



Connection Diagram

Mini SO-8 (MM) Package



Top View

Ordering Information

Order Number	Package Type	NSC Package Drawing	Package Marking	Supplied As
LM2621MMX	Mini SO-8	MUA08A	S06A	3000 Units on Tape and Reel
LM2621MM	Mini SO-8	MUA08A	S06A	1000 Units on Tape and Reel

National Semiconductor

LM2622
600kHz/1.3MHz Step-up PWM DC/DC Converter

General Description

The LM2622 is a step-up DC/DC converter with a 1.6A, 0.2Ω internal switch and pin selectable operating frequency. With the ability to convert 3.3V to multiple outputs of 8V, -8V, and 23V, the LM2622 is an ideal part for biasing TFT displays. The LM2622 can be operated at switching frequencies of 600kHz and 1.3MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM2622 is available in a low profile 8-lead MSOP package.

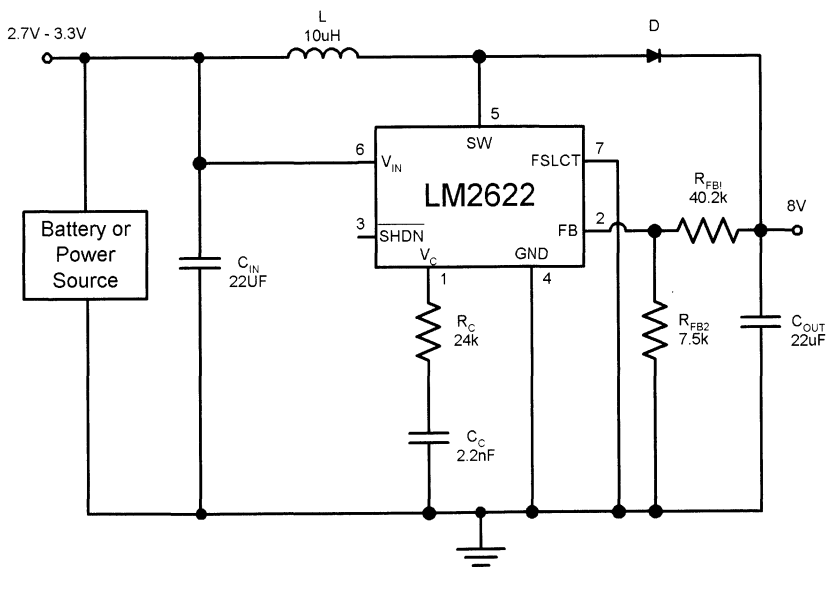
Features

- 1.6A, 0.2Ω, internal switch
- Operating voltage as low as 2.0V
- 600kHz/1.3MHz pin selectable frequency operation
- Over temperature protection
- 8-Lead MSOP package

Applications

- TFT Bias Supplies
- Handheld Devices
- Portable Applications
- GSM/CDMA Phones
- Digital Cameras

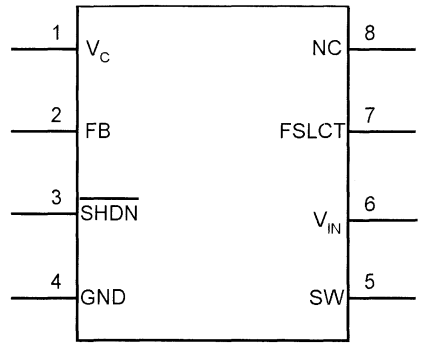
Typical Application Circuit



600 kHz Operation

Connection Diagram

Top View



10127304

8-Lead Plastic MSOP
NS Package Number MUA08A

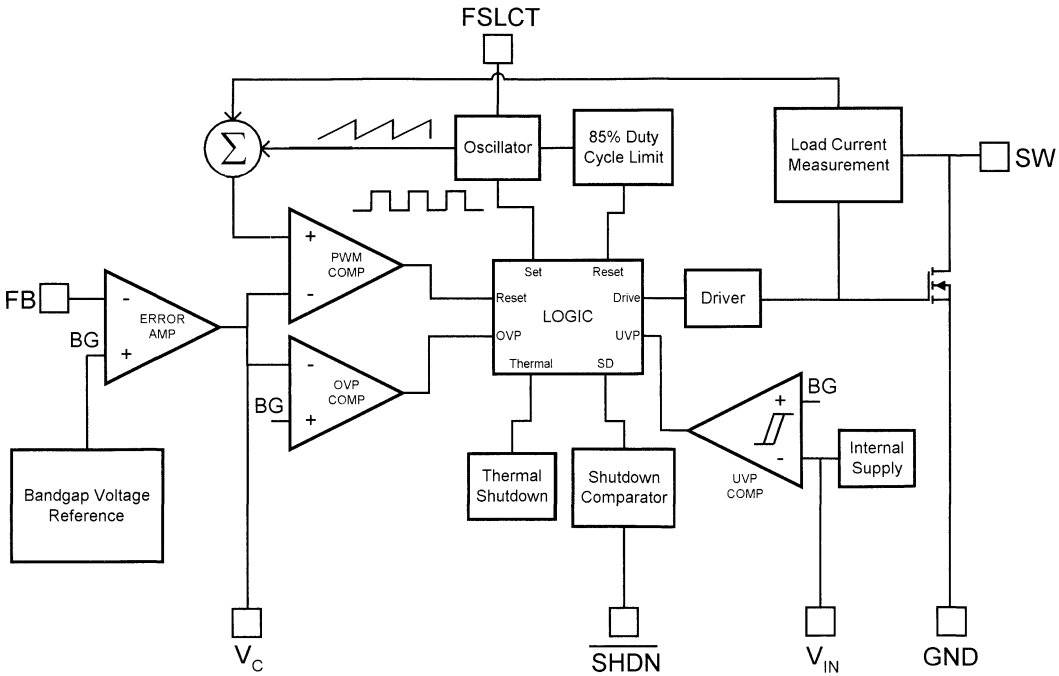
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As	Package ID
LM2622MM-ADJ	MSOP-8	MUA08A	1000 Units, Tape and Reel	S18B
LM2622MMX-ADJ	MSOP-8	MUA08A	3500 Units, Tape and Reel	S18B

Pin Description

Pin	Name	Function
1	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	Output voltage feedback input.
3	$\overline{SHDN}$	Shutdown control input, active low.
4	GND	Analog and power ground.
5	SW	Power switch input. Switch connected between SW pin and GND pin.
6	V_{IN}	Analog power input.
7	FSLCT	Switching frequency select input. V_{IN} = 1.3MHz. Ground = 600kHz.
8	NC	Connect to ground.

Block Diagram



10127303

National Semiconductor

LM2633
Advanced Two-Phase Synchronous Triple Regulator Controller for Notebook CPUs

General Description

The LM2633 is a feature-rich IC that combines three regulator controllers - two current mode synchronous buck regulator controllers and a linear regulator controller.

The two switching regulator controllers operate 180° out of phase. This feature reduces the input ripple RMS current, resulting in a smaller input filter.

The first switching controller (Channel 1) features an Intel mobile CPU compatible precision 5-bit digital-to-analog converter which programs the output voltage from 0.925V to 2.00V. It is also compatible with the dynamic VID requirements. The second switching controller (Channel 2) is adjustable between 1.25V to 6.0V.

Use of synchronous rectification and pulse-skip operation at light load achieves high efficiency over a wide load range. Fixed-frequency operation can be obtained by disabling the pulse-skip mode.

Current-mode feedback control assures excellent line and load regulation and a wide loop bandwidth for good response to fast load transient events. Current mode control is achieved through sensing the Vds of the top FET and thus an external sense resistor is not necessary.

A power good signal is available to indicate the general health of the output voltages.

A unique feature is the analog soft-start for the switching controllers is independent of the slew rate of the input voltage. This will make the soft start behavior more predictable and controllable. An internal 5V rail is available externally for boot-strap circuitry (only) when no 5V is available from other sources.

Current limit for either of the two switching channels is achieved through sensing the top FET V_{DS} and the value is adjustable. The two switching controllers have under-voltage and over-voltage latch protections, and the linear regulator has under-voltage latch protection. Under-voltage latch can be disabled or delayed by a programmable amount of time.

The input voltage for the switching channels ranges from 5V to 30V, which makes possible the choice of different battery chemistries and options.

Features

GENERAL

- Three regulated output voltages
- 4.5V to 30V input range
- Power good function
- Input under-voltage lockout
- Thermal shutdown
- Tiny TSSOP package

SWITCHING SECTION

- Two channels operating 180° out of phase
- Separate on/off control for each channel
- Current mode control without sense resistor
- Skip-mode operation available
- Adjustable cycle-by-cycle current limit
- Negative current limit
- Analog soft start independent of input voltage slew rate
- Power ground pins separate
- Output UVP and OVP
- Programmable output UVP delay
- 250kHz switching frequency (for Vin < 17V)
- Channel 1 output from 0.925V to 2.00V
- ±1.5% DAC accuracy from 0°C to 125°C
- ±1.7% initial tolerance for Channel 2
- Dynamic VID change ready
- Power good flags VID changes
- Channel 2 output from 1.3V to 6.0V

LINEAR SECTION

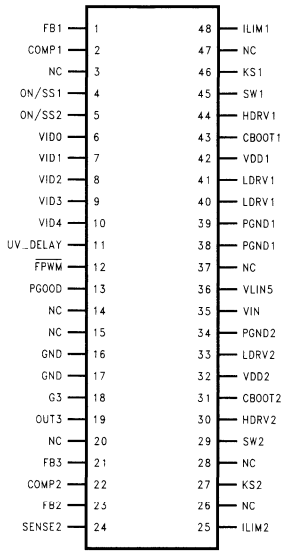
- Output voltage adjustable
- 50mA maximum driving current
- Output UVP
- ±2% initial tolerance

Applications

- Power supply for CPUs of notebook PCs that require the SpeedStep™ technique
- Power supply for information appliances
- General low voltage DC/DC buck regulators

Connection Diagram

TOP VIEW



20000801

48-Lead TSSOP (MTD)
Order Number LM2633MTD
See NS Package Number MTD48

Pin Descriptions

FB1 (Pin 1): The feedback input for Channel 1. Connect to the load directly.

COMP1 (Pin 2): Channel 1 compensation network connection (connected to the output of the voltage error amplifier).

NC (Pins 3, 14, 15, 20, 26, 28, 37 and 47): No internal connection.

ON/SS1 (Pin 4): Adding a capacitor to this pin provides a soft-start function which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 1; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole IC goes into *shut down mode*. The soft-start capacitor voltage will eventually be charged to V_{IN} or 6V, whichever is lower.

ON/SS2 (Pin 5): Adding a capacitor to this pin provides a soft-start function which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 2; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole IC goes into *shut down mode*. The soft-start capacitor voltage will eventually be charged to V_{IN} or 6V, whichever is lower.

VID4-0 (Pins 6-10): Voltage identification code. Each pin has an internal pull-up. They can accept open collector compatible 5-bit binary code from the CPU. The code table is shown in *Table 3*.

UV_ DELAY (Pin 11): A capacitor from this pin to ground adjusts the delay for the output under-voltage lockout.

$\overline{\text{FPWM}}$ (Pin 12): When $\overline{\text{FPWM}}$ is low, pulse-skip mode operation at light load is disabled. The regulator is forced to operate in constant frequency mode.

PGOOD (Pin 13): : A constant monitor on the output voltages. It indicates the general health of the regulators. For more information, *see Power Good Truth Table (Table 2)* and *Power Good Function* in *Operation Descriptions.*

GND (Pin 16-17): Low-noise analog ground.

G3 (Pin 18): Connect to the base or gate of the linear regulator pass transistor.

OUT3 (Pin 19): Connect to the output of the linear regulator.

FB3 (Pin 21): The feedback input for the linear regulator, connected to the center of the external resistor divider.

COMP2 (Pin 22): Channel 2 compensation network connection (it's the output of the voltage error amplifier).

FB2 (Pin 23): The feedback input for Channel 2. Connect to the center of the output resistor divider.

SENSE2 (Pin 24): Remote sense pin of Channel 2. This pin is used for skip-mode operation.

ILIM2 (Pin 25): Current limit threshold setting for Channel 2. It sinks at a constant 10 µA current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 2.

KS2 (Pin 27): The Kelvin sense for the drain of the top MOSFET of Channel 2.

SW2 (Pin 29): Switch-node connection for Channel 2, which is connected to the source of the top MOSFET.

HDRV2 (Pin 30): Top gate-drive output for Channel 2. HDRV2 is a floating drive output that rides on SW2 voltage.

CBOOT2 (Pin 31): Bootstrap capacitor connection for Channel 2 top gate drive. It is the positive supply rail for Channel 2 top gate drive.

VDD2 (Pin 32): The supply rail for Channel 2 bottom gate drive.

LDRV2 (Pin 33): Bottom gate-drive output for Channel 2.

PGND2 (Pin 34): Power ground for Channel 2.

VIN (Pin 35): The regulator input voltage supply.

VLIN5 (Pin 36): The output of the internal 5V linear regulator. Bypass to the ground with a 1UF ceramic capacitor. When regulator input voltage is 5V, this pin can be tied to VIN pin to improve light-load efficiency.

PGND1 (Pin 38-39): Power ground for Channel 1.

LDRV1 (Pin 40-41): Bottom gate-drive output for Channel 1.

VDD1 (Pin 42): The supply rail for the Channel 1 bottom gate drive.

CBOOT1 (Pin 43): Bootstrap capacitor connection for Channel 1 top gate drive. It is the positive supply rail for Channel 1 top gate drive.

HDRV1 (Pin 44): Top gate-drive output for Channel 1. HDRV1 is a floating drive output that rides on SW1 voltage.

SW1 (Pin 45): Switch-node connection for Channel 1, which is connected to the source of the top MOSFET.

KS1 (Pin 46): The Kelvin sense for the drain of the top MOSFET of Channel 1.

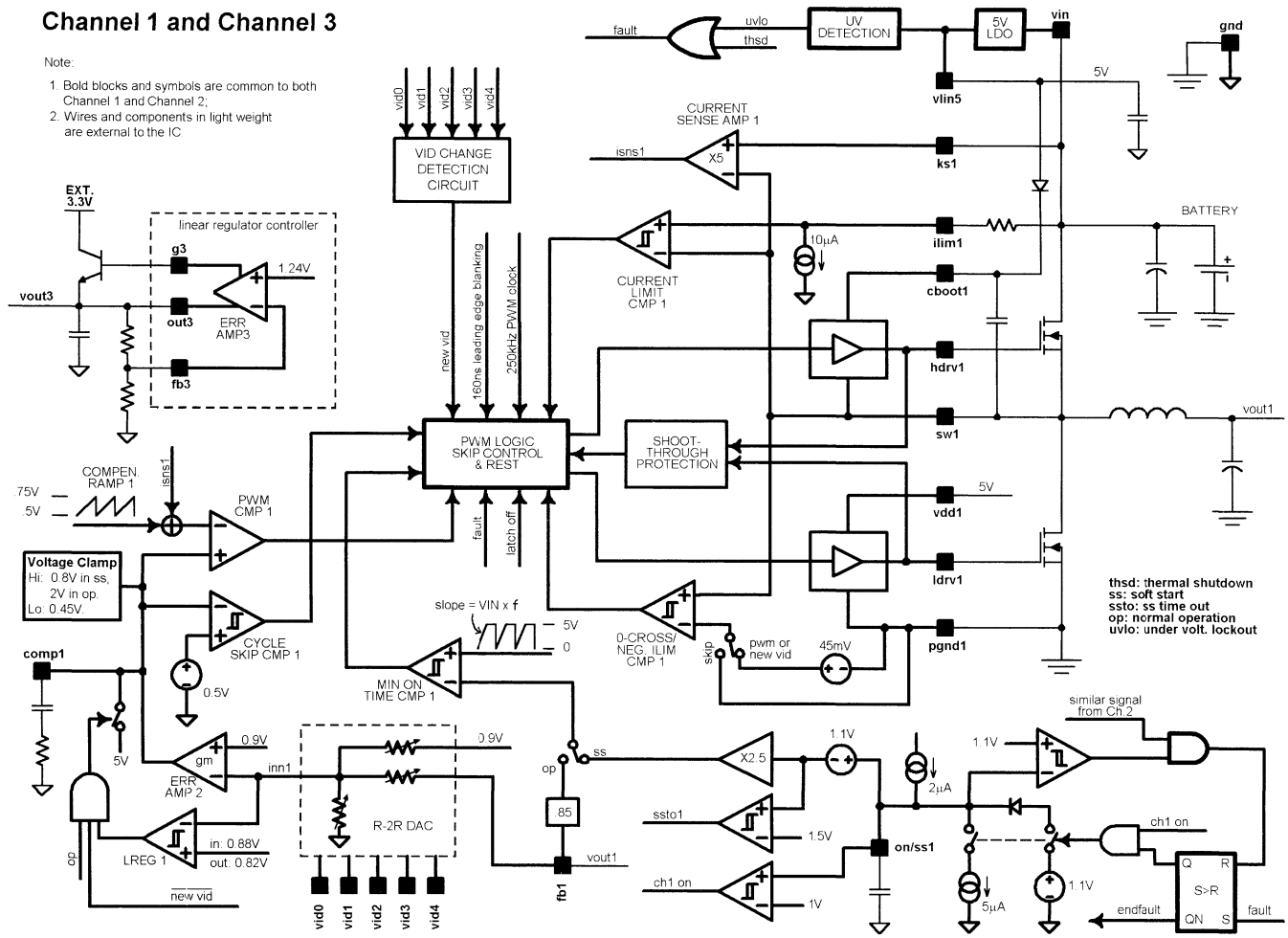
ILIM1 (Pin 48): Current limit threshold setting for Channel 1. It sinks at a constant 10 µA current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 1.

Block Diagrams

Channel 1 and Channel 3

Note:

1. Bold blocks and symbols are common to both Channel 1 and Channel 2;
2. Wires and components in light weight are external to the IC



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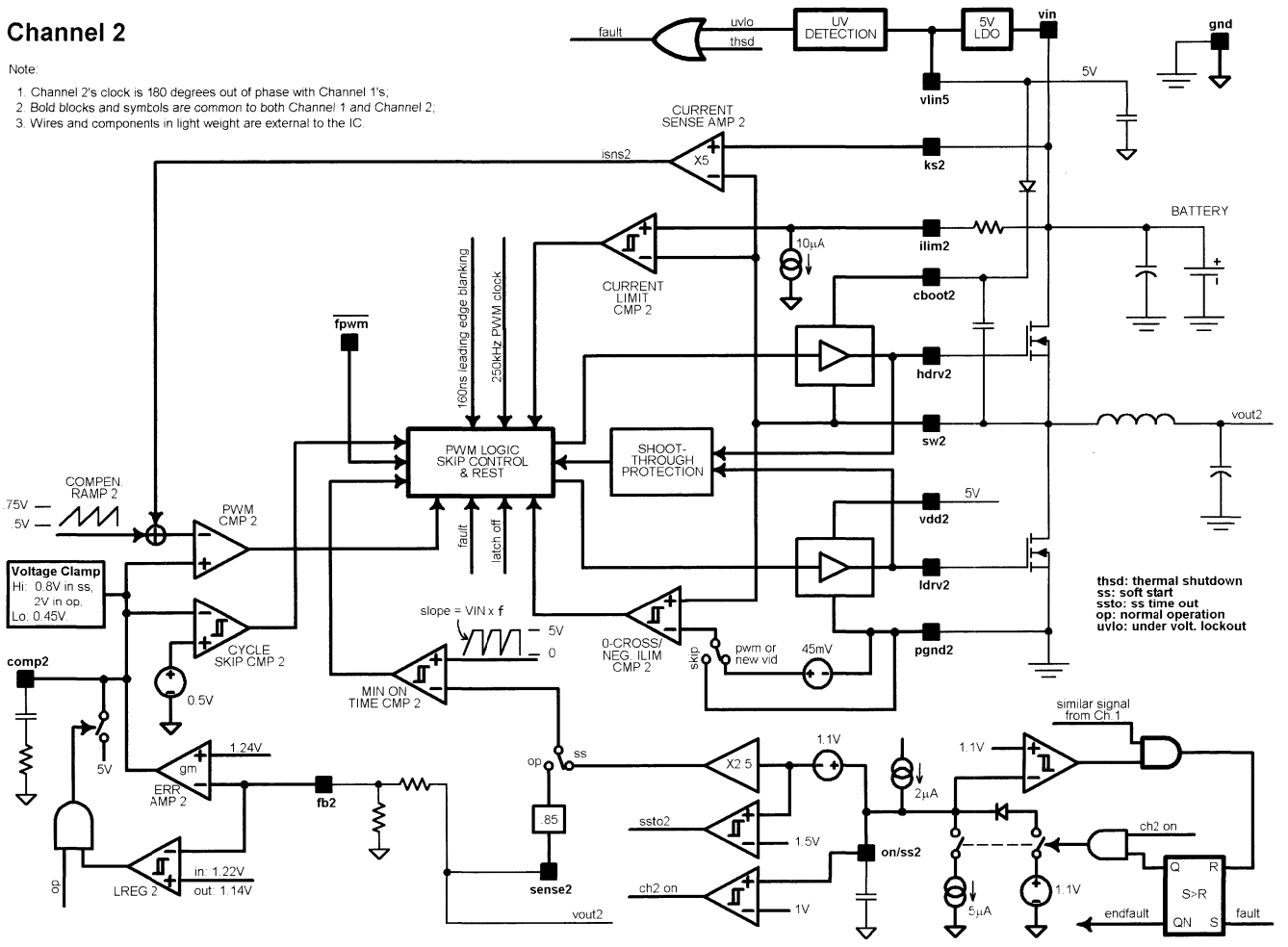
Block Diagrams (Continued)

Channel 2

Note:

1. Channel 2's clock is 180 degrees out of phase with Channel 1's;
2. Bold blocks and symbols are common to both Channel 1 and Channel 2;
3. Wires and components in light weight are external to the IC.



Block Diagrams (Continued)

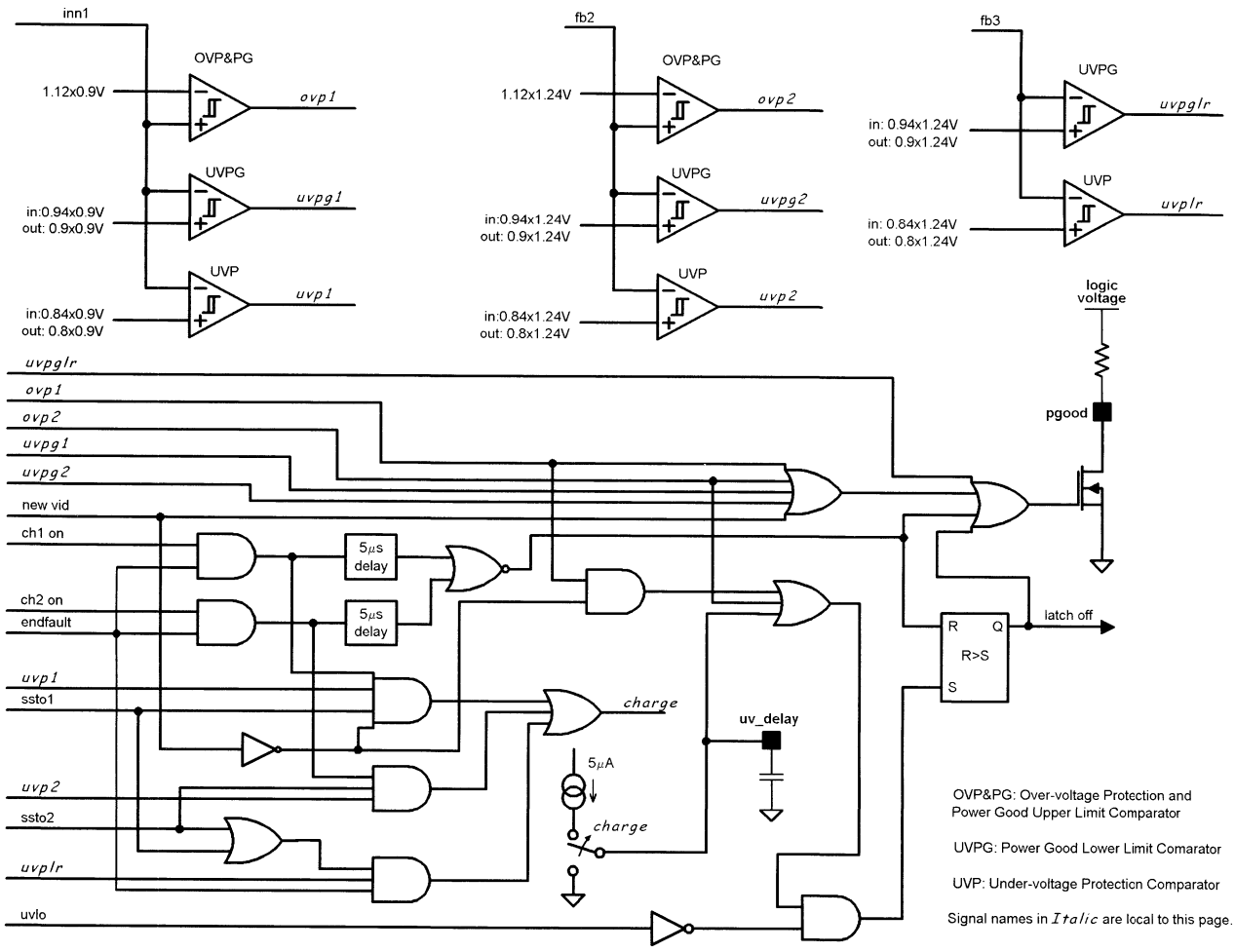


TABLE 1. Shut Down Latch Truth Table

Input												Output
ovp1	ovp2	uvp1	uvp2	uvplr	new vid	ch1 on	ch2 on	fault	ssto1	ssto2	uv_delay	latch off
1					0	Σ=1		0				1
	1					Σ=1		0				1
		1			0	1		0	1		cap	1
			1				1	0		1	cap	1
				1		Σ = 1		0	Σ = 1		cap	1
All other combinations												0

Note 1: 'Σ=1' means at least one variable is high.

Note 2: 'Fault' is the logic OR of UVLO and thermal shutdown.

Note 3: 'Cap' means the pin has a capacitor of appropriate value between it and ground.

Note 4: Positive logic is used.

Note 5: For meanings of the variables, refer to the block diagrams.

Note 6: A blank value means 'don't care'.

TABLE 2. Power Good Truth Table

Input										Output
ovp1	ovp2	uvpg1	uvpg2	uvpglr	new vid	ch1 on	ch2 on	fault	latch off	PGOOD
1										0
	1									0
		1								0
			1							0
				1						0
					1					0
						π = 0				0
								1		0
									1	0
All other combinations										1

Note 7: 'π = 0' means at least one variable is low.

Note 8: Positive logic is used.

Note 9: A blank value means 'don't care'.

Note 10: For meanings of the variables, refer to the block diagrams.

TABLE 3. VID Code and DAC Output

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
1	1	1	1	1	No CPU*
1	1	1	1	0	*0.925*
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	*1.100*
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	1	No CPU
0	1	1	1	0	*1.30*
0	1	1	0	1	*1.35*
0	1	1	0	0	*1.40*
0	1	0	1	1	1.45
0	1	0	1	0	*1.50*
0	1	0	0	1	*1.55*
0	1	0	0	0	*1.60*
0	0	1	1	1	1.65
0	0	1	1	0	1.70
0	0	1	0	1	1.75
0	0	1	0	0	1.80
0	0	0	1	1	1.85
0	0	0	1	0	1.90
0	0	0	0	1	1.95
0	0	0	0	0	*2.00*

*This code is set to 0.900V for convenience.

National Semiconductor

LM2636
5-Bit Programmable Synchronous Buck Regulator Controller

General Description

The LM2636 is a high speed controller designed specifically for use in synchronous DC/DC buck converters for advance d microprocessors. A 5-bit DAC accepts the VID code directly from the CPU and adjusts the output voltage from 1.3V to 3.5V. It provides the power good, over-voltage protection, and output enable features as required by Intel VRM specifications. Current limiting is achieved by monitoring the voltage drop across the r_{DS_ON} of the high side MOSFET, which eliminates an expensive current sense resistor.

The LM2636 employs a fixed-frequency voltage mode PWM architecture. To provide a faster response to a large and fast load transient, two ultra-fast comparators are built in to monitor the output voltage and override the primary control loop when necessary. The PWM frequency is adjustable from 50 kHz to 1 MHz through an external resistor. The wide range of PWM frequency gives the power supply designer the flexibility to make trade-offs between load transient response performance, MOSFET cost and the overall efficiency. The adaptive non-overlapping MOSFET gate drivers help avoid any potential shoot-through problem while maintaining high efficiency. BiCMOS gate drivers with rail-to-rail swing ensure that no spurious turn-on occur. When only 5V is available, a bootstrap structure can be employed to accommodate an NMOS high side switch. The precision reference trimmed to 2.5% over temperature is available externally for use by other regulators. Dynamic positioning of load voltage, which helps cut the number of output capacitors, can also be implemented easily.

Features

- 1.3V to 3.5V 5-bit programmable output voltage
- Synchronous rectification
- Power Good flag and output enable
- Over-voltage protection
- Initial Output Accuracy: 1.5% over temperature
- Current limit without external sense resistor
- Adaptive non-overlapping MOSFET gate drives
- Adjustable switching frequency: 50 kHz to 1 MHz
- Dynamic output voltage positioning
- 1.256V reference voltage available externally
- Plastic SO-20 package and TSSOP-20 package

Applications

- Motherboard power supply/VRM for Cyrix Gxm, Cyrix Gxi, Cyrix MII, Pentium™ II, Pentium Pro, 6x86 and K6 processors
- 5V to 1.3V–3.5V high current power supplies

Typical Application

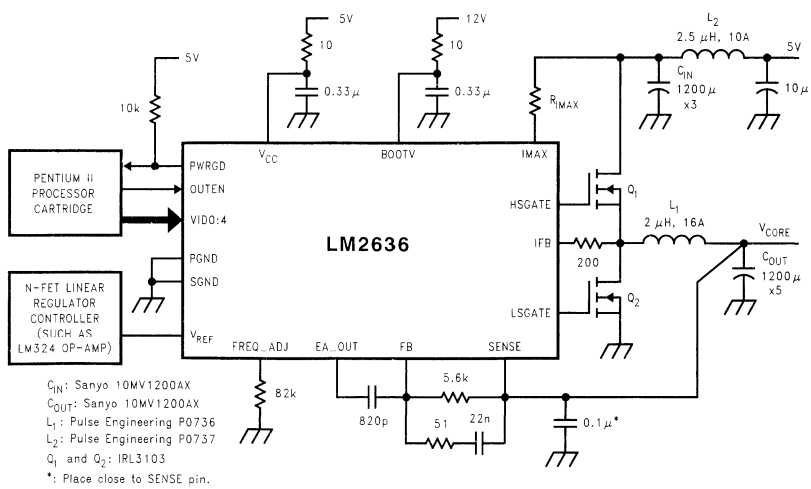
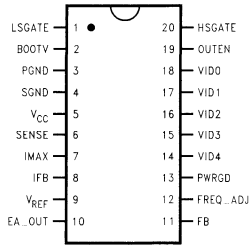


FIGURE 1. 5V to 1.3V–3.5V, 14A Power Supply

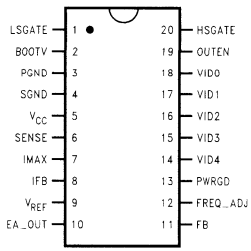
Connection Diagrams

TOP VIEW



Plastic SO-20
Order Number LM2636M
See NS Package Number M20B

TOP VIEW



Plastic TSSOP-20
Order Number LM2636MTC
See NS Package Number MTC20

Pin Descriptions

LSGATE (Pin 1): Gate drive for the low-side N-channel MOSFET. This signal is interlocked with HSGATE (Pin 20) to avoid a shoot-through problem.

BOOTV (Pin 2): Power supply for high-side N-channel MOSFET gate drive. The voltage should be at least one gate threshold above the converter input voltage to properly operate the high-side N-FET.

PGND (Pin 3): Ground for high current circuitry. It should be connected to system ground.

SGND (Pin 4): Ground for signal level circuitry. It should be connected to system ground.

V_{CC} (Pin 5): Power supply for the controller.

SENSE (Pin 6): Converter output voltage sensing. It provides input for power good, fast dual comparator control loop, and over-voltage protection circuitry. It is recommended that a 0.1 µF capacitor be connected between this pin and ground to avoid potential noise problems.

IMAX (Pin 7): Current limit threshold setting. It sinks a fixed 180 µA current. By connecting a resistor between the high side MOSFET drain and this pin, a fixed voltage drop can be built across the resistor. This voltage drop is compared with the V_{DS} of the high-side N-MOSFET to determine if an over-current condition has occurred.

IFB (Pin 8): High-side N-MOSFET source voltage sensing. This pin is one V_{DS} below drain voltage. When this voltage is lower than that of IMAX pin during the time the high-side FET is on, it means V_{DS} is higher than the preset voltage across the IMAX resistor, which can be interpreted as an over-current condition.

V_{REF} (Pin 9): Bandgap reference voltage. This voltage is mainly for use by other power supplies on the motherboard which need a reference.

EA_OUT (Pin 10): Output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to determine the duty cycle. This pin is necessary for compensating the primary control loop.

FB (Pin 11): Inverting input of the error amplifier. A pin necessary for compensating the control loop.

FREQ_ADJ (Pin 12): Switching frequency adjustment. Switching frequency can be adjusted by changing the grounding resistance on this pin.

PWRGD (Pin 13): Power Good. There are two windows around the DAC output voltage that are associated with PWRGD pin, the ±10% window and the ±8% window. If PWRGD is initially high (open drain state) and output voltage travels out of ±10% window, PWRGD goes to low (low impedance to ground). If PWRGD is initially low and output voltage travels into the ±8% window and has stayed within the window for at least 10 ms, PWRGD goes to high. A PWRGD high means the output voltage is at least within the ±10% window whereas a PWRGD low indicates the output voltage is definitely outside the ±8% window.

VID4:0 (Pins 14, 15, 16, 17, 18): Voltage Identification Code. The five pins accept an open-ground pattern 5-bit binary code from outside the chip (typically from the CPU) for generating the desired output voltage. Each VID pin is internally pulled up to V_{CC} via a 90 µA current source. *Table 1* shows the code table.

OUTEN (Pin 19): Output Enable. The output voltage is disabled when this pin is pulled low. It is internally pulled up to V_{CC} via a 90 µA current source.

HSGATE (Pin 20): Gate drive for the high-side N-channel MOSFET. This signal is interlocked with LSGATE (Pin 1) to avoid a shoot-through problem.

TABLE 1. VID Code and DAC Output

V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	Rated Output Voltage (V)
0	1	1	1	1	1.30
0	1	1	1	0	1.35
0	1	1	0	1	1.40
0	1	1	0	0	1.45
0	1	0	1	1	1.50
0	1	0	1	0	1.55
0	1	0	0	1	1.60
0	1	0	0	0	1.65
0	0	1	1	1	1.70
0	0	1	1	0	1.75
0	0	1	0	1	1.80
0	0	1	0	0	1.85
0	0	0	1	1	1.90
0	0	0	1	0	1.95
0	0	0	0	1	2.00

Pin Descriptions (Continued)

TABLE 1. VID Code and DAC Output (Continued)

V_{ID4}	V_{ID3}	V_{ID2}	V_{ID1}	V_{ID0}	Rated Output Voltage (V)
0	0	0	0	0	2.05
1	1	1	1	1	(shutdown)
1	1	1	1	0	2.1
1	1	1	0	1	2.2
1	1	1	0	0	2.3
1	1	0	1	1	2.4
1	1	0	1	0	2.5
1	1	0	0	1	2.6
1	1	0	0	0	2.7
1	0	1	1	1	2.8
1	0	1	1	0	2.9
1	0	1	0	1	3.0
1	0	1	0	0	3.1
1	0	0	1	1	3.2
1	0	0	1	0	3.3
1	0	0	0	1	3.4
1	0	0	0	0	3.5

National Semiconductor

LM2637
Motherboard Power Supply Solution with a 5-Bit Programmable Switching Controller and Two Linear Regulator Controllers

General Description

The LM2637 provides a comprehensive embedded power supply solution for motherboards hosting high performance MPUs such as M II™, Pentium™ II, K6-2 and other similar high performance MPUs. The LM2637 incorporates a 5-bit programmable, synchronous buck switching controller and two high-speed linear regulator controllers in a 24-pin SO package.

Switching Section — The switching regulator controller features a 5-bit programmable DAC, over-current and over-voltage protection, under-voltage latch-off, a power good signal, and output enable. The 5-bit DAC has a typical tolerance of 1%. There are two user-selectable over-current protection methods. One provides accurate over-current protection with the use of an external sense resistor. The other saves cost by taking advantage of the r_{DS_ON} of the high-side FET. The over voltage protection provides two levels of protection. The first level keeps the high-side FET off and the low-side FET on. The second provides a gate signal that can be used to fire an external SCR.

Linear Section — The two linear regulator controllers feature wide control bandwidth, N-FET and NPN transistor driving capability, and an adjustable output voltage. The wide control bandwidth makes meeting fast load transient response requirement such as that of the GTL+ bus an easy job. In minimum configuration, the two controllers default to 1.5V and 2.5V respectively.

Both linear controllers have under voltage latch-off.

Features

- Provides 3 regulated voltages
- Power Good flag and output enable
- Under-voltage latch-off

Switching Section

- Synchronous rectification
- 5-bit DAC programmable from 3.5V to 1.3V
- Typical 1% DAC tolerance
- Switching frequency: 50 kHz to 1 MHz
- Two levels of over-voltage protection
- Two methods of over-current protection
- Adaptive non-overlapping FET gate drives
- Soft start without external capacitor

Linear Section

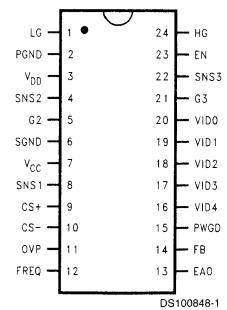
- N-FET and NPN driving capability
- Ultra fast response speed
- Output voltages default to 1.5V and 2.5V yet adjustable

Applications

- Embedded power supplies for PC motherboards
- Triple DC/DC power supplies
- Programmable high current DC/DC power supply

Pin Configuration

24-Lead SOIC



DS100848-1

Top View
NS Package Number M24B

National Semiconductor

LM2638
Motherboard Power Supply Solution with a 5-Bit Programmable Switching Controller and Two Linear Regulator Controllers

General Description

The LM2638 provides a comprehensive embedded power supply solution for motherboards hosting high performance MPUs such as Pentium™ II, M II™, K6™-2 and other similar high performance MPUs. The LM2638 incorporates a 5-bit programmable, synchronous buck switching controller and two high-speed linear regulator controllers in a 24-pin SO package. In a typical application, the switching controller supplies the MPU core, and the linear regulator controllers supply the GTL+ bus and the clock or graphics chip core. A charge pump pin helps provide the necessary voltage to power the linear sections when 12V is shut off during system standby such as STR mode.

Switching Section — The switching regulator controller features an Intel-compatible, 5-bit programmable output voltage, over-current and over-voltage protection, a power good signal, and a logic-controlled output enable. There are two user-selectable over-current protection methods. One provides accurate over-current protection with the use of an external sense resistor. The other saves cost by taking advantage of the r_{DS_ON} of the high-side FET. When there is an over voltage, the controller turns off the high side FET and turns on the low side.

Linear Section — The two linear regulator controllers feature wide control bandwidth, N-FET and NPN transistor driving capability and an adjustable output. The wide control bandwidth makes meeting the GTL+ bus transient response requirement an easy job. In minimum configuration, the two controllers default to 1.5V and 1.25V respectively.

Both linear controllers have under voltage latch-off.

Features

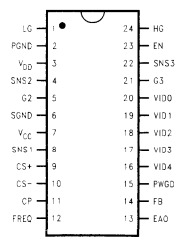
- Provides 3 regulated voltages
- Power Good flag and output enable
- Charge pump pin
  Switching Section
- Synchronous rectification
- 5-bit DAC programmable down to 1.3V
- Typical ±1% DAC tolerance
- Switching frequency: 50 kHz to 1 MHz
- Over-voltage protection
- Two methods of over-current protection
- Adaptive non-overlapping FET gate drives
- Soft start without external capacitor
  Linear Section
- N-FET and NPN drive capability
- Ultra fast response speed
- Under voltage latch-off at 0.63V
- Output voltages default to 1.5V and 2.5V yet adjustable

Applications

- Embedded power supplies for motherboards
- Triple DC/DC power supplies
- Programmable high current DC/DC power supply

Pin Configuration

24-Lead SOIC



DS101034-1

Top View
Order Number LM2638M
See NS Package Number M24B

National Semiconductor

LM2639
5-Bit Programmable, High Frequency Multi-phase PWM Controller

General Description

The LM2639 provides an attractive solution for power supplies of high power microprocessors (such as Pentium II™, M II™, K6™-2, K6™-3, etc.) exhibiting ultra fast load transients. Compared to a conventional single-phase supply, an LM2639 based multi-phase supply distributes the thermal and electrical loading among components in multiple phases and greatly reduces the corresponding stress in each component. The LM2639 can be programmed to control either a 3-phase converter or a 4-phase converter. Phase shift among the phases is 120° in the case of three phase and 90° with four-phase. Because the power channels are out of phase, there can be significant ripple cancellation for both the input and output current, resulting in reduced input and output capacitor size. Due to the nominal operating frequency of 2 MHz per phase, the size of the output inductors can be greatly reduced which results in a much faster load transient response and a dramatically shrunk output capacitor bank. Microprocessor power supplies with all surface mount components can be easily built.

The internal high speed transconductance amplifier guarantees good dynamic performance. The output drive voltages can be adjusted through a resistor divider to control switching loss in the external FETs.

The internal master clock frequency of up to 8 MHz is set by an external reference resistor. An external clock of 10 MHz can also be used to drive the chip to achieve frequency control and multi-chip operation.

The LM2639 also provides input under-voltage lock-out with hysteresis and input over-current protection.

Features

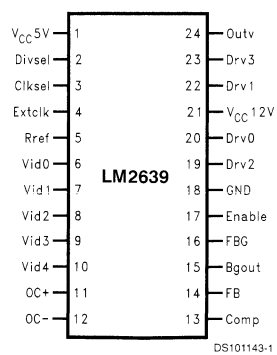
- Ultra fast load transient response
- Enables all surface-mount-design
- Selectable 2, 3, 4 phase operation
- Clock frequency from 40 kHz to 10 MHz
- Precision load current sharing
- 5-bit programmable from 3.5V to 1.3V
- VID code compatible to VRM 8.X specification
- Output voltage is 2.0V for VID code 11111
- Selectable internal or external clock
- Digital 16-step soft start
- Input under-voltage lock-out, over-current protection

Applications

- Servers and workstations
- High current, ultra-fast transient microprocessors

Pin Configuration

24-Pin Plastic SOIC



Top View
See NS Package Number M24B

National Semiconductor

LM2640
Dual Adjustable Step-Down Switching Power Supply Controller

General Description

The LM2640 is a dual step-down power supply controller intended for application in notebook personal computers and other battery-powered equipment.

Fixed-frequency synchronous drive of logic-level N-channel power MOSFETs is combined with an optional pulse-skipping mode to achieve ultra efficient power conversion over a 1000:1 load current range. The pulse-skipping mode can be disabled in favor of fixed-frequency operation regardless of the load current level.

High DC gain and current-mode feedback control assure excellent line and load regulation and a wide loop bandwidth for fast response to dynamic loads.

An internal oscillator fixes the switching frequency at 200 kHz. Optionally, switching can be synchronized to an external clock running as fast as 400 kHz.

An optional soft-start feature limits current surges from the input power supply at start up and provides a simple means of start-up sequencing.

Logic-level inputs allow the controllers to be turned ON and OFF separately.

Key Specifications

- 96% efficient
- 5.5 to 30V input range
- Dual outputs adjustable from 2.2 to 6V
- 0.5% typical load regulation error
- 0.002%/V typical line regulation error

Features

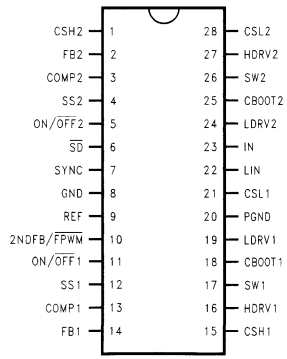
- 200 kHz fixed-frequency switching
- Switching synchronization with an external signal up to 400 kHz
- Optional pulse-skipping mode
- Adjustable secondary feedback
- Input undervoltage lockout
- Output undervoltage shutdown protection
- Output overvoltage shutdown protection
- Programmable soft-start (each controller)
- 5V, 50 mA linear regulator output
- Precision 2.5V reference output
- 28-pin TSSOP

Applications

- Notebook and subnotebook computers
- Wireless data terminals
- Battery-powered instruments

Connection Diagram and Ordering Information

28-Lead TSSOP (MTC)



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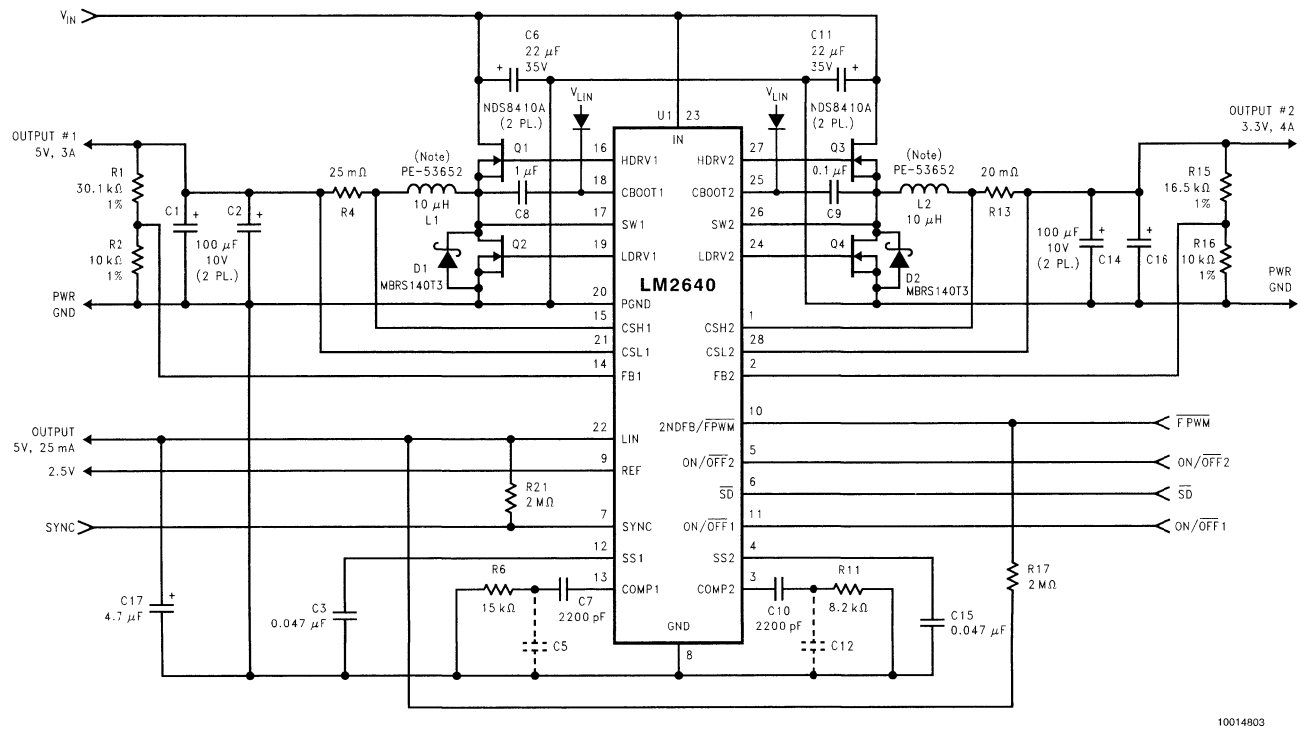
Top View
Order Number LM2640MTC-ADJ
See NS Package Number MTC28

Pin Description

(Refer to Typical Application Circuits)

Pin #	Name	Function
1	CSH2	The sense point for the positive side of the voltage across the current sense resistor (R13) placed in series with output #2.
2	FB2	The regulated output voltage appearing at output #2 is sensed using this pin by connecting it to the center of the output resistive divider (R15 and R16).
3	COMP2	An R-C network made up of R11, C10, and C12 is connected to this pin which provides loop compensation for regulated output #2.
4	SS2	This provides programmable soft-start for the #2 output along with capacitor C15.
5	ON/$\overline{\text{OFF}}$2	This pin turns off only output #2.
6	$\overline{\text{SD}}$	The part can be put into "sleep" mode using this pin, where both outputs are off and the internal chip functions are shut down.
7	SYNC	The internal oscillator may be synchronized to an external clock via this pin.
8	GND	Connect this pin to circuit Signal Ground.
9	REF	Internal 2.5V reference voltage. This voltage is turned off by the $\overline{\text{SD}}$ pin, but remains on if either or both ON/$\overline{\text{OFF}}$ pins are pulled low, which turns off the regulated output(s).
10	2NDFB/$\overline{\text{FPWM}}$	A 12V supply can be generated using an auxiliary winding on the 5V output inductor. Feedback to control this 12V output is brought in through this pin. If the 12V supply is not required, this pin can also force the chip to operate at fixed frequency at light loads by pulling the pin low (this is the "forced-PWM" mode of operation). This will prevent the converter from operating in pulse-skipping mode.
11	ON/$\overline{\text{OFF}}$1	This pin turns off only output #1.
12	SS1	This provides programmable soft-start for the #1 output along with capacitor C3.
13	COMP1	An R-C network made up of R6, C5, and C7 is connected to this pin which provides loop compensation for regulated output #1.
14	FB1	The regulated output voltage appearing at output #1 is sensed using this pin by connecting it to the center of the output resistive divider (R1 and R2).
15	CSH1	The sense point for the positive side of the voltage across the current sense resistor (R4) placed in series with output #1.
16	HDRV1	The drive for the gate of the high-side switching FET used for output #1.
17	SW1	This is the switching output drive point of the two power FETs which produce output #1.
18	CBOOT1	The bootstrap capacitor (C8) for output #1 is returned to this point.
19	LDRV1	The drive for the gate of the low-side switching FET (synchronous rectifier) used for output #1.
20	PGND	Connect this pin to circuit Power Ground.
21	CSL1	The sense point for the negative side of the voltage across the current sense resistor (R4) placed in series with output #1.
22	LIN	This pin provides a low-current (50 mA max) 5V output. This output is always on, and can not be turned off by either the $\overline{\text{SD}}$ or ON/$\overline{\text{OFF}}$ pins.
23	IN	This is the connection for the main input power.
24	LDRV2	The drive for the gate of the low-side switching FET (synchronous rectifier) used for output #2.
25	CBOOT2	The bootstrap capacitor (C9) for output #2 is returned to this point.
26	SW2	This is the switching output drive point of the two power FETs which produce output #2.
27	HDRV2	The drive for the gate of the high-side switching FET used for output #2.
28	CSL2	The sense point for the negative side of the voltage across the current sense resistor (R13) placed in series with output #2.

Typical Application Circuits



Note: Alternate recommended inductor is Sumida CDRH-125-100MC. If this inductor is used, R6 should be changed to 3.3k and R11 should be 5.1k.

FIGURE 1. Application With 5V/3A and 3.3V/4A Outputs

Typical Application Circuits (Continued)

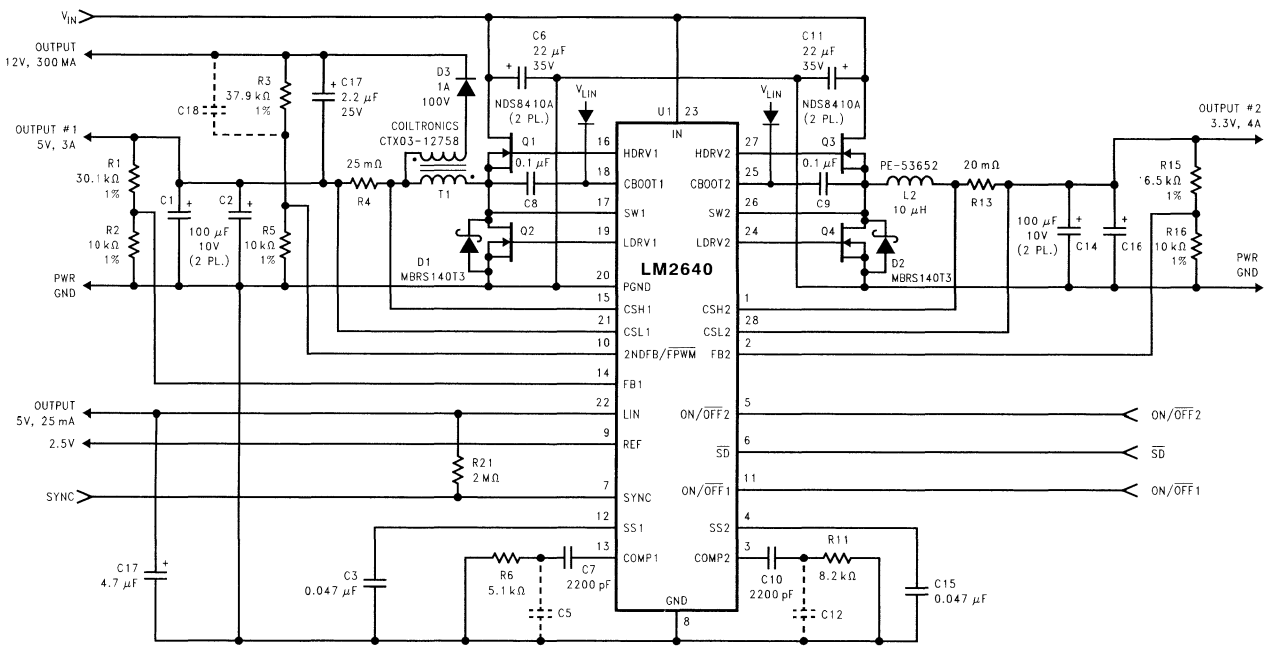


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FIGURE 2. Application With 5V/3A, 3.3V/4A, and 12V/0.3A Outputs

National Semiconductor

LM2641
Dual Adjustable Step-Down Switching Power Supply Controller

General Description

The LM2641 is a dual step-down power supply controller intended for application in notebook personal computers and other battery-powered equipment.

Fixed-frequency synchronous drive of logic-level N-channel power MOSFETs is combined with an optional pulse-skipping mode to achieve ultra efficient power conversion over a 1000:1 load current range. The pulse-skipping mode can be disabled in favor of fixed-frequency operation regardless of the load current level.

High DC gain and current-mode feedback control assure excellent line and load regulation and a wide loop bandwidth for fast response to dynamic loads.

An internal oscillator fixes the switching frequency at 300 kHz. Optionally, switching can be synchronized to an external clock running as fast as 400 kHz.

An optional soft-start feature limits current surges from the input power supply at start up and provides a simple means of start-up sequencing.

Logic-level inputs allow the controllers to be turned ON and OFF separately.

Key Specifications

- 96% efficient
- 5.5 to 30V input range
- Dual outputs adjustable from 2.2 to 8V
- 0.5% typical load regulation error
- 0.002%/V typical line regulation error

Features

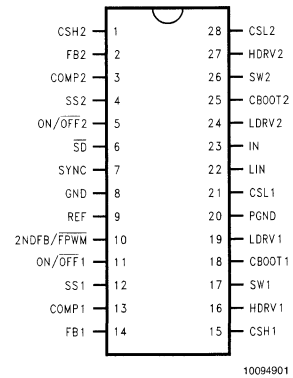
- 300 kHz fixed-frequency switching
- Switching synchronization with an external signal up to 400 kHz
- Optional pulse-skipping mode
- Adjustable secondary feedback
- Input undervoltage lockout
- Output undervoltage shutdown protection
- Output overvoltage shutdown protection
- Programmable soft-start (each controller)
- 5V, 50 mA linear regulator output
- Precision 2.5V reference output
- 28-pin TSSOP

Applications

- Notebook and subnotebook computers
- Wireless data terminals
- Battery-powered instruments

Connection Diagram and Ordering Information

28-Lead TSSOP (MTC)



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Top View
Order Number LM2641MTC-ADJ
See NS Package Number MTC28

Pin Description (Refer to Typical Application Circuits)

Pin #	Name	Function
1	CSH2	The sense point for the positive side of the voltage across the current sense resistor (R13) placed in series with output #2.
2	FB2	The regulated output voltage appearing at output #2 is sensed using this pin by connecting it to the center of the output resistive divider (R15 and R16).
3	COMP2	An R-C network made up of R11, C10, and C12 is connected to this pin which provides loop compensation for regulated output #2.
4	SS2	This provides programmable soft-start for the #2 output along with capacitor C15.
5	ON/$\overline{\text{OFF}}$2	This pin turns off only output #2.
6	$\overline{\text{SD}}$	The part can be put into "sleep" mode using this pin, where both outputs are off and the internal chip functions are shut down.
7	SYNC	The internal oscillator may be synchronized to an external clock via this pin.
8	GND	Connect this pin to circuit Signal Ground.
9	REF	Internal 2.5V reference voltage. This voltage is turned off by the $\overline{\text{SD}}$ pin, but remains on if either or both ON/$\overline{\text{OFF}}$ pins are pulled low, which turns off the regulated output(s).
10	2NDFB/$\overline{\text{FPWM}}$	A 12V supply can be generated using an auxiliary winding on the 5V output inductor. Feedback to control this 12V output is brought in through this pin. If the 12V supply is not required, this pin can also force the chip to operate at fixed frequency at light loads by pulling the pin low (this is the "forced-PWM" mode of operation). This will prevent the converter from operating in pulse-skipping mode.
11	ON/$\overline{\text{OFF}}$1	This pin turns off only output #1.
12	SS1	This provides programmable soft-start for the #1 output along with capacitor C3.
13	COMP1	An R-C network made up of R6, C5, and C7 is connected to this pin which provides loop compensation for regulated output #1.
14	FB1	The regulated output voltage appearing at output #1 is sensed using this pin by connecting it to the center of the output resistive divider (R1 and R2).
15	CSH1	The sense point for the positive side of the voltage across the current sense resistor (R4) placed in series with output #1.
16	HDRV1	The drive for the gate of the high-side switching FET used for output #1.
17	SW1	This is the switching output drive point of the two power FETs which produce output #1.
18	CBOOT1	The bootstrap capacitor (C8) for output #1 is returned to this point.
19	LDRV1	The drive for the gate of the low-side switching FET (synchronous rectifier) used for output #1.
20	PGND	Connect this pin to circuit Power Ground.
21	CSL1	The sense point for the negative side of the voltage across the current sense resistor (R4) placed in series with output #1.
22	LIN	This pin provides a low-current (50 mA max) 5V output. This output is always on, and can not be turned off by either the $\overline{\text{SD}}$ or ON/$\overline{\text{OFF}}$ pins.
23	IN	This is the connection for the main input power.
24	LDRV2	The drive for the gate of the low-side switching FET (synchronous rectifier) used for output #2.
25	CBOOT2	The bootstrap capacitor (C9) for output #2 is returned to this point.
26	SW2	This is the switching output drive point of the two power FETs which produce output #2.
27	HDRV2	The drive for the gate of the high-side switching FET used for output #2.
28	CSL2	The sense point for the negative side of the voltage across the current sense resistor (R13) placed in series with output #2.

Typical Application Circuits

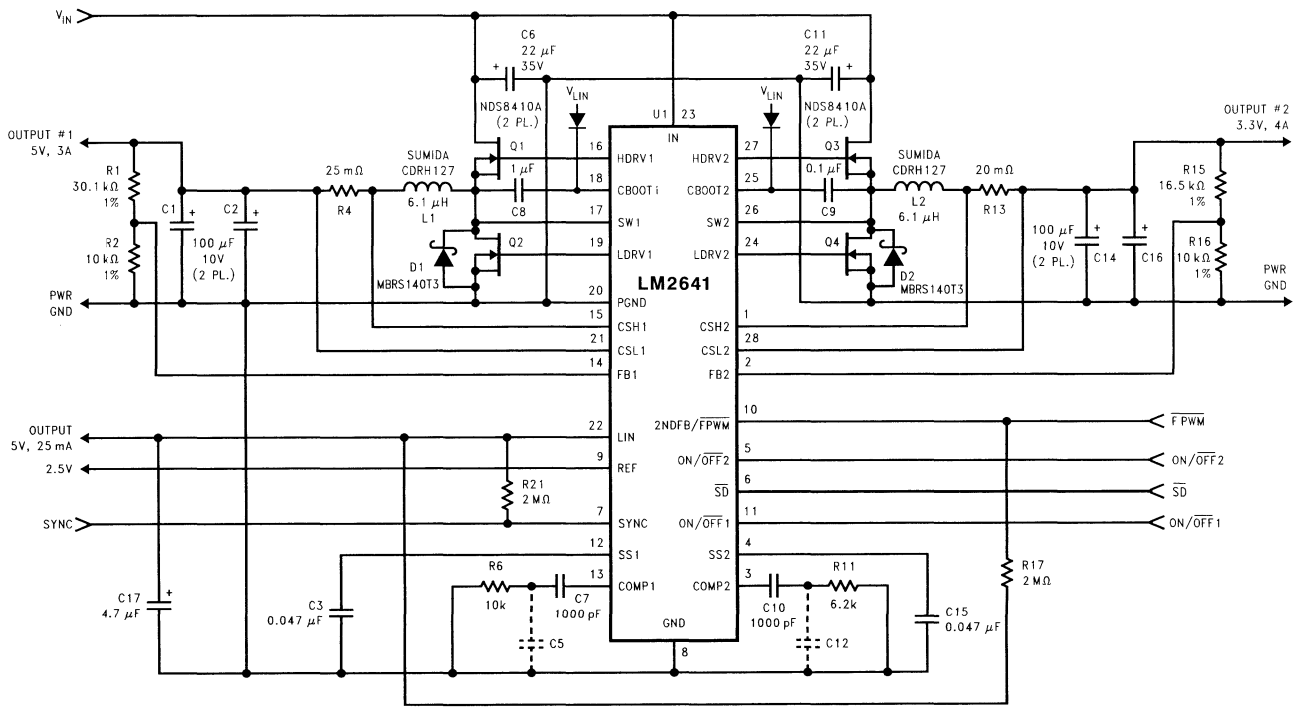


FIGURE 1. Application With 5V/3A and 3.3V/4A Outputs

Typical Application Circuits (Continued)

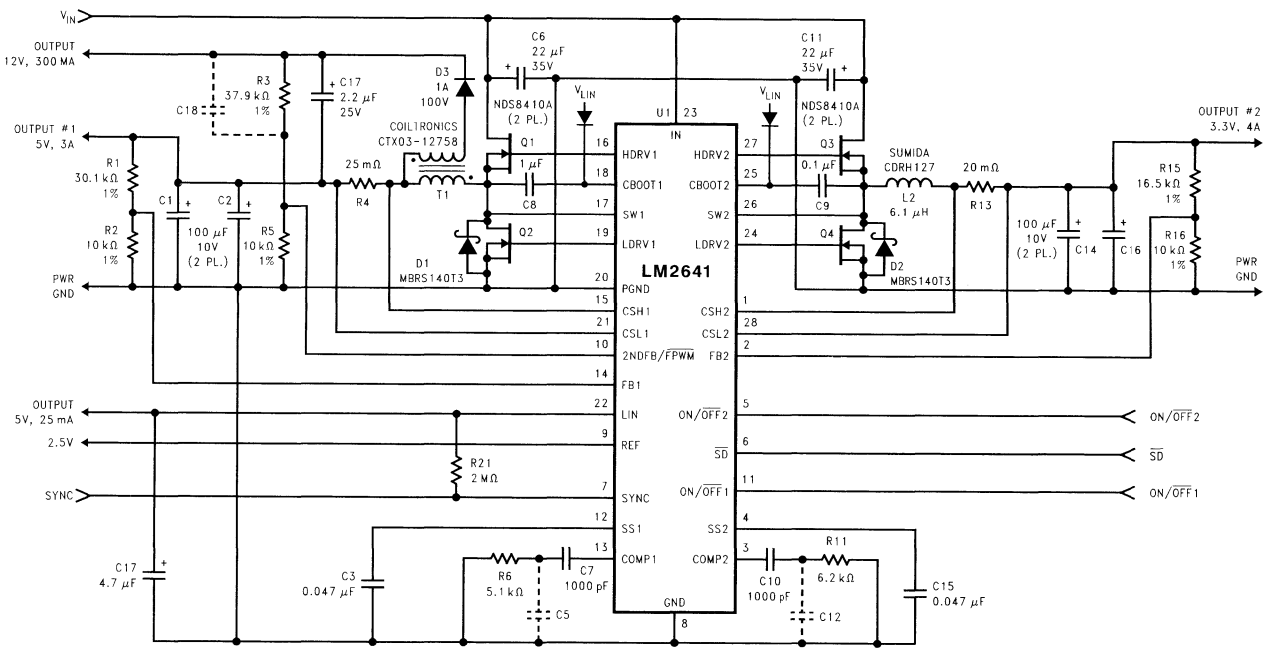


FIGURE 2. Application With 5V/3A, 3.3V/4A, and 12V/0.3A Outputs

National Semiconductor

LM2645
Advanced Two-Phase Switching Controller With Two Linear Outputs

General Description

The LM2645 is a feature-rich IC that combines two current mode synchronous buck regulator controllers, an adjustable linear regulator controller and a fixed 3.3V standby output rail.

The two switching regulator controllers operate 180° out of phase. This feature reduces the input ripple RMS current, thereby significantly reducing the required input capacitance. The two switching regulator outputs can also be paralleled to operate as a dual-phase regulator.

The use of synchronous rectification and pulse-skip operation at light load achieves high efficiency over a wide load range. Fixed-frequency operation can be obtained by disabling the pulse-skip mode. The switching frequency of the LM2645 is user selectable between 200 kHz or 300 kHz.

The first switching controller (Channel 1) features a fixed 5V output, and the second switching controller controller (Channel 2) features a fixed 3.3V output. Both channels can also be independently adjusted from 1.3 to 5.5V. The adjustable linear regulator can be adjusted from 3.3V to 15V. An internal 5V rail is also available externally for driving bootstrap circuitry. This rail also serves as the input for an internal LDO that provides the fixed 3.3V/50mA output rail.

Current-mode feedback control assures excellent line and load regulation and a wide loop bandwidth for excellent response to fast load transients. Current is sensed across either the Vds of the top FET or across an external sense resistor connected in series with the drain of the top FET. Current limit is independently adjustable for each channel.

The analog soft-start for the switching controllers uses an innovative new approach. It is independent of the input voltage which makes the soft-start behavior more predictable and controllable.

Independant PGOOD signals monitor each of the switching regulator outputs. The switching outputs have under-voltage and over-voltage latch protection, while the output of the external linear regulator has undervoltage latch protection. The undervoltage latch can be disabled or adjustably delayed.

Features

GENERAL

- 4.5V to 30V input range
- Power good function
- Input under-voltage lockout
- 10 µA Shutdown/Recycle for entire chip
- Thermal shutdown
- TSSOP package

SWITCHING SECTION

- Two synchronous buck regulators for fixed 5V/3.3V or adjustable outputs
- Outputs adjustable from 1.3V to 5.5V
- 0.04% (typical) line and load regulation error
- Selectable switching frequency 200/300 kHz
- Two channels operating 180° out of phase
- Separate on/off for each channel
- Separate Power Good signals
- Current mode control with or without sense resistor
- Adjustable cycle-by-cycle current limit
- Skip-mode operation available
- Negative current limit
- Separate soft start for each channel
- Output UVP and OVP
- Programmable output UVP delay
- Self discharge of output capacitors when turned off

LINEAR SECTION

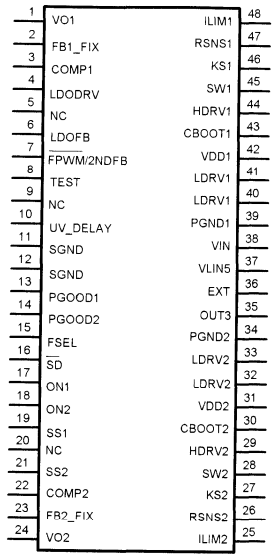
- Adjustable (3.3V to 15V) linear regulator with external PNP pass transistor
- ±2% initial tolerance of set voltage
- Output UVP for adjustable linear regulator
- Fixed 3.3V/50mA output rail
- Fixed 5V reference rail

Applications

- Notebook and sub-notebook computers
- Embedded computer systems
- Battery-powered instruments
- High end gaming systems
- Set-top boxes
- WebPAD

Connection Diagram

TOP VIEW



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48-Lead TSSOP (MTD)
Order Number LM2645MTD
See NS Package Number MTD48

Pin Descriptions

VO1 (Pin 1): The feedback input for Channel 1. Always connect directly to the output. Fixed or adjustable output voltage is selected by FB1_FIX.

FB1_FIX (Pin 2): The feedback input for setting the output voltage of Channel 1. Connecting this pin to VLIN5 sets the output voltage to 5V, or to the center of a voltage divider for an adjustable output.

COMP1 (Pin 3): Compensation pin for Channel 1. This is the output of the internal transconductance amplifier. The compensation network should be connected between this pin and the signal ground, SGND.

LDODRV (Pin 4): The output of the adjustable linear regulator controller. Connects to the base of a PNP Pass transistor. This pin is activated when Channel 1 is enabled.

NC (Pins 5, 9, 20): No internal connection. Connect these pins to ground.

LDOFB (Pin 6): Dual function input pin. When connected to the center of a resistor divider, it serves as the 1.238V feedback input for the LDODRV. Connecting this pin to VLIN5 disables the LDODRV.

$\overline{\text{FPWM}}$/2NDFB (Pin 7): Multi-function input pin. When held HIGH (>2V), pulse-skipping mode is enabled for both switching regulators. When held LOW (<0.8V), both regulators will function in Fixed Frequency PWM mode. This pin can also be connected to the center of a resistor divider for feedback regulation of a secondary winding voltage. In this case, Ch 1 will operate in pulse-skipping mode when the output is lightly loaded. If the linear regulator controller output is heavy loaded, the operating frequency in pulse-skipping will be increased accordingly to maintain the voltage at this pin to 1.5V or higher. Thus, the secondary winding voltage will always have the necessary overhead voltage for the linear regulator to maintain regulation.

TEST (Pin 8): Special purpose input pin for factory use only. This pin must be connected to ground.

UV_DELAY (Pin 10): : A capacitor from this pin to ground adjusts the delay of the undervoltage protection for the two switching outputs and the linear regulated output controlled by the LDODRV. The delay time is set by charging a capacitor to 2.3V from a 5µA current source. Pulling this pin to ground disables undervoltage protection on these outputs.

SGND (Pin 11,12): Ground connection for the signal level circuitry. It should be connected to the ground rail of the system.

PGOOD1 (Pin 13): An open-drain power-good output for Channel 1. It is 'LOW' (low impedance to ground) whenever the output voltage travels out of the ±10% window. It stays latched in a 'LOW' state if the output travels beyond the positive limit that trips the over-volatge protection.

PGOOD2 (Pin 14): An open drain power good output for Channel 2. It serves the same function as the PGOOD1.

FSEL (Pin 15): Selects the Switching Frequency of the two switching controllers. The frequency is 300kHz when this pin is pulled HIGH (>2V), or 200kHz when this pin is pulled LOW (<0.8V).

$\overline{\text{SD}}$ (Pin 16): Shutdown control input. Pulling this pin LOW (<0.6V) turns OFF the entire chip which then draws less than 10 µA of supply current. The chip is ON if this pin is held HIGH (>2V). Toggling this pin from HIGH to LOW and then HIGH again resets the chip causing it to recover from any protection latch.

ON1 (Pin 17): Output enable for Channel 1 and LDODRV (Pin 4). Channel 1 and LDODRV are disabled when this pin is pulled LOW (<0.8V), and are enabled when this pin is pulled HIGH (>2V).

ON2 (Pin 18): Output enable for Channel 2. Channel 2 is enabled when this pin is pulled high (> 2V) and disabled when this is pulled low (<0.8V).

SS1 (Pin 19): Soft-start input pin for Channel 1. The rise time of the output voltage of Channel 1 is programmed by the charge rate of a capacitor connected from this pin to ground by an internal 2 µA current source. If the output does not reach regulation (to within –6% of nominal voltage) by the time this pin exceeds 2V (typical), the UV_DELAY pin begins charging the capacitor connected from it to ground. If the output is not within regulation after the UVP delay, the chip latches off.

SS2 (Pin 21): Soft-start input pin for Channel 2. Serves the same function as the SS1, Pin 19.

COMP2 (Pin 22): Compensation pin for Channel 2. This is the output of the internal transconductance amplifier. The compensation network should be connected between this pin and the signal ground SGND (Pins 11, 12).

FB2_FIX (Pin 23): The feedback input for setting the output voltage of Channel 2. Connecting this pin to VLIN5 sets the output voltage to 3.3V, or to the center of a voltage divider for an adjustable output.

VO2 (Pin 24): The feedback input for Channel 2. Always connect directly to the output. Fixed or adjustable output voltage is selected by FB2_FIX.

ILIM2 (Pin 25): Current limit threshold setting for Channel 2. It sinks a constant current of 10 µA that is converted to a voltage through a resistor connected from this pin to Vin. The voltage across this resistor is compared with either the Vds

Pin Descriptions (Continued)

of the top MOSFET or the voltage across an external current sense resistor to determine if an over-current condition has occurred in Channel 2.

RSNS2 (Pin 26): The negative (–) Kelvin sense for the internal current limit comparator of Channel 2. Always use a separate trace to connect this pin to the current sense point. Connect this pin to the low side of the current sense resistor that is placed between V_{IN} and the drain of the top MOSFET. When the Vds of the top MOSFET is used for current sensing, then connect this pin to the source of the top MOSFET.

KS2 (Pin 27): The positive (+) Kelvin sense for the internal current limit comparator of Channel 2. Use a separate trace to connect this pin to the current sense point. Connect to Vin as close to the node of the current sense resistor; when no current-sense resistor is used, connect it as close to the Drain node of the upper MOSFET.

SW2 (Pin 28): : Switch-node connection for Channel 2, which is connected to the source of the top MOSFET. It serves as the negative supply rail for the topside gate driver, HDRV2.

HDRV2 (Pin 29): Top-side gate-drive output for Channel 2. A floating drive output that rides on the switching-node voltage.

CBOOT2 (Pin 30): Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 2 top-side gate drive.

VDD2 (Pin 31): The supply rail for the Channel 2 low-side gate drive, usually ties together with VDD1. Connect to VLIN5 through a 4.7Ω resistor and bypassed to ground with a ceramic capacitor of at least 1µF.

LDRV2 (Pins 32, 33): Low-side gate-drive output for Channel 2. Tie these two pins together.

PGND2 (Pin 34): Power ground for Channel 2.

OUT3 (Pin 35): The fixed 3.3V linear regulated output. Derived from VLIN5 by an internal LDO, it is current limited at 100mA. The continuous output current is a function of the ambient operating temperature and the total power dissipation in the chip and must be derated accordingly. See (Note 2) in Electrical Characteristics section.

EXT (Pin 36): External power input to an internal switch. This pin is usually connected to the fixed 5V output of Channel 1. When the voltage on this pin is higher than 4.7V, the internal 5V LDO that provides VLIN5 from VIN is disabled, and an internal switch connects VLIN5 to this pin to minimize dissipation in the chip. Connect this pin to ground and VLIN5 to VIN if VIN is operating in 4.5V to 5.5V range.

VLIN5 (Pin 37): This pin is the output of an internal 5V LDO regulator derived from VIN when no external 5V supply is available. It supplies the internal bias for the chip, supplies the boostrap circuitry for gate drive and serves as the input supply of an internal LDO to generate OUT3. Bypass this pin to power ground with a minimum of 4.7µF ceramic capacitor. Connect this pin to the VIN pin when Vin is operating in 4.5V to 5.5V range.

VIN (Pin 38): The input power of the chip. Connects to the upper (+) input rail of the system.

PGND1 (Pin 39): Power ground for Channel 1.

LDRV1 (Pins 40, 41): Low-side gate-drive output for Channel 1. Tie these two pins together.

VDD1 (Pin 42): The supply rail for the low-side gate drive of Channel 1. Same function as VDD2 (Pin 31).

CBOOT1 (Pin 43): Bootstrap capacitor connection. It serves as the positive supply rail for the Channel 1 top-side gate drive.

HDRV1 (Pin 44): Top-side gate-drive output for Channel 1. See HDRV2 (Pin 29).

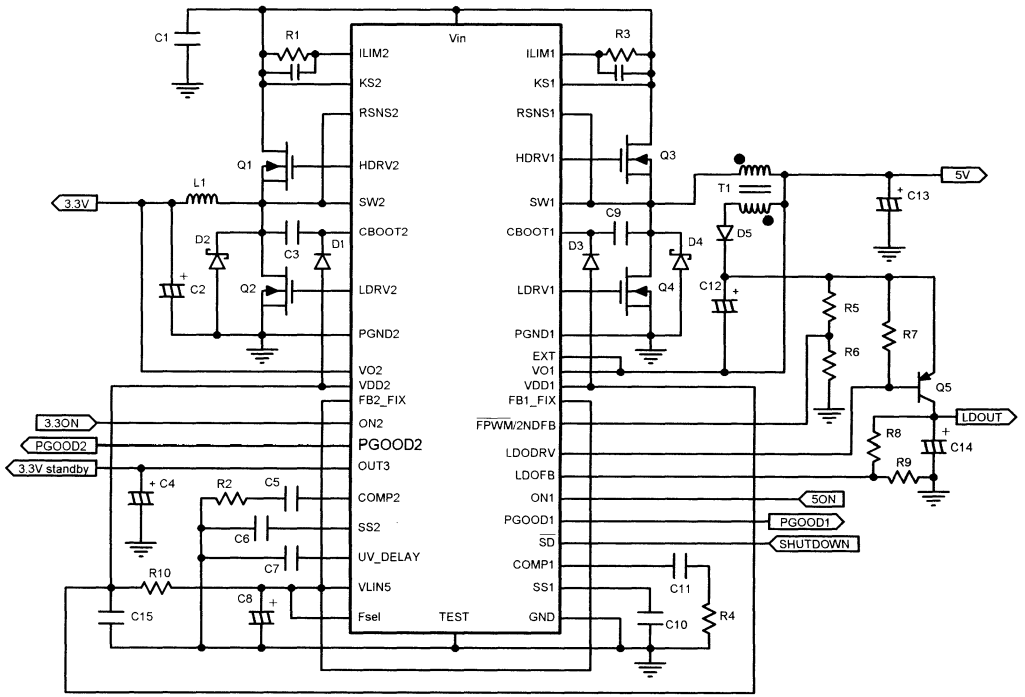
SW1 (Pin 45): Switch-node connection for Channel 1, See SW2 (Pin 28).

KS1 (Pin 46): The upper (+) Kelvin sense for the internal current limit comparator of Channel 1 (see KS2, Pin 27).

RSNS1 (Pin 47): The lower (–) Kelvin sense for the internal current limit comparator of Channel 1 (see RSNS2, Pin 26).

ILIM1 (Pin 48): Current limit threshold setting for Channel 1 (see ILIM2, Pin 25).

Typical Application Circuit



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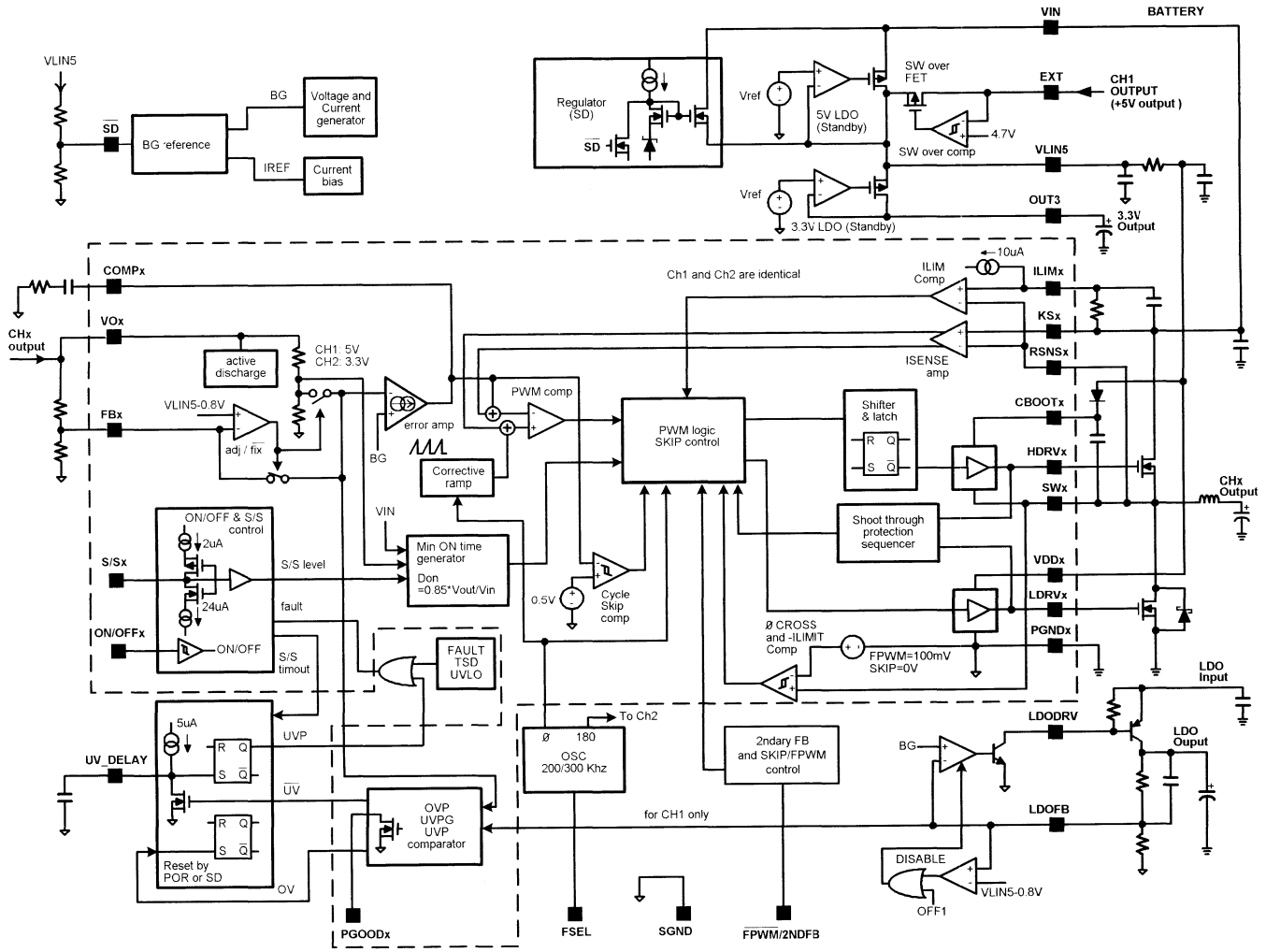
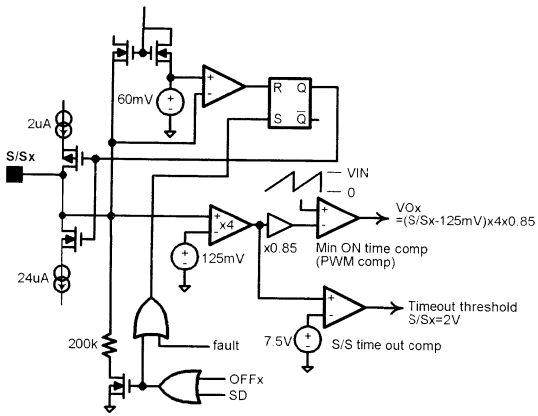
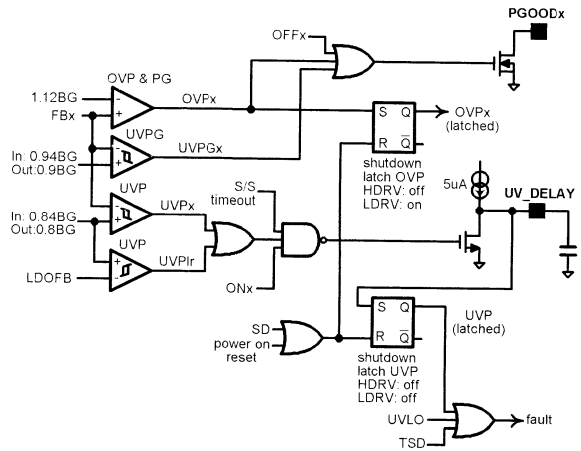
Simplified Block Diagram



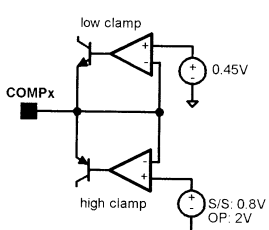
Simplified Block Diagram (Continued)



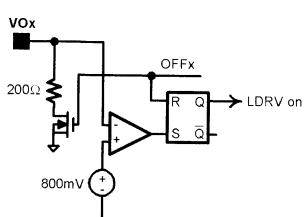
S/S pin Soft Start



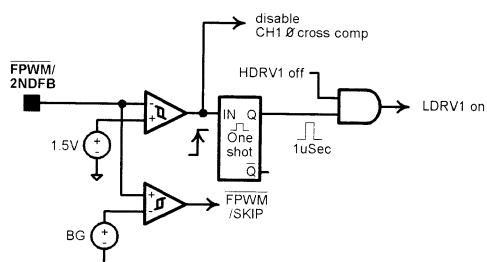
PGOOD, OVP and UVP Protection



COMP pin clamp



VO pin active discharge and VO detector



FPWM/SKIP, 2NDFB control

20015903

TABLE 1. Shut Down Latch Truth Table

Input												Output
ovp1	ovp2	uvp1	uvp2	uvp4	oc3	ch1 on	ch2 on	fault	ssto1	ssto2	uv_delay	latch off
1						1		0				1
	1						1	0				1
		1				1		0	1		cap	1
			1				1	0		1	cap	1
				1		1		0	1		cap	1
0	0	0	0	0	1			0	0	0	cap	0
All other combinations												0

Notes:

1. 'fault' is the logic OR of UVLO and thermal shutdown.
2. 'cap' means the pin has a capacitor of appropriate value between it and ground.
3. Positive logic is used.
4. ssto1, ssto2 means soft start timeout for Ch 1 and Ch 2 respectively.
5. A blank value means 'don't care'.
6. 'oc3' means OUT3 output current over 100mA current.
7. 'uvp4' means UVP of the linear regulated output controlled by LDODRV.
8. $\overline{SD}$ pin is pulled high.

TABLE 2. Power Good Truth Table

Input										Output	
ovp1	ovp2	uvpg1	uvpg2	uvpg4	ch1 on	ch2 on	fault	latch off	$\overline{SD}$	PGOOD1	PGOOD2
1					1			1	1	0	0
	1					1		1	1	0	0
		1			1				1	0	
			1			1			1		0
0		0		1	1		0	0	1	1	
					0				1	0	
						0			1		0
0		0			1		0	0	1	1	
	0		0			1	0	0	1		1
							1		1	0	0
								1	1	0	0
									0	0	0

Notes:

1. Positive logic is used.
2. A blank value means 'don't care'.
3. The symbol uvpg1, 2, 4 means the power good undervoltage threshold of the corresponding channel.

National Semiconductor

LM2650
Synchronous Step-Down DC/DC Converter

General Description

The LM2650 is a step-down DC/DC converter featuring high efficiency over a 3A to milliamperes load range. This feature makes the LM2650 an ideal fit in battery-powered applications that demand long battery life in both run and standby modes.

The LM2650 also features a logic-controlled shutdown mode in which it draws at most 25µA from the input power supply.

The LM2650 employs a fixed-frequency pulse-width modulation (PWM) and synchronous rectification to achieve very high efficiencies. In many applications, efficiencies reach 95%+ for loads around 1A and exceed 90% for moderate to heavy loads from 0.2A to 2A.

A low-power hysteretic or 'sleep' mode keeps efficiencies high at light loads. The LM2650 enters and exits sleep mode automatically as the load crosses 'sleep in' and 'sleep out' thresholds. The LM2650 provides nodes for programming both thresholds via external resistors. A logic input allows the user to override the automatic sleep feature and keep the LM2650 in PWM mode regardless of the load level.

An optional soft-start feature limits current surges from the input power supply at start up and provides a simple means of sequencing multiple power supplies.

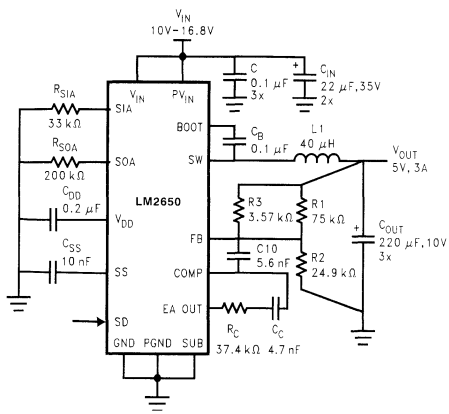
Features

- Ultra high efficiencies (95% possible)
- High efficiency over a 3A to milliamperes load range
- Synchronous switching of internal NMOS power FETs
- Wide input voltage range (4.5V to 18V)
- Output voltage adjustable from 1.5V to 16V
- Automatic low-power sleep mode
- Logic-controlled micropower shutdown ($I_{QSD} \leq 25$ µA)
- Frequency adjustable up to 300 kHz
- Frequency synchronization with external signal
- Programmable soft-start
- Short-circuit current limiting
- Thermal shutdown
- Available in 24-lead Small-Outline package

Applications

- Notebook and palmtop personal computers
- Portable data terminals
- Modems
- Portable Instruments
- Global positioning devices (GPSs)
- Battery-powered digital devices

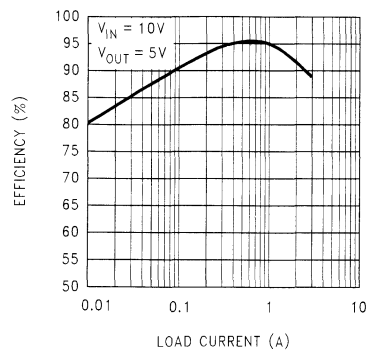
Typical Application



DS012848-1

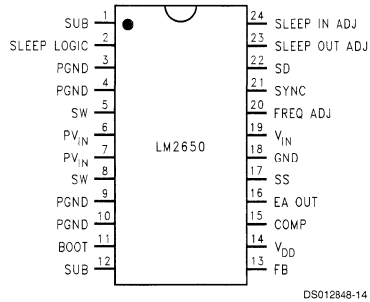
Converting a Four-Cell Li Ion Battery to 5V

LM2650-ADJ Efficiency



DS012848-2

Connection Diagram



Top View
24-Lead Small Outline Package (M)
Order Number LM2650M-ADJ
See Package Number M24B

Pin Descriptions (Refer to the Block Diagrams)

Pins	Description
1, 12	**SUB**: These pins make electrical contact with the substrate of the die. Ground them. For best thermal performance, ground them to the same large, uninterrupted copper plane as the PGND pins.
2	**SLEEP LOGIC**: Use this logic input to select the conversion mode; low selects PWM, high selects sleep, and high impedance (open) permits the LM2650 to move freely and automatically between the modes, using PWM for moderate to heavy loads and sleep for light loads.
3, 4, 9, 10	**PGND**: The ground return of the power stage. The power stage consists of the two power switches Q1 and Q2, the gate drivers DH and DL, and the linear voltage regulators VRegH and VRegL. For best electrical and thermal performance, ground these pins to a large, uninterrupted copper plane.
5, 8	**SW**: The output node of the power stage. It swings from slightly below ground to slightly below the voltage to PV_{IN}. To minimize the effects of switching noise on nearby circuitry, keep all traces originating from SW short and to the point. Route all traces carrying signals well away from the SW traces.
6, 7	**PV_{IN}**: The positive supply rail of the power stage. Bypass each PV_{IN} pin to PGND with a 0.1 µF capacitor. Use capacitors having low ESL and low ESR, and locate them close to the IC.
11	**BOOT**: The positive supply rail of the high-side gate driver DH. Connect a 0.1 µF capacitor from this node to SW. Bootstrapping action creates a supply rail about 9V above that at PV_{IN}, and DH uses this rail to override the gate of the NMOS power FET Q1. Overriding ensures low $R_{DS(on)}$.
13	**FB**: The feedback input.
14	**V_{DD}**: An internal regulator steps the input voltage down to a 4V rail used by the signal-level circuitry. V_{DD} is the output node of this regulator. Bypass V_{DD} to GND close to the IC with a 0.2 µF capacitor.
15	**COMP**: The inverting input of the error amplifier EA.
16	**EA OUT**: The output node of the error amplifier EA.
17	**SS**: The soft start node. Connect a capacitor from SS to GND.
18	**GND**: The ground return of the signal-level circuitry.
19	**V_{IN}**: The positive supply rail of the internal 4V regulator. Bypass V_{IN} to GND close to the IC with a 0.1 µF capacitor.
20	**FREQ ADJ**: The LM2650 switches at a nominal 90 kHz. Connect a resistor between FREQ ADJ and GND to adjust the frequency up from the nominal. Use the graph under Typical performance Characteristics to select the resistor.
21	**SYNC**: The synchronization input. If the switching frequency is to be synchronized with an external clock signal, apply the clock signal here. Ground if not used.
22	**SD**: Use this logic input to control shutdown; pull low for operation, high for shutdown.
23	**SLEEP OUT ADJ (SOA)**: The value of the resistor connected between SIA and ground programs the sleep-in threshold. Higher values program lower thresholds.
24	**SLEEP IN ADJ (SIA)**: The value of the resistor connected between SIA and ground programs the sleep-in threshold. Higher values program lower thresholds.

National Semiconductor

LM2651
1.5A High Efficiency Synchronous Switching Regulator

General Description

The LM2651 switching regulator provides high efficiency power conversion over a 100:1 load range (1.5A to 15mA). This feature makes the LM2651 an ideal fit in battery-powered applications that demand long battery life in both run and standby modes.

Synchronous rectification is used to achieve up to 97% efficiency. At light loads, the LM2651 enters a low power hysteretic or "sleep" mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15mA load. A shutdown pin is available to disable the LM2651 and reduce the supply current to less than 10µA.

The LM2651 contains a patented current sensing circuitry for current mode control. This feature eliminates the external current sensing resistor required by other current-mode DC-DC converters.

The LM2651 has a 300 kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

A programmable soft-start feature limits current surges from the input power supply at start up and provides a simple means of sequencing multiple power supplies.

Other protection features include input undervoltage lockout, current limiting, and thermal shutdown.

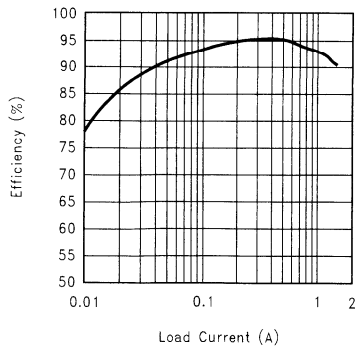
Features

- Ultra high efficiency up to 97%
- High efficiency over a 1.5A to milliamperes load range
- 4V to 14V input voltage range
- 1.8V, 2.5V, 3.3V, or ADJ output voltage
- Internal MOSFET switch with low $R_{DS(on)}$ of 75mΩ
- 300kHz fixed frequency internal oscillator
- 7µA shutdown current
- Patented current sensing for current mode control
- Input undervoltage lockout
- Adjustable soft-start
- Current limit and thermal shutdown
- 16-pin TSSOP package

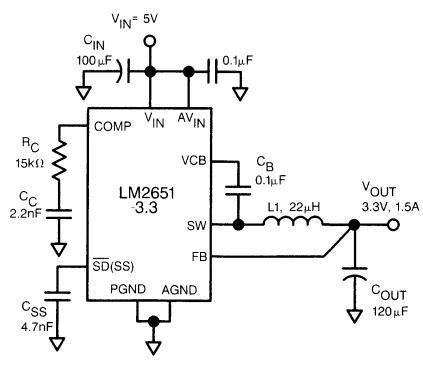
Applications

- Personal digital assistants (PDAs)
- Computer peripherals
- Battery-powered devices
- Handheld scanners
- High efficiency 5V conversion

Typical Application

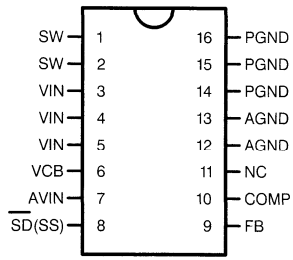


Efficiency vs Load Current (V_{IN} = 5V, V_{OUT} = 3.3V



Connection Diagram

16-Lead TSSOP (MTC)



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Ordering Information

V_{OUT}	Part Number		Package Type	NSC Package Drawing
	Supplied as 94 Units, Rail	Supplied as 2.5k Units, Tape and Reel		
1.8	LM2651MTC-1.8	LM2651MTCX-1.8	TSSOP-16	MTC16
2.5	LM2651MTC-2.5	LM2651MTCX-2.5		
3.3	LM2651MTC-3.3	LM2651MTCX-3.3		
ADJ	LM2651MTC-ADJ	LM2651MTCX-ADJ		

Pin Description

Pin	Name	Function
1, 2	SW	Switched-node connection, which is connected with the source of the internal high-side MOSFET.
3-5	VIN	Main power supply pin.
6	VCB	Bootstrap capacitor connection for high-side gate drive.
7	AVIN	Input supply voltage for control and driver circuits.
8	$\overline{SD}$(SS)	Shutdown and Soft-start control pin. Pulling this pin below 0.3V shuts off the regulator. A capacitor connected from this pin to ground provides a control ramp of the input current. Do not drive this pin with an external source or erroneous operation may result.
9	FB	Output voltage feedback input. Connected to the output voltage.
10	COMP	Compensation network connection. Connected to the output of the voltage error amplifier.
11	NC	No internal connection.
12-13	AGND	Low-noise analog ground.
14-16	PGND	Power ground.

National Semiconductor

LM2653
1.5A High Efficiency Synchronous Switching Regulator

General Description

The LM2653 switching regulator provides high efficient power conversion over a 100:1 load range (1.5A to 15 mA). This feature makes the LM2653 an ideal fit in battery-powered applications.

Synchronous rectification is used to achieve up to 97% efficiency. At light loads, the LM2653 enters a low power hysteretic or "sleep" mode to keep the efficiency high. In many applications, the efficiency still exceeds 80% at 15 mA load. A shutdown pin is available to disable the LM2653 and reduce the supply current to 7µA.

All the power, control, and drive functions are integrated within the ICs. The ICs contain patented current sensing circuity for current mode control. This feature eliminates the external current sensing resistor required by other current-mode DC-DC converters.

The ICs have a 300 kHz fixed frequency internal oscillator. The high oscillator frequency allows the use of extremely small, low profile components.

Protection features include thermal shutdown, input undervoltage lockout, adjustable soft-start, cycle by cycle current limit, output overvoltage and undervoltage protections.

Features

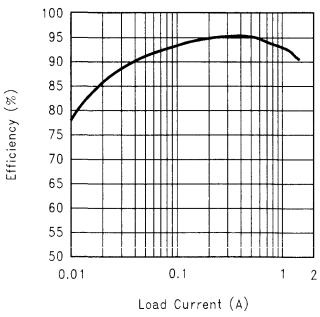
- Efficiency up to 97%
- 4V to 14V input voltage range
- 1.5V to 5.0V adjustable output voltage
- 0.1Ω Switch On Resistance
- 300 kHz fixed frequency internal oscillator
- 7 µA shutdown current
- Patented current sensing for current mode control
- Input undervoltage lockout
- Output overvoltage shutdown protection
- Output undervoltage shutdown protection
- Adjustable soft-start
- Adjustable PGOOD delay
- Current limit and thermal shutdown

Applications

- Webpad
- Personal digital assistants (PDAs)
- Computer peripherals
- Battery-powered devices
- Notebook computer video supply
- Handheld scanners
- GXM I/O and core voltage
- High efficiency 5V conversion

Typical Application

Efficiency vs Load Current
(V_{IN} = 5V, V_{OUT} = 3.3V)



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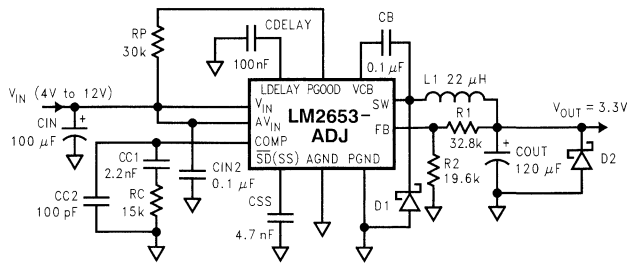

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National Semiconductor

LM2655
2.5A High Efficiency Synchronous Switching Regulator

General Description

The LM2655 is a current-mode controlled PWM step-down switching regulator. It has the unique ability to operate in synchronous or asynchronous mode. This gives the designer flexibility to choose between the high efficiency of synchronous operation, or the low solution cost of asynchronous operation. Along with flexibility, the LM2655 offers high power density with the small footprint of a TSSOP-16 package.

High efficiency (>90%) is obtained through the use of an internal low ON-resistance (33mΩ) MOSFET, and an external N-Channel MOSFET. This feature, together with its low quiescent current, makes the LM2655 an ideal fit in portable applications.

Integrated in the LM2655 are all the power, control, and drive functions for asynchronous operation. In addition, a low-side driver output allows easy synchronous operation. The IC uses patented current sensing circuitry that eliminates the external current sensing resistor required by other current-mode DC-DC converters. A programmable soft-start feature limits start up current surges and provides a means of sequencing multiple power supplies.

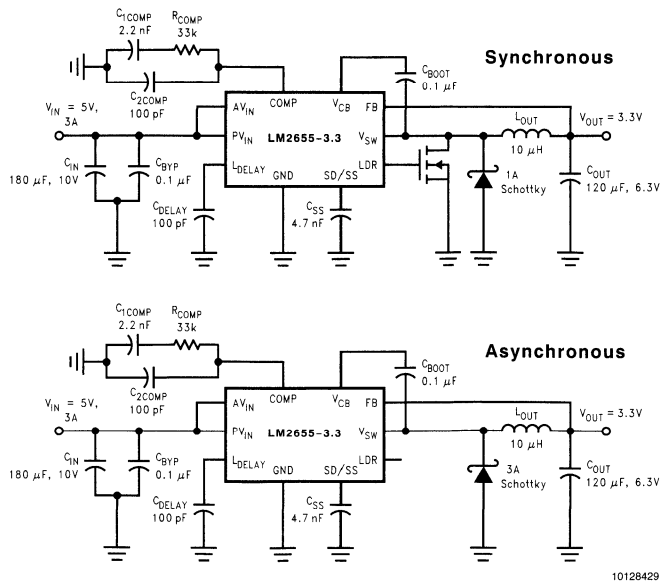
Features

- Ultra-high efficiency up to 96%
- 4V to 14V input voltage range
- Internal high-side MOSFET with low $R_{DS(ON)}$ = 0.033Ω
- 300 kHz fixed frequency internal oscillator
- Low-side drive for synchronous operation
- Guaranteed less than 12 µA shutdown current
- Patented current sensing for current mode control
- Programmable soft-start
- Input undervoltage lockout
- Output overvoltage shutdown protection
- Output undervoltage shutdown protection
- Thermal Shutdown
- 16-pin TSSOP package

Applications

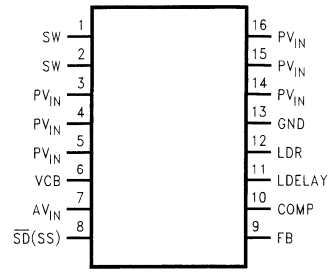
- Hard disk drives
- Internet appliances
- TFT monitors
- Computer peripherals
- Battery powered devices

Typical Application



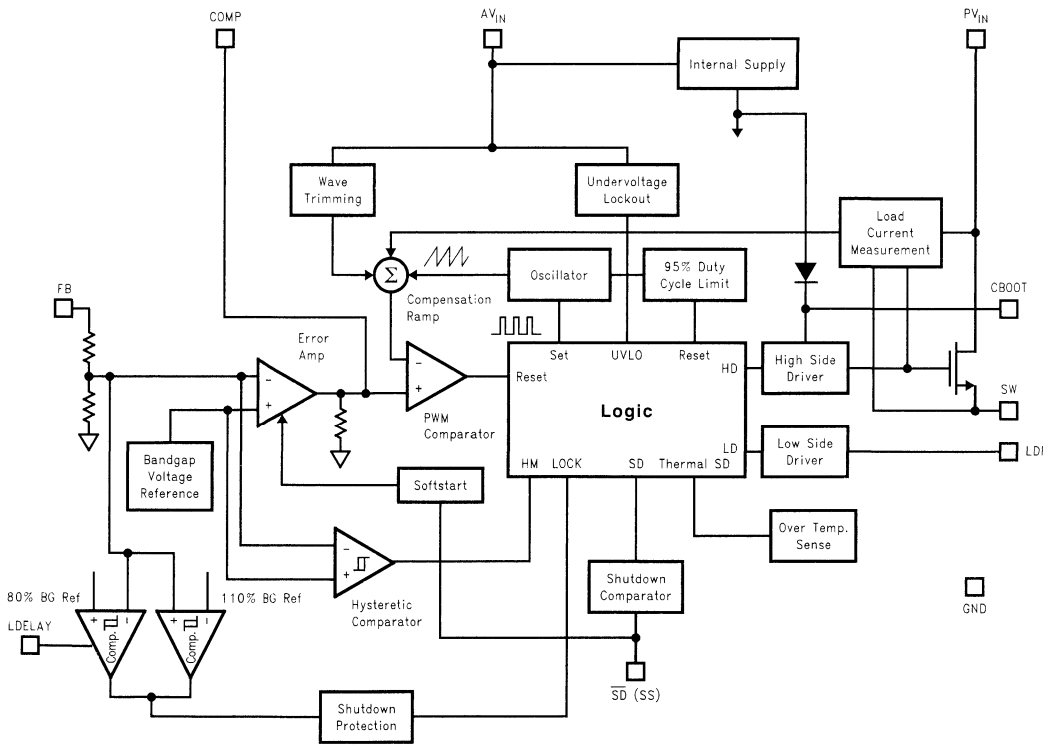
Connection Diagram

16-Lead TSSOP (MTC)



Top View
Order Number LM2655MTC-ADJ
See NS Package Number MTC16

Block Diagram



Pin Description

Pin	Name	Function
1-2	SW	Switched-node connection, which is connected to the source of the internal high-side MOSFET.
3-5	PV_{IN}	Main power supply input pin. Connected to the drain of the internal high-side MOSFET.
6	V_{CB}	Bootstrap capacitor connection for high-side gate drive.
7	AV_{IN}	Input voltage for control and drive circuits.
8	$\overline{SD}$(SS)	Shutdown and Soft-start control pin. Pulling this pin below 0.3V shuts off the regulator. A capacitor connected from this pin to ground provides a control ramp of the input current. Do not drive this pin with an external source or erroneous operation may result.
9	FB	Output voltage feedback input. Connected to the output voltage.
10	COMP	Compensation network connection. Connected to the output of the voltage error amplifier.
11	L_{DELAY}	A capacitor between this pin to ground sets the delay from when the output voltage reaches 80% of its nominal to when the undervoltage latch protection is enabled.
12	LDR	Low-side FET gate drive pin.
13	GND	Power ground.
14-16	PV_{IN}	Main power supply input pin. Connected to the drain of the internal high-side MOSFET.

Ordering Information

Supplied as 1000 units Tape and Reel	Supplied as 3000 units, Tape and Reel
LM2655MTC-3.3	LM2655MTCX-3.3
LM2655MTC-ADJ	LM2655MTCX-ADJ

National Semiconductor

LM2670
SIMPLE SWITCHER® High Efficiency 3A Step-Down Voltage Regulator with Sync

General Description

The LM2670 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 3A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance DMOS power switch. The series consists of fixed output voltages of 3.3V, 5V and 12V and an adjustable output version.

The SIMPLE SWITCHER concept provides for a complete design using a minimum number of external components. The switching clock frequency can be provided by an internal fixed frequency oscillator (260KHz) or from an externally provided clock in the range of 280KHz to 400Khz which allows the use of physically smaller sized components. A family of standard inductors for use with the LM2670 are available from several manufacturers to greatly simplify the design process. The external Sync clock provides direct and precise control of the output ripple frequency for consistent filtering or frequency spectrum positioning.

The LM2670 series also has built in thermal shutdown, current limiting and an ON/OFF control input that can power down the regulator to a low 50µA quiescent current standby condition. The output voltage is guaranteed to a ±2% tolerance.

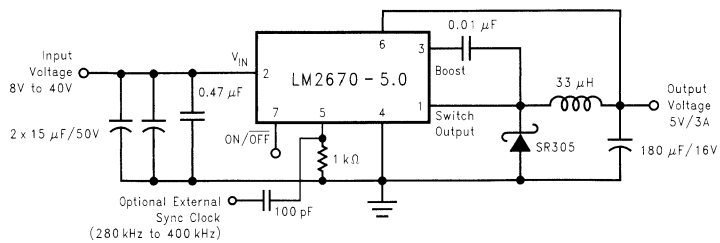
Features

- Efficiency up to 94%
- Simple and easy to design with (using off-the-shelf external components)
- 150 mΩ DMOS output switch
- 3.3V, 5V and 12V fixed output and adjustable (1.2V to 37V) versions
- 50µA standby current when switched OFF
- ±2%maximum output tolerance over full line and load conditions
- Wide input voltage range: 8V to 40V
- External Sync clock capability (280KHz to 400KHz)
- 260 KHz fixed frequency internal oscillator
- −40 to +125°C operating junction temperature range

Applications

- Simple to design, high efficiency (>90%) step-down switching regulators
- Efficient system pre-regulator for linear voltage regulators
- Battery chargers
- Communications and radio equipment regulator with synchronized clock frequency

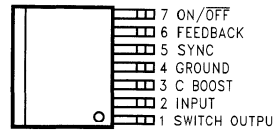
Typical Application



DS100942-3

Connection Diagram and Ordering Information

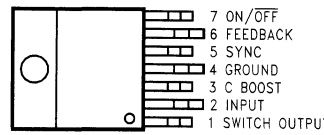
TO-263 Package
Top View



DS100942-1

Order Number
LM2670S-3.3, LM2670S-5.0,
LM2670S-12 or LM2670S-ADJ
See NSC Package Number TS7B

TO-220 Package
Top View



DS100942-2

Order Number
LM2670T-3.3, LM2670T-5.0,
LM2670T-12 or LM2670T-ADJ
See NSC Package Number TA07B

National Semiconductor

LM2671
SIMPLE SWITCHER® Power Converter High Efficiency 500mA Step-Down Voltage Regulator with Features

General Description

The LM2671 series of regulators are monolithic integrated circuits built with a LMDMOS process. These regulators provide all the active functions for a step-down (buck) switching regulator, capable of driving a 500mA load current with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5.0V, 12V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include patented internal frequency compensation (Patent Nos. 5,382,918 and 5,514,947), fixed frequency oscillator, external shutdown, soft-start, and frequency synchronization.

The LM2671 series operates at a switching frequency of 260 kHz, thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its very high efficiency (>90%), the copper traces on the printed circuit board are the only heat sinking needed.

A family of standard inductors for use with the LM2671 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies using these advanced ICs. Also included in the datasheet are selector guides for diodes and capacitors designed to work in switch-mode power supplies.

Other features include a guaranteed ±1.5% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring typically 50 µA stand-by current. The output switch includes current limiting, as well as thermal shutdown for full protection under fault conditions.

To simplify the LM2671 buck regulator design procedure, there exists computer design software, ***LM267X Made Simple*** (version 6.0).

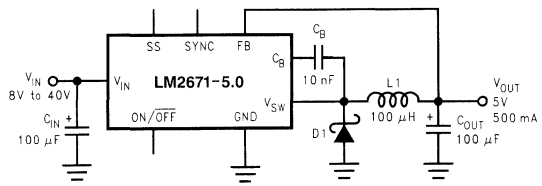
Features

- Efficiency up to 96%
- Available in SO-8, 8-pin DIP and LLP packages
- Computer Design Software ***LM267X Made Simple*** (version 6.0)
- Simple and easy to design with
- Requires only 5 external components
- Uses readily available standard inductors
- 3.3V, 5.0V, 12V, and adjustable output versions
- Adjustable version output voltage range: 1.21V to 37V
- ±1.5% max output voltage tolerance over line and load conditions
- Guaranteed 500mA output load current
- 0.25Ω DMOS Output Switch
- Wide input voltage range: 8V to 40V
- 260 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- Soft-start and frequency synchronization
- Thermal shutdown and current limit protection

Applications

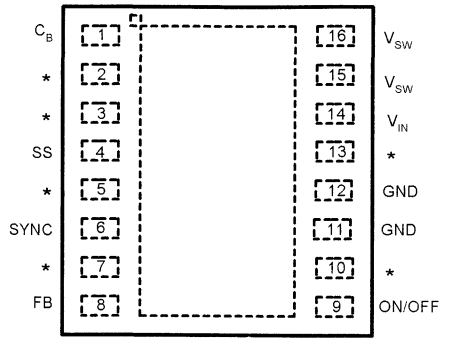
- Simple High Efficiency (>90%) Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators

Typical Application (Fixed Output Voltage Versions)



Connection Diagrams

16-Lead LLP Surface Mount Package
Top View

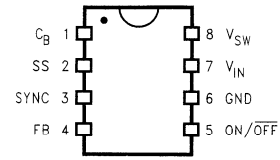


* No Connections

10004241

LLP Package
See NSC Package Drawing Number LDA16A

8-Lead Package
Top View



10004202

SO-8/DIP Package
See NSC Package Drawing Number MO8A/N08E

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Information	Package Marking	Supplied as:
16 Lead LLP			
12	LM2671LD-12	S0005B	1000 Units on Tape and Reel
12	LM2671LDX-12	S0005B	4500 Units on Tape and Reel
3.3	LM2671LD-3.3	S0006B	1000 Units on Tape and Reel
3.3	LM2671LDX-3.3	S0006B	4500 Units on Tape and Reel
5.0	LM2671LD-5.0	S0007B	1000 Units on Tape and Reel
5.0	LM2671LDX-5.0	S0007B	4500 Units on Tape and Reel
ADJ	LM2671LD-ADJ	S0008B	1000 Units on Tape and Reel
ADJ	LM2671LDX-ADJ	S0008B	4500 Units on Tape and Reel
SO-8			
12	LM2671M-12	2671M-12	Shipped in Anti-Static Rails
12	LM2671MX-12	2671M-12	2500 Units on Tape and Reel
3.3	LM2671M-3.3	2671M-3.3	Shipped in Anti-Static Rails
3.3	LM2671MX-3.3	2671M-3.3	2500 Units on Tape and Reel
5.0	LM2671M-5.0	2671M-5.0	Shipped in Anti-Static Rails
5.0	LM2671MX-5.0	2671M-5.0	2500 Units on Tape and Reel
ADJ	LM2671M-ADJ	2671M-ADJ	Shipped in Anti-Static Rails
ADJ	LM2671MX-ADJ	2671M-ADJ	2500 Units on Tape and Reel
DIP			
12	LM2671N-12	LM2671N-12	Shipped in Anti-Static Rails
3.3	LM2671N-3.3	LM2671N-3.3	Shipped in Anti-Static Rails
5.0	LM2671N-5.0	LM2671N-5.0	Shipped in Anti-Static Rails
ADJ	LM2671N-ADJ	LM2671N-ADJ	Shipped in Anti-Static Rail

National Semiconductor

LM2672
SIMPLE SWITCHER® Power Converter High Efficiency 1A Step-Down Voltage Regulator with Features

General Description

The LM2672 series of regulators are monolithic integrated circuits built with a LMDMOS process. These regulators provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load current with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5.0V, 12V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include patented internal frequency compensation (Patent Nos. 5,382,918 and 5,514,947), fixed frequency oscillator, external shutdown, soft-start, and frequency synchronization.

The LM2672 series operates at a switching frequency of 260 kHz, thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its very high efficiency (>90%), the copper traces on the printed circuit board are the only heat sinking needed.

A family of standard inductors for use with the LM2672 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies using these advanced ICs. Also included in the datasheet are selector guides for diodes and capacitors designed to work in switch-mode power supplies.

Other features include a guaranteed ±1.5% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring typically 50 µA stand-by current. The output switch includes current limiting, as well as thermal shutdown for full protection under fault conditions.

To simplify the LM2672 buck regulator design procedure, there exists computer design software, ***LM267X Made Simple*** version 6.0.

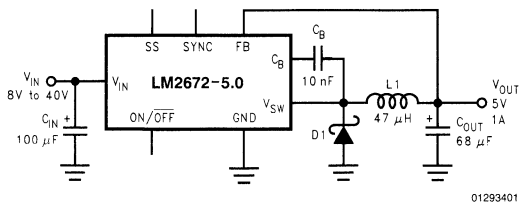
Features

- Efficiency up to 96%
- Available in SO-8, 8-pin DIP and LLP packages
- Computer Design Software ***LM267X Made Simple*** version 6.0
- Simple and easy to design with
- Requires only 5 external components
- Uses readily available standard inductors
- 3.3V, 5.0V, 12V, and adjustable output versions
- Adjustable version output voltage range: 1.21V to 37V
- ±1.5% max output voltage tolerance over line and load conditions
- Guaranteed 1A output load current
- 0.25Ω DMOS Output Switch
- Wide input voltage range: 8V to 40V
- 260 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- Soft-start and frequency synchronization
- Thermal shutdown and current limit protection

Typical Applications

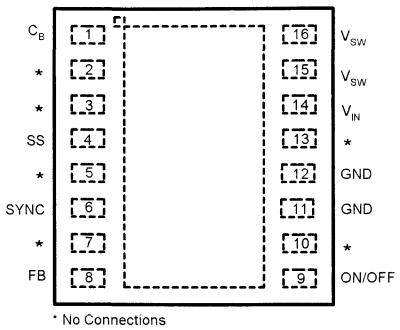
- Simple High Efficiency (>90%) Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators

Typical Application (Fixed Output Voltage Versions)



Connection Diagrams

16-Lead LLP Surface Mount Package
Top View

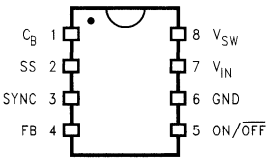


* No Connections

01293441

LLP Package
See NSC Package Drawing Number LDA16A

8-Lead Package
Top View



01293402

SO-8/DIP Package
See NSC Package Drawing Number MO8A/N08E

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Information	Package Marking	Supplied as:
16 Lead LLP			
12	LM2672LD-12	S0001B	1000 Units on Tape and Reel
12	LM2672LDX-12	S0001B	4500 Units on Tape and Reel
3.3	LM2672LD-3.3	S0002B	1000 Units on Tape and Reel
3.3	LM2672LDX-3.3	S0002B	4500 Units on Tape and Reel
5.0	LM2672LD-5.0	S0003B	1000 Units on Tape and Reel
5.0	LM2672LDX-5.0	S0003B	4500 Units on Tape and Reel
ADJ	LM2672LD-ADJ	S0004B	1000 Units on Tape and Reel
ADJ	LM2672LDX-ADJ	S0004B	4500 Units on Tape and Reel
SO-8			
12	LM2672M-12	2672M-12	Shipped in Anti-Static Rails
12	LM2672MX-12	2672M-12	2500 Units on Tape and Reel
3.3	LM2672M-3.3	2672M-3.3	Shipped in Anti-Static Rails
3.3	LM2672MX-3.3	2672M-3.3	2500 Units on Tape and Reel
5.0	LM2672M-5.0	2672M-5.0	Shipped in Anti-Static Rails
5.0	LM2672MX-5.0	2672M-5.0	2500 Units on Tape and Reel
ADJ	LM2672M-ADJ	2672M-ADJ	Shipped in Anti-Static Rails
ADJ	LM2672MX-ADJ	2672M-ADJ	2500 Units on Tape and Reel
DIP			
12	LM2672N-12	LM2672N-12	Shipped in Anti-Static Rails
3.3	LM2672N-3.3	LM2672N-3.3	Shipped in Anti-Static Rails
5.0	LM2672N-5.0	LM2672N-5.0	Shipped in Anti-Static Rails
ADJ	LM2672N-ADJ	LM2672N-ADJ	Shipped in Anti-Static Rails

National Semiconductor

LM2673
SIMPLE SWITCHER® 3A Step-Down Voltage Regulator with Adjustable Current Limit

General Description

The LM2673 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 3A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance DMOS power switch. The series consists of fixed output voltages of 3.3V, 5V and 12V and an adjustable output version.

The SIMPLE SWITCHER concept provides for a complete design using a minimum number of external components. A high fixed frequency oscillator (260KHz) allows the use of physically smaller sized components. A family of standard inductors for use with the LM2673 are available from several manufacturers to greatly simplify the design process.

Other features include the ability to reduce the input surge current at power-ON by adding a softstart timing capacitor to gradually turn on the regulator. The LM2673 series also has built in thermal shutdown and resistor programmable current limit of the power MOSFET switch to protect the device and load circuitry under fault conditions. The output voltage is guaranteed to a ±2% tolerance. The clock frequency is controlled to within a ±11% tolerance.

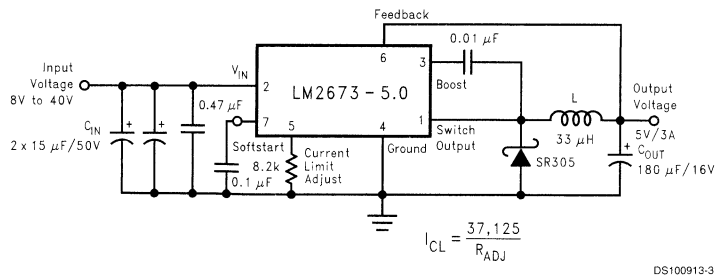
Features

- Efficiency up to 94%
- Simple and easy to design with (using off-the-shelf external components)
- Resistor programmable peak current limit over a range of 2A to 5A.
- 150 mΩ DMOS output switch
- 3.3V, 5V and 12V fixed output and adjustable (1.2V to 37V) versions
- ±2%maximum output tolerance over full line and load conditions
- Wide input voltage range: 8V to 40V
- 260 KHz fixed frequency internal oscillator
- Softstart capability
- −40 to +125°C operating junction temperature range

Applications

- Simple to design, high efficiency (>90%) step-down switching regulators
- Efficient system pre-regulator for linear voltage regulators
- Battery chargers

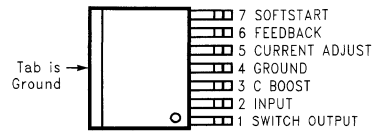
Typical Application



DS100913-3

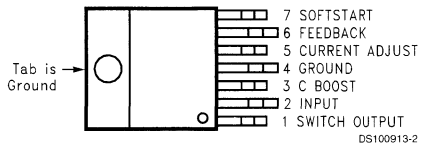
Connection Diagrams and Ordering Information

TO-263 Package
Top View



Order Number
LM2673S-3.3, LM2673S-5.0,
LM2673S-12 or LM2673S-ADJ
See NSC Package Number TS7B

TO-220 Package
Top View



Order Number
LM2673T-3.3, LM2673T-5.0,
LM2673T-12 or LM2673T-ADJ
See NSC Package Number TA07B

National Semiconductor

LM2674
SIMPLE SWITCHER® Power Converter High Efficiency 500 mA Step-Down Voltage Regulator

General Description

The LM2674 series of regulators are monolithic integrated circuits built with a LMDMOS process. These regulators provide all the active functions for a step-down (buck) switching regulator, capable of driving a 500 mA load current with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5.0V, 12V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include patented internal frequency compensation (Patent Nos. 5,382,918 and 5,514,947) and a fixed frequency oscillator.

The LM2674 series operates at a switching frequency of 260 kHz, thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its very high efficiency (>90%), the copper traces on the printed circuit board are the only heat sinking needed.

A family of standard inductors for use with the LM2674 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies using these advanced ICs. Also included in the datasheet are selector guides for diodes and capacitors designed to work in switch-mode power supplies.

Other features include a guaranteed ±1.5% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring typically 50 µA stand-by current. The output switch includes current limiting, as well as thermal shutdown for full protection under fault conditions.

To simplify the LM2674 buck regulator design procedure, there exists computer design software, ***LM267X Made Simple*** (version 6.0).

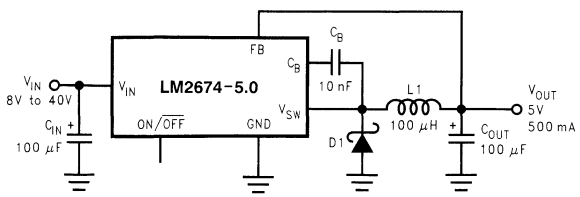
Features

- Efficiency up to 96%
- Available in SO-8, 8-pin DIP and LLP packages
- Computer Design Software ***LM267X Made Simple*** (version 6.0)
- Simple and easy to design with
- Requires only 5 external components
- Uses readily available standard inductors
- 3.3V, 5.0V, 12V, and adjustable output versions
- Adjustable version output voltage range: 1.21V to 37V
- ±1.5% max output voltage tolerance over line and load conditions
- Guaranteed 500mA output load current
- 0.25Ω DMOS Output Switch
- Wide input voltage range: 8V to 40V
- 260 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- Thermal shutdown and current limit protection

Typical Applications

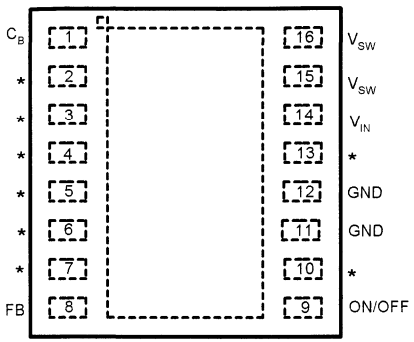
- Simple High Efficiency (>90%) Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- Positive-to-Negative Converter

Typical Application



Connection Diagrams

16-Lead LLP Surface Mount Package
Top View

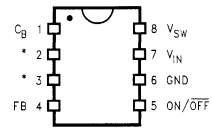


* No Connections

10004138

LLP Package
See NSC Package Drawing Number LDA16A

8-Lead Package
Top View



10004102

SO-8/DIP Package
See NSC Package Drawing Number MO8A/N08E

TABLE 1. Package Marking and Ordering Information

Output Voltage	Order Information	Package Marking	Supplied as:
16 Lead LLP			
12	LM2674LD-12	S0009B	1000 Units on Tape and Reel
12	LM2674LDX-12	S0009B	4500 Units on Tape and Reel
3.3	LM2674LD-3.3	S000AB	1000 Units on Tape and Reel
3.3	LM2674LDX-3.3	S000AB	4500 Units on Tape and Reel
5.0	LM2674LD-5.0	S000BB	1000 Units on Tape and Reel
5.0	LM2674LDX-5.0	S000BB	4500 Units on Tape and Reel
ADJ	LM2674LD-ADJ	S000CB	1000 Units on Tape and Reel
ADJ	LM2674LDX-ADJ	S000CB	4500 Units on Tape and Reel
SO-8			
12	LM2674M-12	2674M-12	Shipped in Anti-Static Rails
12	LM2674MX-12	2674M-12	2500 Units on Tape and Reel
3.3	LM2674M-3.3	2674M-3.3	Shipped in Anti-Static Rails
3.3	LM2674MX-3.3	2674M-3.3	2500 Units on Tape and Reel
5.0	LM2674M-5.0	2674M-5.0	Shipped in Anti-Static Rails
5.0	LM2674MX-5.0	2674M-5.0	2500 Units on Tape and Reel
ADJ	LM2674M-ADJ	2674M-ADJ	Shipped in Anti-Static Rails
ADJ	LM2674MX-ADJ	2674M-ADJ	2500 Units on Tape and Reel
DIP			
12	LM2674N-12	LM2674N-12	Shipped in Anti-Static Rails
3.3	LM2674N-3.3	LM2674N-3.3	Shipped in Anti-Static Rails
5.0	LM2674N-5.0	LM2674N-5.0	Shipped in Anti-Static Rails
ADJ	LM2674N-ADJ	LM2674N-ADJ	Shipped in Anti-Static Rails

National Semiconductor

LM2675
SIMPLE SWITCHER® Power Converter High Efficiency 1A Step-Down Voltage Regulator

General Description

The LM2675 series of regulators are monolithic integrated circuits built with a LMDMOS process. These regulators provide all the active functions for a step-down (buck) switching regulator, capable of driving a 1A load current with excellent line and load regulation. These devices are available in fixed output voltages of 3.3V, 5.0V, 12V, and an adjustable output version.

Requiring a minimum number of external components, these regulators are simple to use and include patented internal frequency compensation (Patent Nos. 5,382,918 and 5,514,947) and a fixed frequency oscillator.

The LM2675 series operates at a switching frequency of 260 kHz, thus allowing smaller sized filter components than what would be needed with lower frequency switching regulators. Because of its very high efficiency (>90%), the copper traces on the printed circuit board are the only heat sinking needed.

A family of standard inductors for use with the LM2675 are available from several different manufacturers. This feature greatly simplifies the design of switch-mode power supplies using these advanced ICs. Also included in the datasheet are selector guides for diodes and capacitors designed to work in switch-mode power supplies.

Other features include a guaranteed ±1.5% tolerance on output voltage within specified input voltages and output load conditions, and ±10% on the oscillator frequency. External shutdown is included, featuring typically 50 µA stand-by current. The output switch includes current limiting, as well as thermal shutdown for full protection under fault conditions.

To simplify the LM2675 buck regulator design procedure, there exists computer design software, ***LM267X Made Simple*** version 6.0.

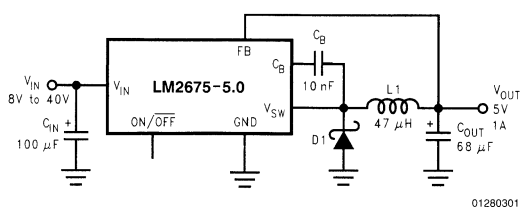
Features

- Efficiency up to 96%
- Available in SO-8, 8-pin DIP and LLP packages
- Computer Design Software ***LM267X Made Simple*** (version 6.0)
- Simple and easy to design with
- Requires only 5 external components
- Uses readily available standard inductors
- 3.3V, 5.0V, 12V, and adjustable output versions
- Adjustable version output voltage range: 1.21V to 37V
- ±1.5% max output voltage tolerance over line and load conditions
- Guaranteed 1A output load current
- 0.25Ω DMOS Output Switch
- Wide input voltage range: 8V to 40V
- 260 kHz fixed frequency internal oscillator
- TTL shutdown capability, low power standby mode
- Thermal shutdown and current limit protection

Typical Applications

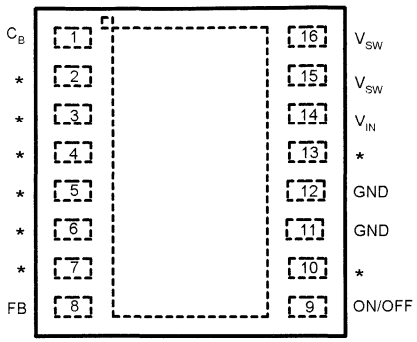
- Simple High Efficiency (>90%) Step-Down (Buck) Regulator
- Efficient Pre-Regulator for Linear Regulators
- Positive-to-Negative Converter

Typical Application



Connection Diagrams

16-Lead LLP Surface Mount Package
Top View

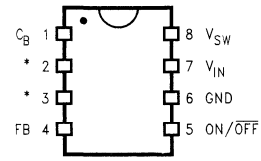


* No Connections

01280338

LLP Package
See NSC Package Drawing Number LDA16A

8-Lead Package
Top View



01280302

SO-8/DIP Package
See NSC Package Drawing Number MO8A/N08E

Package Marking and Ordering Information

TABLE 1.

Output Voltage	Order Information	Package Marking	Supplied as:
16 Lead LLP			
12	LM2675LD-12	S000DB	1000 Units on Tape and Reel
12	LM2675LDX-12	S000DB	4500 Units on Tape and Reel
3.3	LM2675LD-3.3	S000EB	1000 Units on Tape and Reel
3.3	LM2675LDX-3.3	S000EB	4500 Units on Tape and Reel
5.0	LM2675LD-5.0	S000FB	1000 Units on Tape and Reel
5.0	LM2675LDX-5.0	S000FB	4500 Units on Tape and Reel
ADJ	LM2675LD-ADJ	S000GB	1000 Units on Tape and Reel
ADJ	LM2675LDX-ADJ	S000GB	4500 Units on Tape and Reel
SO-8			
12	LM2675M-12	2675M-12	Shipped in Anti-Static Rails
12	LM2675MX-12	2675M-12	2500 Units on Tape and Reel
3.3	LM2675M-3.3	2675M-3.3	Shipped in Anti-Static Rails
3.3	LM2675MX-3.3	2675M-3.3	2500 Units on Tape and Reel
5.0	LM2675M-5.0	2675M-5.0	Shipped in Anti-Static Rails
5.0	LM2675MX-5.0	2675M-5.0	2500 Units on Tape and Reel
ADJ	LM2675M-ADJ	2675M-ADJ	Shipped in Anti-Static Rails
ADJ	LM2675MX-ADJ	2675M-ADJ	2500 Units on Tape and Reel
DIP			
12	LM2675N-12	LM2675N-12	Shipped in Anti-Static Rails
3.3	LM2675N-3.3	LM2675N-3.3	Shipped in Anti-Static Rails
5.0	LM2675N-5.0	LM2675N-5.0	Shipped in Anti-Static Rails
ADJ	LM2675N-ADJ	LM2675N-ADJ	Shipped in Anti-Static Rails

National Semiconductor

LM2676
SIMPLE SWITCHER® High Efficiency 3A Step-Down Voltage Regulator

General Description

The LM2676 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 3A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance DMOS power switch. The series consists of fixed output voltages of 3.3V, 5V and 12V and an adjustable output version.

The SIMPLE SWITCHER concept provides for a complete design using a minimum number of external components. A high fixed frequency oscillator (260KHz) allows the use of physically smaller sized components. A family of standard inductors for use with the LM2676 are available from several manufacturers to greatly simplify the design process.

The LM2676 series also has built in thermal shutdown, current limiting and an ON/OFF control input that can power down the regulator to a low 50µA quiescent current standby condition. The output voltage is guaranteed to a ±2% tolerance. The clock frequency is controlled to within a ±11% tolerance.

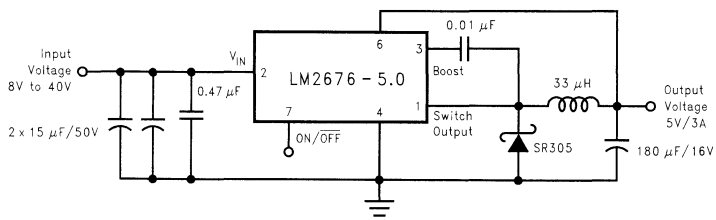
Features

- Efficiency up to 94%
- Simple and easy to design with (using off-the-shelf external components)
- 150 mΩ DMOS output switch
- 3.3V, 5V and 12V fixed output and adjustable (1.2V to 37V) versions
- 50µA standby current when switched OFF
- ±2%maximum output tolerance over full line and load conditions
- Wide input voltage range: 8V to 40V
- 260 KHz fixed frequency internal oscillator
- −40 to +125°C operating junction temperature range

Applications

- Simple to design, high efficiency (>90%) step-down switching regulators
- Efficient system pre-regulator for linear voltage regulators
- Battery chargers

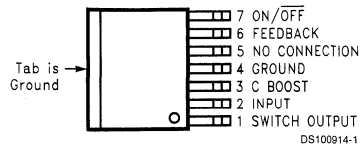
Typical Application



DS100914-3

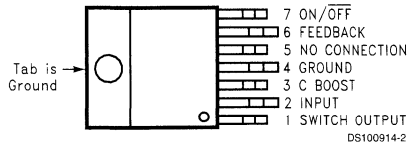
Connection Diagrams and Ordering Information

TO-263 Package
Top View



Order Number
LM2676S-3.3, LM2676S-5.0,
LM2676S-12 or LM2676S-ADJ
See NSC Package Number TS7B

TO-220 Package
Top View



Order Number
LM2676T-3.3, LM2676T-5.0,
LM2676T-12 or LM2676T-ADJ
See NSC Package Number TA07B

National Semiconductor

LM2677
SIMPLE SWITCHER® High Efficiency 5A Step-Down Voltage Regulator with Sync

General Description

The LM2677 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 5A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance DMOS power switch. The series consists of fixed output voltages of 3.3V, 5V and 12V and an adjustable output version.

The SIMPLE SWITCHER concept provides for a complete design using a minimum number of external components. The switching clock frequency can be provided by an internal fixed frequency oscillator (260KHz) or from an externally provided clock in the range of 280KHz to 400Khz which allows the use of physically smaller sized components. A family of standard inductors for use with the LM2677 are available from several manufacturers to greatly simplify the design process. The external Sync clock provides direct and precise control of the output ripple frequency for consistent filtering or frequency spectrum positioning.

The LM2677 series also has built in thermal shutdown, current limiting and an ON/OFF control input that can power down the regulator to a low 50μA quiescent current standby condition. The output voltage is guaranteed to a ±2% tolerance.

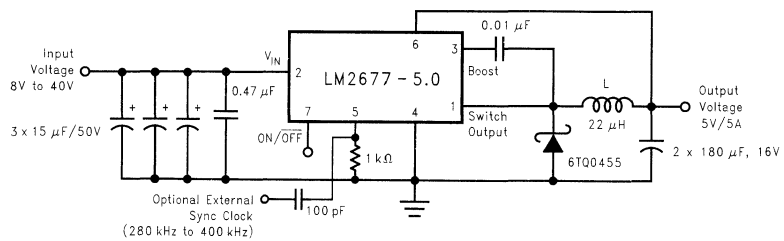
Features

- Efficiency up to 92%
- Simple and easy to design with (using off-the-shelf external components)
- 100 mΩ DMOS output switch
- 3.3V, 5V and 12V fixed output and adjustable (1.2V to 37V) versions
- 50μA standby current when switched OFF
- ±2%maximum output tolerance over full line and load conditions
- Wide input voltage range: 8V to 40V
- External Sync clock capability (280KHz to 400KHz)
- 260 KHz fixed frequency internal oscillator
- −40 to +125°C operating junction temperature range

Applications

- Simple to design, high efficiency (>90%) step-down switching regulators
- Efficient system pre-regulator for linear voltage regulators
- Battery chargers
- Communications and radio equipment regulator with synchronized clock frequency

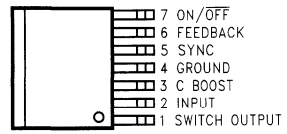
Typical Application



DS101301-3

Connection Diagrams and Ordering Information

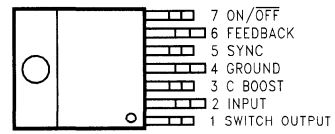
TO-263 Package
Top View



DS101301-1

Order Number
LM2677S-3.3, LM2677S-5.0,
LM2677S-12 or LM2677S-ADJ
See NSC Package Number TS7B

TO-220 Package
Top View



DS101301-2

Order Number
LM2677T-3.3, LM2677T-5.0,
LM2677T-12 or LM2677T-ADJ
See NSC Package Number TA07B

National Semiconductor

LM2678
SIMPLE SWITCHER® High Efficiency 5A Step-Down Voltage Regulator

General Description

The LM2678 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 5A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance DMOS power switch. The series consists of fixed output voltages of 3.3V, 5V and 12V and an adjustable output version.

The SIMPLE SWITCHER concept provides for a complete design using a minimum number of external components. A high fixed frequency oscillator (260KHz) allows the use of physically smaller sized components. A family of standard inductors for use with the LM2678 are available from several manufacturers to greatly simplify the design process.

The LM2678 series also has built in thermal shutdown, current limiting and an ON/OFF control input that can power down the regulator to a low 50μA quiescent current standby condition. The output voltage is guaranteed to a ±2% tolerance. The clock frequency is controlled to within a ±11% tolerance.

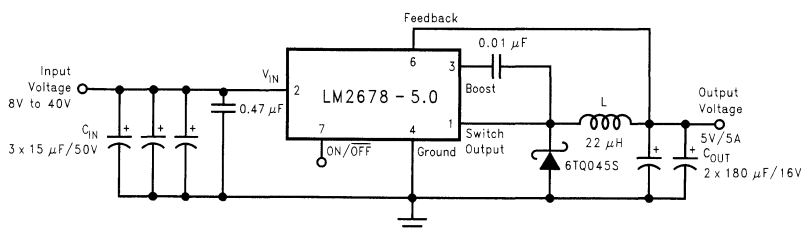
Features

- Efficiency up to 92%
- Simple and easy to design with (using off-the-shelf external components)
- 120 mΩ DMOS output switch
- 3.3V, 5V and 12V fixed output and adjustable (1.2V to 37V) versions
- 50μA standby current when switched OFF
- ±2%maximum output tolerance over full line and load conditions
- Wide input voltage range: 8V to 40V
- 260 KHz fixed frequency internal oscillator
- −40 to +125°C operating junction temperature range

Applications

- Simple to design, high efficiency (>90%) step-down switching regulators
- Efficient system pre-regulator for linear voltage regulators
- Battery chargers

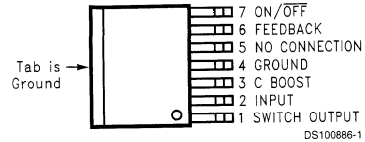
Typical Application



DS100886-3

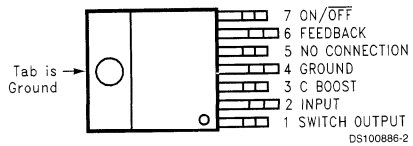
Connection Diagrams and Ordering Information

TO-263 Package
Top View



Order Number
LM2678S-3.3, LM2678S-5.0,
LM2678S-12 or LM2678S-ADJ
See NSC Package Number TS7B

TO-220 Package
Top View



Order Number
LM2678T-3.3, LM2678T-5.0,
LM2678T-12 or LM2678T-ADJ
See NSC Package Number TA07B

National Semiconductor

LM2679
SIMPLE SWITCHER® 5A Step-Down Voltage Regulator with Adjustable Current Limit

General Description

The LM2679 series of regulators are monolithic integrated circuits which provide all of the active functions for a step-down (buck) switching regulator capable of driving up to 5A loads with excellent line and load regulation characteristics. High efficiency (>90%) is obtained through the use of a low ON-resistance DMOS power switch. The series consists of fixed output voltages of 3.3V, 5V and 12V and an adjustable output version.

The SIMPLE SWITCHER concept provides for a complete design using a minimum number of external components. A high fixed frequency oscillator (260KHz) allows the use of physically smaller sized components. A family of standard inductors for use with the LM2679 are available from several manufacturers to greatly simplify the design process.

Other features include the ability to reduce the input surge current at power-ON by adding a softstart timing capacitor to gradually turn on the regulator. The LM2679 series also has built in thermal shutdown and resistor programmable current limit of the power MOSFET switch to protect the device and load circuitry under fault conditions. The output voltage is guaranteed to a ±2% tolerance. The clock frequency is controlled to within a ±11% tolerance.

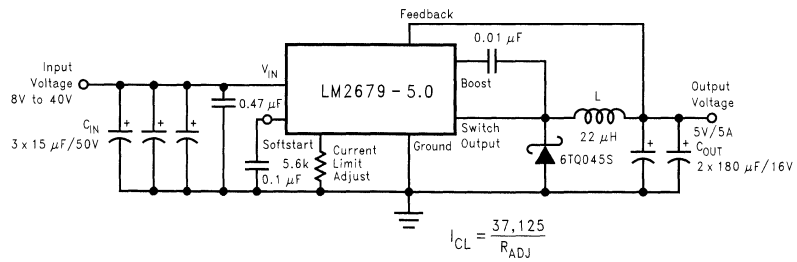
Features

- Efficiency up to 92%
- Simple and easy to design with (using off-the-shelf external components)
- Resistor programmable peak current limit over a range of 3A to 7A.
- 120 mΩ DMOS output switch
- 3.3V, 5V and 12V fixed output and adjustable (1.2V to 37V) versions
- ±2%maximum output tolerance over full line and load conditions
- Wide input voltage range: 8V to 40V
- 260 KHz fixed frequency internal oscillator
- Softstart capability
- −40 to +125°C operating junction temperature range

Applications

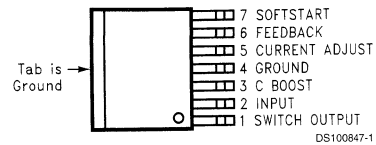
- Simple to design, high efficiency (>90%) step-down switching regulators
- Efficient system pre-regulator for linear voltage regulators
- Battery chargers

Typical Application



Connection Diagrams and Ordering Information

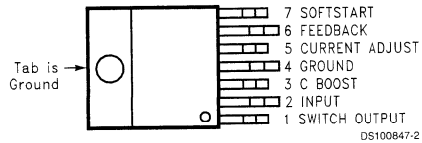
TO-263 Package
Top View



DS100847-1

Order Number
LM2679S-3.3, LM2679S-5.0,
LM2679S-12 or LM2679S-ADJ
See NSC Package Number TS7B

TO-220 Package
Top View



DS100847-2

Order Number
LM2679T-3.3, LM2679T-5.0,
LM2679T-12 or LM2679T-ADJ
See NSC Package Number TA07B

National Semiconductor

LM2698
SIMPLE SWITCHER® 1.35A Boost Regulator

General Description

The LM2698 is a general purpose PWM boost converter. The 1.9A, 18V, 0.2ohm internal switch enables the LM2698 to provide efficient power conversion to outputs ranging from 2.2V to 17V. It can operate with input voltages as low as 2.2V and as high as 12V. Current-mode architecture provides superior line and load regulation and simple frequency compensation over the device's 2.2V to 12V input voltage range. The LM2698 sets the standard in power density and is capable of supplying 12V at 400mA from a 5V input. The LM2698 can also be used in flyback or SEPIC topologies.

The LM2698 SIMPLE SWITCHER® features a pin selectable switching frequency of either 600kHz or 1.25MHz. This promotes flexibility in component selection and filtering techniques. A shutdown pin is available to suspend the device and decrease the quiescent current to 5µA. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. Switchers Made Simple® software is available to insure a quick, easy and guaranteed design. The LM2698 is available in a low profile 8-lead MSOP package.

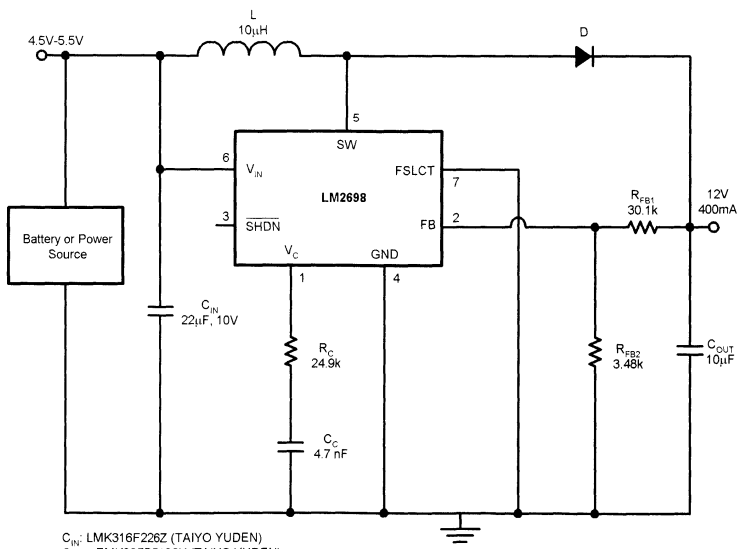
Features

- 1.9A, 0.2Ω, internal switch (typical)
- Operating voltage as low as 2.2V
- 600kHz/1.25MHz adjustable frequency operation
- Switchers Made Simple® software
- 8-Lead MSOP package

Applications

- 3.3V to 5V, 5V to 12V conversion
- Distributed Power
- Set-Top Boxes
- DSL Modems
- Diagnostic Medical Instrumentation
- Boost Converters
- Flyback Converters
- SEPIC Converters

Typical Application Circuit

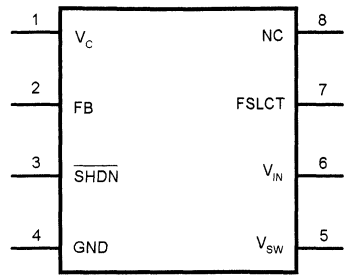


C_{IN}: LMK316F226Z (TAIYO YUDEN)
C_{OUT}: EMK325B5106K (TAIYO YUDEN)
L: DO3316-103 (COILCRAFT)
D: 0MQ040N (MOTOROLA)

20012658

Connection Diagram

Top View



20012604

8-Lead Plastic MSOP
NS Package Number MUA08A

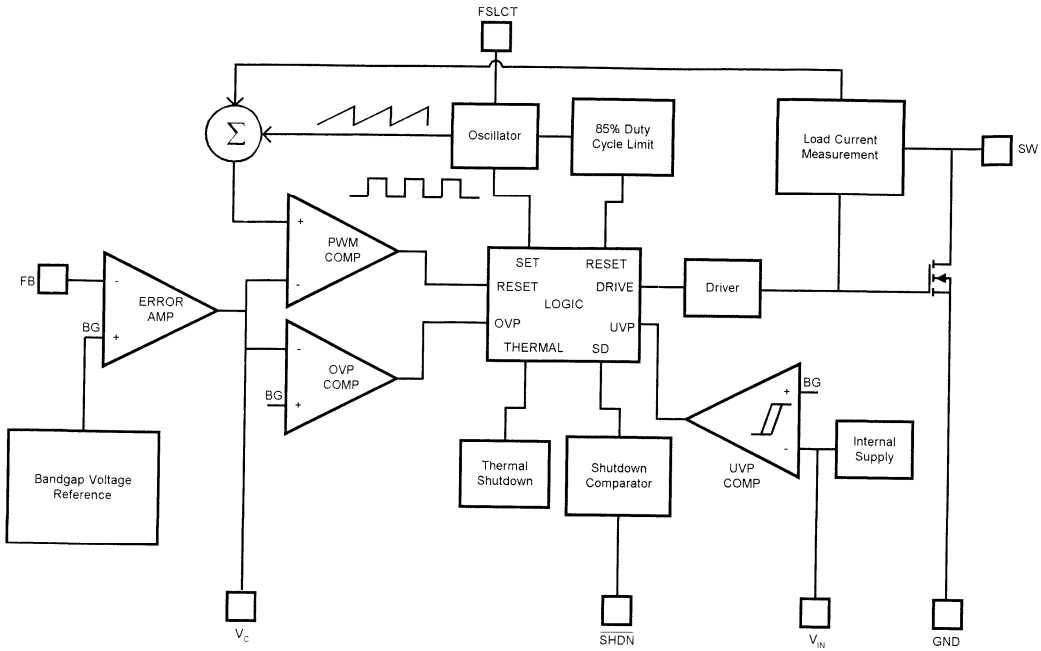
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As	Package ID
LM2698MM-ADJ	MSOP-8	MUA08A	1000 Units, Tape and Reel	S22B
LM2698MMX-ADJ	MSOP-8	MUA08A	3500 Units, Tape and Reel	S22B

Pin Description

Pin	Name	Function
1	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	Output voltage feedback input.
3	$\overline{SHDN}$	Shutdown control input, active low.
4	GND	Analog and power ground.
5	V_{SW}	Power switch input. Switch connected between SW pin and GND pin.
6	V_{IN}	Analog power input.
7	FSLCT	Switching frequency select input. V_{IN}= 1.25MHz. Ground = 600kHz.
8	NC	Connect to ground.

Block Diagram



20012603

National Semiconductor

LM2700
600kHz/1.25MHz, 2.5A, Step-up PWM DC/DC Converter

General Description

The LM2700 is a step-up DC/DC converter with a 3.6A, 80mΩ internal switch and pin selectable operating frequency. With the ability to produce 500mA at 8V from a single Lithium Ion battery, the LM2700 is an ideal part for biasing LCD displays. The LM2700 can be operated at switching frequencies of 600kHz and 1.25MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM2700 features continuous switching at light loads and operates with a switching quiescent current of 2.0mA at 600kHz and 3.0mA at 1.25MHz. The LM2700 is available in a low profile 14-lead TSSOP package or a 14-lead LLP package.

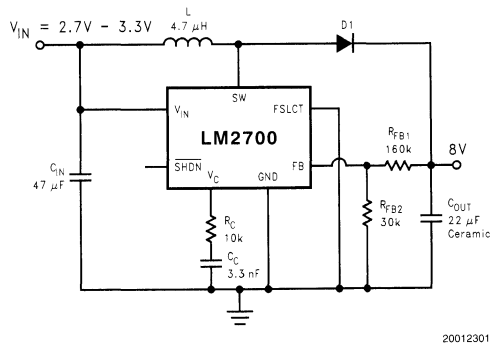
Features

- 3.6A, 0.08Ω, internal switch
- Operating input voltage range of 2.2V to 12V
- Input undervoltage protection
- Adjustable output voltage up to 17.5V
- 600kHz/1.25MHz pin selectable frequency operation
- Over temperature protection
- Small 14-Lead TSSOP or LLP package

Applications

- LCD Bias Supplies
- Handheld Devices
- Portable Applications
- GSM/CDMA Phones
- Digital Cameras

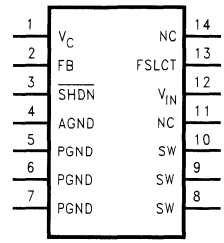
Typical Application Circuit



600 kHz Operation

Connection Diagram

Top View



20012304

14-Lead TSSOP or LLP

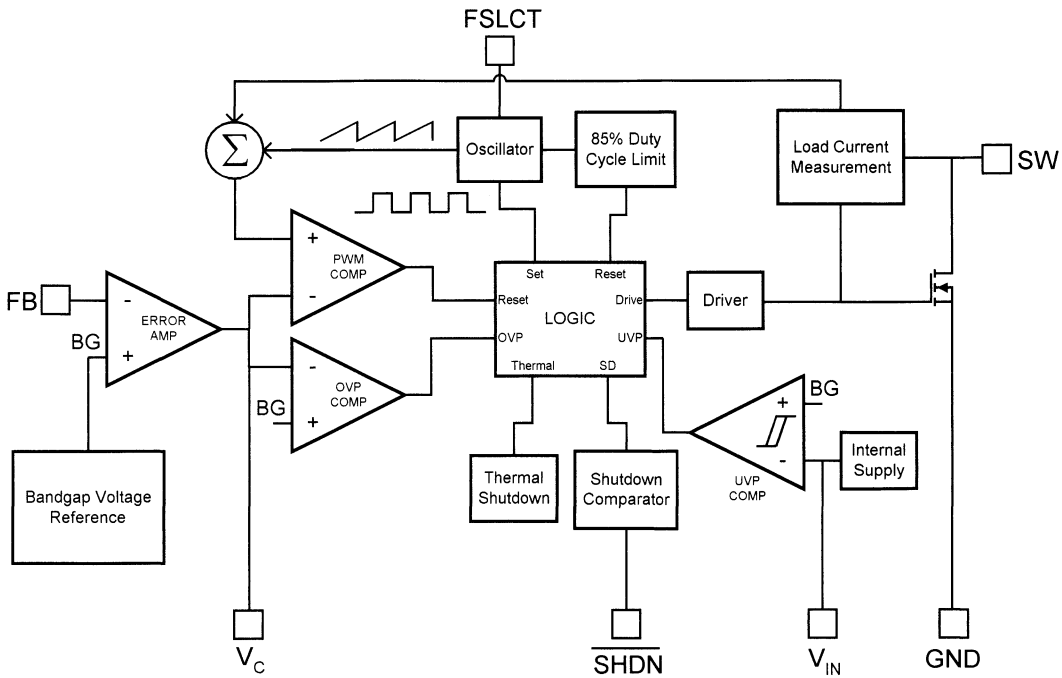
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2700MT-ADJ	TSSOP-14	MTC14	94 Units, Rail
LM2700MTX-ADJ	TSSOP-14	MTC14	2500 Units, Tape and Reel
LM2700LD-ADJ	LLP-14	LDA14A	1000 Units, Tape and Reel
LM2700LDX-ADJ	LLP-14	LDA14A	4500 Units, Tape and Reel

Pin Description

Pin	Name	Function
1	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	Output voltage feedback input.
3	$\overline{SHDN}$	Shutdown control input, active low.
4	AGND	Analog ground.
5	PGND	Power ground. PGND pins must be connected together directly at the part.
6	PGND	Power ground. PGND pins must be connected together directly at the part.
7	PGND	Power ground. PGND pins must be connected together directly at the part.
8	SW	Power switch input. Switch connected between SW pins and PGND pins.
9	SW	Power switch input. Switch connected between SW pins and PGND pins.
10	SW	Power switch input. Switch connected between SW pins and PGND pins.
11	NC	Pin not connected internally.
12	V_{IN}	Analog power input.
13	FSLCT	Switching frequency select input. V_{IN} = 1.25MHz. Ground = 600kHz.
14	NC	Connect to ground.

Block Diagram



20012303

Detailed Description

The LM2700 utilizes a PWM control scheme to regulate the output voltage over all load conditions. The operation can best be understood referring to the block diagram and *Figure 1* of the *Operation* section. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device conducting current through the inductor, cycle 1 of *Figure 1* (a). During this cycle, the voltage at the V_C pin controls the peak inductor current. The V_C voltage will increase with larger loads and decrease with smaller. This voltage is compared with the summation of the SW voltage and the ramp compensation. The ramp compensation is used in PWM architectures to eliminate the sub-harmonic oscillations that occur during duty cycles greater than 50%. Once the summation of the ramp compensation and switch voltage equals the V_C voltage, the PWM comparator resets the driver logic turning off the NMOS power device. The inductor current then flows through the schottky diode to the load and output capacitor, cycle 2 of *Figure 1* (b). The NMOS power device is then set by the oscillator at the end of the period and current flows through the inductor once again.

The LM2700 has dedicated protection circuitry running during normal operation to protect the IC. The Thermal Shutdown circuitry turns off the NMOS power device when the die temperature reaches excessive levels. The UVP comparator protects the NMOS power device during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM2700 also features a shutdown mode decreasing the supply current to 5µA.

National Semiconductor

LM2720
5-Bit Programmable, High Frequency Multi-phase PWM Controller

General Description

The LM2720 provides an attractive solution for power supplies of high power microprocessors exhibiting ultra fast load transients. Compared to a conventional single-phase supply, an LM2720 based multi-phase supply distributes the thermal and electrical loading among components in multiple phases and greatly reduces the corresponding stress in each component. The LM2720 can be programmed to control either a 3-phase converter or a 4-phase converter. Phase shift among the phases is 120° in the case of three phase and 90° with four-phase. Because the power channels are out of phase, there can be significant ripple cancellation for both the input and output current, resulting in reduced input and output capacitor size. Due to the nominal operating frequency of 2 MHz per phase, the size of the output inductors can be greatly reduced which results in a much faster load transient response and a dramatically shrunk output capacitor bank. Microprocessor power supplies with all surface mount components can be easily built.

The internal high speed transconductance amplifier guarantees good dynamic performance.

The internal master clock frequency of up to 8 MHz is set by an external reference resistor. An external clock of 10 MHz can also be used to drive the chip to achieve frequency control and multi-chip operation.

The LM2720 also provides input under-voltage lock-out with hysteresis, input over-current protection and output voltage power good detection.

Features

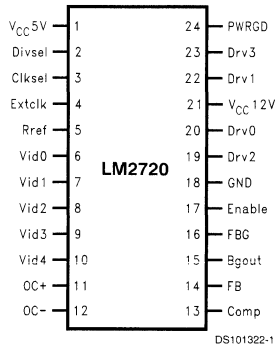
- Ultra fast load transient response
- Enables all surface-mount-design
- Selectable 2, 3, 4 phase operation
- Clock frequency from 40 kHz to 10 MHz
- Precision load current sharing
- 5-bit programmable from 3.5V to 1.3V
- VID code compatible to VRM 8.X specification
- Output voltage is 2.0V for VID code 11111
- Selectable internal or external clock
- Digital 16-step soft start
- Input under-voltage lock-out, over-current protection
- Open-drain power good signal output

Applications

- Servers and workstations
- High current, ultra-fast transient microprocessors

Pin Configuration

24-Pin Plastic SOIC



Top View
See NS Package Number M24B

National Semiconductor

LM2825
Integrated Power Supply 1A DC-DC Converter

General Description

The LM2825 is a complete 1A DC-DC Buck converter packaged in a 24-lead molded Dual-In-Line integrated circuit package.

Contained within the package are all the active and passive components for a high efficiency step-down (buck) switching regulator. Available in fixed output voltages of 3.3V, 5V and 12V, as well as two adjustable versions, these devices can provide up to 1A of load current with fully guaranteed electrical specifications.

Self-contained, this converter is also fully protected from output fault conditions, such as excessive load current, short circuits, or excessive temperatures.

Highlights

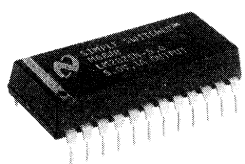
- No external components required (fixed output voltage versions)
- Integrated circuit reliability
- MTBF over 20 million hours
- Radiated EMI meets Class B stipulated by CISPR 22
- High power density, 35 W/in^3
- 24-pin DIP package profile (1.25 x 0.54 x 0.26 inches)

Features

- Minimum design time required
- 3.3V, 5V and 12V fixed output versions
- Two adjustable versions allow 1.23V to 15V outputs
- Wide input voltage range, up to 40V
- Low-power standby mode, I_Q typically 65 µA
- High efficiency, typically 80%
- ±4% output voltage tolerance
- Excellent line and load regulation
- TTL shutdown capability/programmable Soft-start
- Thermal shutdown and current limit protection
- −40˚C to +85˚C ambient temperature range

Applications

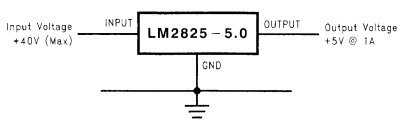
- Simple high-efficiency step-down (buck) regulator
- On-card switching regulators
- Efficient pre-regulator for linear regulators
- Distributed power systems
- DC/DC module replacement



DS012661-27

Standard Application

(Fixed output voltage versions)



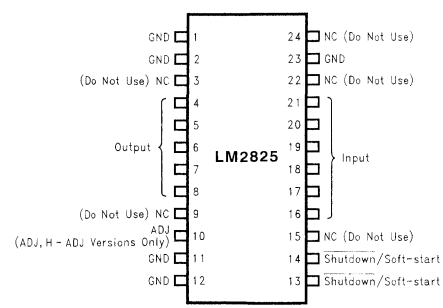
DS012661-1

Radiated EMI

Radiated emission of electromagnetic fields is measured at 10m distance. The emission levels are within the Class B limits stipulated by CISPR 22.

30. . . .230 MHz	30 dB µV/m
230. . . .1000 MHz	37 dB µV/m
1. . . .10 GHz	46 dB µV/m

Connection Diagram



DS012661-2

"NC (Do not use)" pins: See *Figure 11.*

Top View

Ordering Information

Order Number LM2825N-3.3, LM2825N-5.0, LM2825N-12, LM2825N-ADJ or LM2825HN-ADJ

See NS Package Number NA24F

17

National Semiconductor

LM3477
High Efficiency High-Side N-Channel Controller for Switching Regulator

General Description

The LM3477 is a versatile High-Side N-FET switching regulator controller. It is suitable for use in topologies requiring a high side FET, such as buck regulator and inverting regulator. The LM3477 operates at a high switching frequency of 500kHz in order to reduce the overall solution size. Using an optimized current mode control loop, LM3477 provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor. LM3477 provides high efficiency under light conditions. Light load efficiency is improved by using hysteretic mode of operation.

The LM3477 has built in features such as thermal shutdown, internal soft-start, short-circuit protection, over voltage protection, etc. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

Key Specifications

- **Wide supply voltage range of 2.95V to 35V**
- 500kHz internal clock frequency
- ±1.5% (over temperature) internal reference
- 8µA shutdown current (Over temperature)

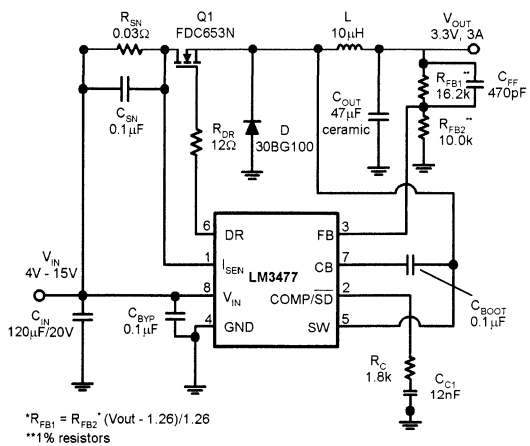
Features

- 8-lead Mini-SO8 (MSOP-8) package
- Internal push-pull driver with 1A peak current capability
- Low current hysteretic mode improves light load efficiency.
- Current limit and thermal shutdown
- Frequency compensation optimized with a capacitor and a resistor
- Internal softstart
- Current mode operation
- Undervoltage lockout with hysteresis

Applications

- Distributed Power Systems
- Switching regulator topologies such as buck regulator and inverting regulators
- Battery Chargers
- Telecom Power Supplies
- Automotive Power Systems

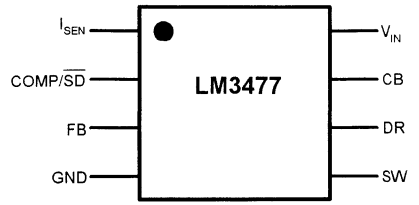
Typical Application Circuit



20003333

Typical High Efficiency Step-Down (Buck) Converter

Connection Diagram



8 Lead Mini SO8 Package (MSOP-8 Package)

Package Marking and Ordering Information

Order Number	Package Type	Package Marking	Supplied As:
LM3477MM	MSOP-8	S13B	1000 units on Tape and Reel
LM3477MMX	MSOP-8	S13B	3500 units on Tape and Reel

Pin Description

Pin Name	Pin Number	Description
I_{SEN}	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
COMP	2	Compensation pin. A resistor-capacitor combination connected to this pin provides compensation for the control loop.
FB	3	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.265V at this pin.
GND	4	Ground pin.
SW	5	Switch Node. Source of the external MOSFET is connected to this node.
DR	6	Drive pin. The gate of the external MOSFET should be connected to this pin.
CB	7	Boot-strap pin. A capacitor must be connected between this pin and SW pin (pin 5) for proper operation. The voltage developed across this capacitor provides the gate drive for the external MOSFET.
V_{IN}	8	Power Supply Input pin.

National Semiconductor

LM3478
High Efficiency Low-Side N-Channel Controller for Switching Regulator

General Description

The LM3478 is a versatile Low-Side N-FET switching regulator controller. It is suitable for use in topologies requiring low side FET, such as boost, flyback, SEPIC, etc. Moreover, the LM3478 can be operated at extremely high switching frequency in order to reduce the overall solution size. The switching frequency of LM3478 can be adjusted to any value between 100kHz and 1MHz by using a single external resistor. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor.

The LM3478 has built in features such as thermal shutdown, short-circuit protection, over voltage protection, etc. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

Key Specifications

- **Wide supply voltage range of 2.95V to 40V**
- 100kHz to 1MHz Adjustable clock frequency
- ±2.5% (over temperature) internal reference
- 10µA shutdown current (over temperature)

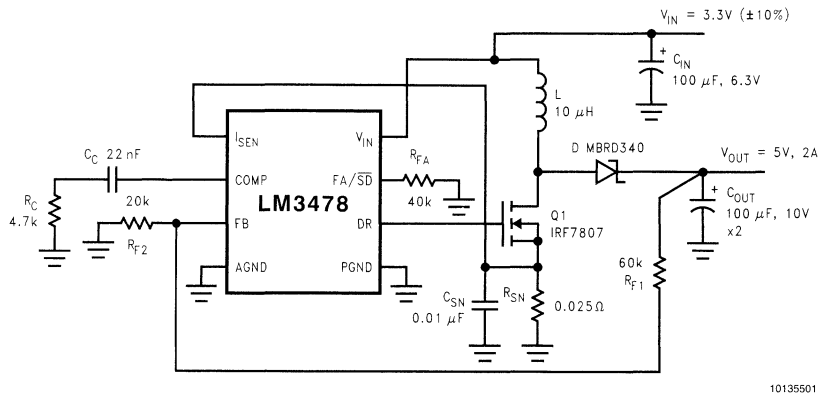
Features

- 8-lead Mini-SO8 (MSOP-8) package
- Internal push-pull driver with 1A peak current capability
- Current limit and thermal shutdown
- Frequency compensation optimized with a capacitor and a resistor
- Internal softstart
- Current Mode Operation
- Undervoltage Lockout with hysteresis

Applications

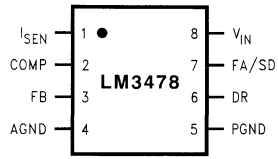
- Distributed Power Systems
- Battery Chargers
- Offline Power Supplies
- Telecom Power Supplies
- Automotive Power Systems

Typical Application Circuit



Typical High Efficiency Step-Up (Boost) Converter

Connection Diagram



10135502

8 Lead Mini SO8 Package (MSOP-8 Package)

Package Marking and Ordering Information

Order Number	Package Type	Package Marking	Supplied As:
LM3478MM	MSOP-8	S14B	1000 units on Tape and Reel
LM3478MMX	MSOP-8	S14B	3500 units on Tape and Reel

Pin Description

Pin Name	Pin Number	Description
I_{SEN}	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
COMP	2	Compensation pin. A resistor, capacitor combination connected to this pin provides compensation for the control loop.
FB	3	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.26V at this pin.
AGND	4	Analog ground pin.
PGND	5	Power ground pin.
DR	6	Drive pin of the IC. The gate of the external MOSFET should be connected to this pin.
FA/SD	7	Frequency adjust and Shutdown pin. A resistor connected to this pin sets the oscillator frequency. A high level on this pin for ≥ 30µs will turn the device off. The device will then draw less than 10µA from the supply.
V_{IN}	8	Power Supply Input pin.

National Semiconductor

LM3488
High Efficiency Low-Side N-Channel Controller for Switching Regulators

General Description

The LM3488 is a versatile Low-Side N-FET high performance controller for switching regulators. It is suitable for use in topologies requiring low side FET, such as boost, flyback, SEPIC, etc. Moreover, the LM3488 can be operated at extremely high switching frequency in order to reduce the overall solution size. The switching frequency of LM3488 can be adjusted to any value between 100kHz and 1MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response, besides cycle-by-cycle current limiting. Output current can be programmed with a single external resistor.

The LM3488 has built in features such as thermal shutdown, short-circuit protection and over voltage protection. Power saving shutdown mode reduces the total supply current to 5µA and allows power supply sequencing. Internal soft-start limits the inrush current at start-up.

Key Specifications

- **Wide supply voltage range of 2.95V to 40V**
- 100kHz to 1MHz Adjustable and Synchronizable clock frequency
- ±1.5% (over temperature) internal reference
- 5µA shutdown current (over temperature)

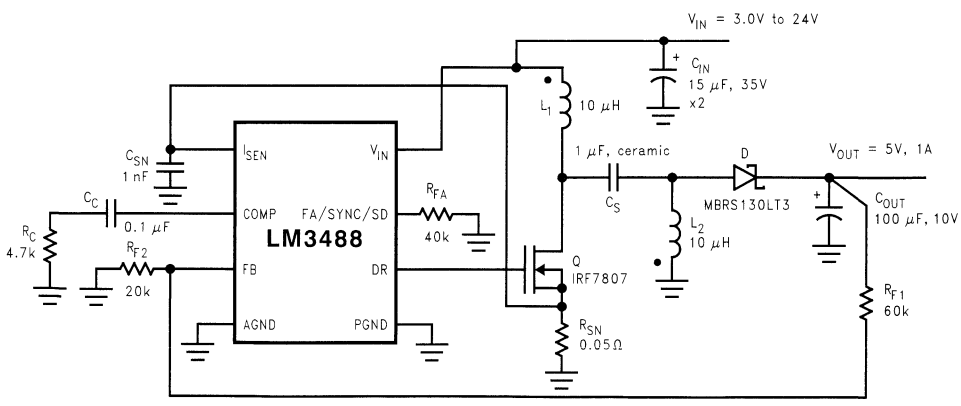
Features

- 8-lead Mini-SO8 (MSOP-8) package
- Internal push-pull driver with 1A peak current capability
- Current limit and thermal shutdown
- Frequency compensation optimized with a capacitor and a resistor
- Internal softstart
- Current Mode Operation
- Undervoltage Lockout with hysteresis

Applications

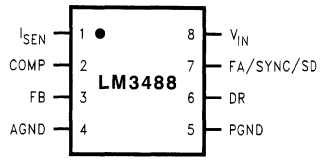
- Distributed Power Systems
- Notebook, PDA, Digital Camera, and other Portable Applications
- Offline Power Supplies
- Set-Top Boxes

Typical Application Circuit



Typical SEPIC Converter

Connection Diagram



10138802

8 Lead Mini SO8 Package (MSOP-8 Package)

Package Marking and Ordering Information

Order Number	Package Type	Package Marking	Supplied As:
LM3488MM	MSOP-8	S21B	1000 units on Tape and Reel
LM3488MMX	MSOP-8	S21B	3500 units on Tape and Reel

Pin Description

Pin Name	Pin Number	Description
I_{SEN}	1	Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.
COMP	2	Compensation pin. A resistor, capacitor combination connected to this pin provides compensation for the control loop.
FB	3	Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.26V at this pin.
AGND	4	Analog ground pin.
PGND	5	Power ground pin.
DR	6	Drive pin of the IC. The gate of the external MOSFET should be connected to this pin.
FA/SYNC/SD	7	Frequency adjust, synchronization, and Shutdown pin. A resistor connected to this pin sets the oscillator frequency. An external clock signal at this pin will synchronize the controller to the frequency of the clock. A high level on this pin for ≥ 30µs will turn the device off. The device will then draw less than 10µA from the supply.
V_{IN}	8	Power supply input pin.

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Related Products

National Semiconductor

LM2725/LM2726
High Speed Synchronous MOSFET Drivers

General Description

The LM2725/LM2726 is a family of dual MOSFET drivers that can drive both the top MOSFET and bottom MOSFET in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in shoot-through protection circuitry prevents the top and bottom FETs from turning on simultaneously. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2725 is about 1.2A and that of the LM2726 is about 3A. In an SO-8 package, each driver is able to handle 50mA average current. Input UVLO (Under-Voltage-Lock-Out) ensures that all the driver outputs stay low until the supply rail exceeds the power-on threshold during system power on, or after the supply rail drops below power-on threshold by a specified hysteresis during system power down. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. The top gate bias voltage needed by the top MOSFET can be obtained through an external bootstrap structure. Minimum pulse width is as low as 55ns.

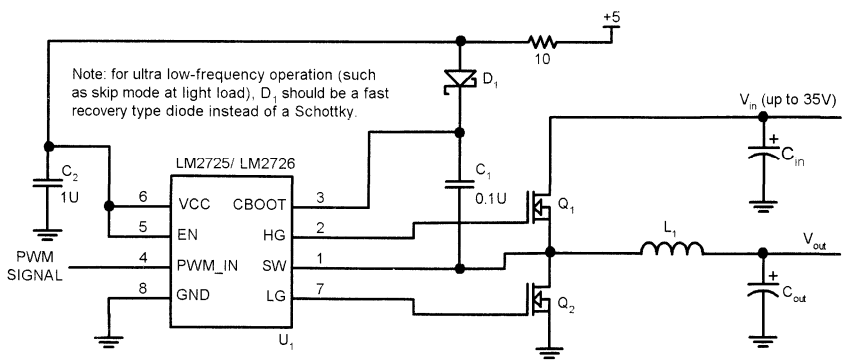
Features

- High peak output current
- Adaptive shoot-through protection
- 36V SW pin absolute maximum voltage
- Input Under-Voltage-Lock-Out
- Typical 20ns internal delay
- Plastic 8-pin SO package

Applications

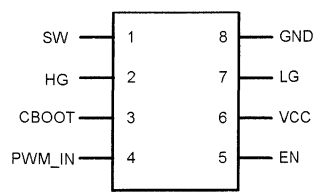
- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Microprocessors

Typical Application



Connection Diagram

8-Lead Small Outline Package



Top View

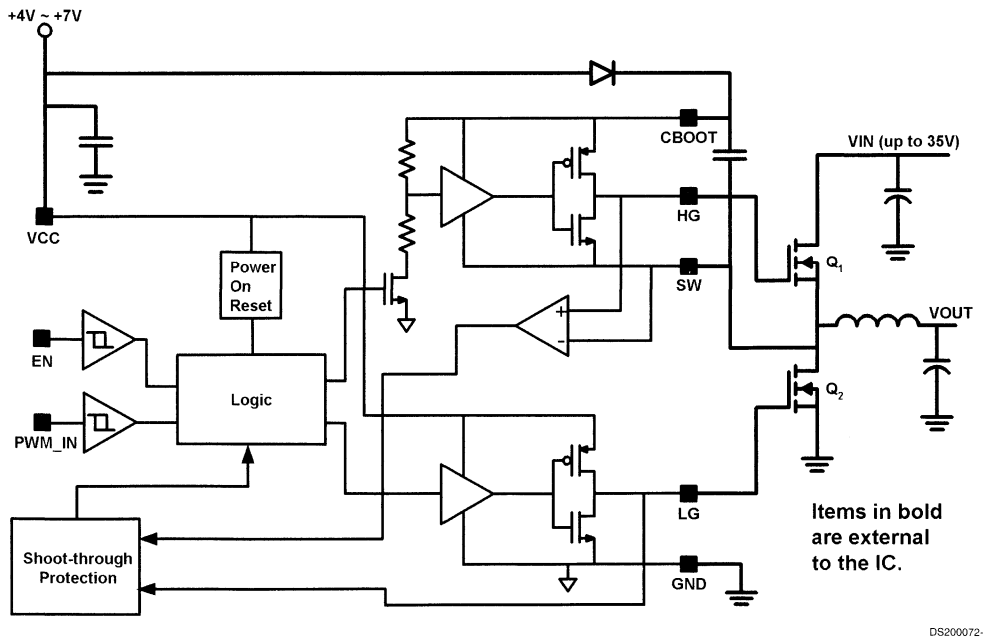
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2725	LM2725M	M08A	95 Units/Rail
	LM2725MX		2500 Units/Reel
LM2726	LM2726M		95 Units/Rail
	LM2726MX		2500 Units/Reel

Pin Description

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	PWM_IN	Accepts a 5V-logic control signal
5	EN	Chip Enable
6	VCC	Connect to +5V supply
7	LG	Bottom gate drive output
8	GND	Ground

Block Diagram



National Semiconductor

LM3411
Precision Secondary Regulator/Driver

General Description

The LM3411 is a low power fixed-voltage (3.3V or 5.0V) precision shunt regulator designed specifically for driving an optoisolator to provide feedback isolation in a switching regulator.

The LM3411 circuitry includes an internally compensated op amp, a bandgap reference, NPN output transistor, and voltage setting resistors.

A trimmed precision bandgap reference with temperature drift curvature correction, provides a guaranteed 1% precision over the operating temperature range (A grade version). The amplifier's inverting input is externally accessible for loop frequency compensation when used as part of a larger servo system. The output is an open-emitter NPN transistor capable of driving up to 15 mA of load current.

Because of its small die size, the LM3411 has been made available in the sub-miniature 5-lead SOT23-5 surface mount package. This package is ideal for use in space critical applications.

Although its main application is to provide a precision output voltage (no trimming required) and maintain very good regulation in isolated DC/DC converters, it can also be used with other types of voltage regulators or power semiconductors to provide a precision output voltage without precision resistors or trimming.

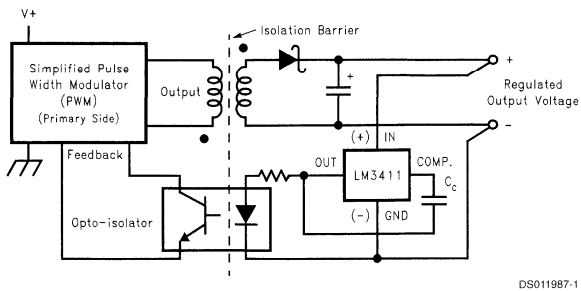
Features

- Fixed voltages of 3.3V and 5.0V with initial tolerance of ±1% for standard grade and ±0.5% for A grade
- Custom voltages available (3V–17V)
- Wide output current range, 20 µA–15 mA
- Low temperature coefficient
- Available in 5-lead SOT23-5 surface mount package (tape and reel)

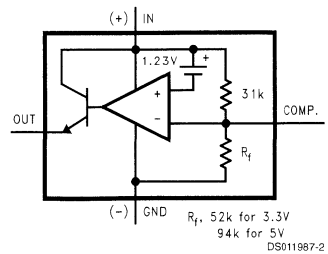
Applications

- Secondary controller for isolated DC/DC PWM switching regulators systems
- Use with LDO regulator for high-precision fixed output regulators
- Precision monitoring applications
- Use with many types of regulators to increase precision and improve performance

Typical Application and Functional Diagram



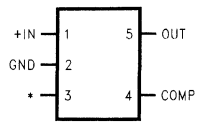
Basic Isolated DC/DC Converter



LM3411 Functional Diagram

Connection Diagrams and Order Information

5-Lead Small Outline Package (M5)



DS011987-3

*No internal connection, but should be soldered to PC board for best heat transfer.

Top View

Actual Size

DS011987-4

For Ordering Information
See *Figure 1* in this Data Sheet
See NS Package Number MF05A

Five Lead Surface Mount Package Marking and Order Information (SOT23-5)

The small SOT23-5 package allows only 4 alphanumeric characters to identify the product. The table below contains the field information marked on the package.

	Grade	Order Information	Package Marking	Supplied as
3.3V	A (Prime)	LM3411AM5-3.3	D00A	1000 unit increments on tape and reel
3.3V	A (Prime)	LM3411AM5X-3.3	D00A	3000 unit increments on tape and reel
3.3V	B (Standard)	LM3411M5-3.3	D00B	1000 unit increments on tape and reel
3.3V	B (Standard)	LM3411M5X-3.3	D00B	3000 unit increments on tape and reel
5.0V	A (Prime)	LM3411AM5-5.0	D01A	1000 unit increments on tape and reel
5.0V	A (Prime)	LM3411AM5X-5.0	D01A	3000 unit increments on tape and reel
5.0V	B (Standard)	LM3411M5-5.0	D01B	1000 unit increments on tape and reel
5.0V	B (Standard)	LM3411M5X-5.0	D01B	3000 unit increments on tape and reel

FIGURE 1. SOT23-5 Marking and Order Information

The first letter "D" identifies the part as a Driver, the next two numbers indicate the voltage, "00" for 3.3V part and "01" for a 5V part. The fourth letter indicates the grade, "B" for standard grade, "A" for the prime grade.

The SOT23-5 surface mount package is only available on tape in quantities increments of 250 on tape and reel (indicated by the letters "M5" in the part number), or in quantities increments of 3000 on tape and reel (indicated by the letters "M5X" in the part number).

National Semiconductor

LM2722
High Speed Synchronous/Asynchronous MOSFET Driver

General Description

The LM2722, part of the LM2726 family, is designed to be used with multi-phase controllers. This part differs from the LM2726 by changing the functionality of the SYNC_EN pin from a whole chip enable to a low side MOSFET enable. As a result, the SYNC_EN pin now provides control between Synchronous and Asynchronous operations. Having this control can be advantageous in portable systems since Asynchronous operations can be more efficient at very light loads.

The LM2722 drives both top and bottom MOSFETs in a push-pull structure simultaneously. It takes a logic level PWM input and splits it into two complimentary signals with a typical 20ns dead time in between. The built-in cross-conduction protection circuitry prevents the top and bottom FETs from turning on simultaneously. The cross-conduction protection circuitry detects both the driver outputs and will not turn on a driver until the other driver output is low. With a bias voltage of 5V, the peak sourcing and sinking current for each driver of the LM2722 is typically 3A. In an SO-8 package, each driver is able to handle 50mA average current. Input UVLO (Under-Voltage-Lock-Out) forces both driver outputs low to ensure proper power-up and power-down operation. The gate drive bias voltage needed by the high side MOSFET is obtained through an external bootstrap. Minimum pulse width is as low as 55ns.

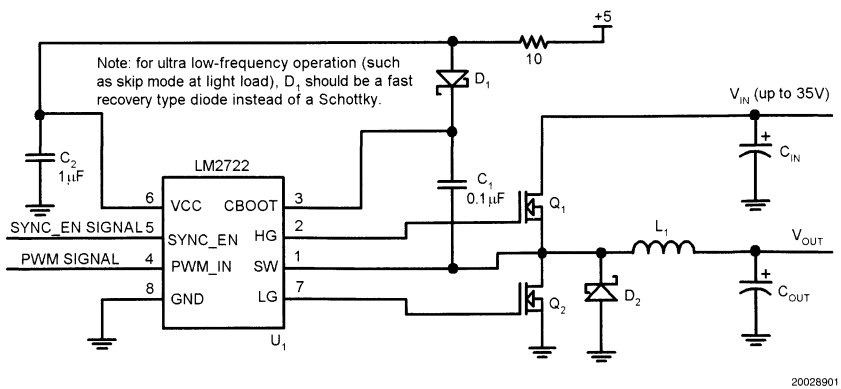
Features

- Synchronous or Asynchronous Operation
- Adaptive shoot-through protection
- Input Under-Voltage-Lock-Out
- Typical 20ns internal delay
- Plastic 8-pin SO package

Applications

- Driver for LM2723 Intel Mobile Northwood CPU core power supply.
- High Current DC/DC Power Supplies
- High Input Voltage Switching Regulators
- Fast Transient Microprocessors

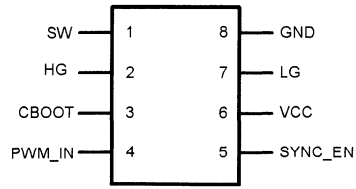
Typical Application



Note: National is an Intel Mobile Voltage Positioning (IMVP) licensee.

Connection Diagram

8-Lead Small Outline Package



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Top View

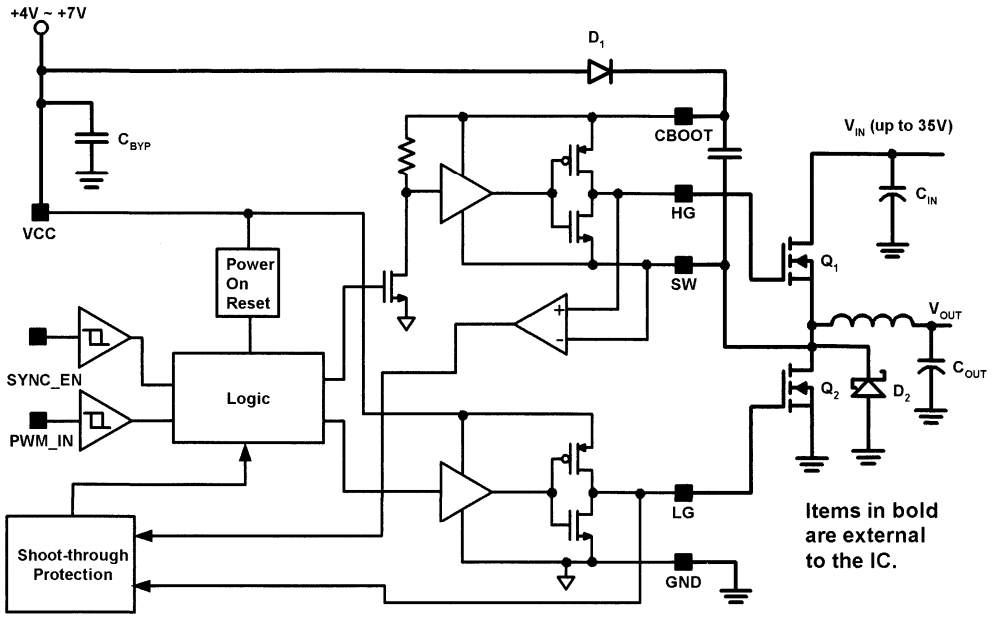
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2722	LM2722M	M08A	95 Units/Rail
	LM2722MX		2500 Units/Reel

Pin Description

Pin	Name	Function
1	SW	Top driver return. Should be connected to the common node of top and bottom FETs
2	HG	Top gate drive output
3	CBOOT	Bootstrap. Accepts a bootstrap voltage for powering the high-side driver
4	PWM_IN	Accepts a 5V-logic control signal
5	SYNC_EN	Low gate Enable
6	VCC	Connect to +5V supply
7	LG	Bottom gate drive output
8	GND	Ground

Block Diagram



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Section 18

Voltage Regulators and Converters - Switched Capacitor

Section 18 Contents

National Semiconductor

Switched Capacitor Converter Selection Guide

Part Number	Function	Output Impedance (ohms)	Output Current (mA)	Input Range (V) (Note 1)	Oscillator Frequency (kHz)	Package (Note 2)
DOUBLER/SPLITTER						
LM2660	2 (V_{IN}) or ½ (V_{IN})	6.5	100	1.5 to 5.5	10/80	MSOP-8/SO-8
LM2661	2 (V_{IN}) or ½ (V_{IN})	6.5	100	1.5 to 5.5	80	MSOP-8/SO-8
LM2662	2 (V_{IN}) or ½ (V_{IN})	3.5	200	1.5 to 5.5	20/150	SO-8
LM2663	2 (V_{IN}) or ½ (V_{IN})	3.5	200	1.5 to 5.5	150	SO-8
LM2665	2 (V_{IN}) or ½ (V_{IN})	12	40	1.8 to 5.5	160	SOT23-6
LM2681	2 (V_{IN}) or ½ (V_{IN})	15	20	2.5 to 5.5	160	SOT23-6
LM2682	2 (V_{IN}) or ½ (V_{IN})	90	10	2.0 to 5.5	6	MSOP-8/SO-8
LM2685	2 (V_{IN}) or ½ (V_{IN})	20	50	2.85 to 6.5	130	TSSOP-14
LM2686	2 (V_{IN}) or ½ (V_{IN})	5.0	50	2.85 to 6.5	130	TSSOP-14
LM2765	2 (V_{IN}) or ½ (V_{IN})	20	20	1.8 to 5.5	50	SOT23-6
LM2766	2 (V_{IN}) or ½ (V_{IN})	20	20	1.8 to 5.5	200	SOT23-6
LM2767	2 (V_{IN}) or ½ (V_{IN})	20	15	1.8 to 5.5	11	SOT23-5
LM2792	Double (2X) White LED Driver		32	3.0 to 5.8	900 (min)	LLP-10
LMC7660	2 (V_{IN}) or ½ (V_{IN})	55	20	1.5 to 10	10	SO-8 / N-8
MAX660	2 (V_{IN}) or ½ (V_{IN})	6.5	100	1.5 to 5.5	10/80	MSOP-8/SO-8
FRACTIONAL						
LM3350	3/2 (V_{IN}) or 2/3 (V_{IN})	4.2/1.8	50	1.5 to 5.5	1600	MSOP-8
LM3351	3/2 (V_{IN}) or 2/3 (V_{IN})	4.2/1.8	50	1.5 to 5.5	400	MSOP-8
LM3352	Regulated Output, 2.5V, 3.0V, or 3.3V	n/a	200	2.5 to 5.5	1000	TSSOP-16
BUCK-BOOST						
LM2787					520	micro SMD
LM3354	1.8V, 3.3V, 4.1V		70	2.5 to 5.5	900	MSOP-10
LM3355	1.8V, 3.3V, 4.1V		50	2.5 to 5.5	900	MSOP-10
INVERTER						
LM2660	$-(V_{IN})$	6.5	100	1.5 to 5.5	10/80	MSOP-8/SO-8
LM2661	$-(V_{IN})$	6.5	100	1.5 to 5.5	80	MSOP-8/SO-8
LM2662	$-(V_{IN})$	3.5	200	1.5 to 5.5	20/150	MSOP-8/SO-8
LM2663	$-(V_{IN})$	3.5	200	1.5 to 5.5	150	SO-8
LM2664	$-(V_{IN})$	12	40	1.8 to 5.5	160	SOT23-6
LM2682	$-(V_{IN})$	90	10	2.0 to 5.5	6	MSOP-8/SO-8
LM2685	$-(V_{IN}$	20	50	2.85 to 6.5	130	TSSOP-14
LM2686	$-(V_{IN})$	5.0	50	2.85 to 6.5	130	TSSOP-14
LM2687	$-(V_{IN})$	30	10	2.7 to 5.5	100	MSOP-8
LM828	$-(V_{IN})$	20	25	1.8 to 5.5	12	SOT23-5
LMC7660	$-(V_{IN})$	55	20	1.5 to 10	10	SO-8 / N-8
MAX660	$-(V_{IN})$	6.5	100	1.5 to 5.5	10/80	MSOP-8/SO-8

Note 1: For voltage splitting function, the applied input voltage can be up to twice the specified Input Range.

Note 2: Package designation includes the number of pins.

National Semiconductor

LM2660/LM2661
Switched Capacitor Voltage Converter

General Description

The LM2660/LM2661 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5V to 5.5V to the corresponding negative voltage. The LM2660/LM2661 uses two low cost capacitors to provide 100 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the LM2660/LM2661 provides ideal performance for battery powered systems. The LM2660/LM2661 may also be used as a positive voltage doubler.

The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2660/LM2661 with an external clock. For LM2660, a frequency control (FC) pin selects the oscillator frequency of 10 kHz or 80 kHz. For LM2661, an external shutdown (SD) pin replaces the FC pin. The SD pin can be used to disable the device and reduce the quiescent current to 0.5 µA. The oscillator frequency for the LM2661 is 80 kHz.

Features

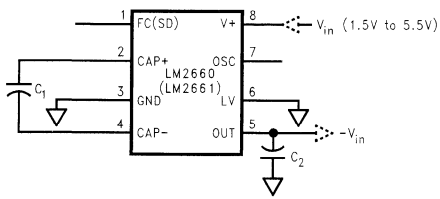
- Inverts or doubles input supply voltage
- Narrow SO-8 and Mini SO-8 Package
- 6.5Ω typical output resistance
- 88% typical conversion efficiency at 100 mA
- (LM2660) selectable oscillator frequency: 10 kHz/80 kHz
- (LM2661) low current shutdown mode

Applications

- Laptop computers
- Cellular phones
- Medical instruments
- Operational amplifier power supplies
- Interface power supplies
- Handheld instruments

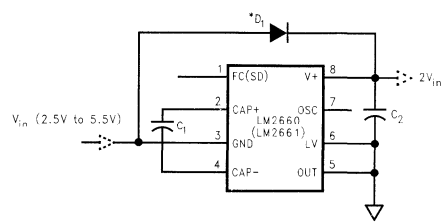
Basic Application Circuits

Voltage Inverter



DS012911-3

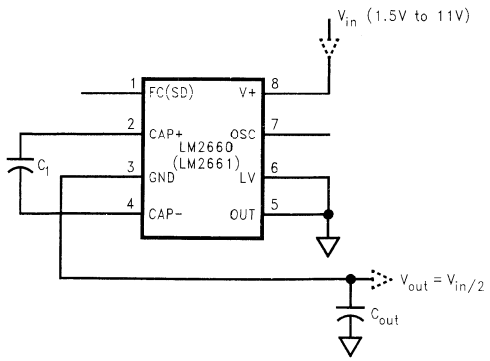
Positive Voltage Doubler



* See Application Information for selecting D_1

DS012911-4

Splitting V_{IN} in Half



DS012911-26

National Semiconductor

LM2662/LM2663
Switched Capacitor Voltage Converter

General Description

The LM2662/LM2663 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5V to 5.5V to the corresponding negative voltage. The LM2662/LM2663 uses two low cost capacitors to provide 200 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 300 µA and operating efficiency greater than 90% at most loads, the LM2662/LM2663 provides ideal performance for battery powered systems. The LM2662/LM2663 may also be used as a positive voltage doubler.

The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the LM2662/LM2663 with an external clock. For LM2662, a frequency control (FC) pin selects the oscillator frequency of 20 kHz or 150 kHz. For LM2663, an external shutdown (SD) pin replaces the FC pin. The SD pin can be used to disable the device and reduce the quiescent current to 10 µA. The oscillator frequency for LM2663 is 150 kHz.

Features

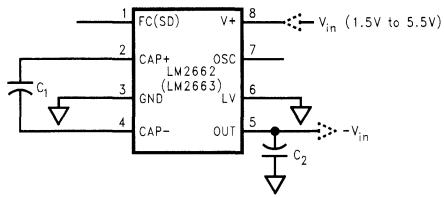
- Inverts or doubles input supply voltage
- Narrow SO-8 Package
- 3.5Ω typical output resistance
- 86% typical conversion efficiency at 200 mA
- (LM2662) selectable oscillator frequency: 20 kHz/150 kHz
- (LM2663) low current shutdown mode

Applications

- Laptop computers
- Cellular phones
- Medical instruments
- Operational amplifier power supplies
- Interface power supplies
- Handheld instruments

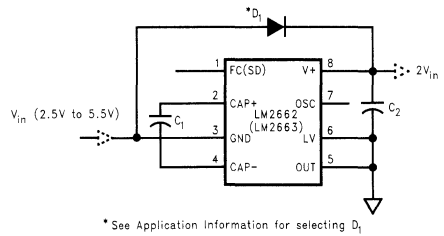
Basic Application Circuits

Voltage Inverter



DS100003-1

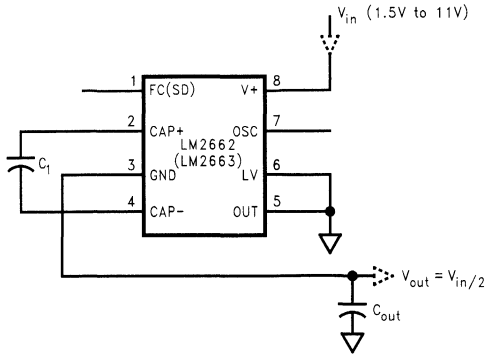
Positive Voltage Doubler



* See Application Information for selecting D_1

DS100003-2

Splitting V_{IN} in Half



DS100003-3

National Semiconductor

LM2664
Switched Capacitor Voltage Converter

General Description

The LM2664 CMOS charge-pump voltage converter inverts a positive voltage in the range of +1.8V to +5.5V to the corresponding negative voltage of −1.8V to −5.5V. The LM2664 uses two low cost capacitors to provide up to 40 mA of output current.

The LM2664 operates at 160 kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 220 µA (operating efficiency greater than 91% with most loads) and 1 µA typical shutdown current, the LM2664 provides ideal performance for battery powered systems. The device is in SOT-23-6 package.

Features

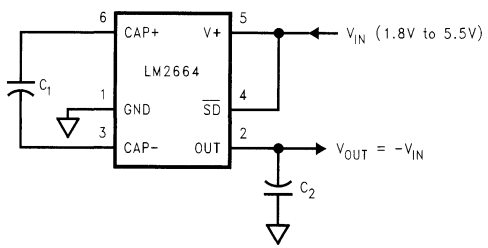
- Inverts Input Supply Voltage
- SOT23-6 Package
- 12Ω Typical Output Impedance
- 91% Typical Conversion Efficiency at 40 mA
- 1µA Typical Shutdown Current

Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

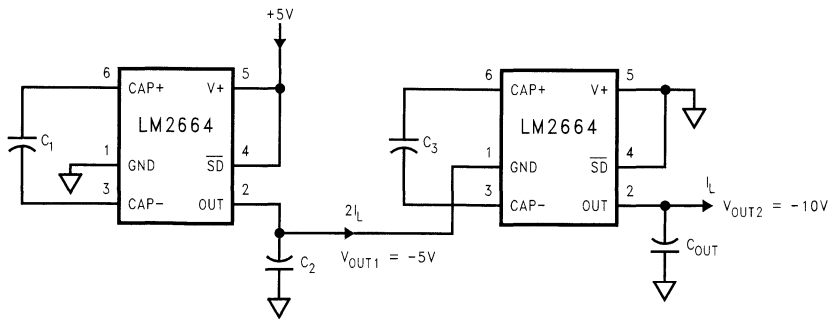
Basic Application Circuits

Voltage Inverter



DS100031-1

+5V to −10V Converter



DS100031-25

National Semiconductor

LM2665
Switched Capacitor Voltage Converter

General Description

The LM2665 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of +2.5V to +5.5V. Two low cost capacitors and a diode (needed during start-up) are used in this circuit to provide up to 40 mA of output current. The LM2665 can also work as a voltage divider to split a voltage in the range of +1.8V to +11V in half.

The LM2665 operates at 160 kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 650 µA (operating efficiency greater than 90% with most loads) and 1µA typical shutdown current, the LM2665 provides ideal performance for battery powered systems. The device is in SOT-23-6 package.

Features

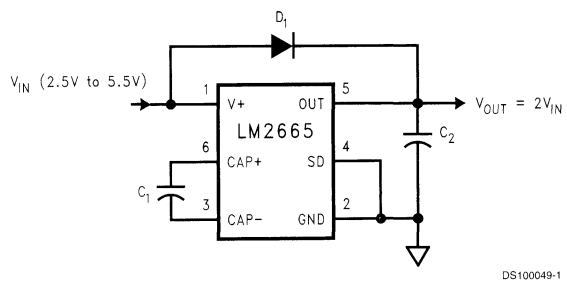
- Doubles or Splits Input Supply Voltage
- SOT23-6 Package
- 12Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 40 mA
- 1µA Typical Shutdown Current

Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

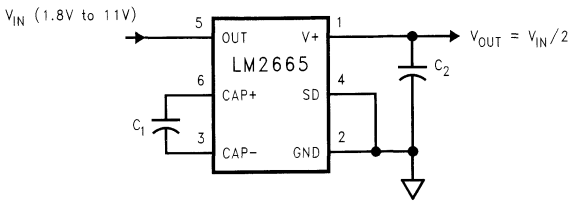
Basic Application Circuits

Voltage Doubler



DS100049-1

Splitting V_{in} in Half



DS100049-2

National Semiconductor

LM2681
Switched Capacitor Voltage Converter

General Description

The LM2681 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of +2.5V to +5.5V. Two low cost capacitors and a diode (needed during start-up) is used in this circuit to provide up to 20 mA of output current. The LM2681 can also work as a voltage divider to split a voltage in the range of +1.8V to +11V in half.

The LM2681 operates at 160 kHz oscillator frequency to reduce output resistance and voltage ripple. With an operating current of only 550 µA (operating efficiency greater than 90% with most loads) the LM2681 provides ideal performance for battery powered systems. The device is in SOT-23-6 package.

Features

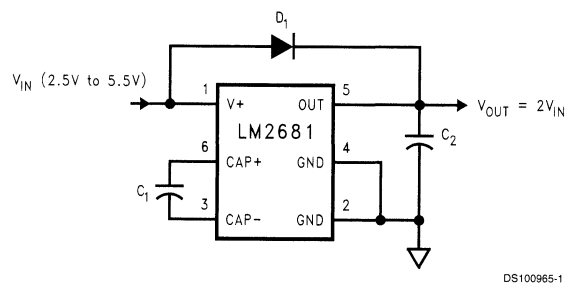
- Doubles or Splits Input Supply Voltage
- SOT23-6 Package
- 15Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 20 mA

Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

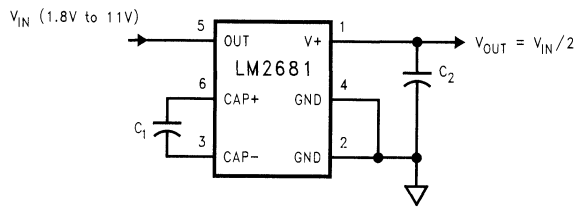
Basic Application Circuits

Voltage Doubler



DS100965-1

Splitting V_{in} in Half



DS100965-2

National Semiconductor

LM2682
Switched Capacitor Voltage Doubling Inverter

General Description

The LM2682 is a CMOS charge-pump voltage inverter capable of converting positive voltage in the range of +2.0V to +5.5V to the corresponding doubled negative voltage of −4.0V to −11.0V respectively. The LM2682 uses three low cost capacitors to provide 10 mA of output current without the cost, size, and EMI related to inductor based circuits. With an operating current of only 150 µA and an operating efficiency greater than 90% with most loads, the LM2682 provides ideal performance for battery powered systems. The LM2682 offers a switching frequency of 6 kHz.

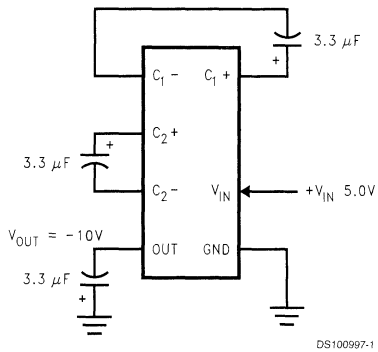
Features

- Inverts then doubles input supply voltage
- Small MSOP-8 package (mini SO-8) and SO-8 package
- 90Ω typical output impedance
- 94% typical power efficiency at 10 mA

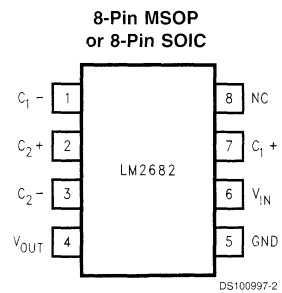
Applications

- LCD contrast biasing
- GaAs power amplifier biasing
- Interface power supplies
- Handheld instrumentation
- Laptop computers and PDAs

Typical Operating Circuit and Pin Configuration



DS100997-1



DS100997-2

Ordering Information

Order Number	Package	Package Number	Package Marking	Supplied As
LM2682MM	MSOP-8	MUA08A	S11A	Tape and Reel (1000 units/reel)
LM2682MMX	MSOP-8	MUA08A	S11A	Tape and Reel (3500 units/reel)
LM2682M	SO-8	M08A	LM2682M	Rail (95 units/rail)
LM2682MX	SO-8	M08A	LM2682M	Tape and Reel (2500 units/reel)

National Semiconductor

LM2685
Dual Output Regulated Switched Capacitor Voltage Converter

General Description

The LM2685 CMOS charge-pump voltage converter operates as an input voltage doubler, +5V regulator and inverter for an input voltage in the range of +2.85V to +6.5V. Five low cost capacitors are used in this circuit to provide up to 50mA of output current at +5V (± 5%), and 15mA at −5V. The LM2685 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 800µA (operating efficiency greater than 80% with most loads) and 6µA typical shutdown current, the LM2685 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

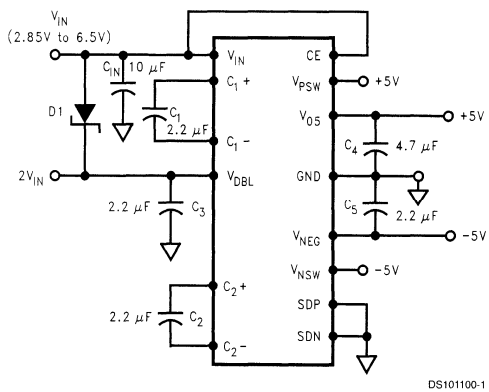
Features

- +5V regulated output
- Inverts V_{O5}(+5V) to V_{NEG}(−5V)
- Doubles input supply voltage
- TSSOP-14 package
- 80% typical conversion efficiency at 25mA
- Input voltage range of 2.85V to 6.5V
- Independent shutdown control pins

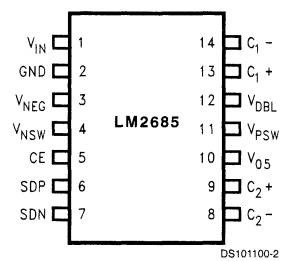
Applications

- Cellular phones
- Pagers
- PDAs
- Handheld instrumentation
- 3.3V to 5V voltage conversion applications

Typical Application and Connection Diagram



DS101100-1



DS101100-2

14-Pin TSSOP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2685MTC	TSSOP-14	MTC14	94 Units, Rail
LM2685MTCX	TSSOP-14	MTC14	2.5k Units, Tape and Reel

Pin Description

Pin No.	Name	Function
1	V_{IN}	Power supply input voltage.
2	GND	Power supply ground.
3	V_{NEG}	Negative output voltage created by inverting V_{05}.
4	V_{NSW}	V_{NEG} output connected through a series switch, NSW.
5	CE	Chip enable input. This pin is high for normal operation and low for shutdown. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
6	SDP	Positive side shutdown input. This pin is low for normal operation and high for positive side shutdown and V_{PSW} load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
7	SDN	Negative side shutdown input. This pin is low for normal operation and high for negative side shutdown and V_{NSW} load disconnect. (See Shutdown and Load Disconnect section in the Detailed Device Description division).
8	C_2^-	The negative terminal of inverting charge-pump capacitor, C2.
9	C_2^+	The positive terminal of inverting charge-pump capacitor, C2.
10	V_{05}	Regulated +5V output.
11	V_{PSW}	V_{05} output connected through a series switch, PSW.
12	V_{DBL}	Voltage Doubler Output. ($2.85V \leq V_{IN} \leq 5.4V$. See Voltage Doubler section).
13	C_1^+	The positive terminal of doubling charge-pump capacitor, C1.
14	C_1^-	The negative terminal of doubling charge-pump capacitor, C1.

National Semiconductor

LM2686
Regulated Switched Capacitor Voltage Converter

General Description

The LM2686 CMOS charge-pump voltage converter operates as an input voltage doubler and a +5V regulator for an input voltage in the range of +2.85V to +6.5V. Three low cost capacitors are used in this circuit to provide up to 50mA of output current at +5.0V (± 5%). The LM2686 operates at a 130 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 450µA (operating efficiency greater than 80% with most loads) and 6.0µA typical shutdown current, the LM2686 is ideal for use in battery powered systems. The device is in a small 14-pin TSSOP package.

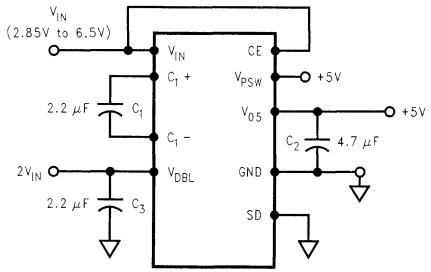
Features

- +5V regulated output
- Doubles input supply voltage
- TSSOP 14 package
- 80% typical conversion efficiency at 25mA
- Input voltage range of 2.85V to 6.5V
- Independent shutdown control pins

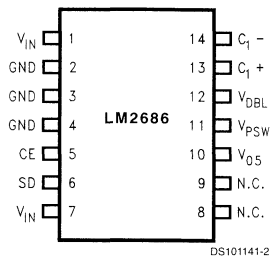
Applications

- Cellular phones
- Pagers
- PDAs
- Handheld Instrumentation
- 3.3V to 5V Voltage Conversion Applications

Typical Application and Connection Diagram



DS101141-1



DS101141-2

14-Pin TSSOP

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2686MTC	TSSOP-14	MTC14	94 Units, Rail
LM2686MTCX	TSSOP-14	MTC14	2.5k Units, Tape and Reel

Pin Description

Pin No.	Name	Function
1	V_{IN}*	Power supply input voltage.
2	GND**	Power supply ground.
3	GND**	Power supply ground.
4	GND**	Power supply ground.
5	CE	Chip enable input. This pin is high for normal operation and low for shutdown and V_{PSW} load disconnect.
6	SD	Shutdown input. This pin is low for normal operation and high for shutdown and V_{PSW} load disconnect.
7	V_{IN}*	Power supply input voltage.
8	NC	No connection.
9	NC	No connection.
10	V_{05}	Regulated +5V output.
11	V_{PSW}	V_{05} output connected through a series switch, PSW.
12	V_{DBL}	Output of doubled input voltage.
13	C_1^+	The positive terminal of doubling charge-pump capacitor, C1.
14	C_1^-	The negative terminal of doubling charge-pump capacitor, C1.

* All V_{IN} pins, pin 1 and pin 7 must be tied together for proper operation.
** All ground pins, pin 2, pin 3 and pin 4 must be tied together for proper operation.

National Semiconductor

LM2687
Low Noise Regulated Switched Capacitor Voltage Inverter

General Description

The LM2687 CMOS Negative Regulated Switched Capacitor Voltage Inverter delivers a very low noise adjustable output for an input voltage in the range of +2.7V to +5.5V. Four low cost capacitors are used in this circuit to provide up to 10mA of output current. The regulated output for the LM2687 is adjustable between −1.5V and −5.2V. The LM2687 operates at 100 kHz (typical) switching frequency to reduce output resistance and voltage ripple. With an operating current of only 500 µA (charge pump power efficiency greater than 90% with most loads) and 0.05 µA typical shutdown current, the LM2687 provides ideal performance for cellular phone power amplifier bias and other low current, low noise negative voltage needs. The device comes in a small 8-pin MSOP package.

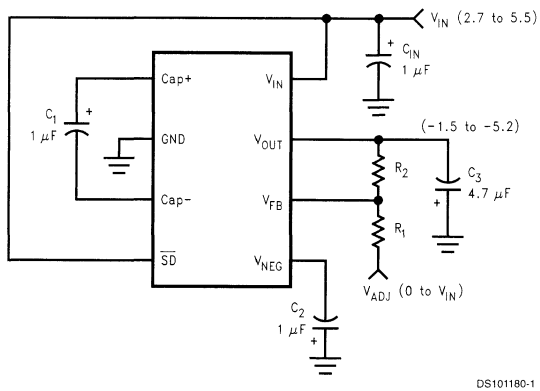
Features

- Inverts and regulates the input supply voltage
- Small MSOP-8 package
- 91% typical charge pump power efficiency at 10mA
- Low output ripple (1mV typical)
- Shutdown lowers Quiescent current to 0.05 µA (typical)

Applications

- Wireless Communication Systems
- Cellular Phone Power Amplifier Biasing
- Interface Power Supplies
- Handheld Instrumentation
- Laptop Computers and PDA's

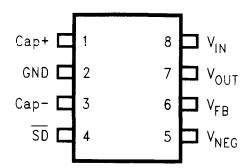
Typical Application Circuit



DS101180-1

Connection Diagram

8-Pin MSOP



DS101180-2

Ordering Information

Device Order Number	Package Number	Package Marking*	Supplies As
LM2687MM	MUA08A	S12A	Tape and Reel (1000 units/reel)
LM2687MMX	MUA08A	S12A	Tape and Reel (3500 units/reel)

Note: * The small physical size of the MSOP-8 package does not allow for the full part number marking. Devices will be marked with the designation shown in the column Package Marking.

Pin Description

Pin No.	Name	Function
1	Cap+	Positive terminal for C_1.
2	GND	Ground.
3	Cap–	Negative terminal for C_1.
4	$\overline{SD}$	Active low, logic-level shutdown input.
5	V_{NEG}	Negative unregulated output voltage.
6	V_{FB}	Feedback input. Connect V_{FB} to an external resistor divider between V_{OUT} and a positive adjust voltage V_{ADJ} ($0 \le V_{ADJ} \le V_{IN}$). **DO NOT** leave unconnected.
7	V_{OUT}	Regulated negative output voltage.
8	V_{IN}	Positive power supply input.

National Semiconductor

LM2765
Switched Capacitor Voltage Converter

General Description

The LM2765 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of +1.8V to +5.5V. Two low cost capacitors and a diode are used in this circuit to provide up to 20 mA of output current.

The LM2765 operates at 50 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 130 µA (operating efficiency greater than 90% with most loads) and 0.1µA typical shutdown current, the LM2765 provides ideal performance for battery powered systems. The device is manufactured in a SOT-23-6 package.

Features

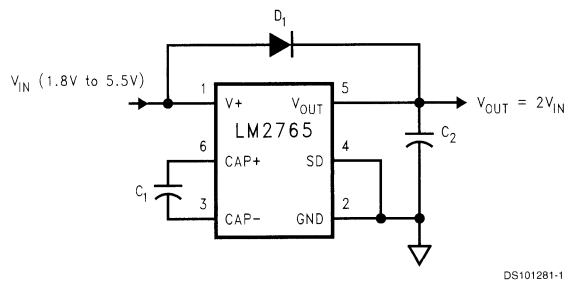
- Doubles Input Supply Voltage
- SOT23-6 Package
- 20Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 20 mA
- 0.1µA Typical Shutdown Current

Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

Basic Application Circuits

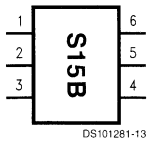
Voltage Doubler



DS101281-1

Connection Diagram

6-Lead SOT (M6)



DS101281-13

Top View With Package Marking

DS101281-22

Actual Size

Ordering Information

Order Number	Package Number	Package Marking	Supplied as
LM2765M6	MA06A	S15B (Note 1)	Tape and Reel (1000 units/reel)
LM2765M6X	MA06A	S15B (Note 1)	Tape and Reel (3000 units/reel)

Note 1: The small physical size of the SOT-23 package does not allow for the full part number marking. Devices will be marked with the designation shown in the column Package Marking.

Pin Description

Pin	Name	Function
1	V+	Power supply positive voltage input.
2	GND	Power supply ground input.
3	CAP–	Connect this pin to the negative terminal of the charge-pump capacitor.
4	SD	Shutdown control pin, tie this pin to ground in normal operation.
5	V_{OUT}	Positive voltage output.
6	CAP+	Connect this pin to the positive terminal of the charge-pump capacitor.

National Semiconductor

LM2766
Switched Capacitor Voltage Converter

General Description

The LM2766 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of +1.8V to +5.5V. Two low cost capacitors and a diode are used in this circuit to provide up to 20 mA of output current.

The LM2766 operates at 200 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 350 µA (operating efficiency greater than 90% with most loads) and 0.1µA typical shutdown current, the LM2766 provides ideal performance for battery powered systems. The device is manufactured in a SOT-23-6 package.

Features

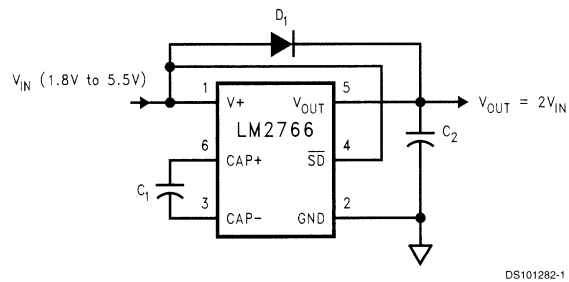
- Doubles Input Supply Voltage
- SOT23-6 Package
- 20Ω Typical Output Impedance
- 90% Typical Conversion Efficiency at 20 mA
- 0.1µA Typical Shutdown Current

Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

Basic Application Circuits

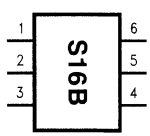
Voltage Doubler



DS101282-1

Connection Diagram

6-Lead SOT (M6)



DS101282-13

Top View With Package Marking

DS101282-22

Actual Size

Ordering Information

Order Number	Package Number	Package Marking	Supplied as
LM2766M6	MA06A	S16B (Note 1)	Tape and Reel (1000 units/reel)
LM2766M6X	MA06A	S16B (Note 1)	Tape and Reel (3000 units/reel)

Note 1: The small physical size of the SOT-23 package does not allow for the full part number marking. Devices will be marked with the designation shown in the column Package Marking.

Pin Description

Pin	Name	Function
1	V+	Power supply positive voltage input.
2	GND	Power supply ground input.
3	CAP−	Connect this pin to the negative terminal of the charge-pump capacitor.
4	$\overline{SD}$	Shutdown control pin, tie this pin to V+ in normal operation.
5	V_{OUT}	Positive voltage output.
6	CAP+	Connect this pin to the positive terminal of the charge-pump capacitor.

National Semiconductor

LM2767
Switched Capacitor Voltage Converter

General Description

The LM2767 CMOS charge-pump voltage converter operates as a voltage doubler for an input voltage in the range of +1.8V to +5.5V. Two low cost capacitors and a diode are used in this circuit to provide at least 15 mA of output current.

The LM2767 operates at 11 kHz switching frequency to avoid audio voice-band interference. With an operating current of only 40 µA (operating efficiency greater than 90% with most loads), the LM2767 provides ideal performance for battery powered systems. The device is manufactured in a SOT23-5 package.

Features

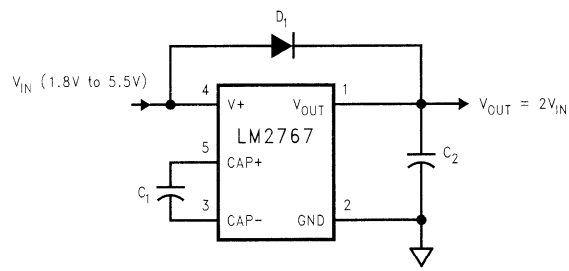
- Doubles Input Supply Voltage
- SOT23-5 Package
- 20Ω Typical Output Impedance
- 96% Typical Conversion Efficiency at 15mA

Applications

- Cellular Phones
- Pagers
- PDAs, Organizers
- Operational Amplifier Power Suppliers
- Interface Power Suppliers
- Handheld Instruments

Basic Application Circuit

Voltage Doubler



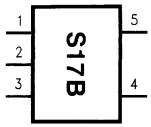
Ordering Information

Order Number	Package Number	Package Marking	Supplied as
LM2767M5	MA05B	S17B (Note 1)	Tape and Reel (1000 units/reel)
LM2767M5X	MA05B	S17B (Note 1)	Tape and Reel (3000 units/reel)

Note 1: The small physical size of the SOT-23 package does not allow for the full part number marking. Devices will be marked with the designation shown in the column Package Marking.

Connection Diagram

5-Lead SOT (M5)



DS101274-13

Top View With Package Marking

DS101274-22

Actual Size

Pin Description

Pin	Name	Function
1	V_{OUT}	Positive voltage output.
2	GND	Power supply ground input.
3	CAP–	Connect this pin to the negative terminal of the charge-pump capacitor.
4	V+	Power supply positive voltage input.
5	CAP+	Connect this pin to the positive terminal of the charge-pump capacitor.

National Semiconductor

LM2787
Low Noise Regulated Switched Capacitor Voltage Inverter in micro SMD

General Description

The LM2787 CMOS Negative Regulated Switched Capacitor Voltage Inverter delivers a very low noise adjustable output for an input voltage in the range of +2.7V to +5.5V. Four low cost capacitors are used in this circuit to provide up to 10mA of output current. The regulated output for the LM2787 is adjustable between −1.5V and −5.2V. The LM2787 operates at 260 kHz (typical) switching frequency to reduce output resistance and voltage ripple. With an operating current of only 400 µA (charge pump power efficiency greater than 90% with most loads) and 0.05 µA typical shutdown current, the LM2787 provides ideal performance for cellular phone power amplifier bias and other low current, low noise negative voltage needs. The device comes in a small 8-Bump micro SMD package.

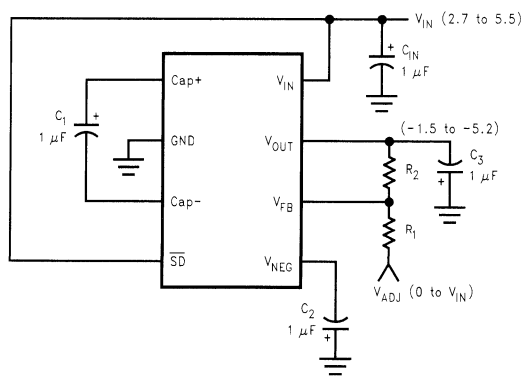
Features

- Inverts and regulates the input supply voltage
- Small 8-Bump micro SMD package
- 91% typical charge pump power efficiency at 10mA
- Low output ripple
- Shutdown lowers Quiescent current to 0.05 µA (typical)

Applications

- Wireless Communication Systems
- Cellular Phone Power Amplifier Biasing
- Interface Power Supplies
- Handheld Instrumentation
- Laptop Computers and PDA's

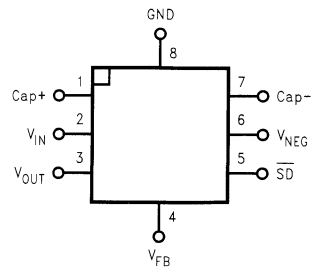
Typical Application Circuit



DS101313-25

Connection Diagram

8-Bump micro SMD (Top View)



DS101313-2

Ordering Information

Device Order Number	Package Number	Package Marking*	Supplies As
LM2787BP	BPA08CCB	S8	Tape and Reel (250 units/reel)
LM2787BPX	BPA08CCB	S8	Tape and Reel (3000 units/reel)

Note: * The small physical size of the micro SMD package does not allow for the full part number marking. Devices will be marked with the designation shown in the column Package Marking.

Pin Description

Pin No.	Name	Function
1	Cap+	Positive terminal for C_1.
2	V_{IN}	Positive power supply input.
3	V_{OUT}	Regulated negative output voltage.
4	V_{FB}	Feedback input. Connect V_{FB} to an external resistor divider between V_{OUT} and a positive adjust voltage V_{ADJ} ($0 \le V_{ADJ} \le V_{IN}$). **DO NOT** leave unconnected.
5	$\overline{SD}$	Active low, logic-level shutdown input.
6	V_{NEG}	Negative unregulated output voltage.
7	Cap–	Negative terminal for C_1.
8	GND	Ground.

National Semiconductor

PRELIMINARY

LM2792
Current Regulated Switched Capacitor LED Driver with Analog Brightness Control

General Description

The LM2792 is a CMOS charge-pump voltage doubler and regulator that provides two regulated current sources. They are designed to drive two white (or blue) LEDs with matched currents (within ± 0.3%) to produce balanced light sources for display backlights. The LM2792 accepts an input voltage range from 3.0V to 5.8V and maintain a constant current determined by an external set resistor.

The LM2792 delivers up to 32mA of load current to accommodate two high forward voltage (typically white) LEDs. The switching frequency is 900kHz (min.) to keep the conducted noise spectrum away from sensitive frequencies within portable RF devices.

The LM2792 offers full off to maximum current control through the BRGT pin. The output current linearly tracks the BRGT pin voltage. The LM2792 is available in active high or low shutdown versions. The shutdown pin reduces the operating current to 1µA (max.).

The LM2792 is available in a 10 pin leadless leadframe (LLP) CSP package.

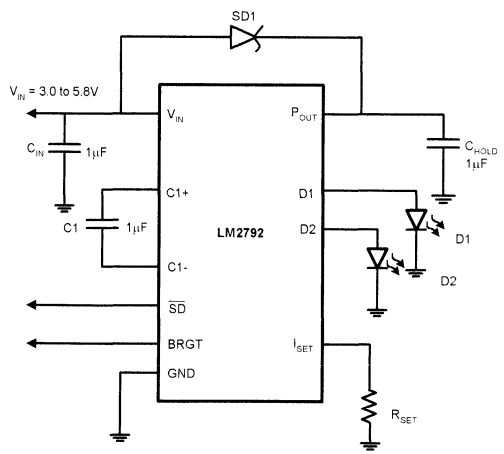
Features

- Output matching of ± 0.3% (typ.)
- Drives up to two LED's
- 3.0V to 5.8V Input Voltage
- Up to 32mA output current
- Soft start limits inrush current
- Analog brightness control
- Separate shutdown input
- Very small solution size and no inductor
- 1.4mA typical operating current
- 1µA (max.) shutdown current
- 900kHz switching frequency (min.)
- Linear regulation generates predictable noise spectrum
- LLP-10 package: 3mm X 3mm X 0.8mm

Applications

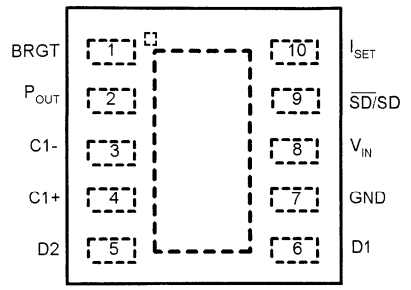
- White LED Display Backlights
- White LED Keypad Backlights
- 1-Cell Li-Ion battery-operated equipment including PDAs, hand-held PCs, cellular phones
- Flat Panel Dispalys

Basic Application Circuit



20024201

Connection Diagram



Top View
10-Lead LLP

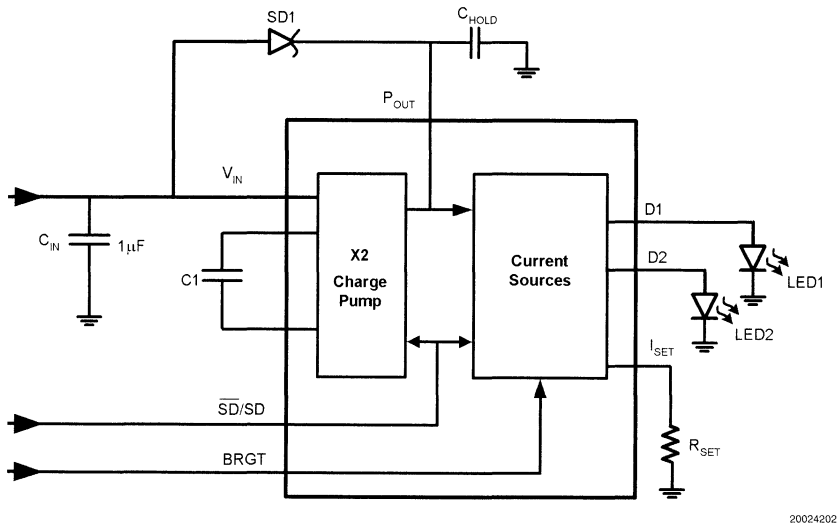
Ordering Information

Order Number	Shutdown Polarity	NSC Package Drawing	Package Marking	Supplied As
LM2792LD-L	Active Low	LLP-10	SRB	1000 Units, Tape and Reel
LM2792LDX-L	Active Low	LLP-10	SRB	4500 Units, Tape and Reel
LM2792LD-H	Active High	LLP-10	SPB	1000 Units, Tape and Reel
LM2792LDX-H	Active High	LLP-10	SPB	4500 Units, Tape and Reel

Pin Description

Pin	Name	Function
1	BRGT	Variable voltage input controls output current.
2	P_{OUT}	Charge pump output.
3	C1−	Connect this pin to the negative terminal of C1.
4	C1+	Connect this pin to the positive terminal of C1.
5	D2	Current source outputs. Connect directly to LED.
6	D1	Current source outputs. Connect directly to LED.
7	GND	Power supply ground input.
8	V_{IN}	Power supply voltage input.
9	$SD/\overline{SD}$	Shutdown input. Device operation is inhibited when pin is asserted.
10	I_{SET}	Current Sense Input. Connect resistor to ground to set constant current through LED.

Block Diagram



National Semiconductor

LM3350
Switched Capacitor Voltage Converter

General Description

The LM3350 is a CMOS charge-pump voltage converter which efficiently provides a 3.3V to 5V step-up, or 5V to 3.3V step-down. The LM3350 uses four small, low cost capacitors to provide the voltage conversion. It eliminates the cost, size and radiated EMI related to inductor based circuits, or the power loss of a linear regulator. Operating power conversion efficiency greater than 90% provides ideal performance for battery powered portable systems.

The architecture provides a fixed voltage conversion ratio of 3/2 or 2/3. Thus it can be used for other DC-DC conversions as well.

Key Specifications

- 800 kHz switch frequency allows use of very small, inexpensive capacitors.
- 4.2Ω typical step-up output impedance
- 1.8Ω typical step-down output impedance
- 90% typical power conversion efficiency at 50 mA
- 250 nA typical shutdown current

Features

- Conversion of 3.3V to 5V, or 5V to 3.3V
- Small Mini SO-8 package
- No inductor required

Applications

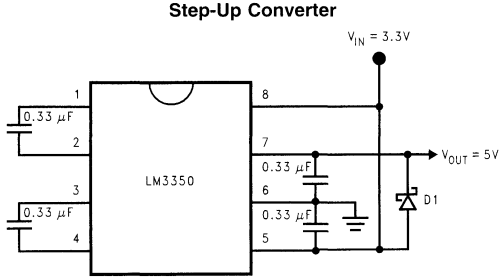
- Any mixed 5V and 3.3V system
- Laptop computers and PDAs
- Handheld instrumentation
- PCMCIA cards

Ordering Information

Order Number	Package Type	NSC Package Drawing	Package Marking	Supplied As
LM3350MMX	Mini SO-8	MUA08A	S00A	3500k Units on Tape and Reel
LM3350MM	Mini SO-8	MUA08A	S00A	1000 Units on Tape and Reel

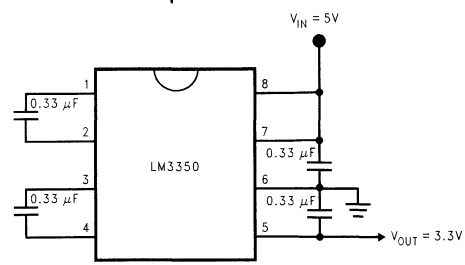
Basic Operating Circuits

Step-Up Converter



DS100002-1

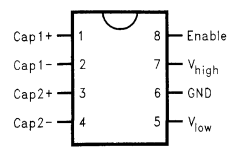
Step-Down Converter



DS100002-2

Connection Diagram

Mini SO8 Package



DS100002-3

Top View

National Semiconductor

LM3351
Switched Capacitor Voltage Converter

General Description

The LM3351 is a CMOS charge-pump voltage converter which efficiently provides a 3.3V to 5V step-up, or 5V to 3.3V step-down. The LM3351 is pin for pin compatible with the LM3350 but consumes 66% less quiescent current. The LM3351 uses four small, low cost capacitors to provide the voltage conversion. It eliminates the cost, size and radiated EMI related to inductor based circuits, or the power loss of a linear regulator. Operating power conversion efficiency greater than 90% provides ideal performance for battery powered portable systems.

The architecture provides a fixed voltage conversion ratio of 3/2 or 2/3. Thus it can be used for other DC-DC conversions as well.

Key Specifications

- 200 kHz switch frequency allows use of very small, inexpensive capacitors.
- 4.2Ω typical step-up output impedance
- 1.8Ω typical step-down output impedance
- 95% typical power conversion efficiency at 50 mA
- 250 nA typical shutdown current
- Low quiescent current extends battary life

Features

- Conversion of 3.3V to 5V, or 5V to 3.3V
- Small Mini SO-8 package
- No inductor required

Applications

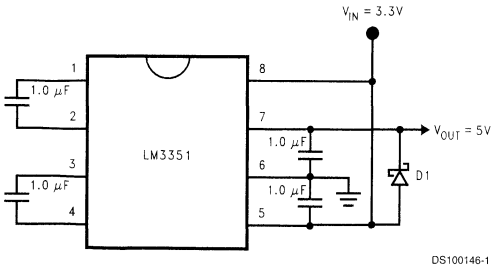
- Any mixed 5V and 3.3V system
- Laptop computers and PDAs
- Handheld instrumentation
- PCMCIA cards

Ordering Information

Order Number	Package Type	NSC Package Drawing	Package Marking	Supplied As
LM3351MMX	Mini SO-8	MUA08A	S05A	3500 Units on Tape and Reel
LM3351MM	Mini SO-8	MUA08A	S05A	1000 Units on Tape and Reel

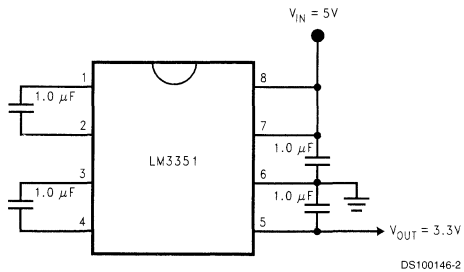
Basic Operating Circuits

Step-Up Converter



DS100146-1

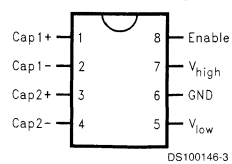
Step-Down Converter



DS100146-2

Connection Diagram

Mini SO8 Package



DS100146-3

Top View

National Semiconductor

LM3352
Regulated 200 mA Buck-Boost Switched Capacitor DC/DC Converter

General Description

The LM3352 is a CMOS switched capacitor DC/DC converter that produces a regulated output voltage by automatically stepping up (boost) or stepping down (buck) the input voltage. It accepts an input voltage between 2.5V and 5.5V. The LM3352 is available in three standard output voltage versions: 2.5V, 3.0V and 3.3V. If other output voltage options between 1.8V and 4.0V are desired, please contact your National Semiconductor representative.

The LM3352's proprietary buck-boost architecture enables up to 200 mA of load current at an average efficiency greater than 80%. Typical operating current is only 400 µA and the typical shutdown current is only 2.5 µA.

The LM3352 is available in a 16-pin TSSOP package. This package has a maximum height of only 1.1 mm.

The high efficiency of the LM3352, low operating and shutdown currents, small package size, and the small size of the overall solution make this device ideal for battery powered, portable, and hand-held applications.

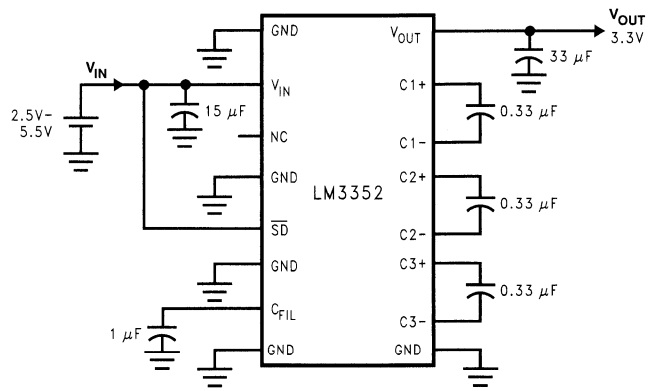
Features

- Regulated V_{OUT} with ±3% accuracy
- Standard output voltage options: 2.5V, 3.0V and 3.3V
- Custom output voltages available from 1.8V to 4.0V in 100 mV increments
- 2.5V to 5.5V input voltage
- Up to 200 mA output current
- >80% average efficiency
- Uses few, low-cost external components
- Very small solution size
- 400 µA typical operating current
- 2.5 µA typical shutdown current
- 1 MHz switching frequency (typical)
- Architecture and control methods provide high load current and good efficiency
- TSSOP-16 package
- Over-temperature protection

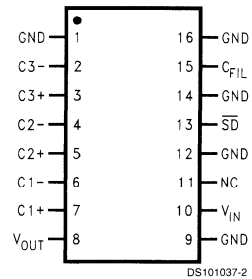
Applications

- 1-cell Lilon battery-operated equipment including PDAs, hand-held PCs, cellular phones
- Flat panel displays
- Hand-held instruments
- NiCd, NiMH, or alkaline battery powered systems
- 3.3V to 2.5V and 5.0V to 3.3V conversion

Typical Operating Circuit



Connection Diagram



Top View
TSSOP-16 Pin Package
See NS Package Number MTC16

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM3352MTCX-2.5	TSSOP-16	MTC16	2.5k Units, Tape and Reel
LM3352MTC-2.5	TSSOP-16	MTC16	94 Units, Rail
LM3352MTCX-3.0	TSSOP-16	MTC16	2.5k Units, Tape and Reel
LM3352MTC-3.0	TSSOP-16	MTC16	94 Units, Rail
LM3352MTCX-3.3	TSSOP-16	MTC16	2.5k Units, Tape and Reel
LM3352MTC-3.3	TSSOP-16	MTC16	94 Units, Rail

Pin Description

Pin Number	Name	Function
1	GND	Ground*
2	C3–	Negative Terminal for C3
3	C3+	Positive Terminal for C3
4	C2–	Negative Terminal for C2
5	C2+	Positive Terminal for C2
6	C1–	Negative Terminal for C1
7	C1+	Positive Terminal for C1
8	V_{OUT}	Regulated Output Voltage
9	GND	Ground*
10	V_{IN}	Input Supply Voltage
11	NC	This pin must be left unconnected.
12	GND	Ground*
13	$\overline{SD}$	Active Low CMOS Logic-Level Shutdown Input
14	GND	Ground*
15	C_{FIL}	Filter Capacitor; A 1 µF ceramic capacitor is suggested.
16	GND	Ground*

*All GND pins of the LM3352 must be connected to the same ground.

National Semiconductor

LM3354
Regulated 90mA Buck-Boost Switched Capacitor DC/DC Converter

General Description

The LM3354 is a CMOS switched capacitor DC/DC converter that produces a regulated output voltage by automatically stepping up (boost) or stepping down (buck) the input voltage. It accepts an input voltage between 2.5V and 5.5V. The LM3354 is available with standard output voltages of 1.8V, 3.3V, and 4.1V (ideal for white LED applications). If other output voltage options between 1.8V and 4.1V are desired, please contact your National Semiconductor representative.

The LM3354's proprietary buck-boost architecture enables up to 90mA of load current at an average efficiency greater than 75%. Typical operating current is only 375 µA and the typical shutdown current is only 2.3 µA.

The LM3354 is available in a 10-pin MSOP package. This package has a maximum height of only 1.1 mm.

The high efficiency of the LM3354, low operating and shutdown currents, small package size, and the small size of the overall solution make this device ideal for battery powered, portable, and hand-held applications.

See the LM3352 for up to 200mA of output current or the LM3355 for up to 50mA of output current.

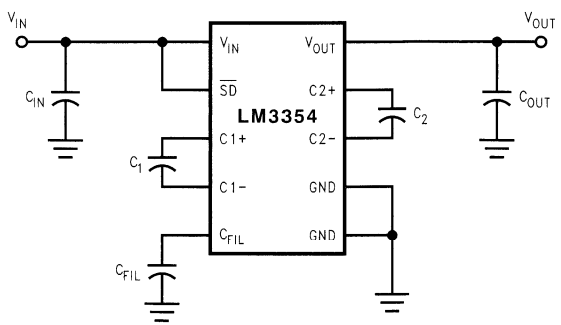
Features

- Regulated V_{OUT} with ±3% (4.1V and 3.3V options) or ±4% (1.8V option) accuracy
- Standard output voltages of 1.8V, 3.3V, and 4.1V
- Custom output voltages available from 1.8V to 4.1V in 100 mV increments with volume order
- 2.5V to 5.5V input voltage range
- Up to 90mA (4.1V and 1.8V options) or 70mA (3.3V option) output current
- >75% average efficiency
- Uses few, low-cost external components
- Very small solution size
- 375 µA typical operating current
- 2.3 µA typical shutdown current
- 1 MHz typical switching frequency
- Architecture and control methods provide high load current and good efficiency
- MSOP-10 package
- Over-temperature protection

Applications

- White LED display backlights
- 1-cell Lilon battery-operated equipment including PDAs, hand-held PCs, cellular phones
- Flat panel displays
- Hand-held instruments
- Li-Ion, NiCd, NiMH, or alkaline battery powered systems

Typical Operating Circuit



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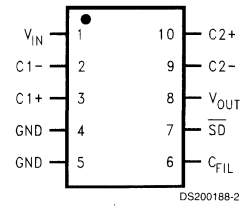
Connection Diagram



Top View
MSOP-10 Pin Package
See NS Package Number MM

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM3354MMX-4.1	MSOP-10	MUB10A	3.5k Units, Tape and Reel
LM3354MM-4.1	MSOP-10	MUB10A	1k Units, Tape and Reel
LM3354MMX-3.3	MSOP-10	MUB10A	3.5k Units, Tape and Reel
LM3354MM-3.3	MSOP-10	MUB10A	1k Units, Tape and Reel
LM3354MMX-1.8	MSOP-10	MUB10A	3.5k Units, Tape and Reel
LM3354MM-1.8	MSOP-10	MUB10A	1k Units, Tape and Reel

Pin Description

Pin Number	Name	Function
1	V_{IN}	Input Supply Voltage
2	C1−	Negative Terminal for C1
3	C1+	Positive Terminal for C1
4	GND	Ground
5	GND	Ground
6	C_{FIL}	Filter Capacitor, a 1µF capacitor is recommended.
7	$\overline{SD}$	Shutdown, active low
8	V_{OUT}	Regulated Output Voltage
9	C2−	Negative Terminal for C2
10	C2+	Positive Terminal for C2

National Semiconductor

LM3355
Regulated 50mA Buck-Boost Switched Capacitor DC/DC Converter

General Description

The LM3355 is a CMOS switched capacitor DC/DC converter that produces a regulated output voltage by automatically stepping up (boost) or stepping down (buck) the input voltage. It accepts an input voltage between 2.5V and 5.5V. The LM3355 is available with a standard output voltage of 4.1V (ideal for white LED applications). If other output voltage options between 1.8V and 4.1V are desired for other applications, please contact your National Semiconductor representative.

The LM3355's proprietary buck-boost architecture enables up to 50 mA of load current at an average efficiency greater than 75%. Typical operating current is only 375 µA and the typical shutdown current is only 2.3 µA.

The LM3355 is available in a 10-pin MSOP package. This package has a maximum height of only 1.1 mm.

The high efficiency of the LM3355, low operating and shutdown currents, small package size, and the small size of the overall solution make this device ideal for battery powered, portable, and hand-held applications.

See the LM3352 for up to 200mA of output current.

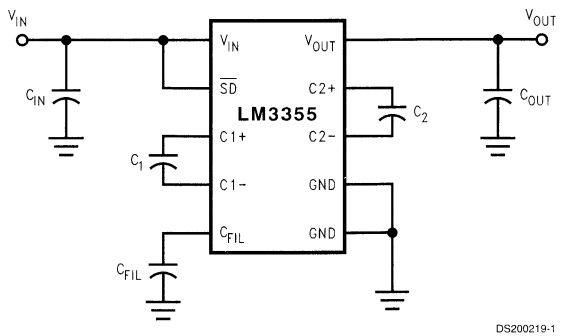
Features

- Regulated V_{OUT} with ±3% accuracy
- Standard output voltage of 4.1V
- Custom output voltages available from 1.8V to 4.1V in 100 mV increments
- 2.5V to 5.5V input voltage
- Up to 50 mA output current
- >75% average efficiency
- Uses few, low-cost external components
- Very small solution size
- 375 µA typical operating current
- 2.3 µA typical shutdown current
- 1 MHz switching frequency (typical)
- Architecture and control methods provide high load current and good efficiency
- MSOP-10 package
- Over-temperature protection

Applications

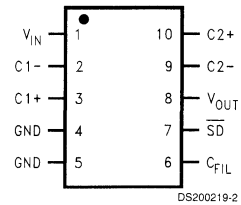
- White LED display backlights
- 1-cell Lilon battery-operated equipment including PDAs, hand-held PCs, cellular phones
- Flat panel displays
- Hand-held instruments
- NiCd, NiMH, or alkaline battery powered systems

Typical Operating Circuit



DS200219-1

Connection Diagram



Top View
MSOP-10 Pin Package
See NS Package Number MUB10A

Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM3355MMX-4.1	MSOP-10	MUB10A	3.5k Units, Tape and Reel
LM3355MM-4.1	MSOP-10	MUB10A	1k Units, Tape and Reel

Pin Description

Pin Number	Name	Function
1	V_{IN}	Input Supply Voltage
2	C1−	Negative Terminal for C1
3	C1+	Positive Terminal for C1
4	GND	Ground
5	GND	Ground
6	C_{FIL}	Filter Capacitor, a 1µF capacitor is recommended.
7	$\overline{SD}$	Shutdown, active low
8	V_{OUT}	Regulated Output Voltage
9	C2−	Negative Terminal for C2
10	C2+	Positive Terminal for C2

National Semiconductor

LM828
Switched Capacitor Voltage Converter

General Description

The LM828 CMOS charge-pump voltage converter inverts a positive voltage in the range of +1.8V to +5.5V to the corresponding negative voltage of −1.8V to −5.5V. The LM828 uses two low cost capacitors to provide up to 25 mA of output current.

The LM828 operates at 12 kHz switching frequency to reduce output resistance and voltage ripple. With an operating current of only 40 µA (operating efficiency greater than 96% with most loads), the LM828 provides ideal performance for battery powered systems. The device is in a tiny SOT-23-5 package.

Features

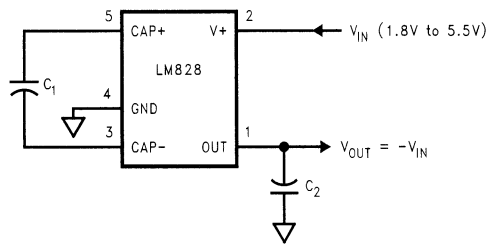
- Inverts Input Supply Voltage
- SOT-23-5 Package
- 20Ω Typical Output Impedance
- 97% Typical Conversion Efficiency at 5 mA

Applications

- Cellular Phones
- Pagers
- PDAs
- Operational Amplifier Power Supplies
- Interface Power Supplies
- Handheld Instruments

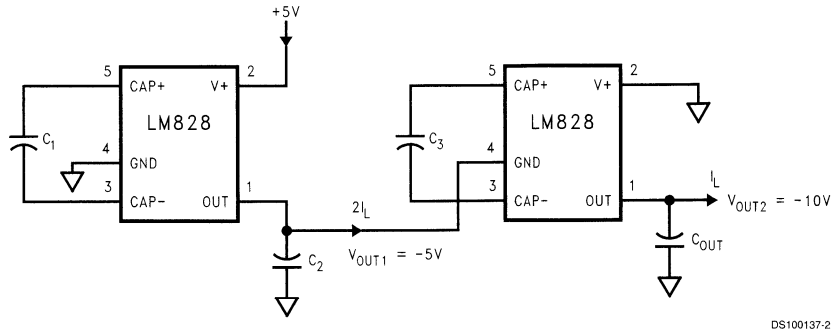
Basic Application Circuits

Voltage Inverter



DS100137-1

+5V to −10V Converter



DS100137-2

National Semiconductor

LMC7660
Switched Capacitor Voltage Converter

General Description

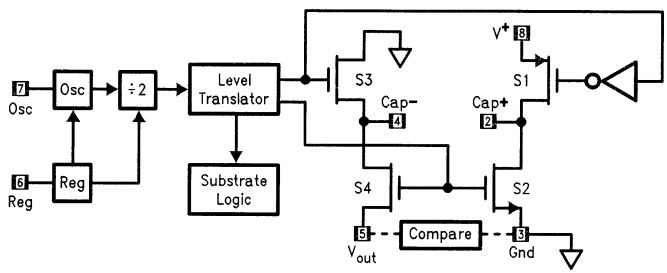
The LMC7660 is a CMOS voltage converter capable of converting a positive voltage in the range of +1.5V to +10V to the corresponding negative voltage of −1.5V to −10V. The LMC7660 is a pin-for-pin replacement for the industry-standard 7660. The converter features: operation over full temperature and voltage range without need for an external diode, low quiescent current, and high power efficiency.

The LMC7660 uses its built-in oscillator to switch 4 power MOS switches and charge two inexpensive electrolytic capacitors.

Features

- Operation over full temperature and voltage range without an external diode
- Low supply current, 200 µA max
- Pin-for-pin replacement for the 7660
- Wide operating range 1.5V to 10V
- 97% Voltage Conversion Efficiency
- 95% Power Conversion Efficiency
- Easy to use, only 2 external components
- Extended temperature range
- Narrow SO-8 Package

Block Diagram



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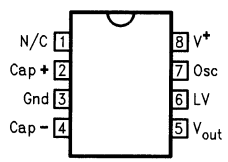
Pin Configuration



DS009136-2

Ordering Information

Package	Temperature Range Industrial −40°C to +85°C	NSC Drawing
8-Lead Molded DIP	LMC7660IN	N08E
8-Lead Molded Small Outline	LMC7660IM	M08A

National Semiconductor

MAX660
Switched Capacitor Voltage Converter

General Description

The MAX660 CMOS charge-pump voltage converter inverts a positive voltage in the range of 1.5V to 5.5V to the corresponding negative voltage. The MAX660 uses two low cost capacitors to provide 100 mA of output current without the cost, size, and EMI related to inductor based converters. With an operating current of only 120 µA and operating efficiency greater than 90% at most loads, the MAX660 provides ideal performance for battery powered systems. The MAX660 may also be used as a positive voltage doubler.

The oscillator frequency can be lowered by adding an external capacitor to the OSC pin. Also, the OSC pin may be used to drive the MAX660 with an external clock. A frequency control (FC) pin selects the oscillator frequency of 10 kHz or 80 kHz.

Features

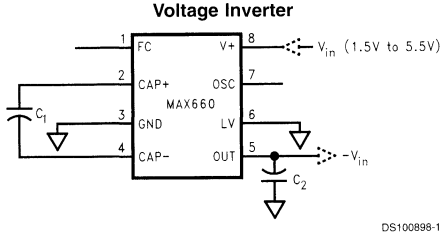
- Inverts or doubles input supply voltage
- Narrow SO-8 Package
- 6.5Ω typical output resistance
- 88% typical conversion efficiency at 100 mA
- Selectable oscillator frequency: 10 kHz/80 kHz

Applications

- Laptop computers
- Cellular phones
- Medical instruments
- Operational amplifier power supplies
- Interface power supplies
- Handheld instruments

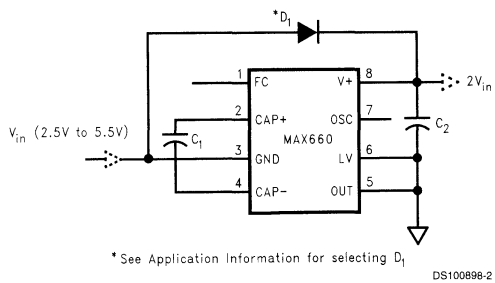
Typical Application Circuits

Voltage Inverter



DS100898-1

Positive Voltage Doubler

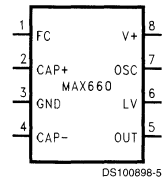


*See Application Information for selecting D_1

DS100898-2

Connection Diagram

8-Lead SO



Top View

Ordering Information

Order Number	Top Mark	Package	Supplied as
MAX660M	Date Code MAX660M	M08A	Rail (95 units/rail)
MAX660MX	Date Code MAX660M	M08A	Tape and Reel (2500 units/rail)

Section 19
Wireless

Section 19 Contents

National Semiconductor

PRELIMINARY

LMX1600/LMX1601/LMX1602
PLLatinum™ Low Cost Dual Frequency Synthesizer

LMX1600 2.0 GHz/500 MHz
LMX1601 1.1 GHz/500 MHz
LMX1602 1.1 GHz/1.1 GHz

General Description

The LMX1600/01/02 is part of a family of monolithic integrated dual frequency synthesizers designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using National's 0.5u ABiC V silicon BiCMOS process.

The LMX1600/01/02 contains two dual modulus prescalers, four programmable counters, two phase detectors and two selectable gain charge pumps necessary to provide the control voltage for two external loop filters and VCO loops. Digital filtered lock detects for both PLLs are included. Data is transferred into the LMX1600/01/02 via a MICROWIRE™ serial interface (Data, Clock, LE).

V_{CC} supply voltage can range from 2.7V to 3.6V. The LMX1600/01/02 features very low current consumption - typically 4.0 mA at 3V for LMX1601, 5.0 mA at 3V for LMX1600 or LMX1602. Powerdown for the PLL is hardware controlled.

The LMX1600/01/02 is available in a 16 pin TSSOP surface mount plastic package.

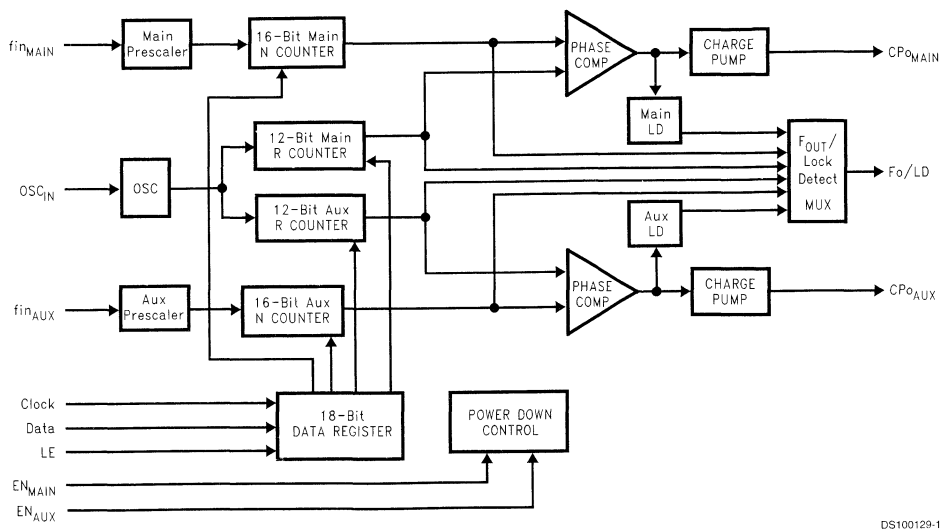
Features

- V_{CC} = 2.7V to 3.6V operation
- Low current consumption:
  4 mA @ 3V (typ) for LMX1601
  5 mA @ 3V (typ) for LMX1600 or LMX1602
- PLL Powerdown mode: I_{CC} = 1 µA typical
- Digital Filtered Lock Detects
- Dual modulus prescaler:
  — 2 GHz/500 MHz option: (Main) 32/33 (Aux) 8/9
  — 1.1 GHz/500 MHz option: (Main) 16/17 (Aux) 8/9
  — 1.1 GHz/1.1 GHz option: (Main) 16/17 (Aux) 16/17

Applications

- Cordless / Cellular / PCS phones
- Other digital mobile phones

Functional Block Diagram



DS100129-1

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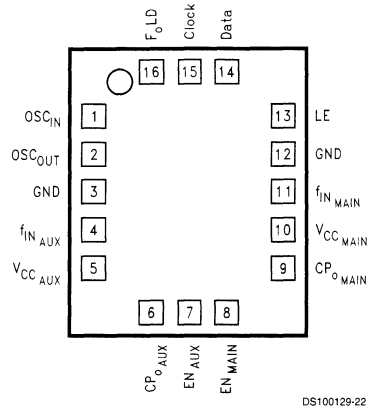
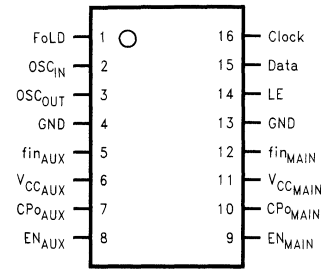
Connection Diagrams



DS100129-22

Order Number LMX1600SLB, LMX1601SLB, or LMX1602SLB
NS Package Number SLB16A



DS100129-2

Order Number LMX1600TM, LMX1601TM, or LMX1602TM
NS Package Number MTC16

Pin Descriptions

Pin No. for 16-pin CSP Package	Pin No. for 16-pin TSSOP Package	Pin Name	I/O	Description
16	1	FoLD	O	Multiplexed output of the Main/Aux programmable or reference dividers and Main/Aux lock detect. CMOS output. (See Programming Description 2.5)
1	2	OSC_{IN}	I	PLL reference input which drives both the Main and Aux R counter inputs. Has about 1.2V input threshold and can be driven from an external CMOS or TTL logic gate. Typically connected to a TCXO output. Can be used with an external resonator (See Programming Description 2.5.4).
2	3	OSC_{OUT}	O	Oscillator output. Used with an external resonator.
3	4	GND	—	Aux PLL ground.
4	5	fin_{AUX}	I	Aux prescaler input. Small signal input from the VCO.
5	6	$V_{CC_{AUX}}$	—	Aux PLL power supply voltage input. Must be equal to $V_{CC_{MAIN}}$. May range from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
6	7	CPo_{AUX}	O	Aux PLL Charge Pump output. Connected to a loop filter for driving the control input of an external VCO.
7	8	EN_{AUX}	I	Powers down the Aux PLL when LOW (N and R counters, prescaler, and tristates charge pump output). Bringing EN_{AUX} HIGH powers up the Aux PLL.
8	9	EN_{MAIN}	I	Powers down the Main PLL when LOW (N and R counters, prescaler, and tristates charge pump output). Bringing EN_{MAIN} HIGH powers up the Main PLL.
9	10	CPo_{MAIN}	O	Main PLL Charge Pump output. Connected to a loop filter for driving the control input of an external VCO.
10	11	$V_{CC_{MAIN}}$	—	Main PLL power supply voltage input. Must be equal to $V_{CC_{AUX}}$. May range from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
11	12	fin_{MAIN}	I	Main prescaler input. Small signal input from the VCO.
12	13	GND	—	Main PLL ground.

Pin Descriptions (Continued)

Pin No. for 16-pin CSP Package	Pin No. for 16-pin TSSOP Package	Pin Name	I/O	Description
13	14	LE	I	Load enable high impedance CMOS input. Data stored in the shift registers is loaded into one of the 4 internal latches when LE goes HIGH (control bit dependent).
14	15	Data	I	High impedance CMOS input. Binary serial data input. Data entered MSB first. The last two bits are the control bits.
15	16	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 18-bit shift register.

National Semiconductor

LMX2306/LMX2316/LMX2326
PLLatinum™ Low Power Frequency Synthesizer for RF Personal Communications
LMX2306 550 MHz
LMX2316 1.2 GHz
LMX2326 2.8 GHz

General Description

The LMX2306/16/26 are monolithic, integrated frequency synthesizers with prescalers that are designed to be used to generate a very stable low noise signal for controlling the local oscillator of an RF transceiver. They are fabricated using National's ABiC V silicon BiCMOS 0.5µ process.

The LMX2306 contains a 8/9 dual modulus prescaler while the LMX2316 and the LMX2326 have a 32/33 dual modulus prescaler. The LMX2306/16/26 employ a digital phase locked loop technique. When combined with a high quality reference oscillator and loop filter, the LMX2306/16/26 provide the feedback tuning voltage for a voltage controlled oscillator to generate a low phase noise local oscillator signal. Serial data is transferred into the LMX2306/16/26 via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.3V to 5.5V. The LMX2306/16/26 feature ultra low current consumption; LMX2306 - 1.7 mA at 3V, LMX2316 - 2.5 mA at 3V, and LMX2326 - 4.7 mA at 3V.

The LMX2306/16/26 synthesizers are available in a 16-pin TSSOP surface mount plastic package.

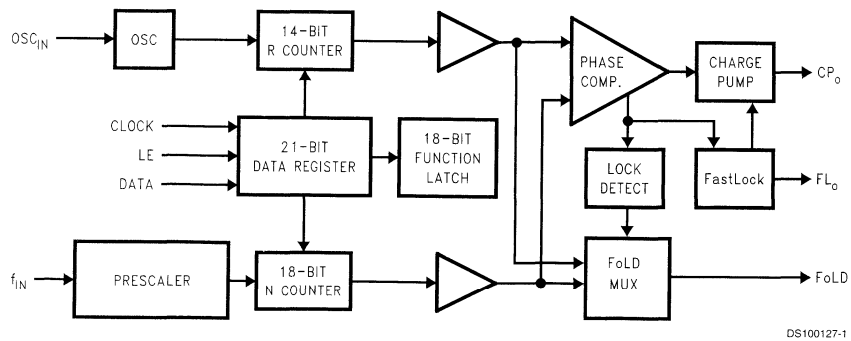
Features

- 2.3V to 5.5V operation
- Ultra low current consumption
- 2.5V V_{CC} JEDEC standard compatible
- Programmable or logical power down mode:
  — I_{CC} = 1 µA typical at 3V
- Dual modulus prescaler:
  — LMX2306 8/9
  — LMX2316/26 32/33
- Selectable charge pump TRI-STATE® mode
- Selectable FastLock™ mode with timeout counter
- MICROWIRE™ Interface
- Digital Lock Detect

Applications

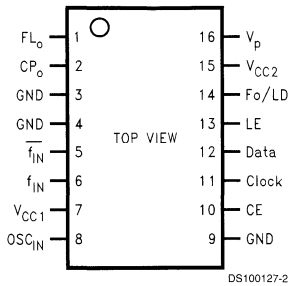
- Portable wireless communications (PCS/PCN, cordless)
- Wireless Local Area Networks (WLANs)
- Cable TV tuners (CATV)
- Pagers
- Other wireless communication systems

Functional Block Diagram



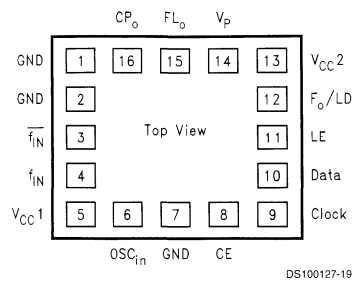
Connection Diagrams

LMX2306/16/26



16-Lead (0.173" Wide) Thin Shrink Small Outline Package(TM)
Order Number LMX2306TM, LMX2306TMX, LMX2316TM, LMX2316TMX, LMX2326TM or LMX2326TMX
See NS Package Number MTC16

LMX2306/16/26



16-pin Chip Scale Package
Order Number LMX2306SLBX, LMX2316SLBX or LM2326SLBX
See NS Package Number SLB16A

Pin Descriptions

16-Pin TSSOP	16-Pin CSP	Pin Name	I/O	Description
1	15	FL_o	O	FastLock Output. For connection of parallel resistor to the loop filter. (See Section 1.3.4 FASTLOCK MODES description.)
2	16	CP_o	O	Charge Pump Output. For connection to a loop filter for driving the input of an external VCO.
3	1	GND		Charge Pump Ground.
4	2	GND		Analog Ground.
5	3	$\overline{f_{IN}}$	I	RF Prescaler Complementary Input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The complementary input can be left unbypassed, with some degradation in RF sensitivity.
6	4	f_{IN}	I	RF Prescaler Input. Small signal input from the VCO.
7	5	V_{CC1}		Analog Power Supply Voltage Input. Input may range from 2.3V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. V_{CC1} must equal V_{CC2}.
8	6	OSC_{IN}	I	Oscillator Input. This input is a CMOS input with a threshold of approximately $V_{CC}/2$ and an equivalent 100k input resistance. The oscillator input is driven from a reference oscillator.
9	7	GND		Digital Ground.
10	8	CE	I	Chip Enable. A LOW on CE powers down the device and will TRI-STATE the charge pump output. Taking CE HIGH will power up the device depending on the status of the power down bit F2. (See Section 1.3.1 POWERDOWN OPERATION and Section 1.7.1 DEVICE PROGRAMMING AFTER FIRST APPLYING V_{CC}.)
11	9	Clock	I	High Impedance CMOS Clock Input. Data for the various counters is clocked in on the rising edge into the 21-bit shift register.
12	10	Data	I	Binary Serial Data Input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	11	LE	I	Load Enable CMOS Input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 3 appropriate latches (control bit dependent).
14	12	Fo/LD	O	Multiplexed Output of the RF Programmable or Reference Dividers and Lock Detect. CMOS output. (See *Table 4.*)
15	13	V_{CC2}		Digital Power Supply Voltage Input. Input may range from 2.3V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. V_{CC1} must equal V_{CC2}.
16	14	V_P		Power Supply for Charge Pump. Must be $\geq V_{CC}$.

National Semiconductor

LMX2323
PLLatinum™ 2.0 GHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2323 is a high performance frequency synthesizer with integrated 32/33 dual modulus prescaler designed for RF operation up to 2.0 GHz. Using a proprietary digital phase locked loop technique, the LMX2323's linear phase detector characteristics can generate very stable, low noise control signals for UHF and VHF voltage controlled oscillators.

Serial data is transferred into the LMX2323 via a three-line MICROWIRE™ interface (Data, LE, Clock). Supply voltage range is from 2.7V to 5.5V. The LMX2323 features very low curent consumption, typically 3.5mA at 3V. The charge pump provides 4 mA output current.

The LMX2323 is manufactured using National's ABiC V BiCMOS process and is packaged in a 16-pin TSSOP.

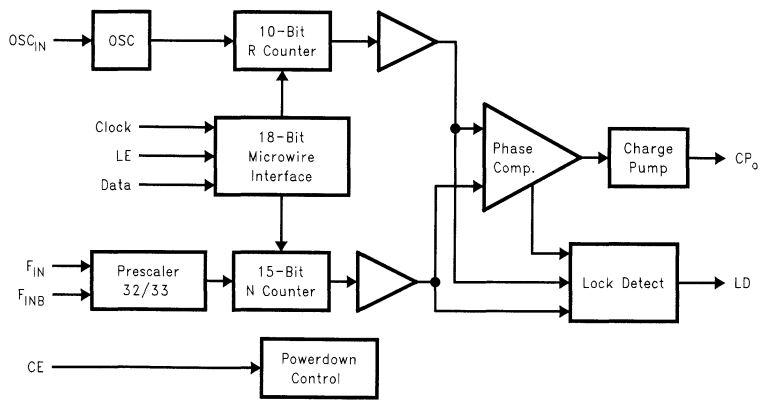
Features

- RF operation up to 2.0 GHz
- 2.7V to 5.5V operation
- Low current consumption: Icc = 3.5mA (typ) at Vcc=3.0V
- Digital Lock Detect
- Dual modulus prescaler: 32/33
- Internal balanced, low leakage charge pump

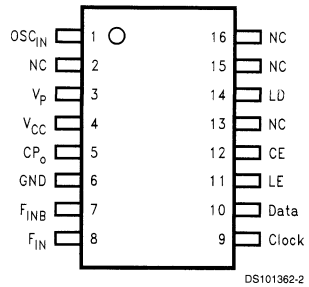
Applications

- Cellular telephone systems (GSM, NADC, CDMA, PDC, PHS)
- Personal wireless communications (DCS-1800, DECT, CT-1+)
- Wireless local area networks (WLANs)
- DCS/PCS infrastructure equipment
- Other wireless communication systems

Functional Block Diagram



Connection Diagram



Top View
Order Number LMX2323TM, LMX2323TMX
See NS Package Number MTC16

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
3	V_P	—	Power supply for charge pump. Must be ≥ V_{CC}.
4	V_{CC}	—	Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
5	CP_o	O	Internal charge pump output. For connection to a loop filter for driving the voltage control input of an external oscillator.
6	GND	—	Ground.
7	f_{INB}	I	RF prescaler complimentary input. In single-ended mode, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The LMX2323 can be driven differentially when a bypass capacitor is omitted.
8	f_{IN}	I	RF prescaler input. Small signal input from the voltage controlled oscillator.
9	Clock	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, into the various counters and registers.
10	Data	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
11	LE	I	Load Enable input. When Load Enable transitions HIGH, data is loaded into either the N or R register (control bit dependent). See timing diagram.
12	CE	I	PLL Enable. A LOW on CE powers down the device asynchronously and TRI-STATE®s the charge pump output.
14	LD	O	Lock detect output. This pin can be programmed to provide R counter output, N counter output, digital lock detect (CMOS logic) or analog lock detect (open drain).
2, 13, 15, 16	NC		No Connect.

National Semiconductor

LMX2324
PLLatinum™ 2.0 GHz Frequency Synthesizer for RF Personal Communications

General Description

The LMX2324 is a high performance frequency synthesizer with integrated 32/33 dual modulus prescaler designed for RF operation up to 2.0 GHz. Using a proprietary digital phase locked loop technique, the LMX2324's linear phase detector characteristics can generate very stable, low noise control signals for UHF and VHF voltage controlled oscillators.

Serial data is transferred into the LMX2324 via a three-line MICROWIRE™ interface (Data, LE, Clock). Supply voltage range is from 2.7V to 5.5V. The LMX2324 features very low current consumption, typically 3.5 mA at 3V. The charge pump provides 4 mA output current.

The LMX2324 is manufactured using National's ABiC V BiCMOS process and is packaged in a 16-pin TSSOP and a 16-pin Chip Scale Package (CSP).

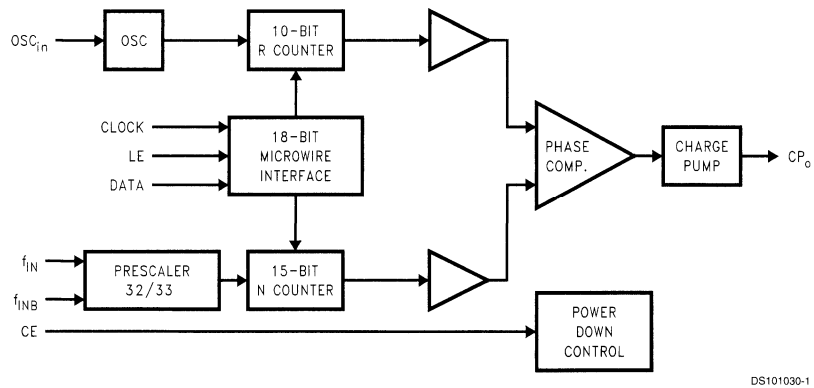
Features

- RF operation up to 2.0 GHz
- 2.7V to 5.5V operation
- Low current consumption: I_{CC} = 3.5 mA (typ) at V_{CC} = 3.0V
- Dual modulus prescaler: 32/33
- Internal balanced, low leakage charge pump

Applications

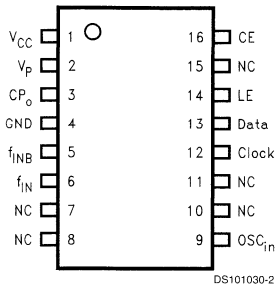
- Cellular telephone systems (GSM, NADC, CDMA, PDC)
- Personal wireless communications (DCS-1800, DECT, CT-1+)
- Wireless local area networks (WLANs)
- Other wireless communication systems

Functional Block Diagram



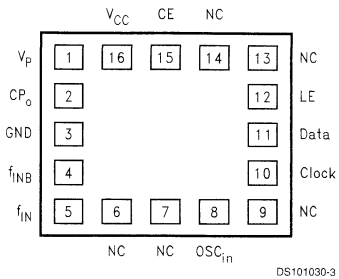
Connection Diagrams

TSSOP 16-Pin Package



Order Number LMX2324TM, LM2324TMX
See NS Package Number MTC16

CSP 16-Pin Package



Top View
Order Number LMX2324SLBX
See NS Package Number SLB16A

Pin Descriptions

Pin No.		Pin Name	I/O	Description
TSSOP16	CSP16			
2	1	V_P	—	Power supply for charge pump. Must be ≥ V_{CC}
3	2	CP_o	O	Internal charge pump output. For connection to a loop filter for driving the voltage control input of an external oscillator.
4	3	GND	—	Ground.
5	4	f_{INB}	I	RF prescaler complimentary input. In single-ended mode, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. The LMX2324 can be driven differentially when the bypass capacitor is omitted.
6	5	f_{IN}	I	RF prescaler input. Small signal input from the voltage controlled oscillator.
7	6	NC		No Connect
8	7	NC		No Connect
9	8	OSC_{in}	I	Oscillator input. A CMOS inverting gate input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
10	9	NC		No Connect
12	10	Clock	I	High impedance CMOS Clock input. Data is clocked in on the rising edge, for the various counters and registers.
13	11	Data	I	Binary serial data input. Data entered MSB first. LSB is control bit. High impedance CMOS input.
14	12	LE	I	Load Enable input. When Load Enable transitions HIGH, data is loaded into either the N or R register (control bit dependent). See timing diagram.
15	13	NC		No Connect
11	14	NC		No Connect
16	15	CE	I	CHIP Enable. A LOW on CE powers down the device asynchronously and will TRI-STATE® the charge pump output.
1	16	V_{CC}	I	Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

National Semiconductor

LMX2330L/LMX2331L/LMX2332L
PLLatinum™ Low Power Dual Frequency Synthesizer for RF Personal Communications
LMX2330L 2.5 GHz/510 MHz
LMX2331L 2.0 GHz/510 MHz
LMX2332L 1.2 GHz/510 MHz

General Description

The LMX233XL family of monolithic, integrated dual frequency synthesizers, including prescalers, is to be used as a local oscillator for RF and first IF of a dual conversion transceiver. It is fabricated using National's 0.5μ ABiC V silicon BiCMOS process.

The LMX233XL contains dual modulus prescalers. A 64/65 or a 128/129 prescaler (32/33 or 64/65 in the 2.5 GHz LMX2330L) can be selected for the RF synthesizer and a 8/9 or a 16/17 prescaler can be selected for the IF synthesizer. LMX233XL, which employs a digital phase locked loop technique, combined with a high quality reference oscillator, provides the tuning voltages for voltage controlled oscillators to generate very stable, low noise signals for RF and IF local oscillators. Serial data is transferred into the LMX233XL via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX233XL family features very low current consumption;

LMX2330L—5.0 mA at 3V, LMX2331L—4.0 mA at 3V, LMX2332L—3.0 mA at 3V.

The LMX233XL are available in a TSSOP 20-pin, CSP 24-pin surface mount plastic package, and thin CSP 20-pin surface mount plastic package.

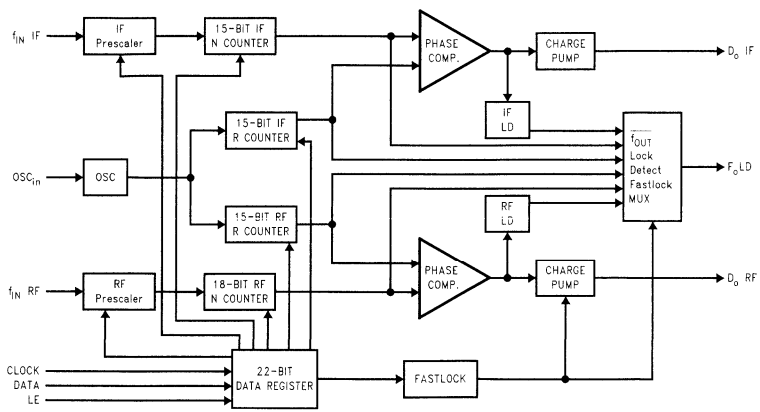
Features

- Ultra low current consumption
- 2.7V to 5.5V operation
- Selectable synchronous or asynchronous powerdown mode:
  I_{CC} = 1 μA typical at 3V
- Dual modulus prescaler:
  LMX2330L (RF) 32/33 or 64/65
  LMX2331L/32L (RF) 64/65 or 128/129
  LMX2330L/31L/32L (IF) 8/9 or 16/17
- Selectable charge pump TRI-STATE® mode
- Selectable charge pump current levels
- Selectable Fastlock™ mode
- Upgrade and compatible to LMX233XA family

Applications

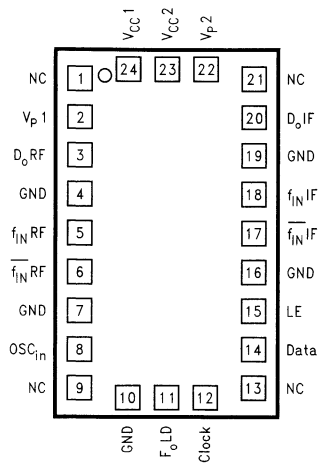
- Portable Wireless Communications (PCS/PCN, cordless)
- Cordless and cellular telephone systems
- Wireless Local Area Networks (WLANs)
- Cable TV tuners (CATV)
- Other wireless communication systems

Functional Block Diagram



Connection Diagrams

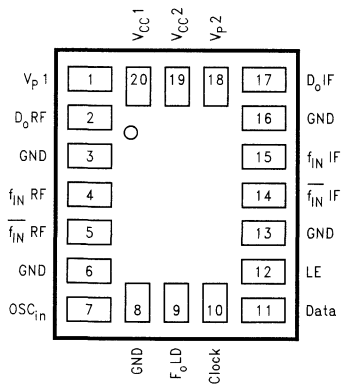
Chip Scale Package (SLB)
(Top View)



01280639

Order Number LMX2330LSBX, LMX2331LSLBX or LMX2332LSLBX
NS Package Number SLB24A

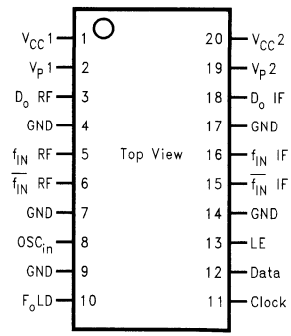
20-Pin Thin Chipscale Package (SLD)
(Top View)



01280640

Order Number LMX2330LSLDX, LMX2331LSLDX, or LMX2332LSLDX
NS Package Number SLD20A

Thin Shrink Small Outline Package (TM)
(Top View)



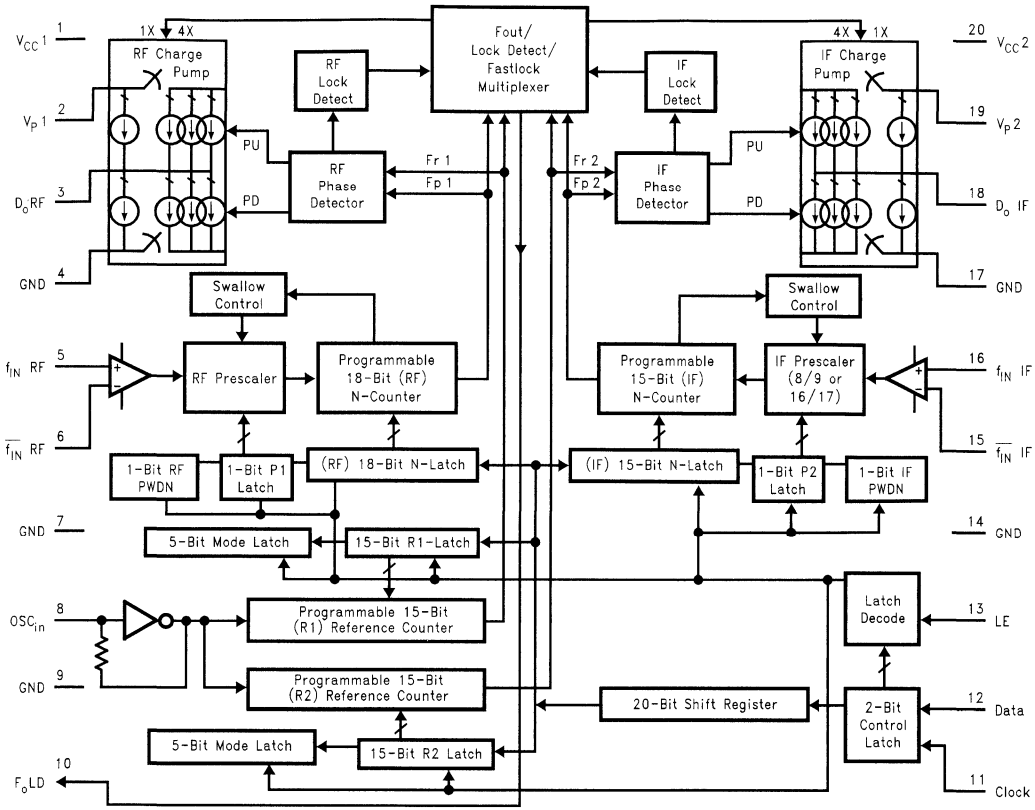
01280602

Order Number LMX2330LTM, LMX2331LTM or LMX2332LTM
Order Number LMX2330LTMX, LMX2331LTMX, or LMX2332LTMX
NS Package Number MTC20

Pin Descriptions

Pin No. LMX233XLSLD 20-pin Thin CSP Package	Pin No. LMX233XLSLB 24-pin CSP Package	Pin No. LMX233XLTM 20-pin TSSOP Package	Pin Name	I/O	Description
20	24	1	$V_{CC}1$	—	Power supply voltage input for RF analog and RF digital circuits. Input may range from 2.7V to 5.5V. $V_{CC}1$ must equal $V_{CC}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
1	2	2	V_P1	—	Power Supply for RF charge pump. Must be ≥ V_{CC}.
2	3	3	D_o RF	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
3	4	4	GND	—	Ground for RF digital circuitry.
4	5	5	f_{IN} RF	I	RF prescaler input. Small signal input from the VCO.
5	6	6	$\overline{f_{IN}}$ RF	I	RF prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
6	7	7	GND	—	Ground for RF analog circuitry.
7	8	8	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
8	10	9	GND	—	Ground for IF digital, MICROWIRE™, F_oLD, and oscillator circuits.
9	11	10	F_oLD	O	Multiplexed output of the RF/IF programmable or reference dividers, RF/IF lock detect signals and Fastlock mode. CMOS output *(see Programmable Modes).*
10	12	11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.
11	14	12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
12	15	13	LE	I	Load enable high impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one o the 4 appropriate latches (control bit dependent).
13	16	14	GND	—	Ground for IF analog circuitry.
14	17	15	$\overline{f_{IN}}$ IF	I	IF prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
15	18	16	f_{IN} RF	I	IF prescaler input. Small signal input from the VCO.
16	19	17	GND	—	Ground for IF digital, MICROWIRE, F_oLD, and oscillator circuits.
17	20	18	D_o IF	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
18	22	19	V_P2	—	Power Supply for IF charge pump. Must be ≥ V_{CC}.
19	23	20	$V_{CC}2$	—	Power supply voltage input for IF analog, IF digital, MICROWIRE, F_oLD, and oscillator circuits. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
X	1, 9, 13, 21	X	NC	—	No connect.

Block Diagram



Note: The RF prescaler for the LMX2331L/32L is either 64/65 or 128/129, while the prescaler for the LMX2330L is 32/33 or 64/65.
Note: V_{CC}1 supplies power to the RF prescaler, N-counter, R-counter and phase detector. V_{CC}2 supplies power to the IF prescaler, N-counter, phase detector, R-counter along with the OSC_{in} buffer, MICROWIRE, and F_oLD. V_{CC}1 and V_{CC}2 are clamped to each other by diodes and must be run at the same voltage level.
Note: V_P1 and V_P2 can be run separately as long as $V_P \geq V_{CC}$.

National Semiconductor

PRELIMINARY

LMX2335L/LMX2336L
PLLatinum™ Low Power Dual Frequency Synthesizer for RF Personal Communications

LMX2335L 1.1 GHz/1.1 GHz
LMX2336L 2.0 GHz/1.1 GHz

General Description

The LMX2335L and LMX2336L are monolithic, integrated dual frequency synthesizers, including two high frequency prescalers, and are designed for applications requiring two RF phase-lock loops. They are fabricated using National's 0.5µ ABiC V silicon BiCMOS process.

The LMX2335L/36L contains two dual modulus prescalers. A 64/65 or a 128/129 prescaler can be selected for each RF synthesizer. A second reference divider chain is included in the IC for improved system noise. The LMX2335L/36L combined with a high quality reference oscillator, two loop filters, and two external voltage controlled oscillators generates very stable low noise RF local oscillator signals.

Serial data is transferred into the LMX2335L/36L via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2335L/36L feature very low current consumption; LMX2335L 4.0 mA at 5V, LMX2336L 5.5 mA at 5V. The LMX2335L is available in SO, TSSOP and CSP 16-pin surface mount plastic packages. The LMX2336L is available in a TSSOP 20-pin and CSP 24-pin surface mount plastic package.

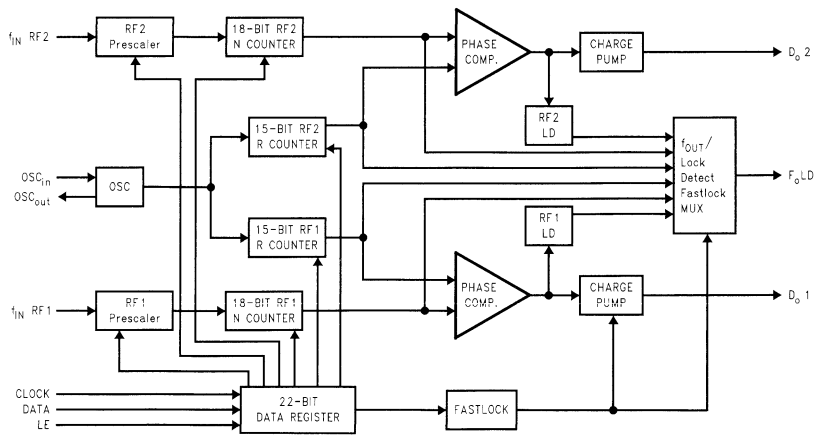
Features

- Ultra low current consumption
- 2.7V to 5.5V operation
- Selectable synchronous and asynchronous powerdown mode:
  I_{CC} = 1 µA (typ)
- Dual modulus prescaler: 64/65 or 128/129
- Selectable charge pump TRI-STATE® mode
- Selectable charge pump current levels
- Selectable Fastlock™ mode
- Upgrade and compatible to LMX2335/36
- Small-outline, plastic, surface mount TSSOP package
- LMX2336 available in CSP package

Applications

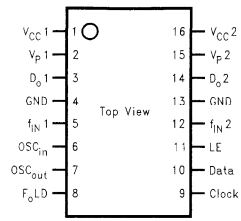
- Cellular telephone systems (AMPS, ETACS, RCR-27)
- Cordless telephone systems (DECT, ISM , PHS, CT-1+)
- Personal Communication Systems (DCS-1800, PCN-1900)
- Dual Mode PCS phones
- Cable TV Tuners (CATV)
- Other wireless communication systems

Functional Block Diagram



Connection Diagrams

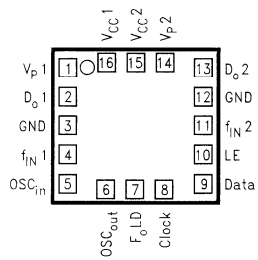
LMX2335L
(Top View)



DS012807-2

Order Number LMX2335LM or LM2335LTM
NS Package Number M16A and MTC16

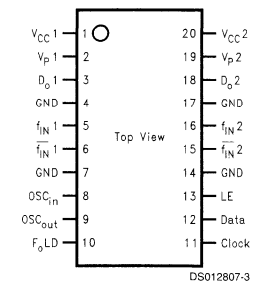
LMX2335L
(Top View)



DS012807-38

Order Number LMX2335LSLB
NS Package Number SLB16A

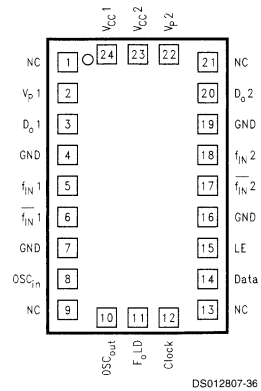
LMX2336L
(Top View)



DS012807-3

Order Number LMX2336LTM
NS Package Number MTC20

LMX2336L
(Top View)



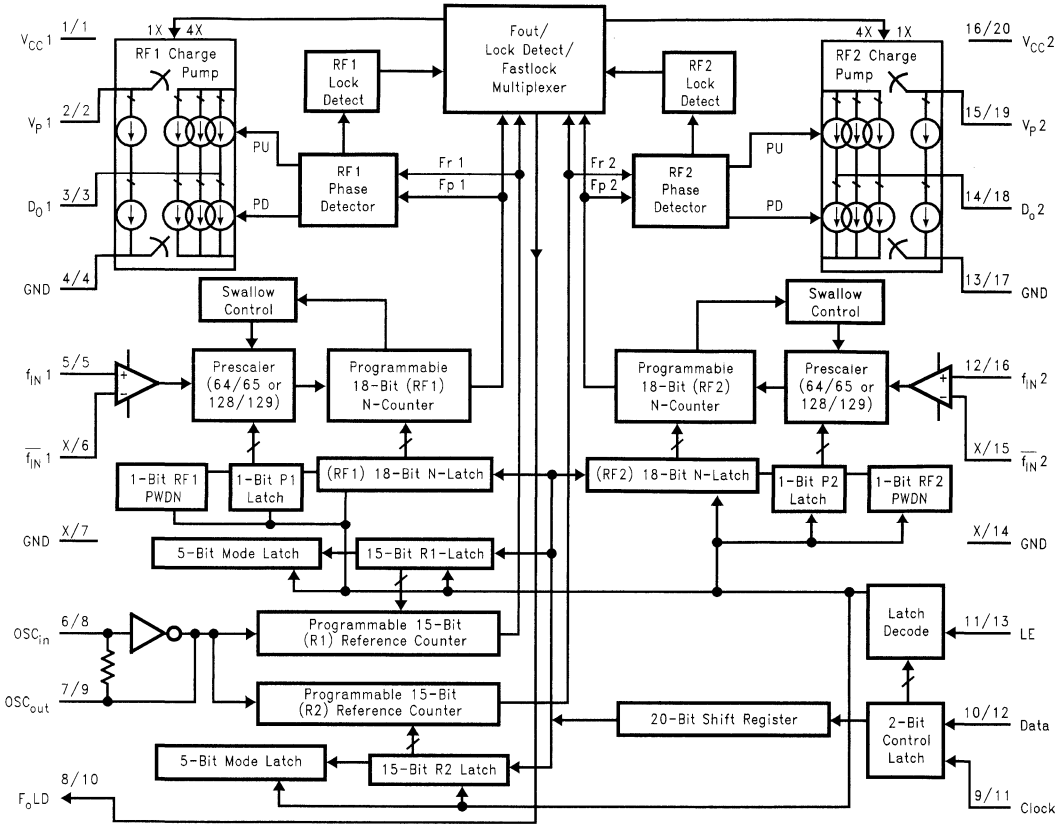
DS012807-36

Order Number LMX2336LSLB
NS Package Number SLB24A

Pin Descriptions

Pin No. 2336LTM	Pin No. 2336LSLB	Pin No. 2335LTM	Pin No. 2335LSLB	Pin Name	I/O	Description
1	24	1	16	$V_{CC}1$		Power supply voltage input for RF1 analog and RF1 digital circuits. Input may range from 2.7V to 5.5V. $V_{CC}1$ must equal $V_{CC}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	2	2	1	V_p1		Power supply for RF1 charge pump. Must be ≥ V_{CC}.
3	3	3	2	D_o1	O	RF1 charge pump output. For connection to a loop filter for driving the input of an external VCO.
4	4	4	3	GND		LMX2335L: Ground for RF1 analog and RF1 digital circuits. LMX2336L: Ground for RF digital circuits.
5	5	5	4	f_{IN} 1	I	RF1 prescaler input. Small signal input from the VCO.
6	6	X	X	/f_{IN} 1	I	RF1 prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with loss of some sensitivity.
7	7	X	X	GND		Ground for RF1 analog circuitry.
8	8	6	5	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
9	10	7	6	OSC_{out}	O	Oscillator output.
10	11	8	7	F_oLD	O	Multiplexed output of the programmable or reference dividers, lock detect signals and Fastlock mode. CMOS output *(see Programmable Modes).*
11	12	9	8	Clock	I	High impedance CMOS Clock input. Data for the various latches is clocked in on the rising edge, into the 20-bit shift register.
12	14	10	9	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	15	11	10	LE	I	Load enable high impedance CMOS input. When LE goes HIGH data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
14	16	X	X	GND		Ground for RF2 analog circuitry.
15	17	X	X	/f_{IN}2	I	RF2 prescaler complementary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with loss of some sensitivity.
16	18	12	11	f_{IN} 2	I	RF2 prescaler input. Small signal input from the VCO.
17	19	13	12	GND		LMX2335L: Ground for RF2 analog, RF2 digital, MICROWIRE, F_oLD and Oscillator circuits. LMX2336L: Ground for IF digital, MICROWIRE, F_oLD and oscillator circuits.
18	20	14	13	D_o 2	O	RF2 charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	22	15	14	V_p2		Power supply for RF2 charge pump. Must be ≥ V_{CC}.
20	23	16	15	$V_{CC}2$		Power supply voltage input for RF2 analog, RF2 digital, MICROWIRE, F_oLD and oscillator circuits. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
X	1, 9, 13, 21	X	X	NC		No connect.

Block Diagram



Note 1: $V_{CC}1$ supplies power to the RF1 prescaler, N-counter, R-counter, and phase detector. $V_{CC}2$ supplies power to the RF2 prescaler, N-counter, phase detector, R-counter along with the OSC_{in} buffer, MICROWIRE, and F_oLD. $V_{CC}1$ and $V_{CC}2$ are clamped to each other by diodes and must be run at the same voltage level.

Note 2: V_P1 and V_P2 can be run separately as long as $V_P \geq V_{CC}$.

LMX2335L Pin # → 8/10 ← LMX2336L Pin #
Pin Name → F_oLD
X signifies a function not bonded out to a pin

National Semiconductor

LMX2350/LMX2352
PLLatinum Fractional N RF / Integer N IF Dual Low Power Frequency Synthesizer

LMX2350 2.5 GHz/550 MHz
LMX2352 1.2 GHz/550 MHz

General Description

The LMX2350/2352 is part of a family of monolithic integrated fractional N/ Integer N frequency synthesizers designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using National's 0.5µ ABiC V silicon BiCMOS process. The LMX2350/2352 contains dual modulus prescalers along with modulo 15 or 16 fractional compensation circuitry in the RF divider. A 16/17 or 32/33 prescale ratio can be selected for the LMX2350, and the LMX2352 provides 8/9 or 16/17 prescale ratios. The IF circuitry for both the LMX2350 and LMX2352 contains an 8/9 prescaler, and is fully programmable. Using a fractional N phase locked loop technique, the LMX2350 /52 can generate very stable low noise control signals for UHF and VHF voltage controlled oscillators (VCOs).

For the RF PLL, a highly flexible 16 level programmable charge pump supplies output current magnitudes from 100µA to 1.6mA. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock™ mode. Serial data is transferred into the LMX2350/2352 via a three wire interface (Data, LE, Clock). Supply voltage can range from 2.7 V to 5.5 V. The LMX2350/ LMX2352 family features very low current consumption; typically LMX2350 (2.5 GHz) 6.5 mA, LMX2352 (1.2 GHz) 4.75 mA at 3.0V. The LMX2350/2352 are available in a 24-pin TSSOP and 24-pin CSP surface mount plastic package.

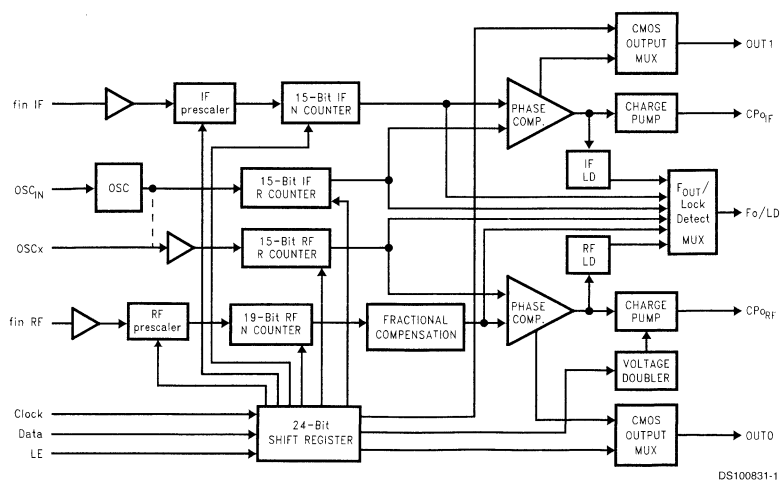
Features

- 2.7 V to 5.5 V operation
- Low current consumption
  LMX2350: Icc = 6.75mA typ at 3v
  LMX2352: Icc = 5.00mA typ at 3v
- Programmable or logical power down mode
  Icc = 5 µA typ at 3v
- Modulo 15 or 16 fractional RF N divider supports ratios of 1, 2, 3, 4, 5, 8, 15, or 16
- Programmable charge pump current levels
  RF 100µA to 1.6mA in 100µA steps
  IF 100µA or 800 µA
- Digital filtered lock detect

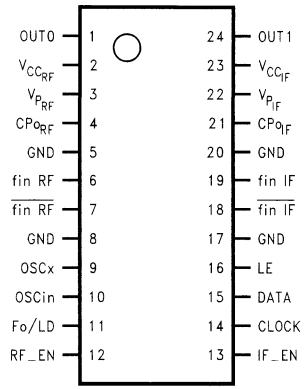
Applications

- Portable wireless communications (PCS/PCN, cordless)
- Dual mode cellular telephone systems
- Zero blind slot TDMA systems
- Spread spectrum communication systems (CDMA)
- Cable TV Tuners (CATV)

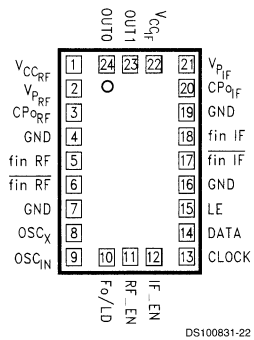
Block Diagram



Connection Diagrams



Order Number LMX2350TM, LMX2350TMX, LMX2352TM, LMX2352TMX
NS Package Number MTC24



Order Number LMX2350SLBX, LMX2352SLBX
NS Package Number SLB24A

Pin Descriptions

Pin No. for CSP Package	Pin No. for TSSOP package	Pin Name	I/O	Description
24	1	OUT0	O	Programmable CMOS output. Level of the output is controlled by IF_N [17] bit.
1	2	Vcc_{RF}	-	RF PLL power supply voltage input. Must be equal to Vcc_{IF}. May range from 2.7 V to 5.5 V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	3	V_{PRF}	-	Power supply for RF charge pump. Must be $\geq V_{cc_{RF}}$ and $V_{cc_{IF}}$.
3	4	$CP_{o_{RF}}$	O	RF charge pump output. Connected to a loop filter for driving the control input of an external VCO.
4	5	GND	-	Ground for RF PLL digital circuitry.
5	6	fin RF	I	RF prescaler input. Small signal input from the VCO.
6	7	$\overline{\text{fin RF}}$	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
7	8	GND	-	Ground for RF PLL analog circuitry.

Pin Descriptions (Continued)

Pin No. for CSP Package	Pin No. for TSSOP package	Pin Name	I/O	Description
8	9	OSCx	I/O	Dual mode oscillator output or RF R counter input. Has a Vcc/2 input threshold when configured as an input and can be driven from an external CMOS or TTL logic gate. Can also be configured as an output to work in conjunction with OSCin to form a crystal oscillator. (See functional description 1.1 and programming description 3.1.)
9	10	OSCin	I	Oscillator input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit. (See functional description 1.1 and programming description 3.1.)
10	11	FoLD	O	Multiplexed output of N or R divider and RF/IF lock detect. Active High/Low CMOS output except in analog lock detect mode. (See programming description 3.1.5.)
11	12	RF_EN	I	RF PLL Enable. Powers down RF N and R counters, prescaler, and will TRI-STATE® the charge pump output when LOW. Bringing RF_EN high powers up RF PLL depending on the state of RF_CTL_WORD. (See functional description 1.9.)
12	13	IF_EN	I	IF PLL Enable. Powers down IF N and R counters, prescaler, and will TRI-STATE the charge pump output when LOW. Bringing IF_EN high powers up IF PLL depending on the state of IF_CTL_WORD. (See functional description 1.9.)
13	14	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked into the 24 - bit shift register on the rising edge.
14	15	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
15	16	LE	I	Load enable high impedance CMOS input. Data stored in the shift registers is loaded into one of the 4 internal latches when LE goes HIGH. (See functional description 1.7.)
16	17	GND	-	Ground for IF analog circuitry.
17	18	$\overline{\text{fin IF}}$	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
18	19	fin IF	I	IF prescaler input. Small signal input from the VCO.
19	20	GND	-	Ground for IF digital circuitry.
20	21	CPo_{IF}	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
21	22	Vp_{IF}	-	Power supply for IF charge pump. Must be $\geq V_{cc_{RF}}$ and $V_{cc_{IF}}$.
22	23	Vcc_{IF}	-	IF power supply voltage input. Must be equal to Vcc_{RF} . Input may range from 2.7 V to 5.5 V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
23	24	OUT1	O	Programmable CMOS output. Level of the output is controlled by IF_N [18] bit.

National Semiconductor

LMX2353
PLLatinum™ Fractional N Single 2.5 GHz Low Power Frequency Synthesizer

General Description

The LMX2353 is a monolithic integrated fractional N frequency synthesizer, designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using National's 0.5µ ABiC V silicon BiCMOS process. The LMX2353 contains dual modulus prescalers along with modulo 15 or 16 fractional compensation circuitry in the N divider. A 16/17 or 32/33 prescale ratio can be selected for the LMX2353. Using a fractional N phase locked loop technique, the LMX2353 can generate very stable low noise control signals for UHF and VHF voltage controlled oscillators (VCOs).

The LMX2353 has a highly flexible 16 level programmable charge pump which supplies output current magnitudes from 100 µA to 1.6 mA. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock™ mode. Serial data is transferred into the LMX2353 via a three wire interface (Data, LE, Clock). Supply voltage can range from 2.7 V to 5.5 V. The LMX2353 features very low current consumption; typically 5.5 mA at 3.0V. The LMX2353 is available in a 16-pin TSSOP or a 16-pin CSP surface mount plastic package.

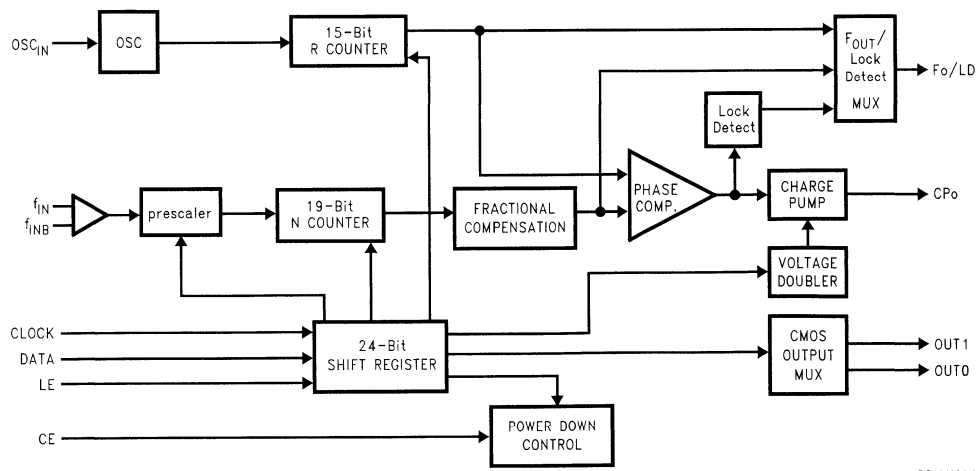
Features

- 2.7 V – 5.5 V operation
- Low Current Consumption
  I_{CC} = 5.5 mA typ at V_{CC} = 3.0 V
- Programmable or Logical Power Down Mode
  I_{CC} = 5 µA typ at V_{CC} = 3.0 V
- Modulo 15 or 16 fractional N divider
  Supports ratios of 1, 2, 3, 4, 5, 8, 15, or 16
- Programmable charge pump current levels
  100 µA to 1.6 mA in 100 µA steps
- Digital Filtered Lock Detect

Applications

- Portable wireless communications (PCS/PCN, cordless)
- Zero blind slot TDMA systems
- Cellular and Cordless telephone systems
- Spread spectrum communication systems (CDMA)
- Cable TV Tuners (CATV)

Functional Block Diagram



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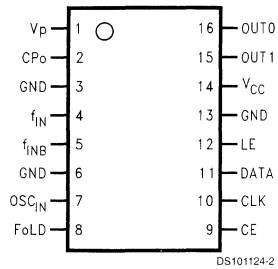
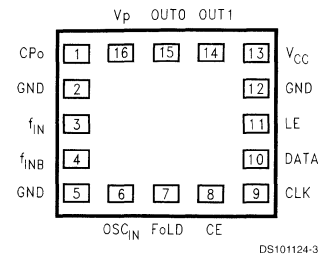
Connection Diagrams



TOP VIEW
Order Number LMX2353TM or LMX2353TMX
See NS Package Number MTC16



TOP VIEW
Order Number LMX2353SLBX
See NS Package Number SLB16A

Pin Descriptions

Pin No.		Pin Name	I/O	Description
CSP	TSSOP			
16	1	V_P	—	Power supply for charge pump. Must be ≥ V_{CC}.
1	2	CP_O	O	Charge pump output. Connected to a loop filter for driving the control input of an external VCO.
2	3	GND	—	Ground for PLL digital circuitry.
3	4	f_{IN}	I	RF prescaler input. Small signal input from the VCO.
4	5	f_{INB}	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
5	6	GND	—	Ground for PLL analog circuitry.
6	7	OSC_{IN}	I	Oscillator input. A CMOS inverting gate input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.
7	8	F_oLD	O	Multiplexed output of N or R divider and lock detect. CMOS output.
8	9	CE	I	PLL Enable. Powers down N and R counters, prescalers, and TRI-STATE® charge pump output when LOW. Bringing CE high powers up PLL depending on the state of CTL_WORD.
9	10	CLK	I	High impedance CMOS Clock input. Data for the various counters is clocked into the 24-bit shift register on the rising edge.
10	11	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
11	12	LE	I	Load enable high impedance CMOS input. Data stored in the shift registers is loaded into one of the 4 internal latches when LE goes HIGH.
12	13	GND	—	Ground.
13	14	V_{CC}	—	PLL power supply voltage input. May range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
14	15	OUT1	—	Programmable CMOS output. Level of the output is controlled by F2[18] bit.
15	16	OUT0	—	Programmable CMOS output. Level of the output is controlled by F2[17] bit.

National Semiconductor

LMX2354
PLLatinum Fractional N RF/ Integer N IF Dual Low Power Frequency Synthesizer
LMX2354 2.5 GHz/550 MHz

General Description

The LMX2354 is part of a family of monolithic integrated fractional N/Integer N frequency synthesizers designed to be used in a local oscillator subsystem for a radio transceiver. It is fabricated using National's 0.5 μ ABiC V silicon BiCMOS process. The LMX2354 contains quadruple modulus prescalers along with modulo 15 or 16 fractional compensation circuitry in the RF divider. The LMX2354 provides a continuous divide ratio of 80 to 32767 in 16/17/20/21 (1.2 GHz–2.5 GHz) fractional mode and 40 to 16383 in 8/9/12/13 (550 MHz–1.2 GHz) fractional mode. The IF circuitry for the LMX2354 contains an 8/9 prescaler, and is fully programmable. Using a fractional N phase locked loop technique, the LMX2354 can generate very stable low noise control signals for UHF and VHF voltage controlled oscillators (VCOs).

For the RF PLL, a highly flexible 16 level programmable charge pump supplies output current magnitudes from 100 μA to 1.6 mA. Two uncommitted CMOS outputs can be used to provide external control signals, or configured to FastLock mode. Serial data is transferred into the LMX2354 via a three wire interface (Data, LE, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX2354 family features very low current consumption; typically LMX2354 (2.5 GHz) — 7.0 mA. The LMX2354 are available in a 24-pin TSSOP surface mount plastic package and 24-pin CSP.

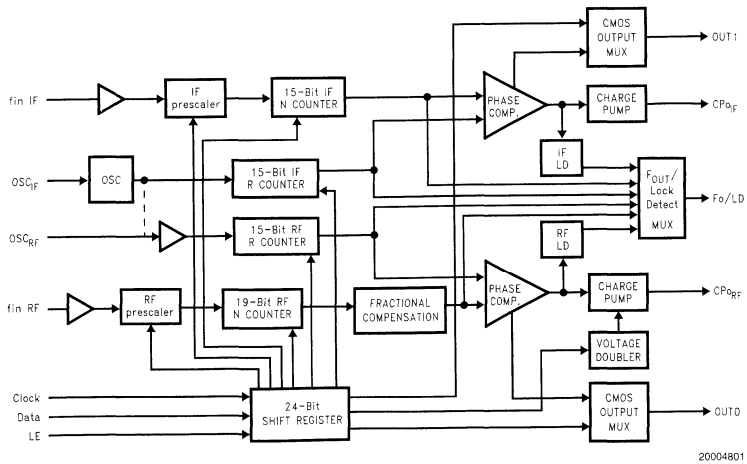
Features

- Pin compatible/functional equivalent to the LMX2350
- Enhanced Low Noise Fractional Engine
- 2.7V to 5.5V operation
- Low current consumption
  LMX2354: I_{CC} = 7 mA typical at 3V
- Programmable or logical power down mode:
  I_{CC} = 5 μA typical at 3V
- Modulo 15 or 16 fractional RF N divider supports ratios of 1, 2, 3, 4, 5, 8, 15, or 16
- Programmable charge pump current levels
  RF 100 μA to 1.6 mA in 100 μA steps
  IF 100 μA or 800 μA
- Digital filtered lock detect
- Available in 24-pin TSSOP and 24-pin CSP

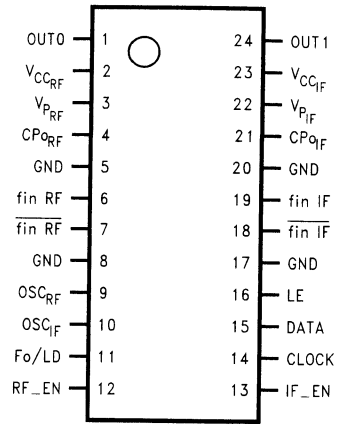
Applications

- Portable wireless communications (PCS/PCN, cordless)
- Dual mode cellular telephone systems
- Zero blind slot TDMA systems
- Spread spectrum communication systems (CDMA)
- Cable TV Tuners (CATV)

Functional Block Diagram



Connection Diagrams



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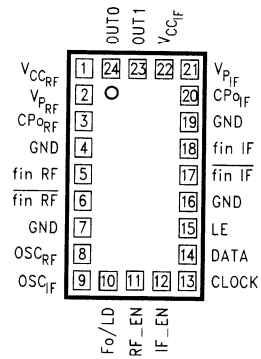
Order Number LMX2354TM or LMX2354TMX
See NS Package Number MTC24



20004822

Order Number LMX2354SLBX
See NS Package Number SLB24A

Pin Descriptions

Pin No. for TSSOP Package	Pin No. for CSP Package	Pin Name	I/O	Description
1	24	OUT0	O	Programmable CMOS output. Level of the output is controlled by IF_N [17] bit.
2	1	$V_{CC_{RF}}$	—	RF PLL power supply voltage input. Must be equal to Vcc_{IF}. May range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
3	2	$V_{P_{RF}}$	—	Power supply for RF charge pump. Must be ≥ $V_{CC_{RF}}$ and $V_{CC_{IF}}$.
4	3	$CP_{o_{RF}}$	O	RF charge pump output. Connected to a loop filter for driving the control input of an external VCO.
5	4	GND	—	Ground for RF PLL digital circuitry.
6	5	fin RF	I	RF prescaler input. Small signal input from the VCO.
7	6	$\overline{\text{fin RF}}$	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
8	7	GND	—	Ground for RF PLL analog circuitry.
9	8	OSC_{RF}	I	Dual mode oscillator output or RF R counter input. Has a $V_{CC}/2$ input threshold when configured as an input and can be driven from an external CMOS or TTL logic gate.
10	9	OSC_{IF}	I	Oscillator input which can be configured to drive both the IF and RF R counter inputs or only the IF R counter depending on the state of the OSC programming bit. (See functional description 1.1 and programming description 3.1.)
11	10	Fo/LD	O	Multiplexed output of N or R divider and RF/IF lock detect. CMOS output. (See programming description 3.1.5.)
12	11	RF_EN	I	RF PLL Enable. Powers down RF N and R counters, prescaler, and TRI-STATE® charge pump output when LOW. Bringing RF_EN high powers up RF PLL depending on the state of RF_CTL_WORD. (See functional description 1.9.)
13	12	IF_EN	I	IF PLL Enable. Powers down IF N and R counters, prescaler, and TRI-STATE charge pump output when LOW. Bringing IF_EN high powers up IF PLL depending on the state of IF_CTL_WORD. (See functional description 1.9.)
14	13	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked into the 24-bit shift register on the rising edge.
15	14	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
16	15	LE	I	Load Enable high impedance CMOS input. Data stored in the shift registers is loaded into one of the 4 internal latches when LE goes HIGH. (See functional description 1.7.)
17	16	GND	—	Ground for IF analog circuitry.
18	17	$\overline{\text{fin IF}}$	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.
19	18	fin IF	I	IF prescaler input. Small signal input from the VCO.
20	19	GND	—	Ground for IF digital circuitry.
21	20	CPo_{IF}	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
22	21	V_{PIF}	—	Power supply for IF charge pump. Must be ≥ $V_{CC_{RF}}$ and $V_{CC_{IF}}$.
23	22	$V_{CC_{IF}}$	—	IF power supply voltage input. Must be equal to $V_{CC_{RF}}$. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
24	23	OUT1	O	Programmable CMOS output. Level of the output is controlled by IF_N [18] bit.

National Semiconductor

LMX2370/LMX2371/LMX2372
PLLatinum™ Dual Frequency Synthesizer for RF Personal Communications

LMX2370 2.5 GHz/1.2 GHz
LMX2371 2.0 GHz/1.2 GHz
LMX2372 1.2 GHz/1.2 GHz

General Description

The LMX237x family of monolithic, integrated dual frequency synthesizers, including prescalers, is designed to be used as a first and second local oscillator for dual mode or dual conversion transceivers. It is fabricated using National's 0.5u ABiCV silicon BiCMOS process. The LMX237x contains two dual modulus prescalers. A 32/33 or a 16/17 prescaler can be selected for the 2.5 GHz and 2.0 GHz RF synthesizers with the 16/17 prescaler rated for input frequencies below 1.2 GHz. A 16/17 or an 8/9 prescaler can be selected for the 1.2 GHz RF synthesizers with the 8/9 prescaler rated for input frequencies below 550 MHz. Using a digital phase locked loop technique, the LMX237x can generate very stable, low noise control signals for UHF and VHF voltage controlled oscillators (VCOs). Serial data is transferred into the LMX237x via a 1.8 V three wire interface (Data, Enable, Clock) compatible with low voltage baseband processors. Supply voltage can range from 2.7V to 5.5V. The LMX237x family features very low current consumption typically: LMX2370 - 6.0 mA at 3V, LMX2371 - 5.0 mA at 3V, LMX2372 - 4.0 mA at 3V.

The LMX237x are available in a 24-pad chip scale (CSP) or a 20-pin TSSOP surface mount plastic package.

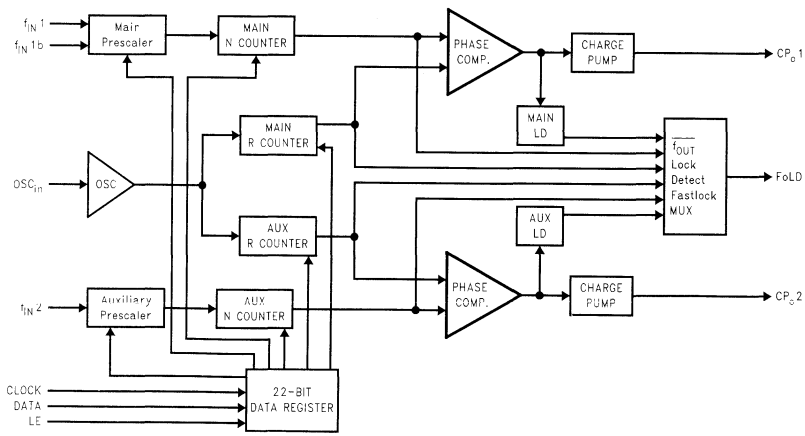
Features

- 2.7V–5.5V operation
- Ultra low current consumption
- Low phase detector noise floor
- Low voltage MICROWIRE™ interface (1.8V up to V_{CC})
- Low prescaler values
  - 32/33 at $f_{IN} \leq 2.5$ GHz
  - 16/17 at $f_{IN} \leq 1.2$ GHz
  - 8/9 at $f_{IN} \leq 550$ MHz
- Selectable charge pump current levels
- Selectable FastLock™ mode
- Enhanced ESD protection
- Available in small 24-pad chip scale package (3.5 x 4.5 x 1.0 mm)

Applications

- Portable wireless communications (PCS/PCN, cordless)
- Dual mode cellular telephone systems
- Spread spectrum communication systems (CDMA)
- Cable TV tuners (CATV)

Functional Block Diagram



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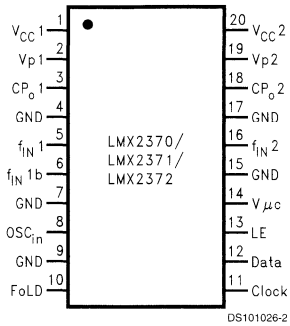
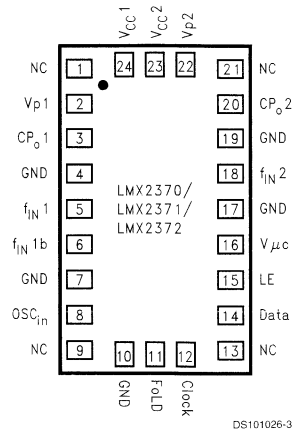
Connection Diagrams

TSSOP 20-Pin Package



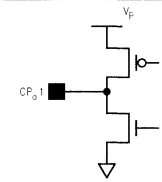
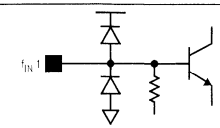
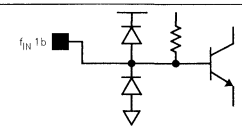
Top View
Order Number LMX2370TM, LMX2370TMX, LMX2371TM, LMX2371TMX, LMX2372TM or LMX2372TMX
See NS Package Number MTC20

CSP 24-Pin Package

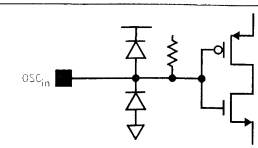
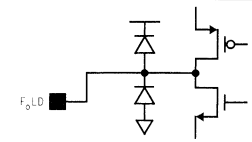
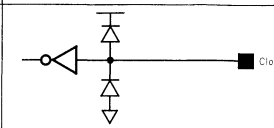
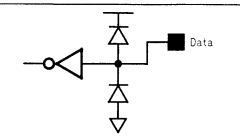
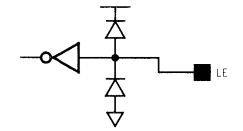
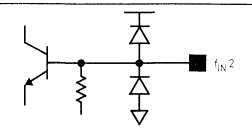
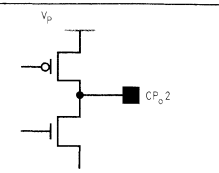


Top View
Order Number LMX2370SLBX, LMX2371SLBX or LMX2372SLBX
See NS Package Number SLB24A

Pin Descriptions

Pin No.		Pin Name	I/O	Description	
24-Pin CSP	20-Pin TSSOP				
24	1	$V_{CC}1$	—	Power supply voltage input for RF analog and RF digital circuits. Input may range from 2.7V to 5.5V. $V_{CC}1$ must equal $V_{CC}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	
2	2	Vp1	—	Power supply for Main charge pump. Must be ≥ V_{CC}.	
3	3	CP_o1	O	Internal Main charge pump output. For connection to a loop filter for driving the input of an external VCO.	
4	4	GND	—	Ground for Main digital circuitry.	
5	5	$f_{IN}1$	I	Main prescaler input. Small signal input from the VCO.	
6	6	$f_{IN}1b$	I	Main prescaler complementary input. For single ended operation, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane.	
7	7	GND	—	Ground for Main analog circuitry.	

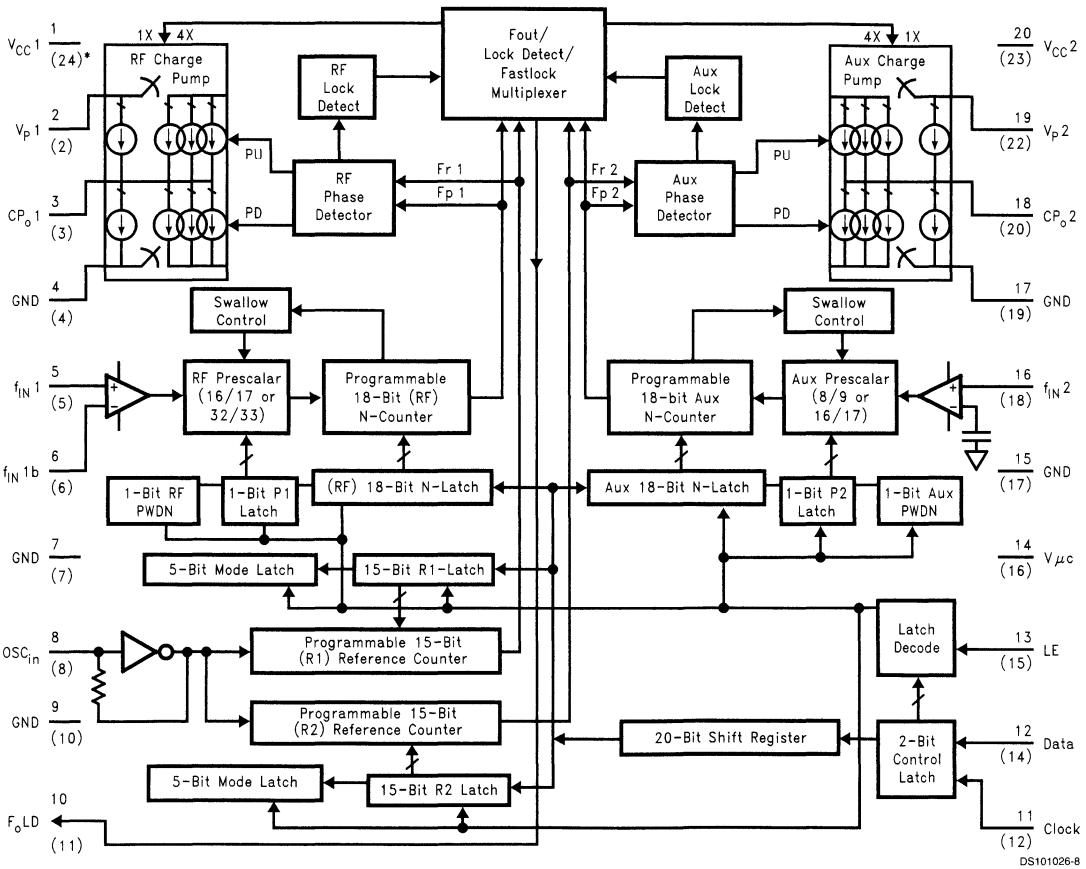
Pin Descriptions (Continued)

Pin No.		Pin Name	I/O	Description	
24-Pin CSP	20-Pin TSSOP				
8	8	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TTL logic gate.	
10	9	GND	—	Ground for Aux digital, MICROWIRE, FoLD, and oscillator circuits.	
11	10	Fo/LD	O	Multiplexed output of the Main/Aux programmable or reference dividers, Main/Auxiliary lock detect signals and Fastlock mode. CMOS output *(see Programmable Modes in the Datasheet).*	
12	11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.	
14	12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.	
15	13	LE	I	Load enable. High impedance CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).	
16	14	Vμc	—	Power supply for MICROWIRE circuitry. Must be $\leq V_{CC}$. Typically connected to same supply level as μprocessor or baseband controller to enable programming at low voltages.	
17	15	GND	—	Ground for Aux analog circuitry.	
18	16	$f_{IN}2$	I	Auxiliary prescaler input. Small signal input from the VCO.	
19	17	GND	—	Ground for Aux digital, MICROWIRE, FoLD, and oscillator.	
20	18	CP_o2	O	Aux internal charge pump output. For connection to a loop filter for driving the input of an external VCO.	
22	19	Vp2	—	Power supply for Aux charge pump. Must be $\geq V_{CC}$.	

Pin Descriptions (Continued)

Pin No.		Pin Name	I/O	Description	
24-Pin CSP	20-Pin TSSOP				
23	20	$V_{CC}2$	—	Power supply voltage input for Aux analog, Aux digital, FoLD, and oscillator circuits. Input may range from 2.7V to 5.5V. $V_{CC}2$ must equal $V_{CC}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	
1, 9, 13, 21	—	NC	—	No Connect	

Block Diagram (Note 1)



Note 1: * The numbers in () represent the equivalent chipscale package (CSP) pinout

National Semiconductor

PRELIMINARY

LMX3161
Single Chip Radio Transceiver

General Description

The LMX3161 Single Chip Radio Transceiver is a monolithic, integrated radio transceiver optimized for use in a Digital Enhanced Cordless Telecommunications (DECT) system. It is fabricated using National's ABiC V BiCMOS process (f_T = 18 GHz).

The LMX3161 contains phase locked loop (PLL), transmit and receive functions. The 1.1 GHz PLL block is shared between transmit and receive section. The transmitter includes a frequency doubler, and a high frequency buffer. The receiver consists of a 2.0 GHz low noise mixer, an intermediate frequency (IF) amplifier, a high gain limiting amplifier, a frequency discriminator, a received signal strength indicator (RSSI), and an analog DC compensation loop. The PLL, doubler, and buffers can be used to implement open loop modulation along with an external VCO and loop filter. The circuit features on-chip voltage regulation to allow supply voltages ranging from 3.0V to 5.5V. Two additional voltage regulators provide a stable supply source to external discrete stages in the Tx and Rx chains.

The IF amplifier, high gain limiting amplifier, and discriminator are optimized for 110 MHz operation, with a total IF gain of 85 dB. The single conversion receiver architecture provides a low cost, high performance solution for communications systems. The RSSI output may be used for channel quality monitoring.

The Single Chip Radio Transceiver is available in a 48-pin 7mm X 7mm X 1.4mm PQFP surface mount plastic package.

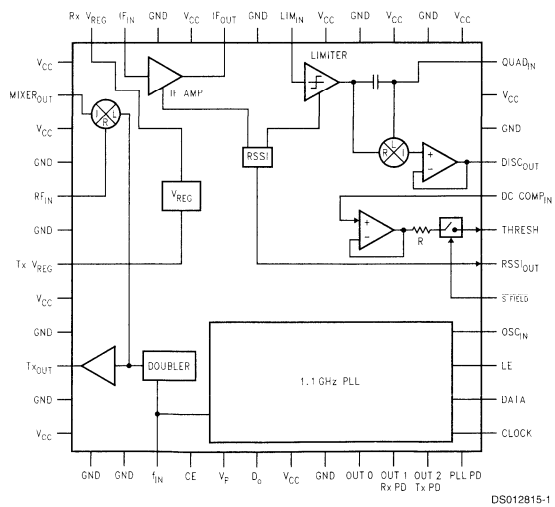
Features

- Single chip solution for DECT RF transceiver
- RF sensitivity to −93 dBm; RSSI sensitivity to −100 dBm
- Two regulated voltage outputs for discrete amplifiers
- High gain (85 dB) intermediate frequency strip
- Allows unregulated 3.0V–5.5V supply voltage
- Power down mode for increased current savings
- System noise figure 6.5 dB (typ)

Applications

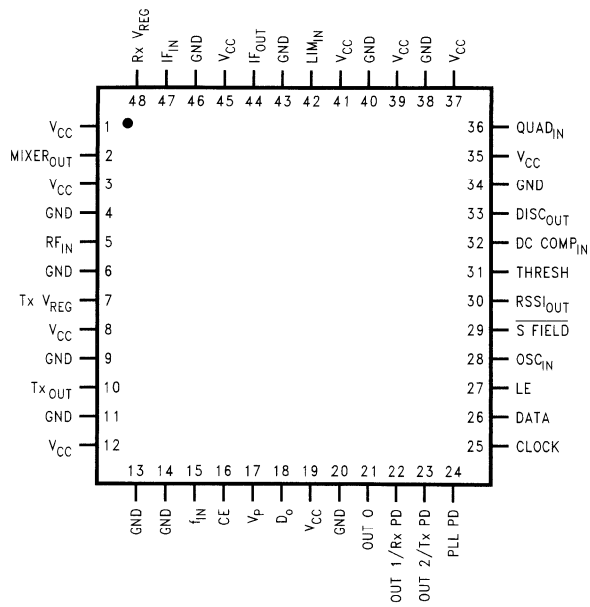
- Digital Enhanced Cordless Telecommunications (DECT)
- Personal wireless communications (PCS/PCN)
- Wireless local area networks (WLANs)
- Other wireless communications systems

Block Diagram



DS012815-1

LMX3161 Pin Diagram



DS012815-2

Top View
Order Number LMX3161VBH or LMX3161VBHX
See NS Package Number VBH48A

LMX3161 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
1	V_{CC}	—	Power supply for CMOS section of PLL and ESD bussing.
2	$MIXER_{OUT}$	O	IF output from the mixer.
3	V_{CC}	—	Power supply for mixer section.
4	GND	—	Ground.
5	RF_{IN}	I	RF input to the mixer.
6	GND	—	Ground.
7	Tx V_{REG}	—	Regulated power supply for external PA gain stage.
8	V_{CC}	—	Power supply for analog sections of PLL and doubler.
9	GND	—	Ground.
10	Tx_{OUT}	O	Frequency doubler output.
11	GND	—	Ground.
12	V_{CC}	—	Power supply for analog sections of PLL and doubler.
13	GND	—	Ground.
14	GND	—	Ground.
15	f_{IN}	I	RF Input to PLL and frequency doubler.
16	CE	I	Chip Enable. Pulling LOW powers down entire chip. Taking CE HIGH powers up the appropriate functional blocks depending on the state of bits F6, F7, F11, and F12 programmed in F-latch. It is necessary to initialize the internal registers once, after the power up reset. The registers' contents are kept even in power-down condition.
17	V_P	—	Power supply for charge pump.
18	D_o	O	Charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	V_{CC}	—	Power supply for CMOS section of PLL and ESD bussing.
20	GND	—	Ground.
21	OUT 0	O	Programmable CMOS output. Refer to Function Register Programming Description section for details.
22	Rx PD/OUT 1	I/O	Receiver power down control input or programmable CMOS output. Refer to Function Register Programming Description section for details.
23	Tx PD/OUT 2	I/O	Transmitter power down control input or programmable CMOS output. Refer to Function Register Programming Description section for details.
24	PLL PD	I	PLL power down control input. LOW for PLL normal operations, and HIGH for PLL power saving.
25	CLOCK	I	MICROWIRE™ clock input. High impedance CMOS input with Schmitt Trigger.
26	DATA	I	MICROWIRE data input. High impedance CMOS input with Schmitt Trigger.
27	LE	I	MICROWIRE load enable input. High impedance CMOS input with Schmitt Trigger.
28	OSC_{IN}	I	Oscillator input. High impedance CMOS input with feedback.
29	$\overline{S\ FIELD}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator threshold is held by the external capacitor.
30	$RSSI_{OUT}$	O	Received signal strength indicator (RSSI) output.
31	THRESH	O	Threshold level to external comparator.
32	DC $COMP_{IN}$	I	Input to DC compensation circuit.
33	$DISC_{OUT}$	O	Demodulated output of discriminator.
34	GND	—	Ground.
35	V_{CC}	—	Power supply for the discriminator circuit.
36	$QUAD_{IN}$	I	Quadrature input for tank circuit.
37	V_{CC}	—	Power supply for limiter output stage.
38	GND	—	Ground.
39	V_{CC}	—	Power supply for limiter gain stages.
40	GND	—	Ground.
41	V_{CC}	—	Power supply for IF amplifier gain stages.

LMX3161 Pin Diagram (Continued)

Pin No.	Pin Name	I/O	Description
42	LIM_{IN}	I	IF input to the limiter.
43	GND	—	Ground.
44	IF_{OUT}	O	IF output from IF amplifier.
45	V_{CC}	—	Power supply for IF amplifier output.
46	GND	—	Ground.
47	IF_{IN}	I	IF input to IF amplifier.
48	Rx V_{REG}	—	Regulated power supply for external LNA stages.

National Semiconductor

PRELIMINARY

LMX3162
Single Chip Radio Transceiver

General Description

The LMX3162 Single Chip Radio Transceiver is a monolithic, integrated radio transceiver optimized for use in ISM 2.45 GHz wireless systems. It is fabricated using National's ABiC V BiCMOS process (f_T = 18 GHz).

The LMX3162 contains phase locked loop (PLL), transmit and receive functions. The 1.3 GHz PLL is shared between transmit and receive sections. The transmitter includes a frequency doubler, and a high frequency buffer. The receiver consists of a 2.5 GHz low noise mixer, an intermediate frequency (IF) amplifier, a high gain limiting amplifier, a frequency discriminator, a received signal strength indicator (RSSI), and an analog DC compensation loop. The PLL, doubler, and buffers can be used to implement open loop modulation along with an external VCO and loop filter. The circuit features on-chip voltage regulation to allow supply voltages ranging from 3.0V to 5.5V. Two additional voltage regulators provide a stable supply source to external discrete stages in the Tx and Rx chains.

The IF amplifier, high gain limiting amplifier, and discriminator are optimized for 110 MHz operation, with a total IF gain of 85 dB. The single conversion receiver architecture provides a low cost, high performance solution for communications systems. The RSSI output may be used for channel quality monitoring.

The Single Chip Radio Transceiver is available in a 48-pin 7mm X 7mm X 1.4mm PQFP surface mount plastic package.

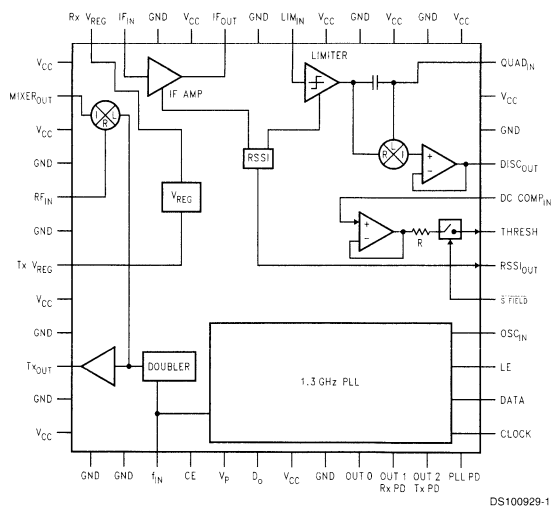
Features

- Single chip solution for ISM 2.45 GHz RF transceiver
- System RF sensitivity to −93 dBm; RSSI sensitivity to −100 dBm
- Two regulated voltage outputs for discrete amplifiers
- High gain (85 dB) intermediate frequency strip
- Allows unregulated 3.0V–5.5V supply voltage
- Power down mode for increased current savings
- System noise figure 6.5 dB (typ)

Applications

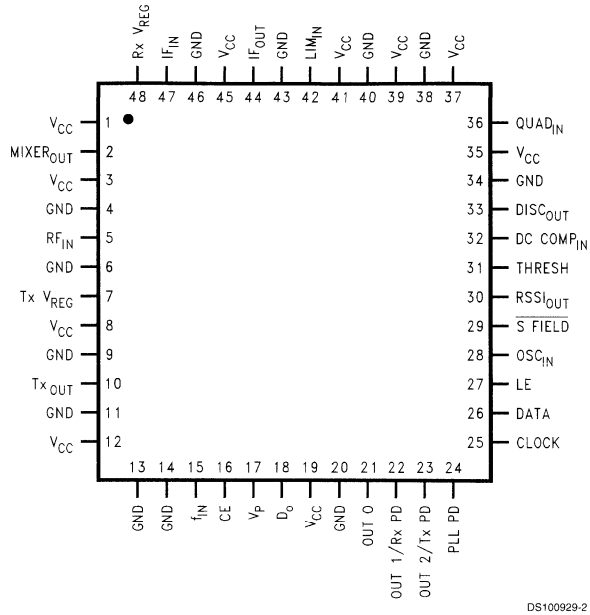
- ISM 2.45 GHz frequency band wireless systems
- Personal wireless communications (PCS/PCN)
- Wireless local area networks (WLANs)
- Other wireless communications systems

Block Diagram



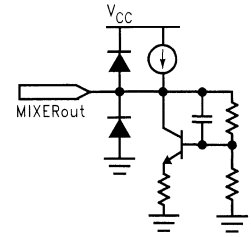
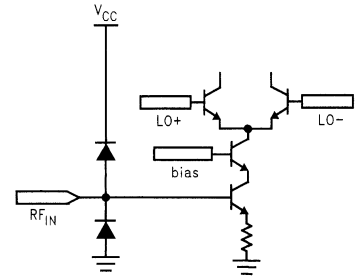
DS100929-1

LMX3162 Connection Diagram

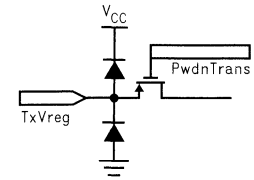
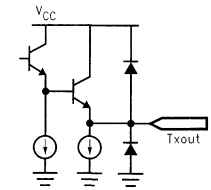
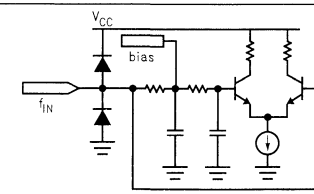
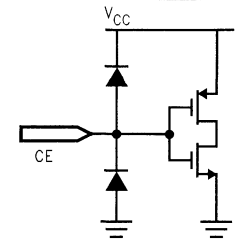
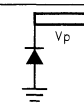
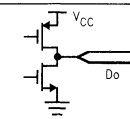


Top View
Order Number LMX3162VBH or LMX3162VBHX
See NS Package Number VBH48A

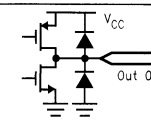
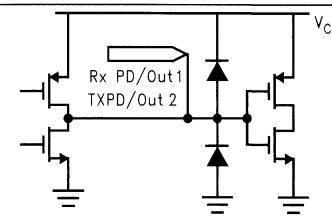
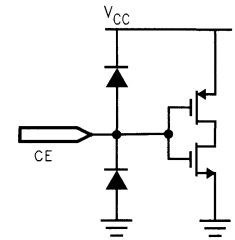
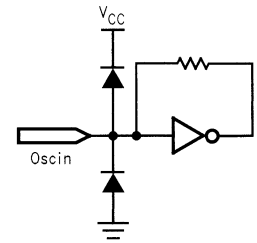
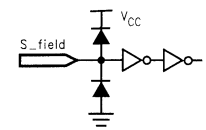
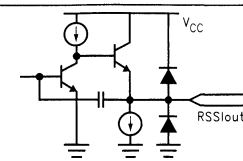
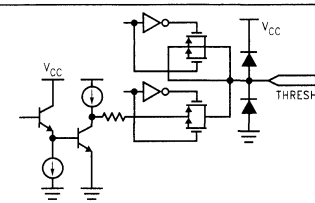
Pin Descriptions

Pin No.	Pin Name	I/O	Description	
1	V_{CC}	—	Power supply for CMOS section of PLL and ESD bussing.	
2	$MIXER_{OUT}$	O	IF output from the mixer.	
3	V_{CC}	—	Power supply for mixer section.	
4	GND	—	Ground.	
5	RF_{IN}	I	RF input to the mixer.	
6	GND	—	Ground.	

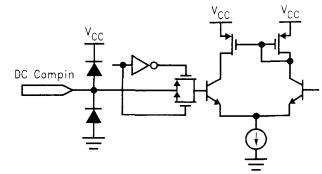
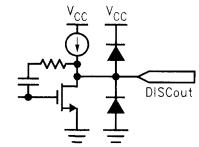
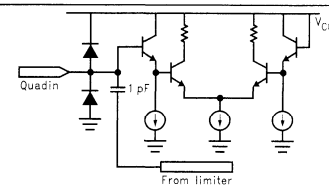
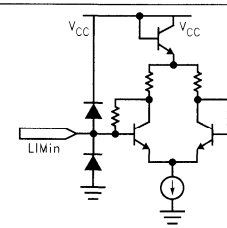
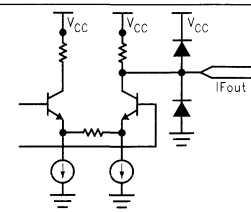
Pin Descriptions (Continued)

Pin No.	Pin Name	I/O	Description	
7	Tx V_{REG}	—	Regulated power supply for external PA gain stage.	
8	V_{CC}	—	Power supply for analog sections of PLL and doubler.	
9	GND	—	Ground.	
10	Tx_{OUT}	O	Frequency doubler output.	
11	GND	—	Ground.	
12	V_{CC}	—	Power supply for analog sections of PLL and doubler.	
13	GND	—	Ground.	
14	GND	—	Ground.	
15	f_{IN}	I	RF Input to PLL and frequency doubler.	
16	CE	I	Chip Enable. Pulling LOW powers down entire chip. Taking CE HIGH powers up the appropriate functional blocks depending on the state of bits F6, F7, F11, and F12 programmed in F-latch. It is necessary to initialize the internal registers once, after the power up reset. The registers' contents are kept even in power-down condition.	
17	V_P	—	Power supply for charge pump.	
18	D_o	O	Charge pump output. For connection to a loop filter for driving the input of an external VCO.	
19	V_{CC}	—	Power supply for CMOS section of PLL and ESD bussing.	
20	GND	—	Ground.	

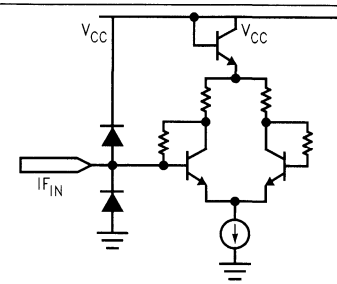
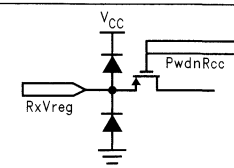
Pin Descriptions (Continued)

Pin No.	Pin Name	I/O	Description	
21	OUT 0	O	Programmable CMOS output. Refer to Function Register Programming Description section for details.	
22	Rx PD/OUT 1	I/O	Receiver power down control input or programmable CMOS output. Refer to Function Register Programming Description section for details.	
23	Tx PD/OUT 2	I/O	Transmitter power down control input or programmable CMOS output. Refer to Function Register Programming Description section for details.	
24	PLL PD	I	PLL power down control input. LOW for PLL normal operations, and HIGH for PLL power saving.	
25	CLOCK	I	MICROWIRE™ clock input. High impedance CMOS input with Schmitt Trigger.	
26	DATA	I	MICROWIRE data input. High impedance CMOS input with Schmitt Trigger.	
27	LE	I	MICROWIRE load enable input. High impedance CMOS input with Schmitt Trigger.	
28	OSC_{IN}	I	Oscillator input. High impedance CMOS input with feedback.	
29	$\overline{S\ FIELD}$	I	DC compensation circuit enable. While LOW, the DC compensation circuit is enabled and the threshold is updated through the DC compensation loop. While HIGH, the switch is opened, and the comparator threshold is held by the external capacitor.	
30	$RSSI_{OUT}$	O	Received signal strength indicator (RSSI) output.	
31	THRESH	O	Threshold level to external comparator.	

Pin Descriptions (Continued)

Pin No.	Pin Name	I/O	Description	
32	DC $COMP_{IN}$	I	Input to DC compensation circuit.	
33	$DISC_{OUT}$	O	Demodulated output of discriminator.	
34	GND	—	Ground.	
35	V_{CC}	—	Power supply for the discriminator circuit.	
36	$QUAD_{IN}$	I	Quadrature input for tank circuit.	
37	V_{CC}	—	Power supply for limiter output stage.	
38	GND	—	Ground.	
39	V_{CC}	—	Power supply for limiter gain stages.	
40	GND	—	Ground.	
41	V_{CC}	—	Power supply for IF amplifier gain stages.	
42	LIM_{IN}	I	IF input to the limiter.	
43	GND	—	Ground.	
44	IF_{OUT}	O	IF output from IF amplifier.	
45	V_{CC}	—	Power supply for IF amplifier output.	
46	GND	—	Ground.	

Pin Descriptions (Continued)

Pin No.	Pin Name	I/O	Description	
47	IF_{IN}	I	IF input to IF amplifier.	
48	Rx V_{REG}	—	Regulated power supply for external LNA stages.	

National Semiconductor

PRELIMINARY

LMX3305
Triple Phase Locked Loop for RF Personal Communications

General Description

The LMX3305 contains three Phase Locked Loops (PLL) on a single chip. It has a RF PLL, an IF Rx PLL and an IF Tx PLL for CDMA applications. The RF fractional-N PLL uses a 16/17/20/21 quadruple modulus prescaler for PCS application and a 8/9/12/13 quadruple modulus prescaler for cellular application. Both quadruple modulus prescalers offer modulo 1 through 16 fractional compensation circuitry. The RF fractional-N PLL can be programmed to operate from 800 MHz to 1400MHz in cellular band and 1200MHz to 2300 MHz in PCS band. The IF Rx PLL and the IF Tx PLL are integer-N frequency synthesizers that operate from 45 MHz to 600 MHz with 8/9 dual modulus prescalers. Serial data is transferred into the LMX3305 via a microwire interface (Clock, Data, & LE).

The RF PLL provides a fastlock feature allowing the loop bandwidth to be increased by 3X during initial lock-on.

The supply voltage of the LMX3305 ranges from 2.7V to 3.6V. It typically consumes 9 mA of supply current and is packaged in a 24-pin CSP package.

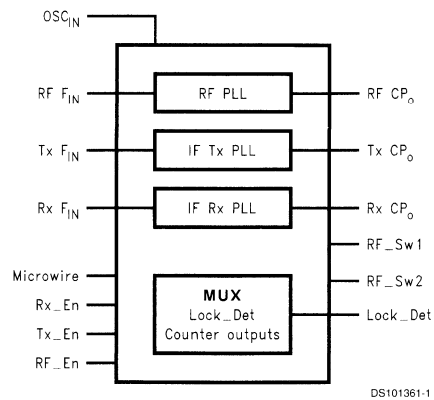
Features

- Three PLLs integrated on a single chip
- RF PLL fractional-N counter
- 16/17/20/21 RF quadruple modulus prescaler for PCS application
- 8/9/12/13 RF quadruple modulus prescaler for cellular application
- 2.7V to 3.6V operation
- Low current consumption: I_{CC} = 9 mA (typ) at 3.0V
- Programmable or logical power down mode: I_{CC} = 10 µA (typ) at 3.0V
- RF PLL Fastlock feature with timeout counter
- Digital lock detect
- Microwire Interface with data preset
- 24-pin CSP package

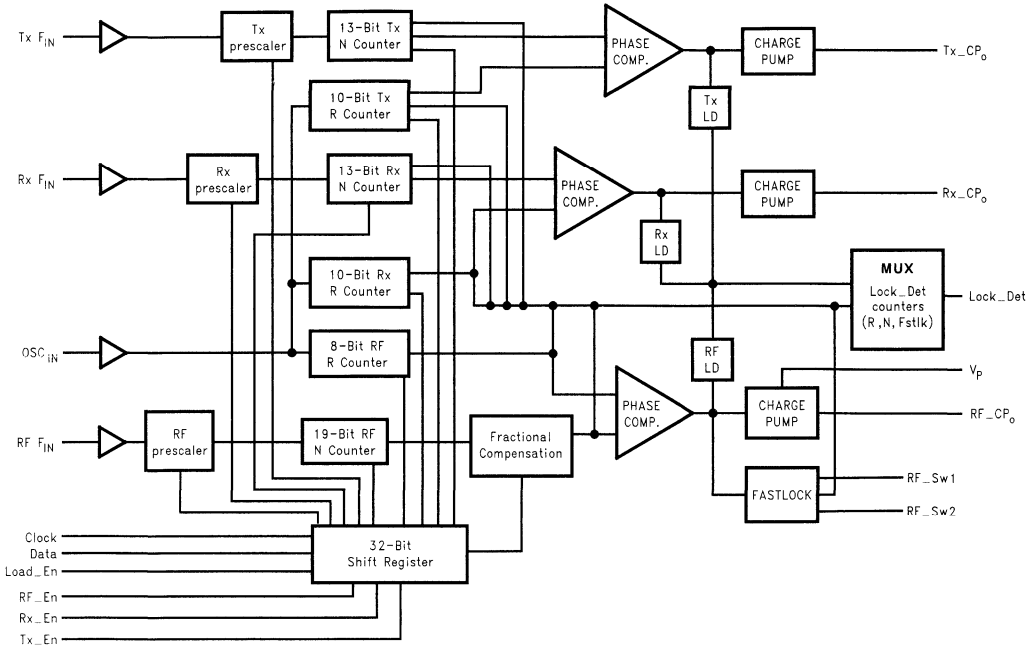
Applications

- CDMA Cellular telephone systems

Block Diagram

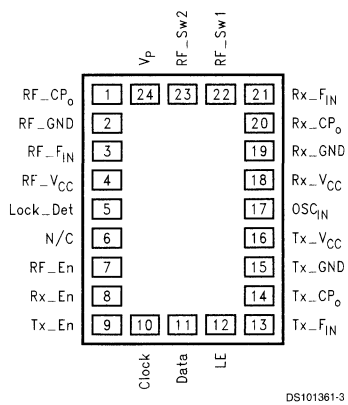


Functional Block Diagram



DS101361-2

Connection Diagram



DS101361-3

Top View
Order Number LMX3305SLBX
See NS Package Number SLB24A

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	RF_CP_o	O	Charge pump output for RF PLL. For connection to a loop filter for driving the input of an external VCO.
2	RF_GND	PWR	RF PLL ground.
3	RF_F_{IN}	I	RF prescaler input. Small signal input from the RF Cellular or PCS VCO.
4	RF_V_{CC}	PWR	RF PLL power supply voltage. Input may range from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. Tx V_{CC} = Rx V_{CC} = RF V_{CC}.
5	Lock_Det	O	Multiplexed output of the RF, Rx, and Tx PLL's analog or digital lock detects. The outputs from the R, N and Fastlock counters can also be selected for test purposes. Refer to Section 2.3.4 for more detail.
6	N/C		No Connect.
7	RF_En	I	RF PLL enable pin. A LOW on RF En powers down the RF PLL and TRI-STATE®s the RF PLL charge pump.
8	Rx_En	I	Rx PLL enable pin. A LOW on Rx En powers down the Rx PLL and TRI-STATEs the Rx PLL charge pump.
9	Tx_En	I	Tx PLL enable pin. A LOW on Tx En powers down the Tx PLL and TRI-STATEs the Tx PLL charge pump.
10	Clock	I	High impedance CMOS clock input. Data for the various counters is clocked on the rising edge into the CMOS input.
11	Data	I	Binary serial data input. Data entered MSB first.
12	LE	I	High impedance CMOS input. When LE goes LOW, data is transferred into the shift registers. When LE goes HIGH, data is transferred from the internal registers into the appropriate latches.
13	Tx_F_{IN}	I	Tx prescaler input. Small signal input from the Tx VCO.
14	Tx_CP_o	O	Charge pump output for Tx PLL. For connection to a loop filter for driving the input of an external VCO.
15	Tx_GND		Tx PLL ground.
16	Tx_V_{CC}	PWR	Tx PLL power supply voltage input. Input may range from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. Tx V_{CC} = Rx V_{CC} = RF V_{CC}.
17	OSC_{IN}	I	PLL reference input which has a $V_{CC}/2$ input threshold and can be driven from an external CMOS or TLL logic gate. The R counter is clocked on the falling edge of the OSC_{IN} signal.
18	Rx_V_{CC}	PWR	Rx PLL power supply voltage. Input ranges from 2.7V to 3.6V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane. Tx V_{CC} = Rx V_{CC} = RF V_{CC}.
19	Rx_GND	PWR	Rx PLL ground.
20	Rx_CP_o	O	Charge pump output for Rx PLL. For connection to a loop filter for driving the input of an external VCO.
21	Rx_F_{IN}	I	Rx prescaler input. Small signal input from the Rx VCO.
22	RF_Sw1	O	An open drain NMOS output which can be use for bandswitching or Fastlocking the RF PLL. (During Fastlock mode a second loop filter damping resistor can be switched in parallel with the first to ground.) Refer to Section 2.5.3 for more detail.
23	RF_Sw2	O	An open drain NMOS output which can be use for bandswitching or Fastlocking the RF PLL. (During Fastlock mode a second loop filter damping resistor can be switched in parallel with the first to ground.) Refer to Section 2.5.3 for more detail.
24	V_P	O	RF PLL charge pump power supply. An internal voltage doubler can be enabled in 3V applications to allow the RF charge pump to operate over a wider tuning range.

National Semiconductor

PRELIMINARY

LMX5001
Dedicated Bluetooth Link Controller

General Description

The LMX5001 Dedicated Bluetooth™ Link Controller has been designed to interface with the LMX3162, Single Chip Radio Transceiver to provide a rapid design path to a complete Bluetooth physical layer.

The LMX5001 also offers a low power and cost competitive solution to the Bluetooth Link Controller function.

The LMX5001 can be attached to a Link Management Controller, or Host processor performing the Link Management function to implement a complete Bluetooth interface.

Bluetooth is a world-wide recognized wireless communication standard, which operates in the ISM band (2.4 GHz), offering a low cost and convenient wireless replacement for data/voice cable links between fixed and mobile electronic devices.

Utilizing a GFSK modulation scheme, with frequency hopping, Bluetooth is able to offer a low power, low cost, robust and spectrally efficient spread spectrum packet data system.

Features

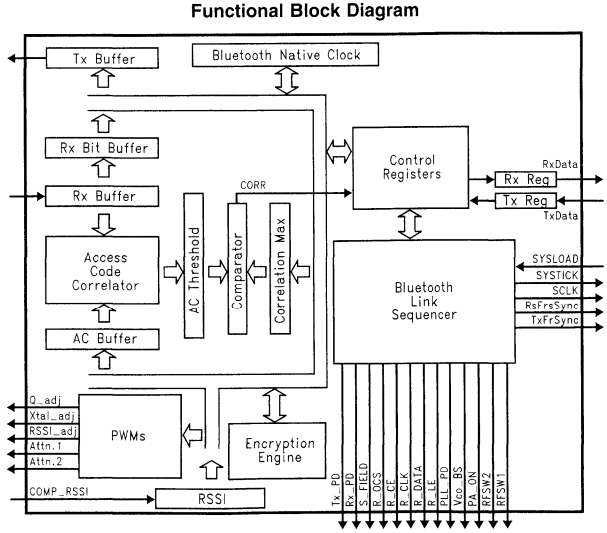
- Bluetooth Specification 1.0B compliant
- Bluetooth physical layer, available today
- Supports Class 1, 2 and 3 Bluetooth (20 dBm, 4 dBm and 0 dBm links)
- 1/8 bit sampling resolution
- Power management for Tx, Rx and PLL
- Piconet and Scatternet communication capable
- Good Bluetooth radio range coverage (when coupled with the LMX3162)
- Support for RSSI channel quality monitoring
- Bluetooth Encryption Engine

Applications

- PCMCIA Cards
- Mobile Phones
- Laptop PCs
- Palmtop PCs
- Desktop PCs
- Computer Peripherals
- Wireless Modems
- PDAs
- Palmtops
- P.O.T.S
- Digital Cameras
- Fax
- Printers
- Bar-code Readers
- Notepads
- Cordless Headsets
- In-vehicle Communications

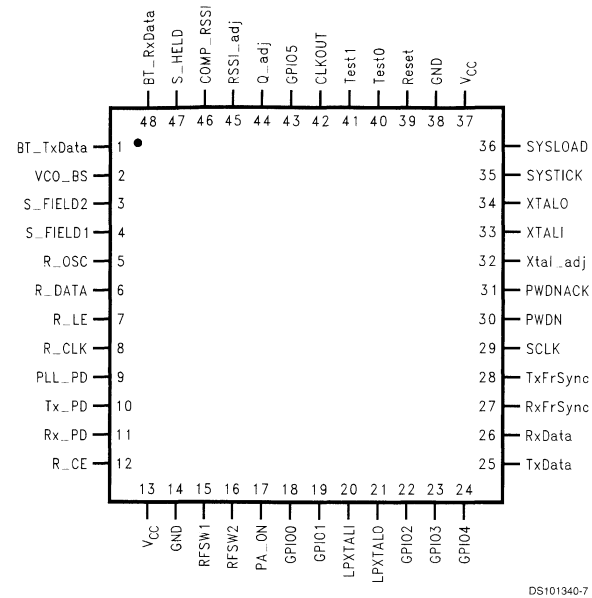
Block Diagram

Functional Block Diagram



DS101340-1

Connection Diagram



DS101340-7

Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	BT_TxData	O	Transmit data
2	VCO_BS	O	VCO band switch control signal.
3	S_FIELD2	O	LMX3162 DC compensation circuit enable. This signal is enabled (low) throughout the correlation phase.
4	S_FIELD1	O	LMX3162 DC compensation circuit enable. At the beginning of the correlation phase this signal is enabled (low) for 15 µs. For the remainder of the correlation phase this signal is PWM by 1/8 (cycle time = 1 µs).
5	R_OSC	O	LMX3162 4 MHz oscillator input to the PLL synthesizer. This signal is only enabled when the LMX3162 is active.
6	R_DATA	O	MICROWIRE™ data to LMX3162.
7	R_LE	O	MICROWIRE load enable to LMX3162.
8	R_CLK	O	MICROWIRE clock to LMX3162.
9	PLL_PD	O	LMX3162 PLL power down. This signal is used to open the PLL loop or powering down the PLL. The PLL loop is opened when transmitting to make it possible to FSK modulate the VCO. When receiving it is optional to open the PLL loop (configured by the PLLOpenRX bit in threshold_msb).
10	Tx_PD	O	LMX3162 Transmitter power down. For power conservation, the Transmitter is only powered during Transmit Frames.
11	Rx_PD	O	LMX3162 Receiver power down. For power conservation, the Receiver is only powered during Receive Frames.
12	R_CE	O	LMX3162 chip enable. When the LMX5001 is in Idle Mode the LMX3162 is powered down.
13	V_{CC}	Power	+3.3V
14	GND	Power	0V
15	RFSW1	O	Antenna switch control.
16	RFSW2	O	Antenna switch control. This signal is RFSW1 inverted,
17	PA_ON	O	Switches the external PA on/off for 20 dBm/0 dBm transmission, respectively.

Pin Descriptions (Continued)

Pin No.	Pin Name	I/O	Description
18	GPIO0 (XTAL Config)	I/O	XTAL configuration during reset (Note 1).
19	GPIO1 (XTAL Config)	I/O	XTAL configuration during reset (Note 1).
20	LPXTALI	I	128 kHz XTAL connection for low power mode. This is used in low power mode. If the low power mode is not used it is not necessary with at XTAL here. External 128 kHz clock can also be feed in here.
21	LPXTALO	O	128 kHz XTAL connection.
22	GPIO2	I/O	General Purpose I/O
23	GPIO3	I/O	General Purpose I/O
24	GPIO4	I/O	General Purpose I/O
25	TxData	I	LCI Data Transmit
26	RxData	O	LCI Data Receive
27	RxFrSync	O	LCI Receive Frame Sync.
28	TrFrSync	O	LCI Transmit Frame Sync.
29	SCLK	O	LCI Serial Clock.
30	PWDN	O	Power Down to Link Management Controller
31	PWDNACK	I	Power Down Acknowledge from Link Management Controller
32	Xtal_adj	O	PWM signal to make adjustments to the XTAL.
33	XTALI	I	16 MHz XTAL connection. (External clock input).
34	XTALO	O	16 MHz XTAL connection.
35	SYSTICK	O	Systick generated from the internal LMX5001 Master/Slave Counter.
36	SYSLOAD	I	When low holds the LMX5001 in Idle Mode. A rising edge causes a system load After a rising edge the LMX5001 will start to load control data from and store status information to the LMC via the LCI.
37	V_{CC}	Power	
38	GND	Power	
39	Reset	I	Reset. After Reset is released the LMX5001 will be in Idle Mode, awaiting a SYSLOAD.
40	Test0	I	Should be tied low. This signal is used in production test.
41	Test1	I	Should be lied low. This signal is used in production test.
42	CLKOUT	O	Xtal clock output to Link Management Controller. This signal can be disabled using the Sysload Command (for power saving).
43	GPIO5	I/O	General Purpose I/O
44	Q_adj	O	PWM signal to make it possible to adjust the quadrature tank circuit to the LMX3162.
45	RSSI_adj	O	PWM signal for use in creating an RSSI AD converter.
46	COMP_RSSI	I	Output from the external comparator in the RSSI AD converter.
47	S_Field3	O	DC Compensation circuit enable. At the beginning of the correlation phase, this signal is enabled (low) for 15 µs.
48	BT_RxData	I	Receive data.

Note 1: During Reset GPIO0 and GPIO1 are sampled to setup the Xtal division ratio. The assumed external Xtal frequency is derived using the following relationship:

GPIO1	GPIO0	Xtal Division Ratio
Low	Low	Divide by 2 (i.e., 16 MHz XTAL or clock input).
Low	High	Divide by 3 (i.e., 24 MHz XTAL or clock input).
High	Low	Divide by 4 (i.e., 32 MHz XTAL or clock input).
High	High	Not used.

After Reset is completed, GPIO0 and GPIO1 can be used as normal general purpose I/Os.

Section 20
Appendices

Section 20 Contents

National Semiconductor

Device Marking Conventions

National Semiconductor marks devices sold in order to provide device identification and manufacturing traceablility information. The method of presenting the information marked on the device is dependent on the size of the device package and the area available for marking, as well as the nature and specifications of the device.

The information presented here describes the majority of the device markings a customer will observe. Specific package marking for a given device is given in the datasheet for that device. A package may have up to four lines of marking. The following information is usually contained in each line.

First line: Manufacturing information

- Company logo
- Wafer and/or assembly plant codes (optional) (see *Table 1* and *Table 2*)
- Date code (see *Table 3*, *Table 4*, and *Table 5*)
- Die run (wafer lot) code

Second Line: Device part number

- Device family (see *Table 6*)
- Device type
- Options
- Package code (see *Table 7*)

Third or fourth line: Optional, depending on device, package size, and customer

- Continuation of device identification (if too long for the second line)
- "Stampoff" number as required by specific customer request and specification
- Notice(s) related to copyright or trademarks

Very small packages, such as SOT-23, SOT-223, SC70, and SC90, are too small to contain all the information discussed above. Device identification marking is assigned differently, consisting of a four-character code:

- Device type (see *Table 9*)
- Device identification code
- Grade

These small packages also have a date code mark on the underside of the package. This is a one-character alpha code that represents a particular 6-week period during a 3-year span.

The specific marking for a given device can be found in the device datasheet. Other date code information, which would be typically found in the "first line" marking, is identified on the container labels.

Figure 1, *Figure 2*, and *Figure 3* show the typical arrangement of marking on large, medium, and very small packages. Codes that are most often used in the device marking are listed in the following tables. For chip scale packaged devices and all other recent updates, please refer to www.national.com/packaging.

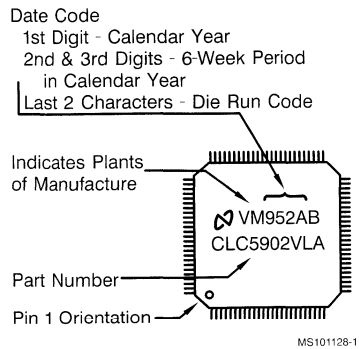


FIGURE 1. Marking Convention for Larger Packages

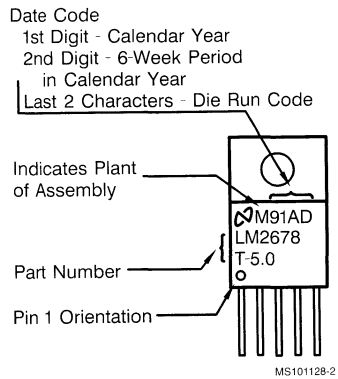


FIGURE 2. Marking Convention for Smaller Packages

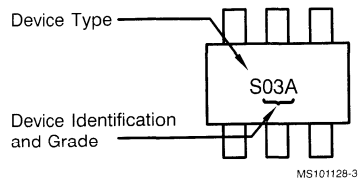


FIGURE 3. Marking Convention for Very Small Packages

Wafer Fab and Assembly Plant Codes

Table 1 lists single-letter codes for National Semiconductor's wafer fabrication plants. Letters that are not in this list indicate wafer fabrication at one of National Semiconductor's approved sub-contractors.

TABLE 1. Wafer Fab Plant Code

Code	Fab Location
E	Arlington, TX
H	Greenock, UK
J	Greenock, UK
R	Santa Clara, CA
V	South Portland, ME
X	Arlington, TX
0	Multiple Fab Origin
1	USA (Sub-con)
2	Taiwan (Sub-con)
3	USA (Sub-con)
8	Singapore (Sub-con)
M	USA (Sub-con)
N	Israel (Sub-con)
P	China (Sub-con)
W	Japan (Sub-con)
Z	USA (Sub-con)

Table 2 lists single-letter codes for National Semiconductor's device assembly plants. Letters that are not in this list indicate device assembly at another of National Semiconductor's approved sub-contractors.

TABLE 2. Assembly Plant Code

Code	Assembly Location
F	Santa Clara, CA
M	Malacca, Malaysia
S	Singapore
B	Thailand (Sub-con)
D	Philippines (Sub-con)
E	Korea (Sub-con)
G	Canada (Sub-con)
H	Philippines (Sub-con)
I	Indonesia (Sub-con)
J	Japan (Sub-con)
K	Hong Kong (Sub-con)
N	Malaysia (Sub-con)
P	Malaysia (Sub-con)
T	Taiwan (Sub-con)
V	Malaysia (Sub-con)
X	USA (Sub-con)
Y	Malaysia (Sub-con)

Date of Manufacture Codes

Marks indicating the date of manufacture occur in four, three, two, or one digit versions. The date code represents a six-week period in which the device was assembled. The one-digit code is an alpha code for the very small packages, such as SOT, SC70, and SC90, and ranges from A to Z plus the character @, representing a 6-week period during a 3-year span. For the four, three, and two digit codes, the allocation of digits between year and week information in each scheme is summarized in *Table 3*:

TABLE 3. Year Code

Version	Year Digits	Week Range Digits
Four-digit (YYWW)	2	2
Three-digit (YWW)	1	2
Two-digit (YW)	1	1

Year: The year code is the last one or two digits of the calendar year of manufacture. For example, a device manufactured in 1999 would have a one-digit code of "9" or a two-digit code of "99".

Week: The week code is based on the starting calendar week of the six-week period during which the device was assembled. *Table 4* summarizes the six-week date code schedule for one- and two-digit codes.

TABLE 4. Six-Week Period Code

Six-Week Period		Two-Digit Code	One-Digit Code
From Week	To Week		
52	05	52	9
06	11	06	1
12	17	12	2
18	23	18	3
24	29	24	4
30	35	30	5
36	41	36	6
42	47	42	7
48	51	48	8

Some example date codes are shown in *Table 5*:

TABLE 5. Date Code Examples

Date of Manufacture	4-Digit Code	3-Digit Code	2-Digit Code
Calendar week 48, 1999	9948	948	98
Calendar week 6, 2000	0006	006	01
Calendar week 14, 2000	0012	012	02
Calendar week 32, 2001	0130	130	15

Die Run (Wafer Lot) Codes

The die run code is a two letter alpha code, ranging from AB through ZZ for each device, that is automatically assigned to each lot by an internal manufacturing system. When the date code is combined with the die run code, a unique identifier is created. In case of any problems with a device, this identification facilitates backward traceability to manufacturing processes where containment and corrective actions can be defined. These actions, in turn, minimize, and eventually eliminate, any negative impact on customers.

Device Family and Package Codes

TABLE 6. Device Family

ADC, ADCV	Data Conversion
CLC	Comlinear Products
COP	Control Oriented Processor
DAC	Data Conversion
DS, DSV	Interface Products
FPD	Flat Panel Devices
LF	Linear (Bi-FET™)
LM	Linear (Monolithic)
LMC	Linear CMOS
LMD	Linear DMOS
LMF, MF	Linear Monolithic Filter
LMS	Linear Second Source
LMV	Linear Low Voltage
LMX	Wireless
LP	Linear Low Power
LPC	Linear CMOS (Low Power)
LPV	Linear Low Power, Low Voltage
SC	Digital Cordless Telephony
SCAN	JTAG Products
TP	Telecom Products

TABLE 7. Package Type

BP	Micro Surface-Mount Device (MicroSMD)
D, DH	Ceramic Sidebrazed Dual-In-Line Package
DT, TD	Molded D-Pak (TO-252)
EL	Ceramic Quad Flatpack with J-Bend Lead Form
H, HA	3-Lead Metal Can (TO-46, TO-39)
J, JA	Ceramic Dual-In-Line Package (CerDIP)
K, KA	TO-3 Metal Can (Steel)
LD, LQ, LQA	Leadless Leadframe Package (LLP)
M, MA	Molded Small Outline Package (SO, SOT)
M3, M5, M6, MF	Molded Small Outline Package (SOT-23)
M7, MG	SC70
MEA, MQ, MS, MSA	Molded Shrink Small Outline Package (SSOP)
MM	Miniature Molded Small Outline Package (MSOP, Mini SO)
MP	Molded Small Outline Package (SOT-223)
MTA, MTC, MTD, MT, MTE	Molded Thin Shrink Small Outline Package (TSSOP)
MW, WM	Wide Body Molded Small Outline Package (SO, SOT)
N, NA	Molded Dual-In-Line Package (DIP)
S, TS	Molded Power Surface Mount Package (TO-263)
SL, SLB	Chip Scale Packaging (CSP)
T, TA	Molded TO-220 Power Package
TF	Molded TO-220 Power Package With Isolated Tab
U, UE	Ceramic Pin Grid Array (PGA)
V, VA	28 & 44-Lead Molded Plastic Leaded Chip Carrier (PLCC)
VBG, VC, VCC, VCE, VD, VE, VEF, VF, VH, VHG, VI, VJ, VJG, VJQ, VK, VLJ, VM, VN, VNG, VO, VP, VQL, VUL, VUW	Molded Plastic Quad Flat Package (PQFP)
VEH, VF, VH, VJD, VS, VT, VU	Molded Plastic Thin Quad Flat Package (TQFP)
W, WA	Ceramic Flatpack
W, WQ	Ceramic Quad Flatpak
WG	Ceramic Small Outline Package and Quad Flatpak with Gullwing Lead Form
Z, ZA	Molded 3-Lead Transistor Package (TO-92)

TABLE 8. Package Type—CLC Products

E	Molded Small Outline Package (SO, SOT)
Q	Molded Plastic Leaded Chip Carrier (PLCC)

Small Surface-Mount Package Marking

For packages such as SOT23 (3-, 5-, and 6-lead), SOT223, and MSOP, there is insufficient space to mark the entire part number, so a four-character code is used instead. The first character represents the device type (see *Table 9*). The second two characters are a code relating to the device part number and options. The fourth character relates to device performance grade. This four-character "top mark" is usually fully specified in the device datasheet, for all options and grades of the product.

TABLE 9. Device Type Code

A	Amplifier
B	Buffer
C	Comparator
D	Driver
H	Comlinear
L	Low-Dropout Linear Regulator
R	Voltage Reference
S	Switched-Capacitor Voltage Converter
T	Temperature Sensor
Z	Audio

National Semiconductor

National Semiconductor's Die Products

As system designers search for ways to derive higher performance with reduced power consumption, size and weight—from their circuit designs, they are turning to suppliers of bare die and known good die for cost-effective solutions. Based on module size, design complexity, substrate, and tolerance for rework, the manufacturer must make a trade-off between the average yield for the die selected for module use and the cost of additional die upscreening.

With more than five years of experience in supplying Known Good Die—and the manufacturing expertise of more than thirty years in the semiconductor business National Semiconductor is uniquely equipped to support your KGD needs, evaluation, and selection. The Die Products Business Unit, or DPBU, will work with established customers under non-disclosure agreements to help them balance the trade-off between die cost and expected yields for the wide variety of die products that National Semiconductor offers.

While there is no single answer for all applications, there is a common goal among die customers that we understand. Whether your module supports cellular telephones ... or anti-lock brakes ... or deep-space satellites ... all die customers must procure die that meet their unique yield requirements at a price that allows their end product to be competitive.

Wide Product Availability of Die

To address the needs of Multi Chip, Chip on Board and Flip Chip Module manufacturers, National offers a complete product portfolio in die form.

- Analog
- Interface
- Logic
- Memory
- Microcontrollers
- SCAN boundary test (IEEE 1149.1)
- Networking
- Wireless

Since National has been manufacturing semiconductors for over thirty years, we know the capabilities and limitations of our products. Many of these technologies require little additional screening to meet 99.9% yields. Others require AC/DC probe as well as burn-in to meet similar yields. The DPBU can work with customers to understand the system specifications and long-term reliability requirements. Our product engineers can tailor an electrical test program around your needs ... or take into consideration the historic wafer yield as well as final package yields and offer the most cost-effective, reliable die in the industry.

Shipping Methods

Die provided through National Semiconductor's Die Products Business Unit are shipped to the customer in several methods, based on the customer's request. Whole wafers are shipped in plastic vials enclosed in anti-static bags. For die shipments, customers have a choice of Waffle Packs, GEL-PAKS@, sawn wafers shipped on adhesive tape, or tape and reel. Information on typical die packaging and labeling is available on request.

Documentation Support

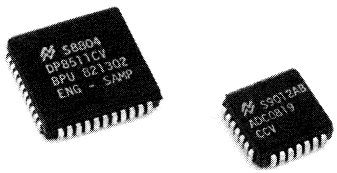
It is great to know that you can get the product you need in die form. However, die by itself is difficult to use, so National Semiconductor makes available all of the documentation you need to assemble our KGD into your multichip module or chip-on-board assembly. Our KGD datasheets, which are available on request, include information such as:

- Electrical specifications
- X, Y Coordinates for the bond pad locations
- A bonding diagram
- Die dimensions
- Bond pad dimensions, including passivation opening size
- Bond pad metal composition and thickness
- Die backside composition
- Die passivation
- Pinout list, including any pads which need to be jumpered or skipped
- Electrical potential of die backside
- LAT attributes data, if specified

National Semiconductor

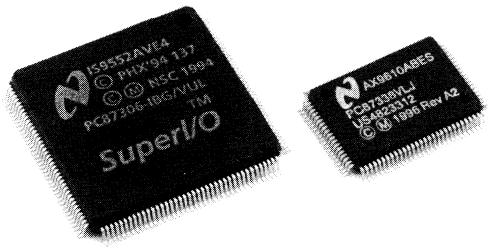
Package Illustrations

Package photos are actual size. Please see web site at **http://www.national.com/packaging/** for specifications. Many National products are available in wafer, die, and known good die form. Please go to www.national.com/kgd for more information on known good die.



MS101192-1

Molded Plastic Leaded Chip Carrier (PLCC)
Product Suffix: V, VA
CLC Product Suffix: Q

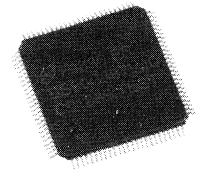


MS101192-2

MS101192-30

Molded Plastic Quad Flatpak (PQFP)
Product Suffix: VBG, VC, VCC, VCE, VD, VE, VEF, VF, VH, VHG, VI, VJ, VJG, VJQ, VK, VLJ, VM, VN, VNG, VO, VP, VQL, VUL, VUW

MS101192-29



MS101192-3

Molded Plastic Thin Quad Flatpak (TQFP)
Product Suffix: VEH, VJD, VF, VH, VS, VT, VU

MS101192-31

Leadless Leadframe Package (LLP)
Product Suffix: LD, LQ, LQA

MS101192-4

Chip Scale Packaging (CSP)
Product Suffix: SL, SLB

MS101192-5

MicroSMD µSMD
Product Suffix: BP

MS101192-6

SC70
Product Suffix: M7, MG

MS101192-7

Miniature Molded Small Outline Package (MSOP, Mini SO)
Product Suffix: MM

MS101192-8

MS101192-27

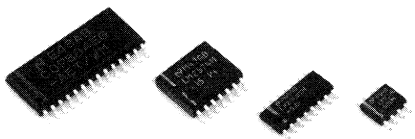
Molded Small Outline Package (SOT-23)
Product Suffix: M3, M5, M6, MF

MS101192-9

Molded Small Outline Package (SOT-223)
Product Suffix: MP

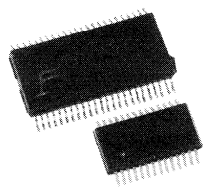
MS101192-10

Molded Thin Shrink Small Outline Package (TSSOP)
Product Suffix: MTA, MTD, MTC, MT, MTE



MS101192-11

Molded Small Outline Package (SO, SOT)
Product Suffix: M, MA, MW, WM
CLC Product Suffix: E

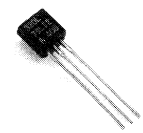


MS101192-12

Molded Shrink Small Outline Package (SSOP)
Product Suffix: MSA, MEA, MQ, MS

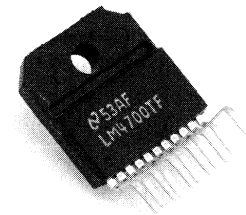
MS101192-13

3-Lead Metal Can Package (TO-46)
Product Suffix: H, HA



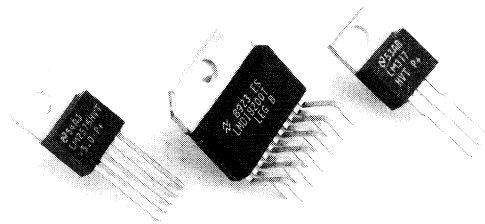
MS101192-14

Molded TO-92
Product Suffix: Z, ZA



MS101192-15

Molded TO-220 Isolated Tab
Product Suffix: TF

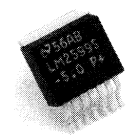


MS101192-16

Molded TO-220
Product Suffix: T, TA

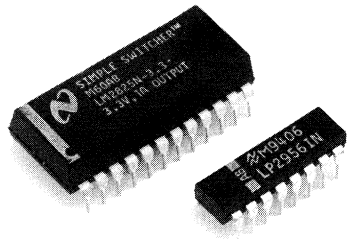
MS101192-32

Molded D-Pak (TO-252)
Product Suffix: DT, TD



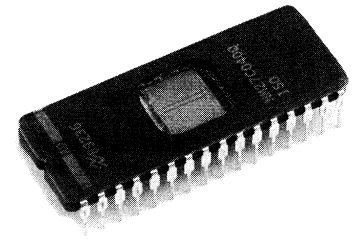
MS101192-17

Molded Power Surface Mount (TO-263)
Product Suffix: S, TS



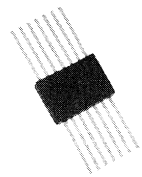
MS101192-18

Molded Dual-in-Line Package (DIP)
Product Suffix: N, NA



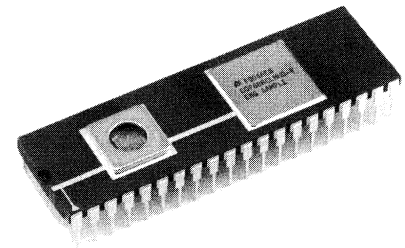
MS101192-22

Ceramic Dual-in-Line Package (CerDIP)
Product Suffix: J, JA



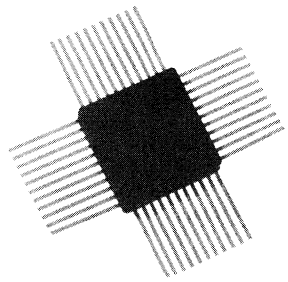
MS101192-19

Ceramic Flatpak
Product Suffix: W, WA



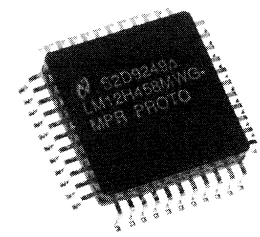
MS101192-23

Ceramic Sidebrazed Dual-in-Line Package
Product Suffix: D, DH



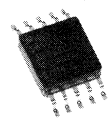
MS101192-20

Ceramic Quad Flatpak
Product Suffix: W, WQ

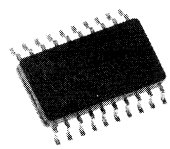


MS101192-24

Ceramic Quad Flatpak (Gullwing)
Product Suffix: WG

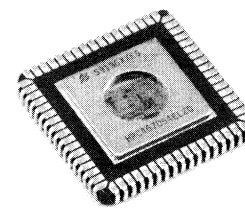


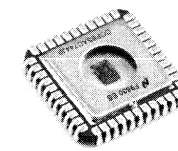
MS101192-21



MS101192-28

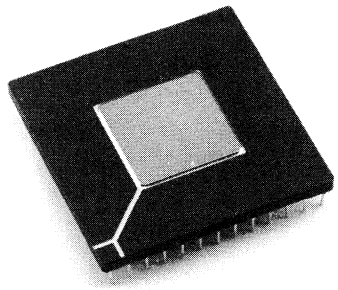
Ceramic Small Outline Integrated Circuit (Gullwing)
(Ceramic SOIC)
Product Suffix: WG





MS101192-25

Ceramic Quad Flatpak J-Bend
Product Suffix: EL



MS101192-26

Ceramic Pin Grid Array (PGA)
Product Suffix: U, UE

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